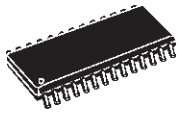
L6917

5 BIT PROGRAMMABLE DUAL-PHASE CONTROLLER

- 2 PHASE OPERATION WITH SYNCRHONOUS RECTIFIER CONTROL
- ULTRA FAST LOAD TRANSIENT RESPONSE
- INTEGRATED HIGH CURRENT GATE DRIVERS: UP TO 2A GATE CURRENT
- TTL-COMPATIBLE 5 BIT PROGRAMMABLE OUTPUT COMPLIANT WITH VRM 9.0
- 0.8% INTERNAL REFERENCE ACCURACY
- 10% ACTIVE CURRENT SHARING ACCURACY
- DIGITAL 2048 STEP SOFT-START
- OVERVOLTAGE PROTECTION
- OVERCURRENT PROTECTION REALIZED USING THE LOWER MOSFET'S R_{dsON} OR A SENSE RESISTOR
- 300 kHz INTERNAL OSCILLATOR
- OSCILLATOR EXTERNALLY ADJUSTABLE UP TO 1MHz
- POWER GOOD OUTPUT AND INHIBIT FUNCTION
- REMOTE SENSE BUFFER
- PACKAGE: SO-28

APPLICATIONS

- POWER SUPPLY FOR SERVER AND WORKSTATION
- POWER SUPPLY FOR HIGH CURRENT MICROPROCESSORS
- DISTRIBUTED POWER SUPPLY



SO-28

ORDERING NUMBERS: L6917D
L6917DTR (Tape & Reel)

DESCRIPTION

The device is a power supply controller specifically designed to provide a high performance DC/DC conversion for high current microprocessors.

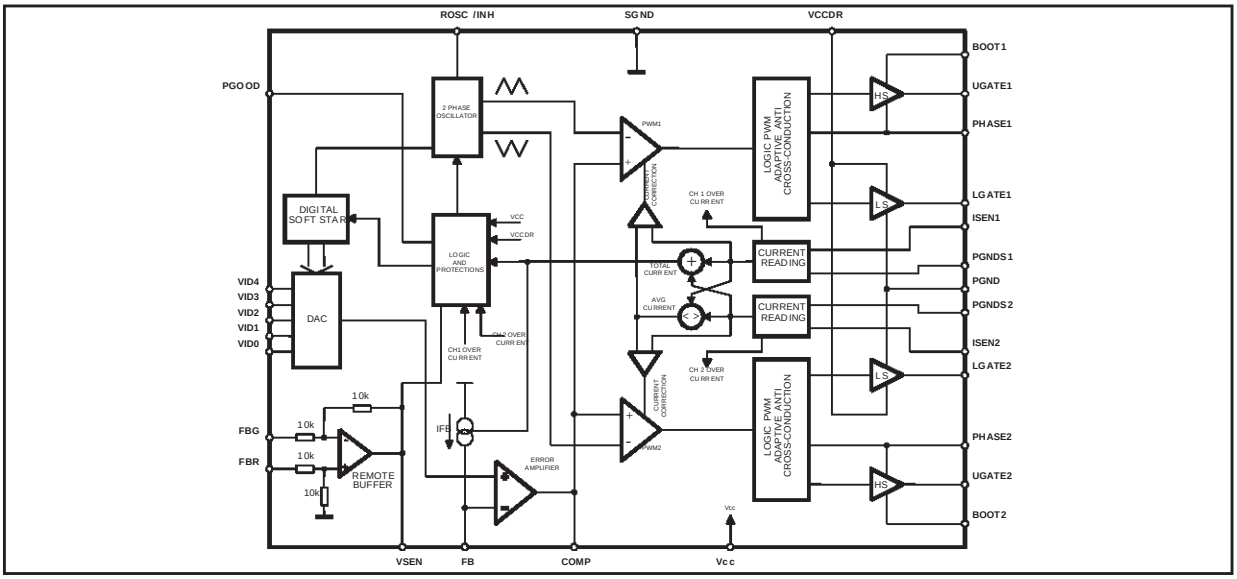
The device implements a dual-phase step-down controller with a 180° phase-shift between each phase.

A precise 5-bit digital to analog converter (DAC) allows adjusting the output voltage from 1.100V to 1.850V with 25mV binary steps.

The high precision internal reference assures the selected output voltage to be within ±0.8%. The high peak current gate drive affords to have fast switching to the external power mos providing low switching losses.

The device assures a fast protection against load over current and load over/under voltage. An internal crowbar is provided turning on the low side mosfet if an over-voltage is detected. In case of over-current or under voltage, the system works in HICCUP mode.

BLOCK DIAGRAM



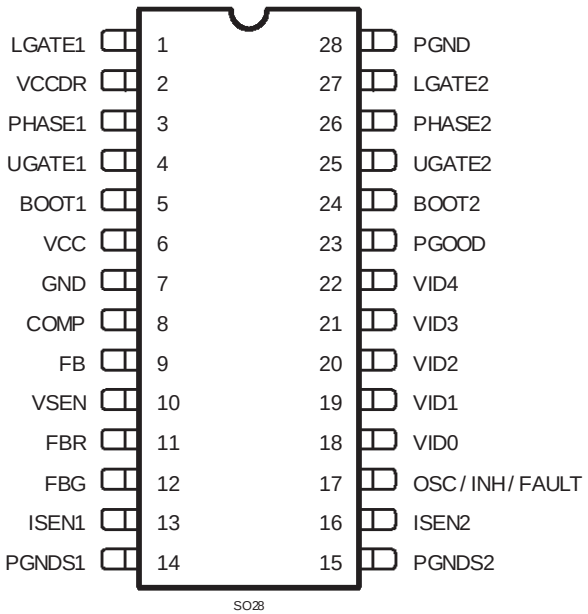
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc, V_{CCDR}	To PGND	15	V
V_{BOOT}-V_{PHASE}	Boot Voltage	15	V
V_{UGATE1}-V_{PHASE1} V_{UGATE2}-V_{PHASE2}		15	V
	LGATE1, PHASE1, LGATE2, PHASE2 to PGND	-0.3 to Vcc+0.3	V
	All other pins to PGND	-0.3 to 7	V

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	60	°C/W
T_{max}	Maximum junction temperature	150	°C
$T_{storage}$	Storage temperature range	-40 to 150	°C
T_j	Junction Temperature Range	-25 to 125	°C
P_{MAX}	Max power dissipation at T_{amb} = 25°C	2	W

PIN CONNECTION



ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vcc SUPPLY CURRENT						
I_{CC}	Vcc supply current	HGATEx and LGATEx open V_{CCDR}=V_{BOOT}=12V	6	8	10	mA
I_{CCDR}	V_{CCDR} supply current	LGATEx open; V_{CCDR}=12V	2	3	4	mA
I_{BOOTx}	Boot supply current	HGATEx open; PHASEx to PGND V_{CC}=V_{BOOT}=12V	0.5	1	1.5	mA
POWER-ON						
	Turn-On V_{CC} threshold	V_{CC} Rising; V_{CCDR}=5V	7.8	9	10.2	V
	Turn-Off V_{CC} threshold	V_{CC} Falling; V_{CCDR}=5V	6.5	7.5	8.5	V
	Turn-On V_{CCDR} Threshold	V_{CCDR} Rising V_{CC}=12V	4.2	4.4	4.6	V
	Turn-Off V_{CCDR} Threshold	V_{CCDR} Falling V_{CC}=12V	4.0	4.2	4.4	V
OSCILLATOR AND INHIBIT						
f_{OSC}	Initial Accuracy	OSC = OPEN OSC = OPEN; Tj=0°C to 125°C	278 270	300	322 330	kHz kHz
$f_{OSC,Rosc}$	Total Accuracy	R_T to GND=74kΩ	450	500	550	kHz
INH	Inhibit threshold	I_{SINK}=5mA	0.8	0.85	0.9	V
d_{MAX}	Maximum duty cycle	OSC = OPEN	80	85		%
ΔVosc	Ramp Amplitude		1.8	2	2.2	V
REFERENCE AND DAC						
	Output Voltage Accuracy	VID0, VID1, VID2, VID3, VID4 see Table1; Tamb=0° to 70°; FBR = V_{OUT}; FBG = GND	-0.8	-	0.8	%
I_{DAC}	VID pull-up Current	VIDx = GND	4	5	6	µA
	VID pull-up Voltage	VIDx = OPEN	3.1	-	3.4	V
ERROR AMPLIFIER						
	DC Gain			80		dB
SR	Slew-Rate	COMP=10pF		15		V/µs
DIFFERENTIAL AMPLIFIER (REMOTE BUFFER)						
	DC Gain			1		V/V
CMRR	Common Mode Rejection Ratio			40		dB
	Input Offset	FBR=1.100V to1.850V; FBG=GND	-12		12	mV

ELECTRICAL CHARACTERISTICS (continued)(V_{CC} = 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SR	Slew Rate	VSEN=10pF		15		V/µs
DIFFERENTIAL CURRENT SENSING						
I_{ISEN1}, I_{ISEN2}	Bias Current	Iload=0	45	50	55	µA
I_{PGNDSx}	Bias Current		45	50	55	µA
I_{ISEN1}, I_{ISEN2}	Bias Current at Over Current Threshold	Positive Negative	80	85 37.5	90	µA µA
I_{FB}	Active Droop Current	Iload<0% Iload=100%	 47.5	0 50	1 52.5	µA µA
GATE DRIVERS						
$t_{RISE\ HGATE}$	High Side Rise Time	V_{BOOTx}-V_{PHASEx}=10V; C_{HGATEx} to PHASEx=3.3nF		15	30	ns
I_{HGATEx}	High Side Source Current	V_{BOOTx}-V_{PHASEx}=10V		2		A
R_{HGATEx}	High Side Sink Resistance	V_{BOOTx}-V_{PHASEx}=12V;	1.5	2	2.5	Ω
$t_{RISE\ LGATE}$	Low Side Rise Time	V_{CCDR}=10V; C_{LGATEx} to PGNDx=5.6nF		30	55	ns
I_{LGATEx}	Low Side Source Current	V_{CCDR}=10V		1.8		A
R_{LGATEx}	Low Side Sink Resistance	V_{CCDR}=12V	0.7	1.1	1.5	Ω
PROTECTIONS						
PGOOD	Upper Threshold (V_{SEN}/DACOUT)	V_{SEN} Rising	109	112	115	%
PGOOD	Lower Threshold (V_{SEN}/DACOUT)	V_{SEN} Falling	84	88	92	%
OVP	Over Voltage Threshold (V_{SEN})	V_{SEN} Rising	2.0	2.1	2.2	V
UVP	Under Voltage Trip (V_{SEN}/DACOUT)	V_{SEN} Falling	76	80	84	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -4mA	0.3	0.4	0.5	V
FAULT	Fault Condition	After OVP or 3 HICCUP cycles	4.75	5.0	5.25	V

Table 1. VID Settings

VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
1	1	1	1	1	OUTPUT OFF
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

PIN FUNCTION

N	Name	Description
1	LGATE1	Channel 1 low side gate driver output.
2	VCCDR	Mosfet driver supply. It can be varied from 5V to 12V Bus.
3	PHASE1	This pin is connected to the source of the upper mosfet and provides the return path for the high side driver of channel 1.
4	UGATE1	Channel 1 high side gate driver output.
5	BOOT1	Channel 1 bootstrap capacitor pin. Through this pin is supplied the high side driver and the upper mosfet. Connect through a capacitor to the PHASE1 pin and through a diode to Vcc (cathode vs. boot).
6	VCC	Device supply voltage. The operative supply voltage is 12V.
7	GND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
8	COMP	This pin is connected to the error amplifier output and is used to compensate the control feedback loop.
9	FB	This pin is connected to the error amplifier inverting input and is used to compensate the voltage control feedback loop. A current proportional to the sum of the current sensed in both channel is sourced from this pin (50µA at full load, 70µA at the Over Current threshold). Connecting a resistor between this pin and VSEN pin allows programming the droop effect.
10	VSEN	Connected to the output voltage it is able to manage Over & Under-voltage conditions and the PGOOD signal. It is internally connected with the output of the Remote Sense Buffer for Remote Sense of the regulated voltage. If no Remote Sense is implemented, connect it directly to the regulated voltage in order to manage OVP, UVP and PGOOD.
11	FBR	Remote sense buffer non-inverting input. It has to be connected to the positive side of the load to perform a remote sense. If no remote sense is implemented, connect directly to the output voltage (in this case connect also the VSEN pin directly to the output regulated voltage).
12	FBG	Remote sense buffer inverting input. It has to be connected to the negative side of the load to perform a remote sense. Pull-down to ground if no remote sense is implemented.
13	ISEN1	Channel 1 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet Rds_{ON}. This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the positive current limit at 140% as follow: $I_{MAX\_POS1} = \frac{35\mu A \cdot R_g}{R_{sense}}$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load). In the same way the negative current limit threshold results to be set at –50% as follow: $I_{MAX\_NEG1} = \frac{-12.5\mu A \cdot R_g}{R_{sense}}$ Where –12.5µA is the current offset information relative to the Negative Over Current condition (offset at Negative OC threshold minus offset at zero load). The net connecting the pin to the sense point must be routed as close as possible to the PGNDS1 net in order to couple in common mode any picked-up noise.
14	PGNDS1	Channel 1 Power Ground sense pin. The net connecting the pin to the sense point (Through a resistor R_g) must be routed as close as possible to the ISEN1 net in order to couple in common mode any picked-up noise.

PIN FUNCTION (continued)

N	Name	Description
15	PGNDS2	Channel 2 Power Ground sense pin. The net connecting the pin to the sense (Through a resistor R_g) point must be routed as close as possible to the ISEN2 net in order to couple in common mode any picked-up noise.
16	ISEN2	Channel 2 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet Rds_{ON}. This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the positive current limit at 140% as follow: $I_{MAX\_POS2} = \frac{35\mu A \cdot R_g}{R_{sense}}$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load). In the same way the negative current limit threshold results to be set at –50% as follow $I_{MAX\_NEG2} = \frac{-12.5\mu A \cdot R_g}{R_{sense}}$ Where –12.5µA is the current offset information relative to the Negative Over Current condition (offset at Negative OC threshold minus offset at zero load). The net connecting the pin to the sense point must be routed as close as possible to the PGNDS2 net in order to couple in common mode any picked-up noise.
17	OSC/INH FAULT	Oscillator switching frequency pin. Connecting an external resistor from this pin to GND, the external frequency is increased according to the equation: $f_S = 300KHz + \frac{14.82 \cdot 10^6}{R_{OSC}(K\Omega)}$ Connecting a resistor from this pin to Vcc (12V), the switching frequency is reduced according to the equation: $f_S = 300KHz + \frac{12.91 \cdot 10^7}{R_{OSC}(K\Omega)}$ If the pin is not connected, the switching frequency is 300KHz. Forcing the pin to a voltage lower than 0.8V, the device stop operation and enter the inhibit state. The pin is forced high when an over voltage is detected and after three hiccup cycles. This condition is latched; to recover it is necessary turn off and on VCC.
18-22	VID4-0	Voltage IDentification pins. These input are internally pulled-up and TTL compatible. They are used to program the output voltage as specified in Table 1 and to set the power good thresholds. Connect to GND to program a ‘0’ while leave floating to program a ‘1’.
23	PGOOD	This pin is an open collector output and is pulled low if the output voltage is not within the above specified thresholds. If not used may be left floating.
24	BOOT2	Channel 2 bootstrap capacitor pin. Through this pin is supplied the high side driver and the upper mosfet. Connect through a capacitor to the PHASE2 pin and through a diode to Vcc (cathode vs. boot).
25	UGATE2	Channel 2 high side gate driver output.
26	PHASE2	This pin is connected to the source of the upper mosfet and provides the return path for the high side driver of channel 2.
27	LGATE2	Channel 2 low side gate driver output.
28	PGND	Power ground pin. This pin is common to both sections and it must be connected through the closest path to the low side mosfets source pins in order to reduce the noise injection into the device.

Device Description

The device is an integrated circuit realized in BCD technology. It provides complete control logic and protections for a high performance multiphase step-down DC-DC converter optimized for microprocessor power supply. It is designed to drive N Channel MOSFETs in a dual-phase synchronous-rectified buck topology. A 180 deg phase shift is provided between the two phases allowing reduction in the input capacitor current ripple, reducing also the size and the losses. The output voltage of the converter can be precisely regulated, programming the VID pins, from 1.100V to 1.850V with 25mV binary steps, with a maximum tolerance of ±0.8% over temperature and line voltage variations. The device provides an average current-mode control with fast transient response. It includes a 300kHz free-running oscillator externally adjustable up to 1MHz. The error amplifier features a 15V/µs slew rate that permits high converter bandwidth for fast transient performances. Current information is read across the lower mosfets rDSON or across a sense resistor in fully differential mode. The current information corrects the PWM output in order to equalize the average current carried by each phase. Current sharing between the two phases is then limited at ±10% over static and dynamic conditions. The device protects against over-current, with an OC threshold for each phase, entering in HICCUP mode. After three hiccup cycles, the condition is latched and the FAULT pin is driven high. The device performs also an under voltage protection that causes a hiccup cycle when detected, and an over voltage protection that disable immediately the device turning ON the lower driver and driving high the FAULT pin.

The device is available in SO28 package.

Oscillator

The switching frequency is internally fixed to 300kHz. The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The current delivered to the oscillator is typically 25µA (F_{SW} = 300KHz) and may be varied using an external resistor (R_{OSC}) connected between OSC pin and GND or Vcc. Since the OSC pin is maintained at fixed voltage (typ). 1.235V, the frequency is varied proportionally to the current sunk (forced) from (into) the pin considering the internal gain of 12KHz/µA.

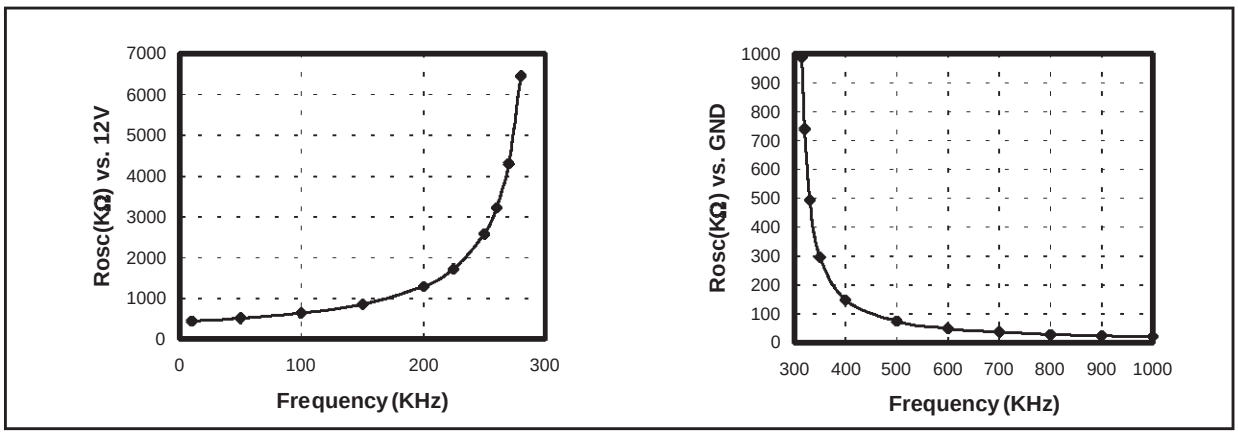
In particular connecting it to GND the frequency is increased (current is sunk from the pin), while connecting ROSC to Vcc=12V the frequency is reduced (current is forced into the pin), according to the following relationships:

$$R_{OSC}\text{vs. GND: } f_S = 300kHz + \frac{1.237}{R_{OSC}(K\Omega)} \cdot 12\frac{kHz}{\mu A} = 300kHz + \frac{14.82 \cdot 10^6}{R_{OSC}(K\Omega)}$$

$$R_{OSC}\text{vs. 12V: } f_S = 300kHz + \frac{12 - 1.237}{R_{OSC}(K\Omega)} \cdot 12\frac{kHz}{\mu A} = 300kHz - \frac{12.918 \cdot 10^7}{R_{OSC}(K\Omega)}$$

Note that forcing a 25µA current into this pin, the device stops switching because no current is delivered to the oscillator.

Figure 1. R_{OSC} vs. Switching Frequency



Digital to Analog Converter

The built-in digital to analog converter allows the adjustment of the output voltage from 1.100V to 1.850V with 25mV steps as shown in the previous table 1. The internal reference is trimmed to ensure the precision of 0.8% and a zero temperature coefficient around 70°C. The internal reference voltage for the regulation is programmed by the voltage identification (VID) pins. These are TTL compatible inputs of an internal DAC that is realized by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the V_{PROG} voltage reference (i.e. the set-point of the error amplifier). Internal pull-ups are provided (realized with a 5µA current generator up to 3.3V max); in this way, to program a logic "1" it is enough to leave the pin floating, while to program a logic "0" it is enough to short the pin to GND.

The voltage identification (VID) pin configuration also sets the power-good thresholds (PGOOD) and the over-voltage protection (OVP) thresholds.

Soft Start and INHIBIT

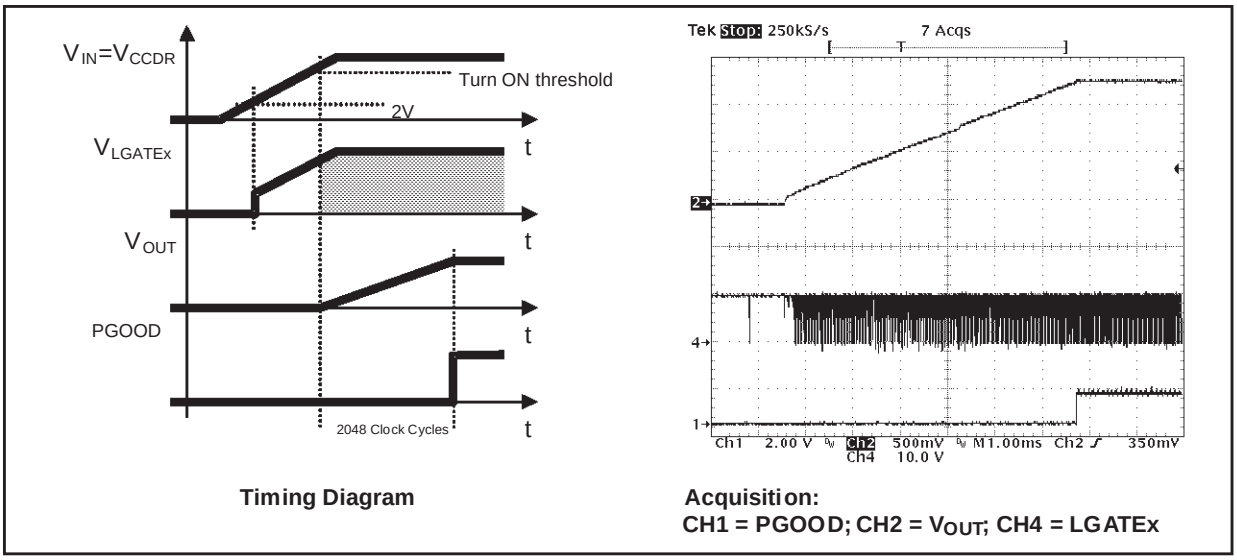
At start-up a ramp is generated increasing the loop reference from 0V to the final value programmed by VID in 2048 clock periods as shown in figure 2.

Before soft start, the lower power MOS are turned ON after that V_{CCDR} reaches 2V (independently by Vcc value) to discharge the output capacitor and to protect the load from high side mosfet failures. Once soft start begins, the reference is increased; when it reaches the bottom of the oscillator triangular waveform (1V typ) also the upper MOS begins to switch and the output voltage starts to increase with closed loop regulation. At the end of the digital soft start, the Power Good comparator is enabled and the PGOOD signal is then driven high (See fig. 2). The Negative Current Limit comparators and Under Voltage comparator are enabled when the reference voltage reaches 0.8V.

The Soft-Start will not take place, if both Vcc and VCCDR pins are not above their own turn-on thresholds. During normal operation, if any under-voltage is detected on one of the two supplies the device shuts down.

Forcing the OSC/INH/FAULT pin to a voltage lower than 0.8V the device enter in INHIBIT mode: all the power mosfets are turned off until this condition is removed. When this pin is freed, the OSC/INH/FAULT pin reaches the band-gap voltage and the soft start begins.

Figure 2. Soft Start



Timing Diagram

Acquisition:
CH1 = PGOOD; CH2 = V_{OUT}; CH4 = LGATEx

Driver Section

The integrated high-current drivers allow using different types of power MOS (also multiple MOS to reduce the RDSON), maintaining fast switching transition.

The drivers for the high-side mosfets use BOOTx pins for supply and PHASEx pins for return. The drivers for the low-side mosfets use VCCDR pin for supply and PGND pin for return. A minimum voltage of 4.6V at VCCDR pin is required to start operations of the device.

The controller embodies a sophisticated anti-shoot-through system to minimize low side body diode conduction time maintaining good efficiency and saving the use of Schottky diodes. The dead time is reduced to few nano-seconds assuring that high-side and low-side mosfets are never switched on simultaneously: when the high-side mosfet turns off, the voltage on its source begins to fall; when the voltage reaches 2V, the low-side mosfet gate drive is applied with 30ns delay. When the low-side mosfet turns off, the voltage at LGATEx pin is sensed. When it drops below 1V, the high-side mosfet gate drive is applied with a delay of 30ns.

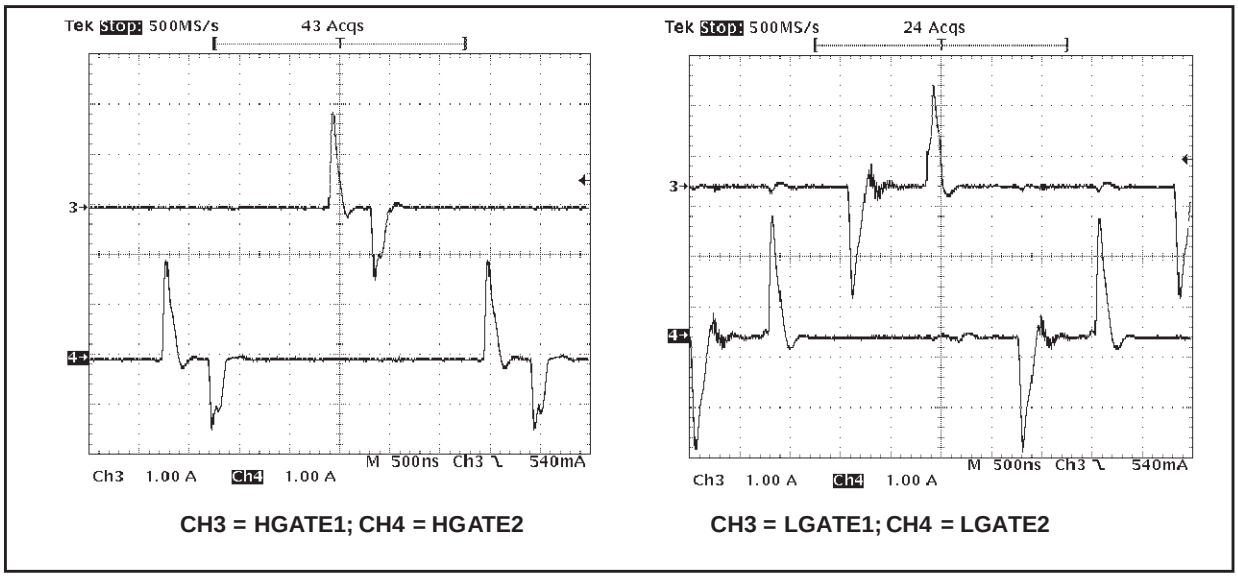
If the current flowing in the inductor is negative, the source of high-side mosfet will never drop. To allow the turning on of the low-side mosfet even in this case, a watchdog controller is enabled: after 240ns, the low side mosfet is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

The BOOTx and VCCDR pins are separated from IC's power supply (VCC pin) as well as signal ground (SGND pin) and power ground (PGND pin) in order to maximize the switching noise immunity. The separated supply for the different drivers gives high flexibility in mosfet choice, allowing the use of logic-level mosfet. Several combination of supply can be chosen to optimize performance and efficiency of the application. Power conversion is also flexible, 5V or 12V bus can be chosen freely.

Placement of the power mosfets is critical: long and narrow trace length from UGATEx and LGATEx pins to the mosfets' gates may cause high amount of ringing due to the resonance between inductance of the trace and the gate capacitance of the mosfet. A gate resistance of a few ohms can help in reducing ringing and power dissipation of the controller without compromising system efficiency.

The peak current is shown for both the upper and the lower driver of the two phases in figure 3. A 10nF capacitive load has been used. For the upper drivers, the source current is 1.9A while the sink current is 1.5A with V_{BOOT}-V_{PHASE} = 12V; similarly, for the lower drivers, the source current is 2.4A while the sink current is 2A with VCCDR = 12V.

Figure 3. Drivers peak current: High Side (left) and Low Side (right)



CH3 = HGATE1; CH4 = HGATE2

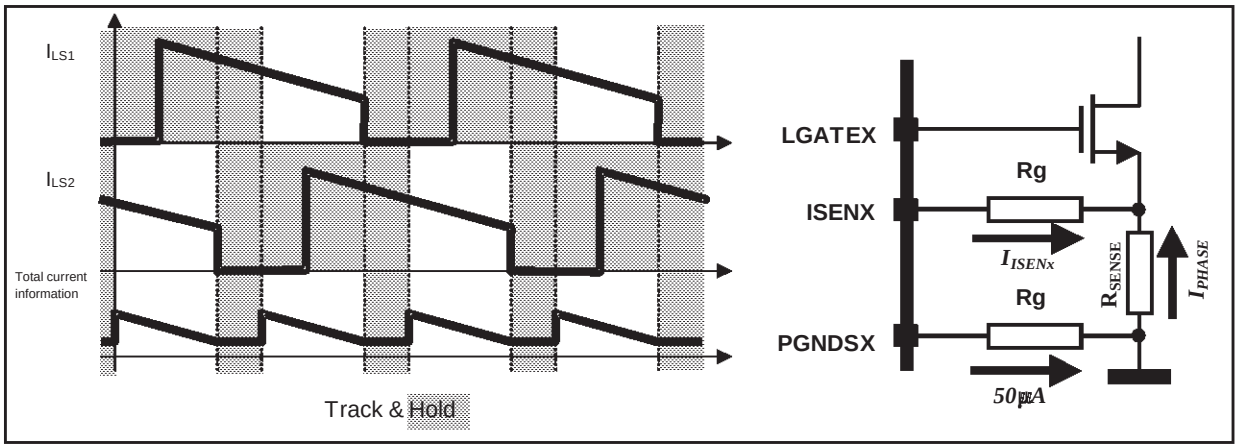
CH3 = LGATE1; CH4 = LGATE2

Current Reading and Over Current

The current flowing trough each phase is read using the voltage drop across the low side mosfets r_{DSON} or across a sense resistor (R_{SENSE}) and internally converted into a current. The transconductance ratio is issued by the external resistor Rg placed outside the chip between ISENx and PGNDSx pins toward the reading points. The full differential current reading rejects noise and allows to place sensing element in different locations without affecting the measurement's accuracy. The current reading circuitry reads the current during the time in which the low-side mosfet is on (OFF Time). During this time, the reaction keeps the pin ISENx and PGNDSx at the same voltage while during the time in which the reading circuitry is off, an internal clamp keeps these two pins at the same voltage sinking from the ISENx pin the necessary current.

The proprietary current reading circuit allows a very precise and high bandwidth reading for both positive and negative current. This circuit reproduces the current flowing through the sensing element using a high speed Track & Hold transconductance amplifier. In particular, it reads the current during the second half of the OFF time reducing noise injection into the device due to the mosfet turn-on (See fig. 4).

Figure 4.



This circuit sources a constant 50µA current from the PGNDSx pin and keeps the pins ISENx and PGNDSx at the same voltage. Referring to figure 4, the current that flows in the ISENx pin is then given by the following equation:

$$I_{ISENx} = 50\mu A + \frac{R_{SENSE} \cdot I_{PHASE}}{R_g} = 50\mu A + I_{INFOx}$$

Where R_{SENSE} is an external sense resistor or the r_{dson}, on of the low side mosfet and Rg is the transconductance resistor used between ISENx and PGNDSx pins toward the reading points; I_{PHASE} is the current carried by each phase and, in particular, the current measured in the middle of the oscillator period

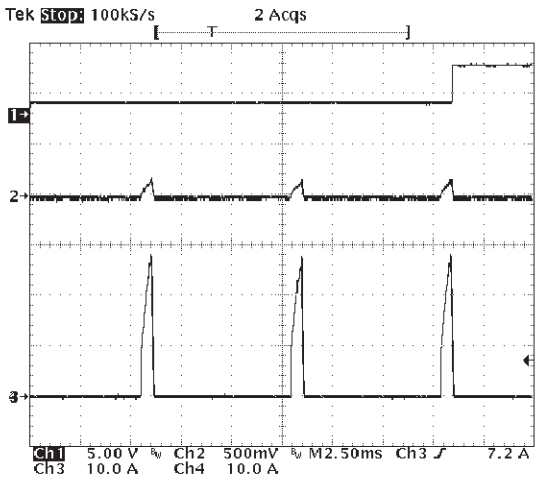
The current information reproduced internally is represented by the second term of the previous equation as follow:

$$I_{INFOx} = \frac{R_{SENSE} \cdot I_{PHASE}}{R_g}$$

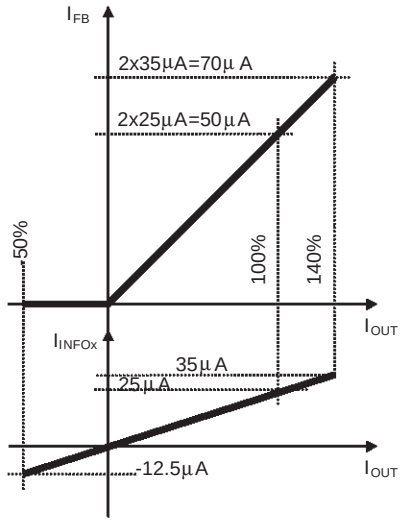
Since the current is read in differential mode, also negative current information is kept; this allow the device to check for dangerous returning current between the two phases assuring the complete equalization between the phase's currents.

From the current information of each phase, information about the total current delivered ($I_{FB} = I_{INFO1} + I_{INFO2}$) and the average current for each phase ($I_{AVG} = (I_{INFO1} + I_{INFO2})/2$) is taken. I_{INFOX} is then compared to I_{AVG} to give the correction to the PWM output in order to equalize the current carried by the two phases.

Figure 5. HICCUP Mode (left) and OCP threshold and Current information (right)



Hiccup Mode:
CH1 = FAULT; CH2 = V_{OUT}; CH3 = I_{L1}; CH4 = I_{L2}



The over current threshold for each phase is set when I_{INFOx} = 35µA. Since the over current detection gives origin to Hiccup cycles (and the output voltage goes down to zero, with information losses for the microprocessor) the over current threshold must be greater than the nominal current.

Placing the OC threshold at +40% gives a margin to sustain the heavy load transient issued by the processor. As a consequence, the transconductance resistor Rg has to be designed in order to have current information of 35µA at 140% of the nominal load, corresponding to 25µA at nominal load. Considering the feedback current (I_{FB}), this will be equal to 50µA at nominal load and 70µA at over current threshold as shown in figure 5.

Since the device is able to read negative current, negative current limit is also provided and it is set when I_{INFOx} = -12.5µA , corresponding to -50% of the full nominal current. No current is sunk from the FB pin in this condition.

According to the above relationship, the positive limiting current (I_{LIM_POS}) for each phase, which has to be placed at one half of the total delivered maximum current and the limiting negative current (I_{LIM_NEG}), results:

$$I_{LIM\_POS} = \frac{35\mu A \cdot Rg}{R_{SENSE}} \qquad I_{LIM\_NEG} = \frac{-12.5\mu A \cdot Rg}{R_{SENSE}} \qquad Rg = \frac{I_{LIM} \cdot R_{SENSE}}{35\mu A}$$

When over current is detected, all mosfets are turned OFF, the device waits for 2048 clock cycles and another soft-start is implemented. Over Current is always active, also during soft-start. After three Over Current event, the condition is latched and the device stops working; Vcc turn OFF and ON is required to restart device operation.

Over current is set anyway when I_{INFOx} reaches 35µA. The full load value is only a convention to work with convenient values for I_{FB}. Since the OPC intervention threshold is fixed, to modify the percentage with respect to the load value, it can be simply considered that, for example, to have on OCP threshold of 170%, this will correspond to I_{INFOx} = 35µA (I_{FB} = 70µA). The full load current will then correspond to I_{INFOx} = 20.5µA (I_{FB} = 41µA). Over current is managed as an under voltage: after a combination of three of then, the device latches the condition and the FAULT pin is driven high.

The full differential path helps the designer to place sensing element where wanted. Transconductance Rg resistors must be placed as close as possible to ISENx and PGNDSx pins in order to reject noise from the device. Keeping the traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Current Sharing

Active current sharing is implemented using the information from transconductance differential amplifier in an average current mode control scheme. A current reference equal to the average of the read current (I_{AVG}) is internally built; the error between the read current and this reference is converted to a voltage with a proper gain and it is used to adjust the duty cycle whose dominant value is set by the error amplifier at COMP pin.

The current sharing control is a high bandwidth control allowing current sharing even during load transients.

The current sharing error is affected by the choose of external components; choose precise Rg resistor (±1% is necessary) to sense the current. The current sharing error is internally dominated by the voltage offset of transconductance differential amplifier; considering a voltage offset equal to 2mV across the sense resistor, the current reading error is given by the following equation:

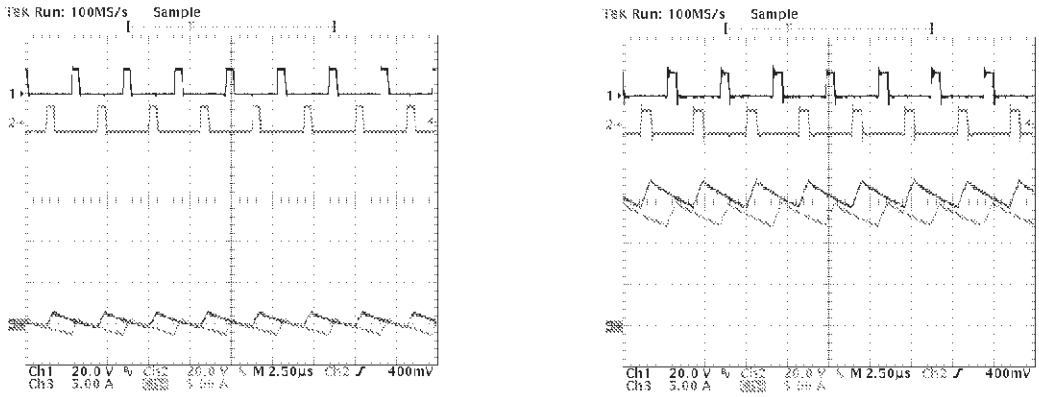
$$\frac{\Delta I_{READ}}{I_{MAX}} = \frac{2mV}{R_{SENSE} \cdot I_{MAX}}$$

Where ΔI_{READ} is the difference between one phase current and the ideal current ($I_{MAX}/2$).

For Rsense=4mΩ and Imax=40A the current sharing error is equal to 2.5%, neglecting errors due to Rg and Rsense mismatches.

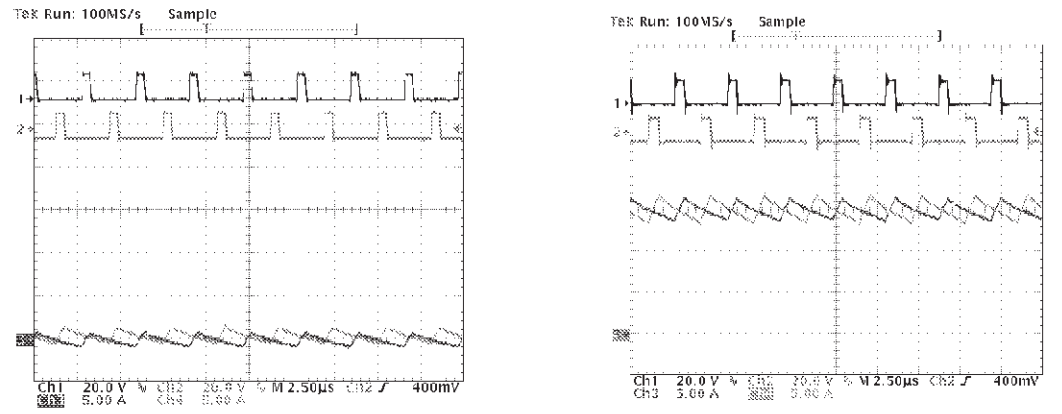
Figures 6 and 7 show the current sharing error obtained at 0A and 30A using a sense resistor or the low side mosfet's R_{dsON} as sensing element. The static error obtained using the R_{dsON} is due to the tolerance of this parameter (up to 30%).

Figure 6. Current Sharing Error using R_{dsON} as sensing element at 0A (left) and 30A (right).



CH1 = PHASE1; CH2 = PHASE2; CH3 = I_{L2}; CH4 = I_{L1}

Figure 7. Current Sharing Error using R_{SENSE} as sensing element at 0A (left) and 30A (right)..



CH1 = PHASE1; CH2 = PHASE2; CH3 = I_{L2}; CH4 = I_{L1}

Integrated Droop Function

The device uses a droop function to satisfy the requirements of high performance microprocessors, reducing the size and the cost of the output capacitor.

This method ”recovers” part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current

As shown in figure 8, the ESR drop is present in any case, but using the droop function the total deviation of the output voltage is minimized. In practice the droop function introduces a static error (Vdroop in figure 8) proportional to the output current. Since the device has an average current mode regulation, the information about the total current delivered is used to implement the Droop Function. This current (equal to the sum of both I_{INFOx}) is sourced from the FB pin. Connecting a resistor between this pin and Vout, the total current information flows only in this resistor because the compensation network between FB and COMP has always a capacitor in series (See fig. 9). The voltage regulated is then equal to:

$$V_{OUT} = V_{ID} - R_{FB} \cdot I_{FB}$$

Since I_{FB} depends on the current information about the two phases, the output characteristic vs. load current is given by:

$$V_{OUT} = VID - R_{FB} \cdot \frac{R_{SENSE}}{Rg} \cdot I_{OUT}$$

Figure 8. Output transient response without (a) and with (b) the droop function

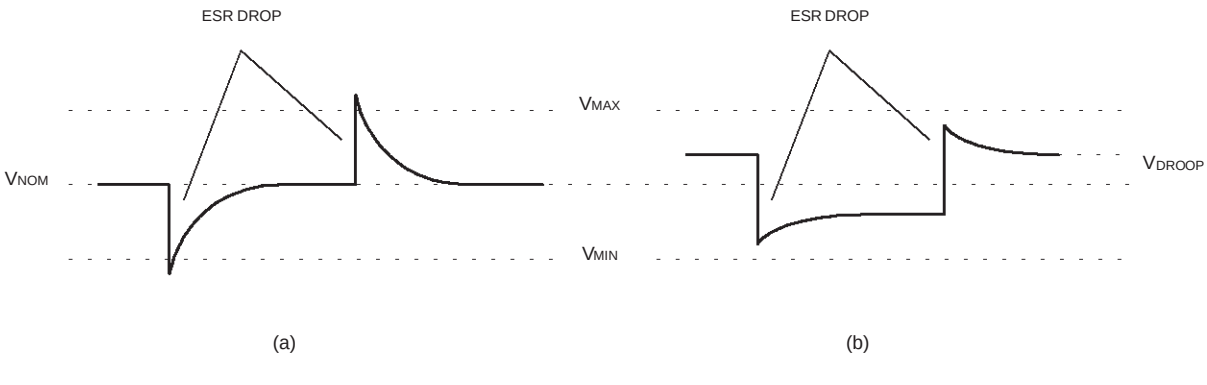
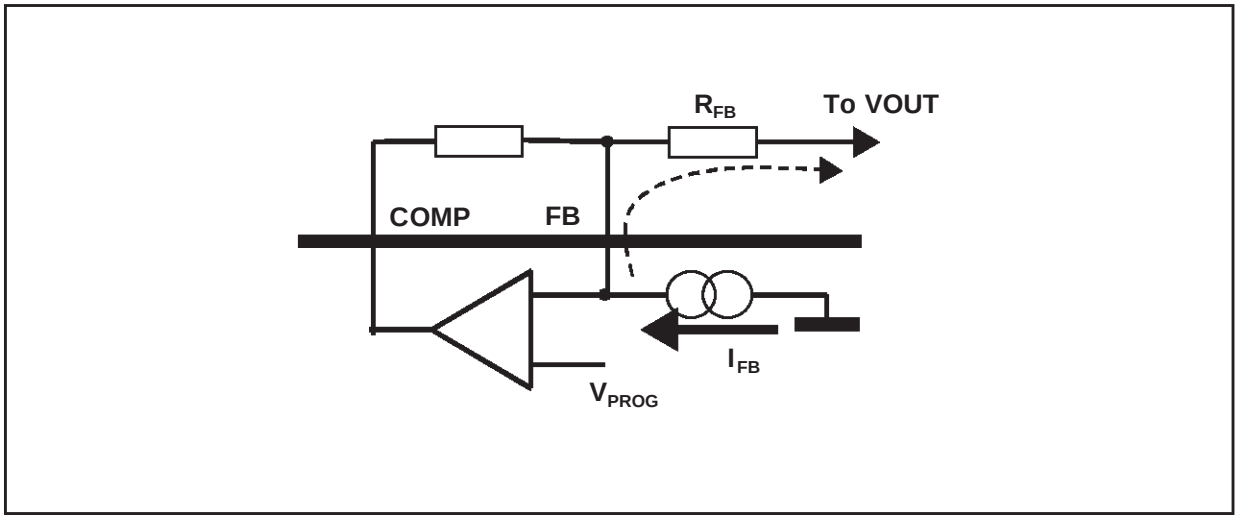


Figure 9. Active Droop Function Circuit



The feedback current is equal to 50µA at nominal full load ($I_{FB} = I_{INFO1} + I_{INFO2}$) and 70µA at the OC threshold, so the maximum output voltage deviation is equal to:

$$\Delta V_{FULL\_POSITIVE\_LOAD} = +R_{FB} \cdot 70\mu A \qquad \Delta V_{POSITIVE\_OC\_THRESHOLD} = +R_{FB} \cdot 70\mu A$$

Droop function is provided only for positive load; if negative load is applied, and then $I_{INFOx} < 0$, no current is sunk from the FB pin. The device regulates at the voltage programmed by the VID.

Output Voltage Protection and Power Good

The output voltage is monitored by pin VSEN. If it is not within +12/-10% (typ.) of the programmed value, the powergood output is forced low. Power good is an open drain output and it is enabled only after the soft start is finished (2048 clock cycles after start-up).

The device provides over voltage protection; when the voltage sensed by the V_{SEN} pin reaches 2.1V (typ.), the controller permanently switches on both the low-side mosfets and switches off both the high-side mosfets in order to protect the CPU. The OSC/INH/FAULT pin is driven high (5V) and power supply (Vcc) turn off and on is required to restart operations. The over Voltage percentage is set by the ratio between the OVP threshold (set at 2.1V) and the reference programmed by VID.

$$OVP[\%] = \frac{2.1V}{\text{Reference Voltage (VID)}} - 100$$

Under voltage protection is also provided. If the output voltage drops below the 85% of the reference voltage for more than one clock period the device turns off all mosfets and waits for 2048 clock cycles before another soft-start. An Under Voltage event is then managed as an Over Current event; after a combination of three of them, the device latches the condition and the FAULT is driven high.

Both Over Voltage and Under Voltage are active also during soft start (Under Voltage after than Vout reaches 0.8V). The reference voltage used to determine the UV thresholds is nowthe increasing voltage driven by the 2048 soft start digital counter.

Remote Voltage Sense

A remote sense buffer is integrated into the device to allow output voltage remote sense implementation without any additional external components. In this way, the output voltage programmed is regulated between the remote buffer inputs compensating motherboard trace losses or connector losses if the device is used for a VRM module. The low offset amplifier senses the output voltage remotely through the pins FBR and FBG (FBR is for the regulated voltage sense while FBG is for the ground sense) and reports this voltage internally at VSEN pin

with unity gain eliminating the errors. Keeping the FBR and FBG traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

If remote sense is not required, the output voltage is sensed by the VSEN pin connecting it directly to the output voltage. In this case the FBG and FBR pins must be connected anyway to the regulated voltage.

Input Capacitor

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFETS. Considering the dual phase topology, the input rms current is highly reduced because of the peak current is one half if compared with a single-phase solution.

Input capacitor must have a low ESR to minimize the losses. The rms value of this ripple is:

$$I_{rms} = \frac{I_{OUT}}{2} \cdot \sqrt{D \cdot (1 - D)}$$

Where D is the duty cycle. The equation reaches its maximum value width D=0.5. The losses in worst case are:

$$P = ESR \cdot I_{rms}^2$$

Input bulk capacitor must be equally divided between high-side drain mosfets and placed as close as possible to reduce switching noise above all during load transient. A symmetrical power path will help to improve transient response. Input coil may be used taking from this point the supply for the controller VCC and VCCDRV, designing a 'star connection'.

IC's power supplies filter capacitor must be placed as close as possible to VCC and VCCDRV pins; for the VCC pins a typical value is of 1µF and must be used connected between VCC and SGND pins. For better noise filtering a series resistor of a few tenth ohm is suggested since the device typically works with the same power supply used for the power conversion (noisy because of the switching mosfet).

Capacitor on VCCDRV pin filter the low-side drivers power supply toward the PGND pin; 1µF capacitor is recommended.

The 12V input power bus can be used to supply the bootstrap capacitor alone or together with a 5.1V zener diode in series and a 1µF capacitor for filtering. A gate-source voltage of 7V is so ready to switch on the high-side mosfets with a good compromise of efficiency and controller power dissipation. Alternatively a linear regulator can be used to produce the supply for high-side and low-side power mosfet drivers. This can help to optimize the choose of switching frequency, controller power dissipation and overall efficiency.

Output Capacitor

Since the microprocessors require a current variation beyond 50A doing load transients, with a slope in the range of tenth A/µs, the output capacitor is a basic component for the fast response of the power supply.

Dual phase topology reduces the amount of output capacitance needed because of faster load transient response (switching frequency is doubled at the load connections). Current ripple cancellation due to the 180° phase shift between the two phases also reduces requirements on the output ESR to sustain a specified voltage ripple.

When a load transient is applied to the converter's output, for first few microseconds the current to the load is supplied by the output capacitors. The controller recognizes immediately the load transient and increases the duty cycle, but the current slope is limited by the inductor value.

The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta V_{OUT} = \Delta I_{OUT} \cdot ESR$$

A minimum capacitor value is required to sustain the current during the load transient without discharge it. The

voltage drop due to the output capacitor discharge is given by the following equation:

$$\Delta V_{OUT} = \frac{\Delta I_{OUT}^2 \cdot L}{2 \cdot C_{OUT} \cdot (V_{INMIN} \cdot D_{MAX} - V_{OUT})}$$

Where D_{MAX} is the maximum duty cycle value. The lower is the ESR, the lower is the output drop during load transient and the lower is the output voltage static ripple.

Inductor design

The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current ΔIL between 20% and 30% of the maximum output current. The inductance value can be calculated with this relationship:

$$L = \frac{V_{IN} - V_{OUT}}{fs \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Where f_S is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage.

Increasing the value of the inductance reduces the ripple current but, at the same time, reduces the converter response time to a load transient. The response time is the time required by the inductor to change its current from initial to final value. Since the inductor has not finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required.

The response time to a load transient is different for the application or the removal of the load: if during the application of the load the inductor is charged by a voltage equal to the difference between the input and the output voltage, during the removal it is discharged only by the output voltage. The following expressions give approximate response time for DI load transient in case of enough fast compensation network response:

$$t_{application} = \frac{L \cdot \Delta I}{V_{IN} - V_{OUT}} \qquad t_{removal} = \frac{L \cdot \Delta I}{V_{OUT}}$$

The worst condition depends on the input voltage available and the output voltage selected. Anyway the worst case is the response time after removal of the load with the minimum output voltage programmed and the maximum input voltage available.

Figure 10. Inductor ripple current vs V_{out}

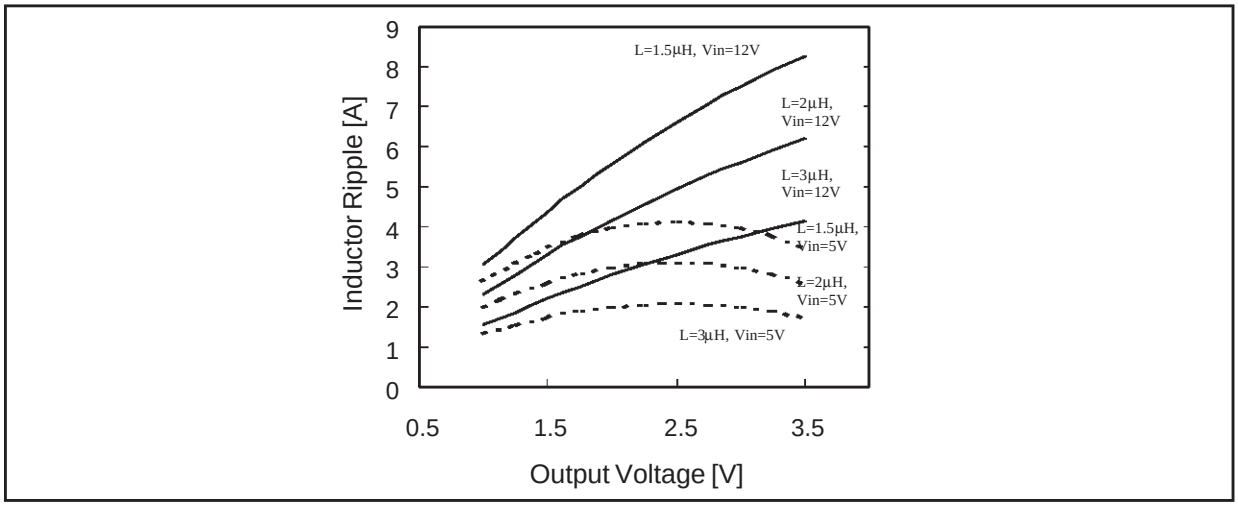
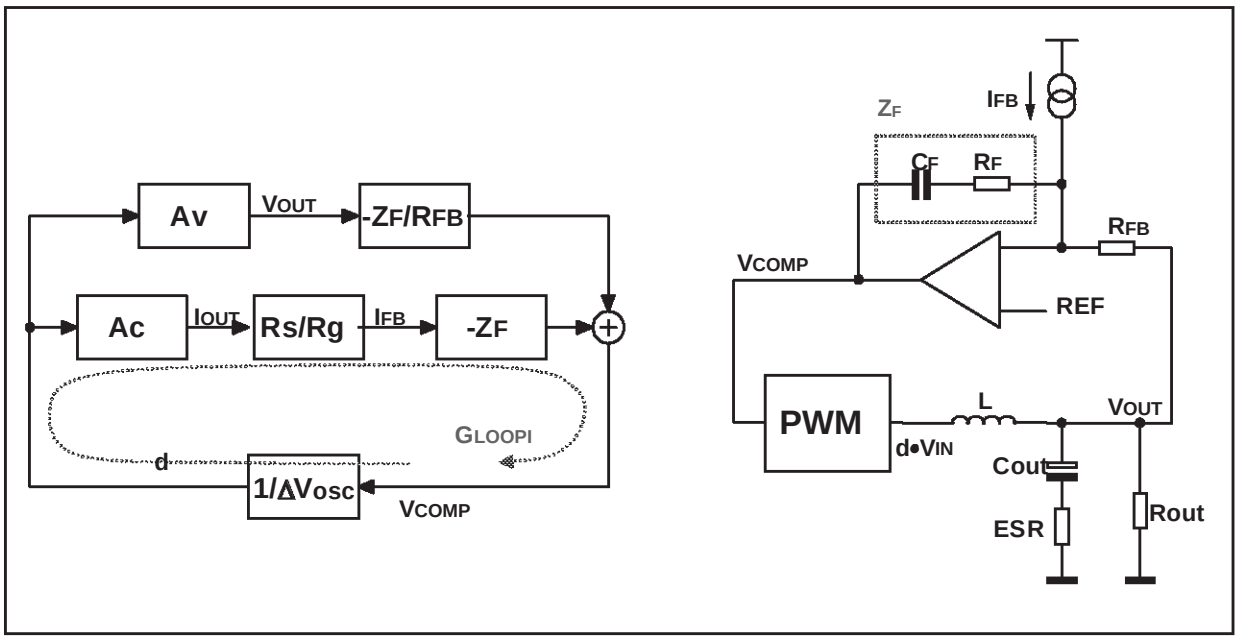


Figure 11. Control Loop Scheme



Average Current Mode Compensation Network Design

The average current mode control loop is reported in figure 11. The current information I_{FB} sourced by the FB pin flows into R_{FB} implementing the dependence of the output voltage from the read current.

Two different loops are present and precisely a current loop internal to a voltage loop. The current gain (Ac) and voltage gain (Av) present in the above figure are defined by the following relationships:

$$Av(s) = \frac{V_{OUT}}{d} = \{....\} = V_{IN} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{S^2 \cdot C_{OUT} \cdot \frac{L}{2} + s \cdot \left(ESR \cdot C_{OUT} + \frac{L}{2 \cdot R_{OUT}}\right) + 1}$$

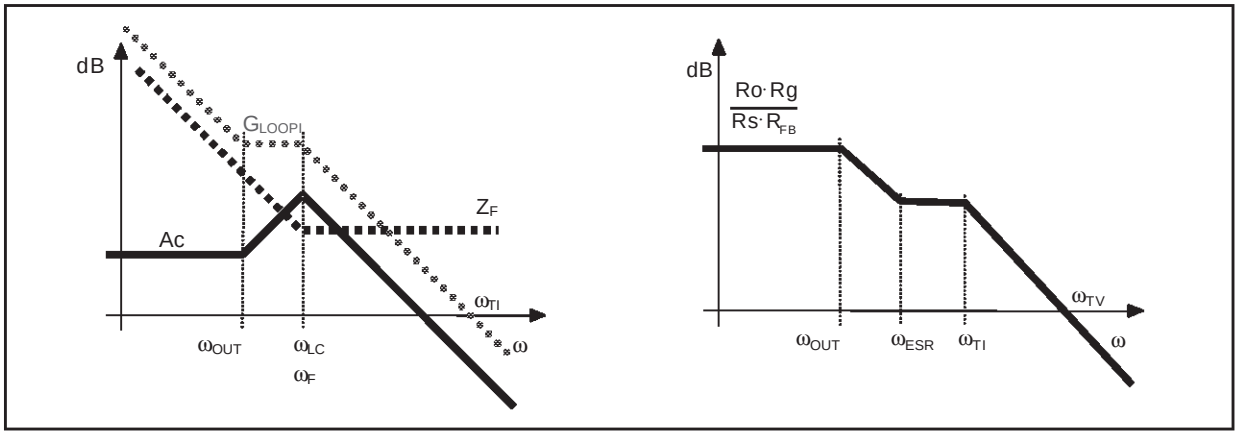
$$Ac(s) = \frac{I_{OUT}}{d} = \{....\} = \frac{V_{IN}}{R_{OUT}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{S^2 \cdot C_{OUT} \cdot \frac{L}{2} + s \cdot \left(ESR \cdot C_{OUT} + \frac{L}{2 \cdot R_{OUT}}\right) + 1}$$

The current loop gain may now be expressed by the following equation:

$$G_{LOOPI}(s) = \frac{Ac(s) \cdot Rs \cdot Z_F(s)}{Rg \cdot \Delta Vosc} = -\frac{V_{IN}}{R_{OUT}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{S^2 \cdot C_{OUT} \cdot \frac{L}{2} + s \cdot \left(ESR \cdot C_{OUT} + \frac{L}{2 \cdot R_{OUT}}\right) + 1} \cdot \frac{Rs}{Rg} \cdot \frac{Z_F(s)}{\Delta Vosc}$$

Where $\Delta Vosc$ has a typical value of 2V and $Z_F(s)$ is the impedance of the series R_F-C_F. The current loop gain is designed to obtain a high DC gain to minimize static error and cross the 0dB axes with a constant -20dB/dec slope with a crossover frequency ω_{TI}. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles. Both the poles are fixed once the output filter is designed and also the zero ($\omega_{OUT}=1/R_{OUT}C_{OUT}$) is fixed by the maximum current deliverable by the converter. To obtain the desired shape an R_F-C_F series network is considered for the $Z_F(s)$ implementation. A zero at $\omega_F=1/R_FC_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero in correspondence with the L-C resonance a simple -20dB/dec shape of the gain is assured (See Figure 12).

Figure 12. Current loop Gain (left) and Voltage loop Gain (right)



The R_F C_F network may be designed considering the desired crossover frequency ω_{TI} as follow:

- Assuming that $\omega_F = \omega_{LC}$, and that $Z_F=R_F$ if $\omega>\omega_F$, it can be observed that:

$$G_{LOOPI}(\omega=\omega_{LC}) = \frac{V_{IN} \cdot R_F \cdot R_S}{Ro \cdot \Delta Vosc \cdot Rg} \cdot \frac{\omega_{LC}}{\omega_O}$$

- Given the cross-over frequency ω_{TI}, it results:

$$R_F = \frac{Rg}{Rs} \cdot \frac{Ro \cdot \Delta Vosc}{Vin} \cdot \frac{\omega_o \cdot \omega_{TI}}{\omega_{LC}^2} = \frac{Rg}{Rs} \cdot \frac{Ro \cdot \Delta Vosc}{Vin} \cdot \frac{\frac{L \cdot C_{OUT} \cdot \omega_{TI}}{2}}{Ro \cdot C_{OUT}} = \frac{Rg}{Rs} \cdot \frac{\Delta Vosc}{Vin} \cdot \frac{L}{2 \cdot \omega_{TI}}$$

- Since $\omega_F=\omega_{LC}$:

$$C_F = \frac{\sqrt{C_{OUT} \cdot \frac{L}{2}}}{R_F}$$

Since the device works in current mode and then the control loop acts to control the current, the highest is ω_{TI}, the fastest is the device to react after a load transient. The placement of this singularity must consider the worst case for the load and precisely the maximum output current (minimum output resistance R_{OUT}).

The voltage loop gain may be expressed by the following relationship:

$$G_{LOOPV}(s) = \frac{V_{OUT}}{V_{COMP}} \cdot \frac{V_{COMP}}{V_{OUT}} = -Av(s) \cdot \frac{\frac{1}{\Delta Vosc}}{1 + G_{LOOPI}} \cdot \frac{Z_F(s)}{R_{FB}}$$

Assuming that $G_{LOOPI}>>1$ and after substitution and simplification the final expression for GLOOPV is given by:

$$G_{LOOPV}(s) = \{...\} = \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot R_{OUT} \cdot C_{OUT}} \cdot \frac{R_{OUT} \cdot Rg}{Rs \cdot R_{FB}} \cdot \frac{1}{1 + \frac{s}{\omega_{TI}}}$$

Where the additional pole placed at the current loop ω_{TI} must be inserted to consider that the current loop gain is not always $G_{LOOPI}>>1$. The LC resonance disappears thanks to the average current mode control and the system is automatically stable if ESR is small enough.

Since all the above modeling are valid at frequencies much lower than the switching frequency, the highest is this, the highest may be the converter's loop bandwidth (both current and voltage). In this way the converter is able to fast react after a load transient following, with the current delivered by the inductors, the current required by the load minimizing the number of the output capacitor required.

The average current mode compensation network is then designed as follow:

■ Given the voltage loop bandwidth ω_{TV}, the current loop bandwidth wTI is extracted from the following:

$$\omega_{TI} = \omega_{TV} \cdot \frac{Rs \cdot R_{FB}}{Ro \cdot Rg} \cdot \frac{\omega_{ESR}}{\omega_O} = \omega_{TV} \cdot \frac{Rs \cdot R_{FB}}{Ro \cdot Rg} \cdot \frac{Ro \cdot C_{OUT}}{ESR \cdot C_{OUT}} = \omega_{TV} \cdot \frac{Rs \cdot R_{FB}}{ESR \cdot Rg}$$

■ Once the current loop bandwidth is defined, the R_F C_F network may be designed as shown previously.

Demo Board Description

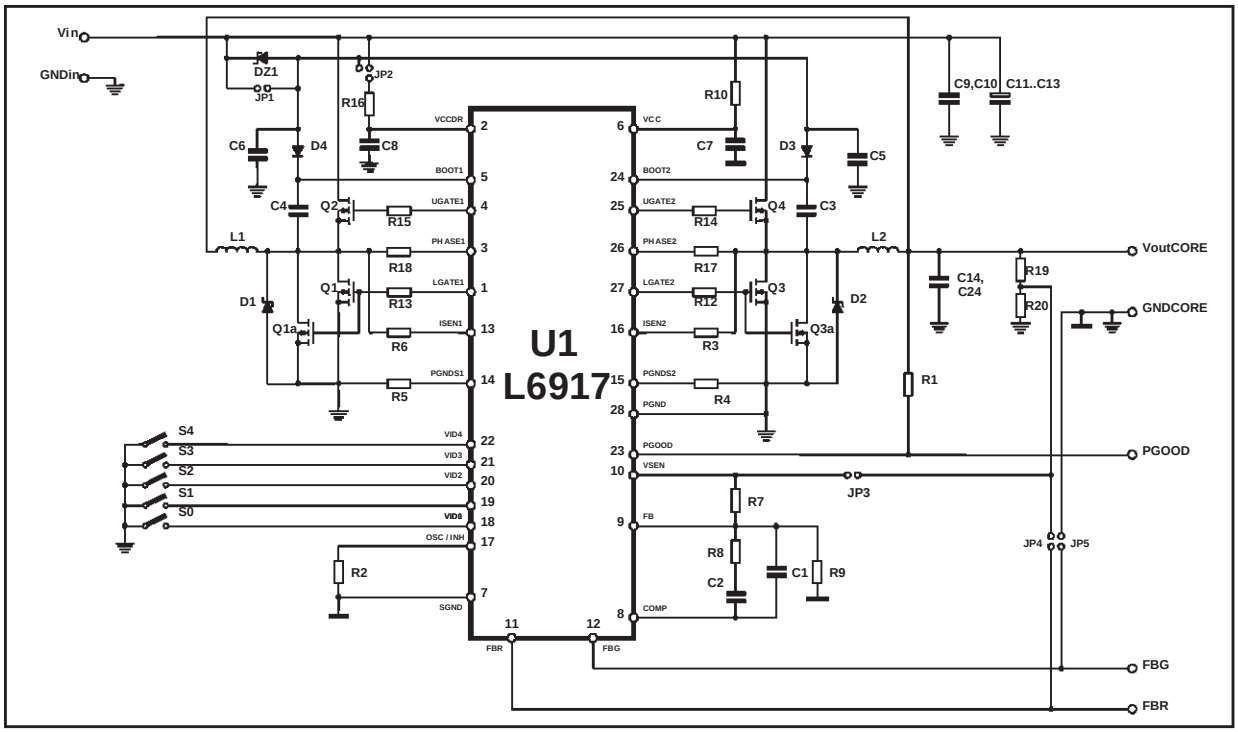
The L6917 demo board shows the operation of the device in a dual phase application. This evaluation board allows voltage adjustability (1.100V - 1.850V) through the switches S0-S4 and high output current capability. The 12V input rail supplies both the device and the high-side drain for the power conversion.

The board has been layed out with the possibility to use up to two D^2PACK mosfets for the low side switch in order to give maximum flexibility in the mosfet's choice.

The four layers demo board's copper thickness is of 70µm in order to minimize conduction losses considering the high current that the circuit is able to deliver.

Figure 13 shows the demo board's schematic circuit.

Figure 13. Demo Board Schematic

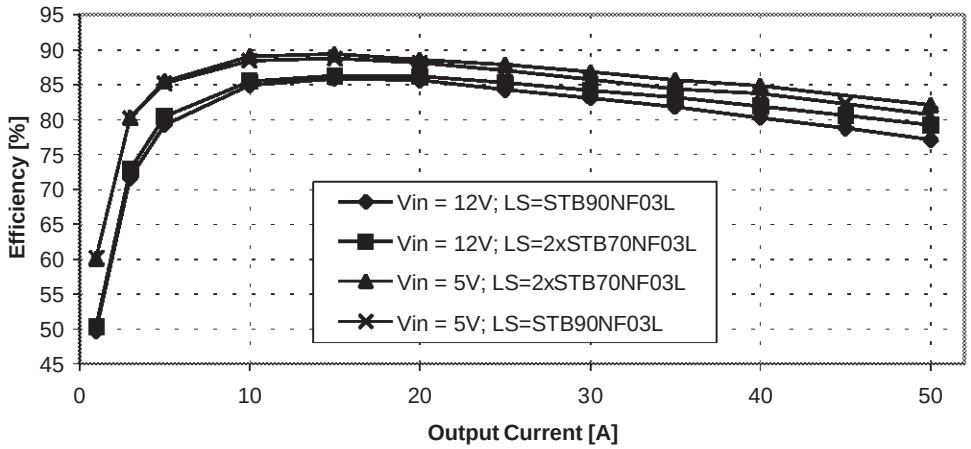


Efficiency

Figure 14 shows the demo board measured efficiency versus load current for different values of input voltage and mosfet configurations.

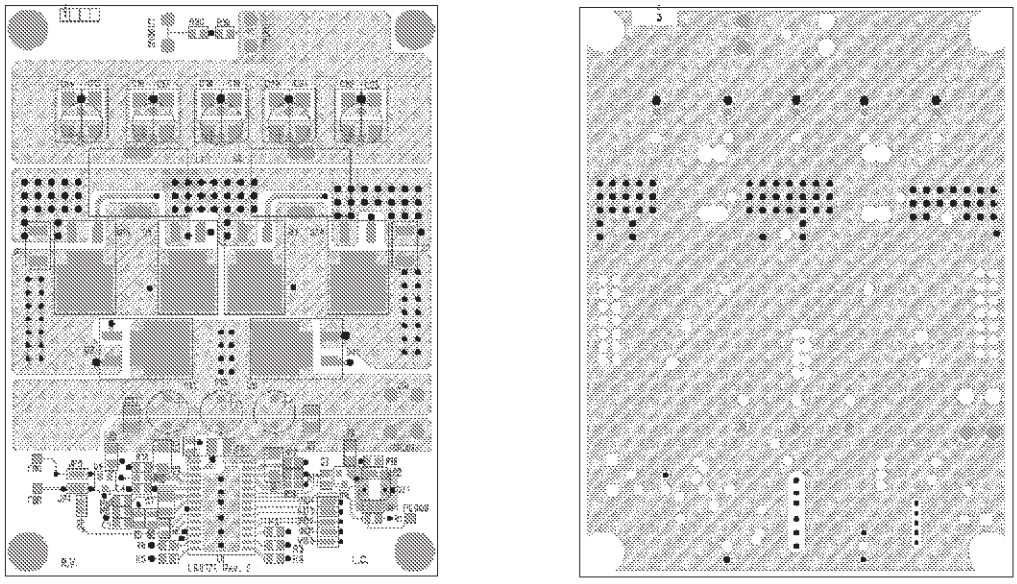
Measures were done at Vin=5V and Vin=12V with low side mosfet composed by a single STB90NF03L (30V, 5.6mΩ typ @ Vgs=10V) or a couple of STB70NF03L (30V, 8mΩ typ @ Vgs=10V) to reduce equivalent R_{dsON}. When 5V input is considered, the 12V bus supplies the IC and the mosfet' drivers.

Figure 14. Efficiency



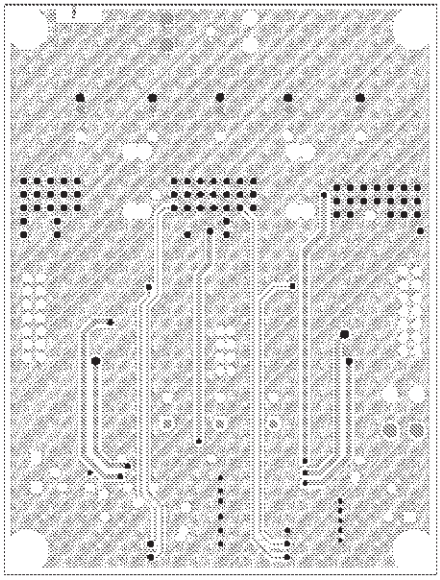
PCB and Components Layouts

Figure 15. PCB and Components Layouts

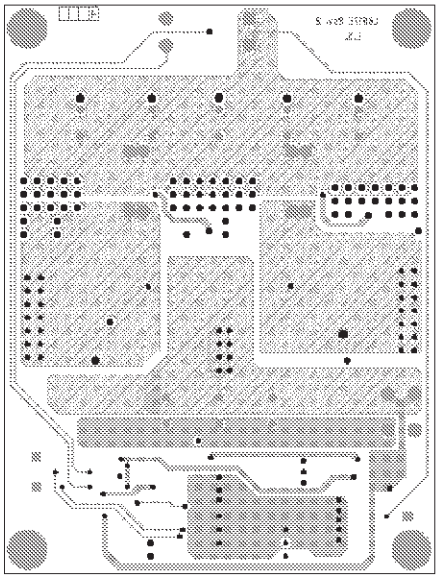


Component Side **Internal PGND Plane**

Figure 16. PCB and Components Layouts



Internal SGND Plane



Solder Side

Design Example.

- Output Voltage (nominal) 1.700V
- Output Current (nominal) 45A
- Static tolerance +100mV; -50mV

Considering the high slope for the load transient, a high switching frequency has to be used. In addition to fast reaction, this helps in reducing output and input capacitor. Inductance value is also reduced.

A switching frequency of 300kHz for each phase is then considered allowing large bandwidth for the compensation network.

- Current Reading Network and Over Current:
  Since the maximum output current is 45A, the over current threshold has to be set at 140% of the maximum nominal current, the over-current threshold has then to be set at 31.5A. Considering to sense the output current across the low-side mosfet RdsON, STB90NF03L has 6.5mΩ max at 25° that becomes 9.1mΩ considering the temperature variation (+40%); the resulting transconductance resistor Rg has to be:

$$Rg = \frac{I_{MAX} \cdot RdsON}{35\mu} = \frac{31.5 \cdot 9.1m}{35\mu} = 8.2k\Omega \text{ (R3 to R6)}$$

- Droop function Design:
  Considering a voltage drop of 100mV at full load, the feedback resistor RFB has to be

$$R_{FB} = \frac{100mV}{50\mu A} = 2k\Omega \text{ (R7)}$$

voltage drop at OCP threshold results in 140mV.

- Inductor design:
  Each phase has to deliver up to 22.5A; considering a current ripple of 5A (<25%), the resulting inductance value is:

$$L = \frac{Vin - Vout}{\Delta I} \cdot \frac{d}{Fsw} = \frac{12 - 1.7}{5} \cdot \frac{1.7}{12} \cdot \frac{1}{300000} = 1\mu H \quad (L1, L2)$$

- Output Capacitor:
  Six PANASONIC SP-CAP EEFUE0D27 (270µF, 15mΩmax) has been used implementing a resulting ESR of 2.5mΩ resulting in a voltage drop of 45A*2.5mΩ =112.5mV after a load transient.
- Compensation Network:
  A voltage loop bandwidth of 40kHz is considered to let the device fast react after load transient.

$$f_{TV} = 20kHz \Rightarrow f_{TI} = f_{TV} \cdot \frac{Rs \cdot R_{FB}}{ESR \cdot Rg} = 20k \cdot \frac{7.8m \cdot 2k}{2.5m \cdot 8.2k} = 15.2kHz$$

The R_F C_F network results:

$$R_F = \frac{Rg}{Rs} \cdot \frac{\Delta Vosc}{Vin} \cdot \frac{L}{2} \cdot \omega_{TI} = \frac{8.2k}{7.8m} \cdot \frac{2}{12} \cdot \frac{1\mu}{2} \cdot 2\pi \cdot 15.2k = 8.2k\Omega \quad (R8)$$

$$C_F = \frac{\sqrt{\frac{L}{2 \cdot C_{OUT}}}}{R_F} = \frac{\sqrt{\frac{1\mu}{2 \cdot 1.62m}}}{8.2k} = 3.4nF \quad (C2)$$

- VID settings:
  Considering the 100mV voltage drop programmed by the feedback resistor and the static tolerance, the VID are set for 1.775V (00011 code) in order to have a ±25mV of margin in the regulation.

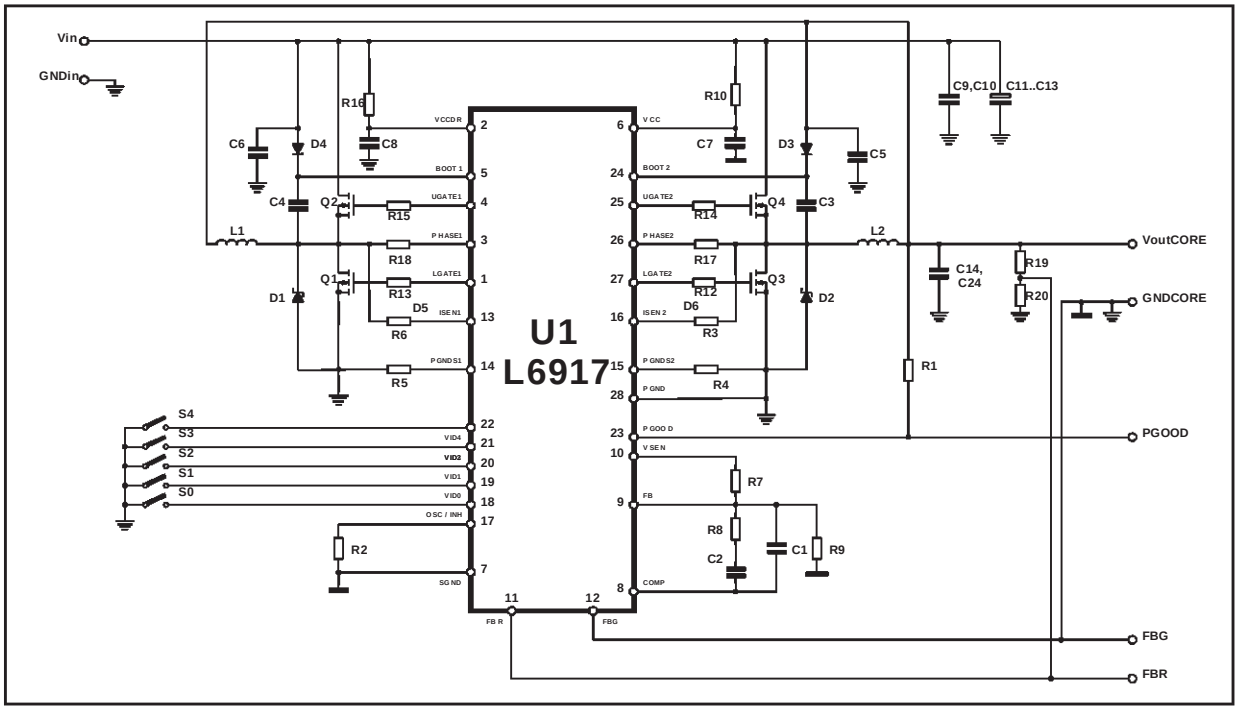
Part List

R1	10k		SMD 0805
R2, R9, R20	Not Mounted		SMD 0805
R3, R4, R5, R6	8.2k	1%	SMD 0805
R7	2k	1%	SMD 0805
R8	10k		SMD 0805
R10	82Ω		SMD 0805
R12 to R15	0Ω		SMD 0805
C2	4.7n		SMD 0805
C3, C4	100n		SMD 0805
C5, C6, C7	1µ	Ceramic	SMD 1206
C8, C9, C10	10µ	Ceramic	SMD 1206
C11, C12, C13	100µ / 20V	OSCON 20SA100M	Radial 10x10.5
C19 to C24	270µ / 2V	PANASONIC SP-CAP	SMD 7343
L1, L2	1µ	77121 Core – 7 Turns or TO50-52B Core – 6 Turns	
U1	L6917	STMicroelectronics	SO28
Q1, Q3	STB90NF03L	STMicroelectronics	D^2PACK
Q2, Q4	STB70NF03L	STMicroelectronics	D^2PACK
D1, D2	STPS340U	STMicroelectronics	SMB
D3, D4	1N4148	STMicroelectronics	SOT23

Application Idea: 12V input 3.3V / 5V 40A output

Figure 17 shows the device in a high current server power supply application.
Adding an external resistor divider after the remote sense buffer gives the possibility to increase the regulated voltage. Considering for example a divider by two (two equal resistors) the DAC range is doubled from 2.200V to 3.700V with 50mV binary steps. It is then possible to regulate the 3.3V and 2.5V rails from the 12V available from the AC/DC converter. The 5V rail can be obtained modifying the external divider. The regulator assures all the advantages of the dual phase conversion (especially in the 5V conversion where the duty cycle is near the 50% and practically no ripple is present in the input capacitors) and a 300kHz free-running frequency that reduces components size. Output current ranges from 35A up to 50A.

Figure 17. Server power supply schematic



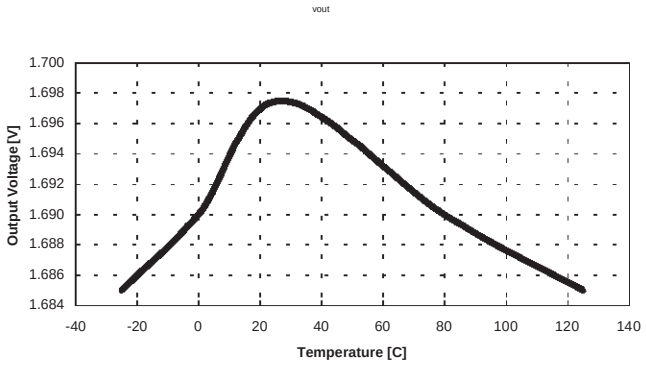
Part List

R1	10k		SMD 0805
R3, R4, R5, R6	8.2k	1%	SMD 0805
R7	820	1%	SMD 0805
R8	10k		SMD 0805
R10	82Ω		SMD 0805
R12 to R16	0Ω		SMD 0805
R17, R18	0Ω		SMD 0805
R19, R20	330Ω		SMD 0805
C2	4.7n		SMD 0805
C3, C4	100n		SMD 0805
C5, C6, C7	1µ	Ceramic	SMD 1206
C8	10µ	Ceramic	SMD 1206
C9 to C13	47µ	Ceramic	SMD 1026

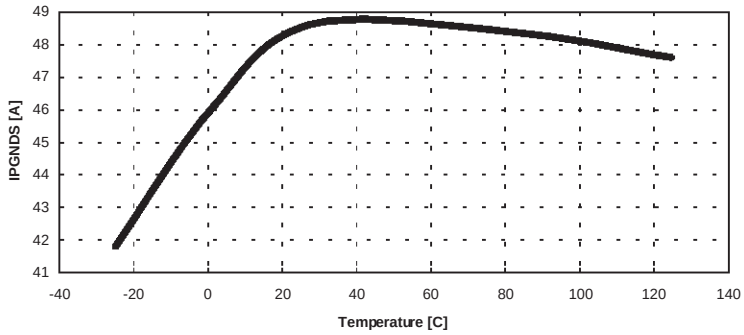
Part List

C14, C15	1500µ / 6.3V		Radial
L1, L2	4µ	77121 Core – 10T (30A Out) or 77848 Core – 11T (45A Out)	
U1	L6917	STMicroelectronics	SO28
Q1, Q3	STB90NF03L	STMicroelectronics	D^2PACK
Q2, Q4	STB70NF03L	STMicroelectronics	D^2PACK
D1, D2	STPS340U	STMicroelectronics	SMB
D3, D4	1N4148	STMicroelectronics	SOT23

Figure 18.



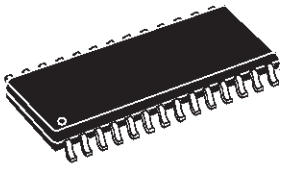
Output Voltage vs. Temperature



PGNDS Bias Current vs. Temperature

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO28