# 2.5V/3.3V SiGe Differential Receiver/Driver with RSECL\* Outputs

## \*Reduced Swing ECL

The SG16 is a Silicon Germanium differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices with much higher bandwidth and lower EMI capabilities.

Inputs incorporate internal 50  $\Omega$  termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), HSTL, GTL, TTL, CMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

The V<sub>BB</sub> and V<sub>MM</sub> pins are internally generated voltage supplies available to this device only. The V<sub>BB</sub> is used for single–ended NECL or PECL inputs and the V<sub>MM</sub> pin is used for CMOS inputs. For all single–ended input conditions, the unused differential input is connected to V<sub>BB</sub> or V<sub>MM</sub> as a switching reference voltage. V<sub>BB</sub> or V<sub>MM</sub> may also rebias AC coupled inputs. When used, decouple V<sub>BB</sub> and V<sub>MM</sub> via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V<sub>BB</sub> and V<sub>MM</sub> outputs should be left open.

- Maximum Frequency > 12 GHz Typical
- 120 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range:  $V_{CC} = 2.375$  V to 3.465 V with  $V_{EE} = 0$  V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -2.375$  V to -3.465 V
- RSECL Output Level (400 mV Peak–to–Peak Output), Differential Output Only
- 50  $\Omega$  Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- $V_{BB}$  and  $V_{MM}$  Reference Voltage Output



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W = Work Week

\*For further details, refer to Application Note AND8002/D

## **ORDERING INFORMATION**

Device	Package	Shipping
NBSG16BA	4x4 mm FCBGA–16	810 Units/Tray
NBSG16BAR2	4x4 mm FCBGA–16	2500/Tape & Reel
NBSG16BA100	4x4 mm FCBGA–16	100 Units/Tray
NBSG16BA500R2	4x4 mm FCBGA–16	500/Tape & Reel

Board	Description
SG16EVB	NBSG16BA Evaluation Board



Figure 1. Pinout (Top View)

NOTE: The NC pins are electrically connected to the die and MUST be left open or both pins can be tied to  $V_{CC}$ .

## **PIN DESCRIPTION**

PIN	FUNCTION
D*, <u>D</u> **	ECL, HSTL, GTL, TTL, CMOS. CML, LVDS compatible inputs
Q, <u>Q</u>	RSECL Data Outputs
VTD, VTD	50 $\Omega$ Internal Input Termination Resistor
V <sub>MM</sub>	CMOS Reference Voltage Output, (V <sub>CC</sub> -V <sub>EE</sub> )/2
V <sub>BB</sub>	ECL Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
NC	No Connect

\* Pin will default low when left open.

\*\* Pin will default to a slightly higher potential than D when both are left open.



## Figure 2. Logic Diagram

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{\text{VTD}}$ to $\text{V}_{\text{CC}}$
LVDS	Connect VTD and $\overline{\text{VTD}}$ together
AC-COUPLED	Bias VTD and VTD Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques

## ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor (D, $\overline{D}$ )		75 kΩ
Internal Input Pullup Resistor (D)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 1)		Level 3
Flammability Rating		UL 94 V–0 @ 0.125 in
Oxygen Index	28 to 34	
Transistor Count	167	
Meets or exceeds JEDEC Spec EIA/JESD7	8 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	Positive Power Supply	$V_{EE} = 0 V$		3.6	V
$V_{EE}$	Negative Power Supply	$V_{CC} = 0 V$		-3.6	V
VI	Positive Input Negative Input	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	$\begin{array}{c} V_{I} \leq V_{CC} \\ V_{I} \geq V_{EE} \end{array}$	3.6 -3.6	V V
l <sub>out</sub>	Output Current	Continuous Surge		25 50	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			1	mA
I <sub>MM</sub>	V <sub>MM</sub> Sink/Source			1	mA
ТА	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction to Ambient) (Note 3)	0 LFPM 500 LFPM	16 FCBGA 16 FCBGA	108 86	°C/W °C/W
$\theta_{\text{JC}}$	Thermal Resistance (Junction to Case)	1S2P (Note 3)	16 FCBGA	5	°C/W
T <sub>sol</sub>	Wave Solder	< 15 sec.		225	°C

Maximum Ratings are those values beyond which device damage may occur.
JEDEC standard multilayer board – 1S2P (1 signal, 2 power)

		-40°C				25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 5)	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
V <sub>PP</sub>	Output P–P Voltage	350	410	525	350	410	525	350	410	525	mV
V <sub>IH</sub>	Input HIGH Voltage (Single Ended) (Note 6)	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V
VIL	Input LOW Voltage (Single Ended) (Note 6)	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V
V <sub>BB</sub>	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 7)	1.2		2.5	1.2		2.5	1.2		2.5	V
V <sub>MM</sub>	CMOS Output Voltage Reference V <sub>CC</sub> /2	1200	1250	1400	1200	1250	1400	1200	1250	1400	mV
R <sub>T</sub>	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
IIH	Input HIGH Current (@ VIH)		30	100		30	100		30	100	μA
IIL	Input LOW Current (@ VIL)		25	50		25	50		25	50	μA

## DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V<sub>CC</sub> = 2.5 V: V<sub>EE</sub> = 0 V (Note 4)

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.125 V to -0.965 V.

5. All loading with 50 ohms to  $V_{CC}$ =2.0 volts. 6.  $V_{THR}$  is the voltage applied to the complementary input, typically  $V_{BB}$  or  $V_{MM}$ .

7. VIHCMR min varies 1:1 with VEE, VIHCMR max varies 1:1 with VCC. The VIHCMR range is referenced to the most positive side of the differential input signal.

\*Typicals used for testing purposes.

#### DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V<sub>CC</sub> = 3.3 V; V<sub>EE</sub> = 0 V (Note 8)

		–40°C			25°C						
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 9)	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
V <sub>PP</sub>	Output P–P Voltage	350	410	525	350	410	525	350	410	525	mV
V <sub>IH</sub>	Input HIGH Voltage (Single Ended) (Note 10)	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage (Single Ended) (Note 10)	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V
V <sub>BB</sub>	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 11)	1.2		3.3	1.2		3.3	1.2		3.3	V
V <sub>MM</sub>	CMOS Output Voltage Reference $V_{CC}/2$	1600	1650	1800	1600	1650	1800	1600	1650	1800	mV
R <sub>T</sub>	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I <sub>IH</sub>	Input HIGH Current (@ VIH)		30	100		30	100		30	100	μΑ
IIL	Input LOW Current (@ VIL)		25	50		25	50		25	50	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.925 V to -0.165 V.

9. All loading with 50 ohms to V<sub>CC</sub>-2.0 volts.

10. V<sub>THR</sub> is the voltage applied to the complementary input, typically V<sub>BB</sub> or V<sub>MM</sub>.

11. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

\*Typicals used for testing purposes.

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>EE</sub>	Power Supply Current	17	23	29	17	23	29	17	23	29	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 13)	-1050	-970	-925	-975	-935	-900	-950	-910	-875	mV
V <sub>PP</sub>	Output P-P Voltage	350	410	525	350	410	525	350	410	525	mV
V <sub>IH</sub>	Input HIGH Voltage (Single Ended) (Note 14)	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V <sub>THR</sub> + 75 mV	V <sub>CC</sub> – 1.0*	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage (Single Ended) (Note 14)	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V <sub>EE</sub>	V <sub>CC</sub> – 1.4*	V <sub>THR</sub> – 75 mV	V
V <sub>BB</sub>	NECL Output Voltage Reference	-1420	-1360	-1300	-1420	-1360	-1300	-1420	-1360	-1300	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Differential) (Note 15)	V <sub>EE</sub> +	-1.2	0.0	V <sub>EE</sub> 4	-1.2	0.0	V <sub>EE</sub> +	+1.2	0.0	V
V <sub>MM</sub>	CMOS Output Voltage Reference (Note 16)	V <sub>MMT</sub> – 50	V <sub>MMT</sub>	V <sub>MMT</sub> + 150	V <sub>MMT</sub> – 50	V <sub>MMT</sub>	V <sub>MMT</sub> + 150	V <sub>MMT</sub> – 50	V <sub>MMT</sub>	V <sub>MMT</sub> + 150	mV
I <sub>IH</sub>	Input HIGH Current (@ VIH)		30	100		30	100		30	100	μΑ
IIL	Input LOW Current (@ VIL)		25	50		25	50		25	50	μΑ

#### DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT V<sub>CC</sub> = 0 V; V<sub>EE</sub> = -3.465 V to -2.375 V (Note 12)

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with  $V_{CC}$ . 13. All loading with 50 ohms to  $V_{CC}$  –2.0 volts. 14.  $V_{THR}$  is the voltage applied to the complementary input, typically  $V_{BB}$  or  $V_{MM}$ . 15.  $V_{HCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{HCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{HCMR}$  range is referenced to the most positive side of the differential input varies 1:1 with  $V_{EE}$ . input signal.

16.  $V_{MM}$  typical =  $|V_{CC} - V_{EE}|/2 + V_{EE} = V_{MMT}$ \*Typicals used for testing purposes.

			–40°C		25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Мах	Min	Тур	Max	Unit
f <sub>max</sub>	Maximum Frequency (See Figure 3. F <sub>max</sub> /JITTER) (Note 17)	10.709	> 12		10.709	> 12		10.709	> 12		GHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay to Output Differential	90	110	130	100	120	140	105	125	145	ps
t <sub>SKEW</sub>	Duty Cycle Skew (Note 18)		3	15		3	15		3	15	ps
<sup>t</sup> JITTER	Cycle-to-Cycle Jitter (RMS) (See Figure 3. F <sub>max</sub> /JITTER) (Note 17)		0.3	< 1		0.3	< 1		0.3	< 1	ps
V <sub>INPP</sub>	Input Voltage Swing/Sensitivity (Differential) (Note 19)	75		2600	75		2600	75		2600	mV
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	30	45	75	20	40	65	20	40	65	ps

#### AC CHARACTERISTICS Voc = 0 V: VEE = -3,465 V to -2,375 V or Voc = 2,375 V to 3,465 V: VEE = 0 V

17. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 ohms to V<sub>CC</sub>-2.0 V.

18. See Figure 5.  $t_{skew} = |t_{PLH} - t_{PHL}|$  for a nominal 50% differential clock input waveform.

19. VINPP(max) cannot exceed V<sub>CC</sub> - V<sub>EE</sub>



Figure 3. F<sub>max</sub>/Jitter



X = 17ps/Div Y = 70 mV/Div

Figure 4. 10.709 Gb/s Diagram (3.0 V, 25°C)



Figure 5. AC Reference Measurement



Figure 6. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

#### PACKAGE DIMENSIONS



NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS 2. INTERPRET DIMENSIONS AND TOLERANCES
- PER ASME Y14.5M. 1994. DIMENSION b IS MEASURED AT THE MAXIMUM
- \_3. SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
- /4.
- LATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF ∕₅. PACKAGE

	MILLIMETERS								
DIM	MIN	MAX							
Α	1.40	MAX							
A1	0.25	0.35							
A2	1.20	REF							
b	0.30	0.50							
D	4.00	BSC							
Е	4.00	BSC							
е	1.00	1.00 BSC							
S	0.50	BSC							

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