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ADMC330 PROCESSOR BOARD

INTRODUCTION

The *ADMC330 PROCESSOR BOARD* is a compact, highly flexible evaluation and development board for the low cost, single-chip DSP-based motor controller, the ADMC330. The device provides the following significant features:

- 20 MIPS, Fixed-Point, 16-bit DSP Core.
- 2K Internal Program and 1K Data Memory RAM.
- 2K Internal Program Memory ROM, offering Debugger Interface and Pre-Programmed Math and Motor Control Functions.
- Seven Analog input channels..
- A Three-Phase, 12-bit PWM Generator.
- 8 General Purpose I/O Lines, Configurable as Inputs or Outputs.
- Two Synchronous Serial Ports.
- Two 8-Bit, Auxiliary PWM Outputs.
- A 16-Bit Watchdog Timer.
- A General Purpose, Interval Timer with Prescaler.

Refer to the ADMC330 datasheet for a full description of all features of the ADMC330.

The *ADMC330 PROCESSOR BOARD* is intended as a compact, highly-integrated evaluation and software development platform for the ADMC330 controller. The processor board permits access through a UART connection to the *Motion Control Debugger* software that operates under Windows 95™ or Windows NT™. The *Motion Control Debugger* is used to download executable code, examine the contents of registers, program memory and data memory, run executable modules, set breakpoints and enable single-step operation.

The processor board is designed for compact size so that all relevant input and output signals are brought to three connector headers underneath the board. The processor board contains the following features and components:

- The ADMC330 Single-Chip DSP-Based Controller.
- A 10 MHz crystal to provide the CLKIN frequency.
- A power-on reset circuit based on the ADM709 that is used to provide a reset signal to the ADMC330 and UART communications port. A push button is also provided to initiate a processor and system reset.
- A socket for a serial memory device (ROM or E^2PROM) that may be used for serial boot loading on power up for stand alone operation.
- An isolated UART interface to the *Motion Control Debugger*. The signals are optically isolated from the remainder of the processor board. The AD7306 is used to drive the appropriate signals on the 9-way UART connector.
- An +5V, and GND input power supply connector.
- An on board 5V to 5V dc-dc converter that provides an isolated 5V supply for the UART interface circuit.
- Analog interface circuitry.
- Jumpers that permit setting of the PWM polarity, enabling or disabling of the PWMTRIP input, enabling the ADMC330 to used as a master or slave device and enabling or disabling the serial memory device in the socket.
- Three socket blocks underneath the processor board that permit access to all of the input and output signals of interest. The three sockets comprise two digital sockets (IF1 and IF3) and one analog socket (IF2).

The *ADMC330 PROCESSOR BOARD* may operate in a stand-alone mode, where the user must supply only the appropriate power supply voltage and either a UART connection to the *Motion Control Debugger* or a suitable serial memory device. In this case, the user must provide suitable connectors to interface to the various input and output signals on the expansion connectors underneath the board. Alternatively, the processor board may be plugged into the *ADMC CONNECTOR BOARD*. The connector board provides easy access to all relevant input and output signals via appropriate connectors and terminal blocks. The connector board also provides an easy interface to the International Rectifier PowIRtrain™ modules to permit development of

complete motor control solutions. In addition, the connector board adds new functionality including an 8-channel, 10-bit, serial DAC, and a large prototype area for system expansion. Refer to the documentation for the *ADMC CONNECTOR BOARD* for further details.

POWER SUPPLY REQUIREMENTS

The *ADMC330 PROCESSOR BOARD* contains a 2-way terminal block for connection of external power supplies. For correct operation, the following supplies are required:

- +5V ± 10%, 200 mA (VDD)
- Ground

The VDD supply powers the digital logic circuits of the processor board, including the ADMC330 controller. In addition, it is used as the analog voltage supply of the ADMC330 and as the input to the dc-dc converter that provides the isolated supply for the UART interface. The processor board is laid out with separate analog and digital ground planes that are connected by a link (JP1) close to the power supply terminal block for noise immunity. This link should not be removed. A LED on the processor board indicates correct connection of the VDD supply.

Appropriate decoupling capacitors are provided on the processor board for the power supply input (VDD) to reduce noise coupling from the external power supply. However, for best performance, well-regulated external power supplies and correct wiring are recommended.

The arrangement on the input power supply connector is illustrated in Figure 1.

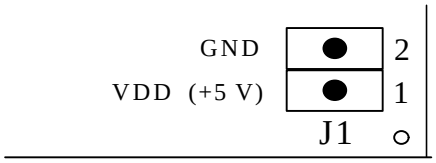


Figure 1: Power Supply Connector of *ADMC330 PROCESSOR BOARD*

FUNCTIONAL DESCRIPTION OF PROCESSOR BOARD

A complete set of schematics of the *ADMC330 PROCESSOR BOARD* are provided at the end of this document. Refer to these schematics for exact description of the functionality of the processor board. This section is intended as a functional description only of the major elements of the board.

UART Interface

A UART interface to the *Motion Control Debugger* is provided on the *ADMC330 PROCESSOR BOARD* via a 9-way D-type connector (P1). In order to separate the ADMC330 and any power conversion stage used in a complete motor drive system, the UART interface is optically isolated from the remainder of the processor board.

The *Motion Control Debugger* communicates through serial port 1 (SPORT1) of the ADMC330 using the DR1B and DT1 pins. In addition, the ADMC330 reset signal (ICRESET) is sent to the UART interface to ensure that a processor board reset is detected by the *Motion Control Debugger*. The three signals, DR1B, DT1 and ICRESET are optically isolated using two HCPL0630 dual isolators (U2 & U4). The signals DT1 and ICRESET are considered as outputs as these signals are sent from the processor board to the debugger. These signals are applied to one opto-isolator. Conversely, the signal DR1B is considered as an input as it is received by the processor board. This signal is isolated using the second isolator U2. The secondary supply for the optical isolators is produced on the processor board by the NME0505S power supply (isolated +5V to +5V dc-dc converter).

The *ADMC330 PROCESSOR BOARD* also contains an AD7306 transceiver (U1) that converts the TTL signals to the appropriate ±10 V levels suitable for the UART connection to the PC. A standard PC serial cable may be used to connect from the 9-way female socket of the processor board to the appropriate COM port of the PC. The baud rate and COM port to be used on the PC may be set from the *ADMC330 Comm Config* software that is part of the *Motion Control Debugger*.
A functional block diagram of the UART interface circuit is shown in Figure 2. The direction of the three

signals is indicated in the figure. Refer to the full schematics at the end of this document for the full circuit. Recall that the secondary supply for the optical isolators and the AD7306 is derived on the processor board by the isolated dc-dc converter, the NME0505S (U3).

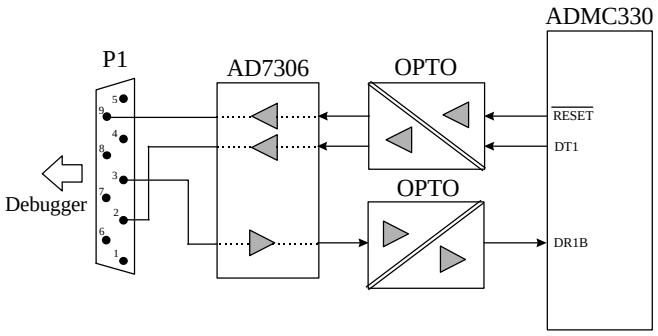


Figure 2: Functional Block Diagram of UART Interface to *Motion Control Debugger* of *ADMC330 PROCESSOR BOARD.*

Power On Reset Circuit

The *ADMC330 PROCESSOR BOARD* contains a power-on reset (POR) based on the ADM709 (U7). The ADM709 generates a low $\overline{\text{RESET}}$ pulse of 140 ms duration whenever the VCC pin is brought below the threshold value. This pulse occurs automatically on power on and is applied directly to the $\overline{\text{RESET}}$ pin of the ADMC330 to reset the device. In addition, the ADMC330 can be reset by pressing the S1 push button that causes the voltage level at the VCC pin to be brought below the threshold. Resistor R10 and capacitor C21 limit the rise of voltage at the VCC pin. The $\overline{\text{RESET}}$ signal is also fed to the UART interface, as described previously, to permit the *Motion Control Debugger* to detect a system reset.

Serial ROM Interface

For normal program development, it is envisaged that the *Motion Control Debugger* would be used to download executable code to the *ADMC330 PROCESSOR BOARD.* However, as program development stabilizes, it may be required to operate the processor board in a stand-alone mode in the target application. For this reason, the processor board contains an 8-pin DIP socket (U6) for installation of a serial memory device that can be used to boot load the program and data memory RAM of the ADMC330.

Either a one-time programmable serial ROM device, such as the XC1765D Xilinx, or an electrically erasable device, such as the AT17C65 E^2PROM from Atmel, are recommended. In both cases, the application executable file can be converted to a form suitable for the serial memory devices using the *MAKEPROM* utility that is installed as part of the *Motion Control Debugger.*

For both memory devices, a three-wire connection to SPORT1 of the ADMC330 is used. An illustration of the connection of the serial memory device to the ADMC330 is shown in Figure 3. The connection of the 10 MHz crystal and associated capacitors is also shown in the figure.

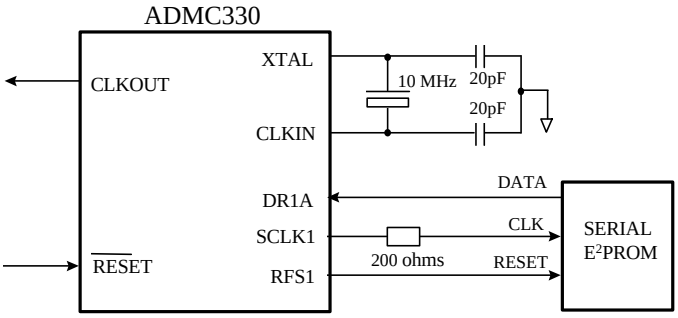


Figure 3: Connection of serial memory (ROM or E^2PROM) and crystal to the ADMC330.

The DATA line of the serial memory device is connected to the DR1A pin of the ADMC330. The RESET line of the memory is connected to the PIO0 pin of the ADMC330 and the CLK line of the memory is driven by the SCLK1 pin of the ADMC330. Following activation of the $\overline{\text{RESET}}$ pin of the ADMC330, the PIO0 pin is pulsed low to reset the serial memory device. Subsequently, data is clocked synchronously into the ADMC330 from the memory device at a rate of CLKOUT/20 (or 1.0 MB/s for the processor board with a 10 MHz crystal). If a serial memory device is not present, the ADMC330 automatically converts to UART communication mode.

The chip enable line (CEB) of the serial memory device is tied to a jumper (JP3) on the processor board. This jumper may be used to tie the CEB pin to either VDD or GND. In order to enable the serial memory device in the socket, it is necessary to tie this pin to GND (position. 2-3). Conversely, the SROM or E^2PROM may be left in

the socket and disabled by tying the CEB pin to VDD (position 1-2).

The programming pin of the serial memory device is pulled high on the processor board to disable this feature. However, this pin is also connected to the IF1 (pin 30 IF1B) interface connector underneath the processor board. This enables this pin to be pulled low by external hardware so that writing to the E^2PROM would be possible. Obviously, it is necessary to respect the particular operational requirements of the chosen serial E^2PROM if such a feature is to be attempted. Clearly, this programming feature is applicable only to E^2PROMs and not to one-time programmable serial ROMs.

Master / Slave configuration

The *ADMC330 PROCESSOR BOARD* can be configured either in a master or slave configuration. The driving capability of the serial clocks (SCLK0, SCLK1) is not enough to send signals over long cables. Therefore a 74F243 transceiver is used. For PCB distances a 200 Ω resistor can be used, as seen in figure 3.

Analog Interface

The *ADMC330 PROCESSOR BOARD* permits up to seven analog inputs to be applied to the ADMC330 via the IF2 interface connector. There is a one stage passive anti-aliasing low pass filter at the input of each of the A/D converter channels. The RC filter values are 10kΩ and 3.3nF which give a cut off frequency of 5kHz. An external capacitor, charged by a constant current source, is required in the socket J2 to generate the reference ramp voltage (0.3-3.3V). The jumper JP2 connects the analog input channel VAUX3 either to an external analog input, through the RC filter or the VREF pin on the ADMC330.

Jumper Settings

The *ADMC330 PROCESSOR BOARD* contains five jumpers that:

- Permit selection of ADMC330 VREF or external analog input to VAUX3 (JP2)
- Permit enabling/disabling of the SROM/E^2PROM in socket U6 (JP3).
- Permit selection of the PWM polarity (JP4).
- Permit enabling/disabling of the $\overline{\text{PWMTRIP}}$ input (JP5).
- Permit selection of Master / Slave configuration (JP6)

The settings of the three jumpers are described in Table 1. Connecting JP2 in the 1-2 position connects the analog input channel VAUX3 to an external analog input. On the other hand, connecting JP2 in the 2-3 position connects VAUX3 to VREF.

Connecting JP3 in the 1-2 position ties the chip enable pin (CEB) of the serial memory socket (U6) to VDD and disables the memory device. If a serial memory device is required, the jumper JP4 must be placed in the 2-3 position to enable the memory.

Connecting JP4 in the 1-2 position ties the PWMPOL pin of the ADMC330 to VDD and enables active HI PWM outputs. On the other hand, connecting JP4 in the 2-3 position creates active LO PWM outputs from the ADMC330. The appropriate setting for this jumper is determined by the exact nature of the gate drive circuit of the target system. The PWMPOL pin is also connected to the interface connector IF3 so that its state can be detected or altered by external hardware.

Connecting jumper JP5 in the 1-2 position ties the $\overline{\text{PWMTRIP}}$ pin of the ADMC330 to VDD and permanently enables PWM outputs. On the other hand, connecting jumper JP5 in the 2-3 position connects the $\overline{\text{PWMTRIP}}$ pin of the ADMC330 to the corresponding pin of the IF3 interface connector. External hardware may be used to derive the appropriate signal for this pin.

Connecting JP6 in the 1-2 position enables the ADMC330 to be configured as a master processor. On the other hand, connecting JP3 in the 2-3 position enables the ADMC330 to be configured as a slave processor.

JP1 is a link that connects the analog and digital ground planes of the processor board together. For correct operation, this link must not be removed.

Jumper	Position	Function
JP2	1-2	Connects external analog input to VAUX3
	2-3	Connects VREF to VAUX3
JP3	1-2	Disable SROM/E^{2}PROM
	2-3	Enable SROM/E^{2}PROM
JP4	1-2	PWM Outputs Active HI
	2-3	PWM Outputs Active LO
JP5	1-2	Enable PWMTRIP via IF3 connector
	2-3	Disable PWMTRIP input
JP6	1-2	Selects ADMC330 as Slave.
	2-3	Selects ADMC330 as Master.

Table 1: Jumper settings of *ADMC330 PROCESSOR BOARD*.

Interface Connectors

In order to create as compact an evaluation and development board as possible, all input and output signals are brought to three interface connectors underneath the processor board. Two connectors (IF1 and IF3) are dedicated to digital signals and the third (IF2) is reserved for analog signals. This three connector interface will be used in future processor boards for future motion control products from Analog Devices. Therefore, many of the pins on the connectors for the *ADMC330 PROCESSOR BOARD* are unconnected (n/c). These pins are reserved for other functions in future products.

Interface connectors IF1 and IF3 are both 3-way by 30 pin connectors. Connector IF2 is 3-way by 24 pins. The exact connections to this interface may be seen in the schematics at the end of this document. The connections are tabulated for connector IF1 in Table 2, for connector IF2 in Table 3 and for connector IF3 in Table 4.

IF1A		IF1B		IF1C	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	n/c	**1**	n/c	**1**	n/c
2	n/c	**2**	n/c	**2**	n/c
3	n/c	**3**	n/c	**3**	n/c
4	n/c	**4**	n/c	**4**	n/c
5	n/c	**5**	n/c	**5**	n/c
6	n/c	**6**	n/c	**6**	n/c
7	n/c	**7**	n/c	**7**	n/c
8	n/c	**8**	n/c	**8**	n/c
9	VDD	**9**	VDD	**9**	VDD
10	GND	**10**	GND	**10**	GND
11	n/c	**11**	n/c	**11**	n/c
12	n/c	**12**	n/c	**12**	n/c
13	n/c	**13**	n/c	**13**	n/c
14	n/c	**14**	n/c	**14**	n/c
15	n/c	**15**	n/c	**15**	n/c
16	n/c	**16**	n/c	**16**	n/c
17	n/c	**17**	n/c	**17**	n/c
18	n/c	**18**	n/c	**18**	ICRESET
19	n/c	**19**	n/c	**19**	n/c
20	n/c	**20**	n/c	**20**	CLKOUT
21	n/c	**21**	n/c	**21**	n/c
22	n/c	**22**	n/c	**22**	n/c
23	GND	**23**	GND	**23**	n/c
24	SCLK0	**24**	SCLK1	**24**	n/c
25	TFS0	**25**	TFS1	**25**	n/c
26	RFS0	**26**	RFS1	**26**	n/c
27	DR0	**27**	DR1A	**27**	n/c
28	DT0	**28**	DR1B	**28**	n/c
29	n/c	**29**	DT1	**29**	n/c
30	n/c	**30**	E^{2}PROG	**30**	n/c

Table 2: Definition of digital interface connector IF1 of *ADMC330 PROCESSOR BOARD*.

IF2A	IF2B	IF2C

Pin	Signal	Pin	Signal	Pin	Signal
1	VIN1	**1**	GND	**1**	n/c
2	VIN2	**2**	GND	**2**	n/c
3	VIN3	**3**	GND	**3**	n/c
4	VIN4	**4**	GND	**4**	n/c
5	VIN5	**5**	GND	**5**	n/c
6	VIN6	**6**	GND	**6**	n/c
7	VIN7	**7**	GND	**7**	n/c
8	n/c	**8**	GND	**8**	n/c
9	n/c	**9**	GND	**9**	n/c
10	n/c	**10**	GND	**10**	n/c
11	n/c	**11**	GND	**11**	n/c
12	n/c	**12**	GND	**12**	n/c
13	n/c	**13**	n/c	**13**	n/c
14	n/c	**14**	n/c	**14**	n/c
15	VREF	**15**	GND	**15**	n/c
16	n/c	**16**	GND	**16**	n/c
17	n/c	**17**	GND	**17**	n/c
18	n/c	**18**	GND	**18**	n/c
19	n/c	**19**	GND	**19**	n/c
20	n/c	**20**	GND	**20**	n/c
21	n/c	**21**	GND	**21**	n/c
22	n/c	**22**	GND	**22**	n/c
23	n/c	**23**	GND	**23**	n/c
24	n/c	**24**	GND	**24**	n/c

Table 3: Definition of analog interface connector IF2 of *ADMC330 PROCESSOR BOARD*.

				n	
1	AH	**1**	BH	**1**	CH
2	AL	**2**	BL	**2**	CL
3	PWMSYNC	**3**	$\overline{\text{PWMTRIP}}$	**3**	n/c
4	PWMPOL	**4**	n/c	**4**	n/c
5	n/c	**5**	n/c	**5**	n/c
6	n/c	**6**	n/c	**6**	n/c
7	n/c	**7**	n/c	**7**	n/c
8	n/c	**8**	n/c	**8**	n/c
9	n/c	**9**	n/c	**9**	n/c
10	n/c	**10**	n/c	**10**	n/c
11	n/c	**11**	n/c	**11**	n/c
12	AUX0	**12**	AUX1	**12**	CLKOUT
13	n/c	**13**	n/c	**13**	n/c
14	VDD	**14**	VDD	**14**	VDD
15	GND	**15**	GND	**15**	GND
16	n/c	**16**	n/c	**16**	n/c
17	n/c	**17**	n/c	**17**	n/c
18	n/c	**18**	n/c	**18**	n/c
19	PIO0	**19**	PIO1	**19**	PIO2
20	PIO3	**20**	PIO4	**20**	PIO5
21	PIO6	**21**	PIO7	**21**	n/c
22	n/c	**22**	n/c	**22**	n/c
23	n/c	**23**	n/c	**23**	n/c
24	n/c	**24**	n/c	**24**	n/c
25	n/c	**25**	n/c	**25**	n/c
26	n/c	**26**	n/c	**26**	n/c
27	n/c	**27**	n/c	**27**	n/c
28	n/c	**28**	n/c	**28**	n/c
29	n/c	**29**	n/c	**29**	n/c
30	n/c	**30**	n/c	**30**	n/c

Table 4: Definition of digital interface connector IF3 of *ADMC330 PROCESSOR BOARD*

The description of the various connections to the three interface connectors is given in Table 5.

IF3A		IF3B		IF3C	
Pin	**Signal**	**Pin**	**Signal**	**Pi**	**Signal**

Signal(s)	Function
VDD	+5 V power supply

GND	Ground
ICRESET	Reset pin of ADMC330
SCLK0, TFS0, RFS0, DT0, DR0	SPORT0 pins of ADMC330
SCLK1, TFS1, RFS1, DR1A, DR1B, DT1	SPORT1 pins of ADMC330
E^2PROG	E^2PROM programming pin
VIN1 - VIN7	Analog inputs
VREF	Reference voltage output
AH - CL	TTL-level PWM outputs
PWMSYNC	PWMSYNC pulse of ADMC330
$\overline{\text{PWMTRIP}}$	$\overline{\text{PWMTRIP}}$ pin of ADMC330
PWMPOL	PWM polarity pin of ADMC330
PIO0 - PIO7	Dedicated programmable input/ outputs of ADMC330.
PIO0	SROM / E^2PROM Reset signal
CLKOUT	TTL-level CLKOUT signal
AUX0, AUX1	TTL-level auxiliary PWM outputs

Table 5: Function of signals on interface connectors of *ADMC330 PROCESSOR BOARD*.

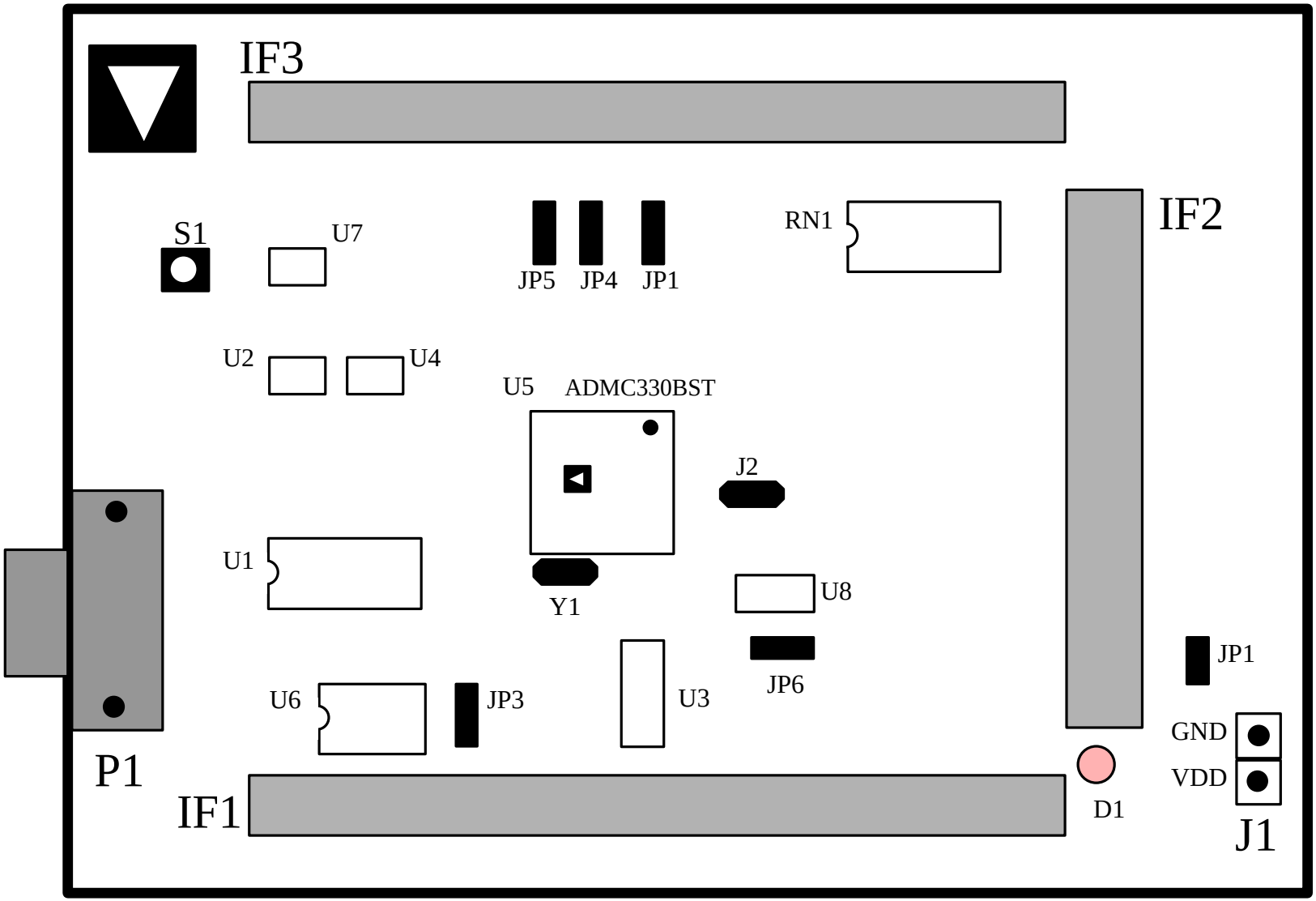
Components, Placement & Schematics

The various integrated circuits on the *ADMC330 PROCESSOR BOARD* are tabulated in Table 6..

Designator	Integrated circuit
U1	AD7306JR Transceiver
U2	HCPL0630 Opto-isolator
U3	NME0505S dc/dc converter
U4	HCPL0630 Opto-isolator
U5	ADMC330 DSP Controller
U6	SROM/E^2PROM socket
U7	ADM709MAR - Power on Reset

Table 6: Main integrated circuits of *AMDC330 PROCESSOR BOARD.*

The board layout and circuit schematics are shown in the following pages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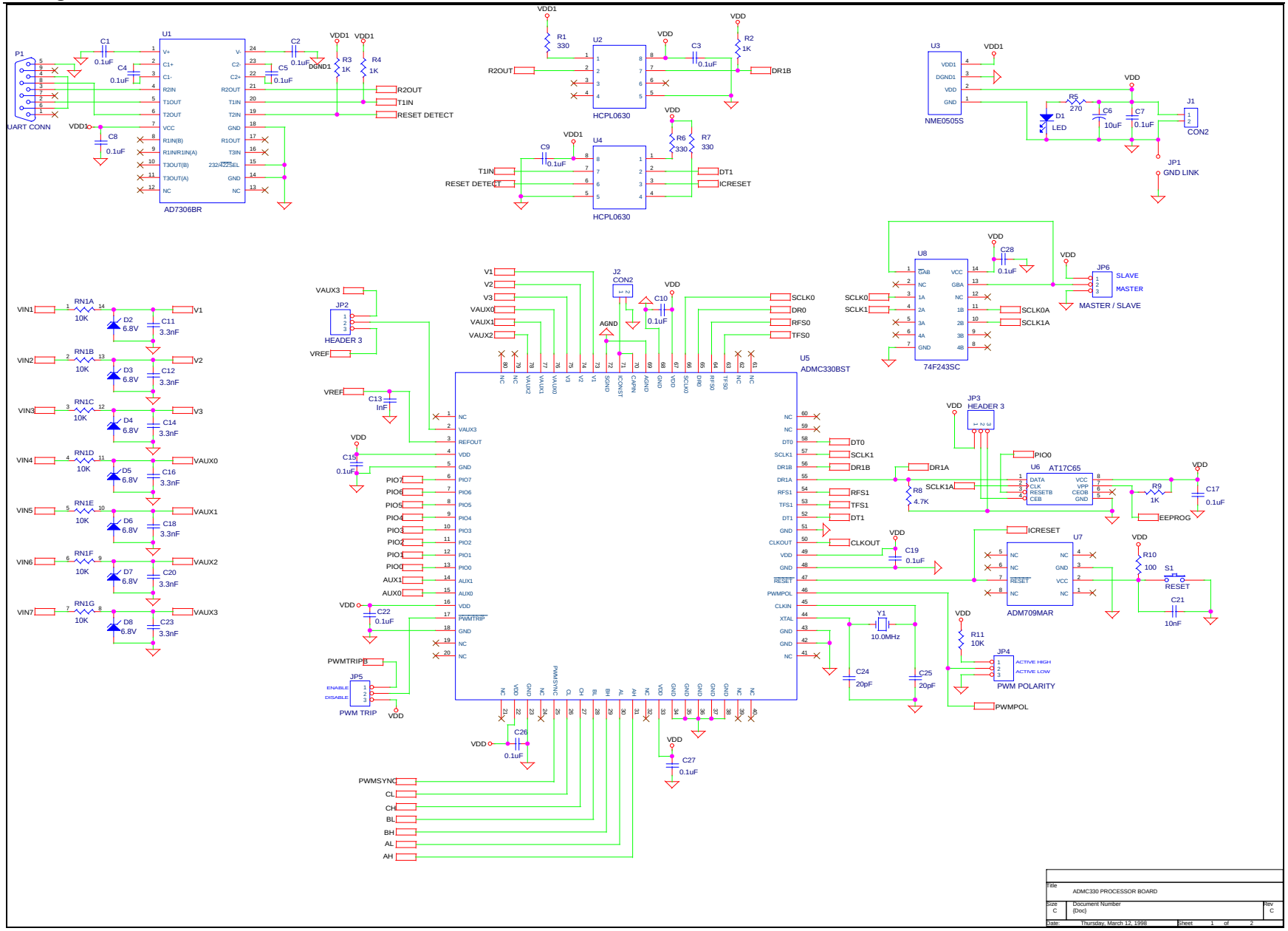

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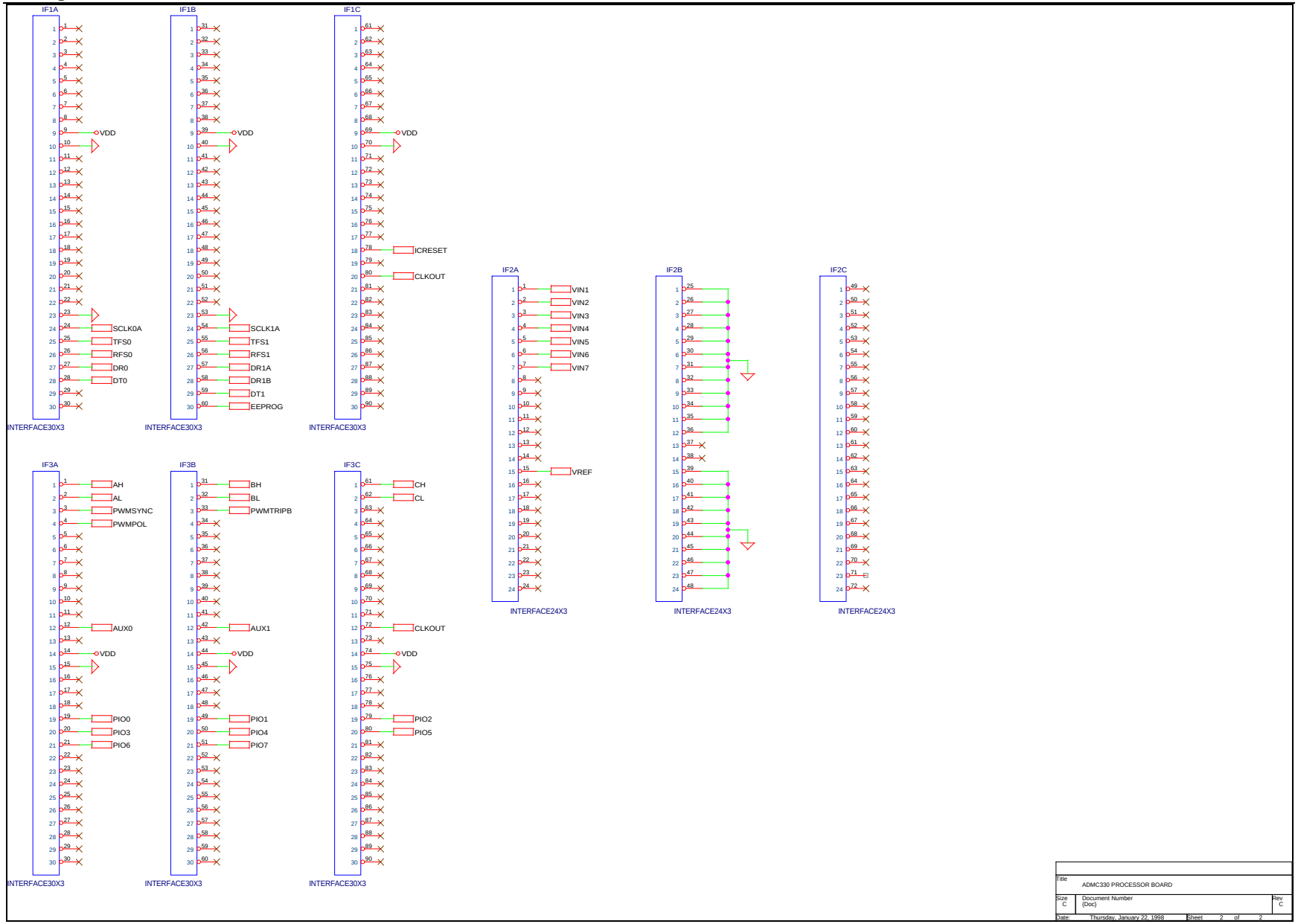
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DR1B
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