



DSM2150F5V

DSM (Digital Signal Processor System Memory) For Analog Devices General Purpose DSPs

FEATURES SUMMARY

■ Glueless Connection to DSP

- 512K x 8 or 256K x 16 (8 or 16 bit operation)
- Easily add memory, logic, and I/O to the external memory interface (EMI) of Analog Devices' general purpose DSP families

■ Dual Flash Memories

- 512K x 8 Main Flash memory divided into eight, 64 KByte sectors.
- 32K x 8 Secondary Flash memory divided into four, 8 KByte sectors.
- Small sector size ideal for storing small data sets, and calibration or configuration constants.
- Concatenate Secondary Flash with Main Flash for total of 544 KBytes.
- Each Flash sector can be write protected.
- Built-in programmable address decoding logic allows mapping individual Flash sectors to any address boundary.

■ Up to 40 Multifunction I/O Pins

- Increase total DSP system I/O capability
- I/O controlled by DSP software or PLD logic

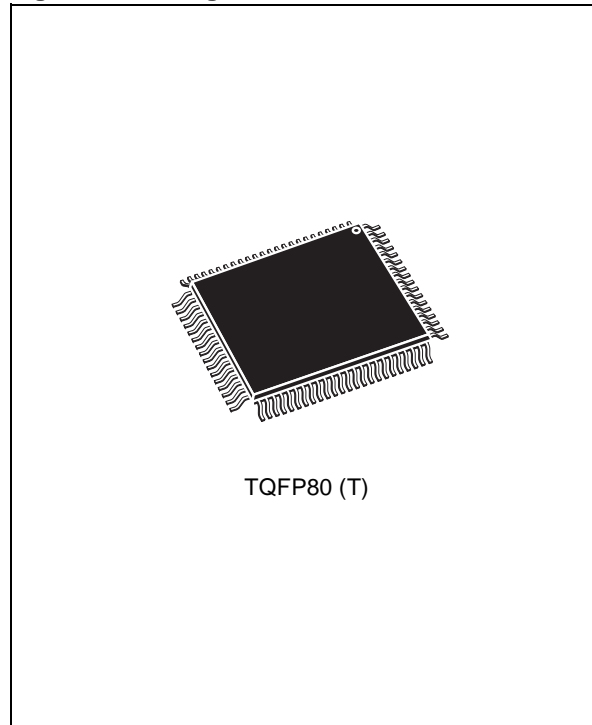
■ General purpose PLD

- Over 3,000 Gates of PLD with 16 macrocells
- Use for peripheral glue logic to keypads, control panel, displays, LCDs, and other devices.
- Eliminate PLDs and external logic devices
- Create state machines, chip selects, simple shifters and counters, clock dividers, delays
- Simple PSDsoft Express software ...Free

■ In-System Programming (ISP) with JTAG

- Program entire chip in 20-35 seconds with no involvement of the DSP
- Links with JTAG debug port on DSP
- Eliminate sockets for pre-programmed memory and logic devices
- ISP allows efficient manufacturing and product testing supporting Just-In-Time inventory
- Use low-cost FlashLINK™ JTAG programmer with PC

Figure 1. Packages



TQFP80 (T)

■ Content Security

- Programmable Security Bit blocks access of device programmers and readers

■ Operating Range

- V_{CC} : 3.3V±10%
- Temperature: -40°C to +85°C

■ Zero-Power Technology

- 100 μ A standby current (typical)

■ Packaging

- 80-pin TQFP

■ Flash Memory Speed, Endurance, Retention

- 120 ns, 100K cycles, 15 year retention

SUMMARY DESCRIPTION

The DSM2150F5 provides a turn-key system memory solution for the Analog Devices general purpose DSP families. With dual in-system programmable (ISP) Flash memories, parameter storage, programmable logic, and additional I/O, the combination of the DSM2150F5 with the DSP results in a simple and flexible two-chip DSP system. On-chip memory decode logic simplifies mapping the dual banks of Flash memory to the DSP for boot loading, code execution, data recording, code swapping, and parameter storage. An on-chip JTAG ISP port allows blank DSM devices to be programmed on the circuit board, thus reducing development time, simplifying manufacturing flow, lowering the cost of field upgrades, and eliminating the need for sockets and pre-programmed memory and logic devices. The DSM's JTAG interface may also be chained with the DSP's JTAG debug interface for quick code iterations on the bench. JTAG ISP is accomplished via the FlashLINK JTAG programmer which plugs into any PC or laptop parallel port.

In addition to ISP Flash memory, DSM devices add programmable logic (PLD) and up to 16 con-

figurative I/O pins to the DSP system. PLD and I/O configuration are programmable by JTAG ISP, just like the Flash memory. The PLD consists of more than 3000 gates and has 16 macrocell registers. Common uses for the PLD include chip selects for external devices, state-machines, simple shifters and counters, key-pad and control panel interfaces, clock dividers, handshake delay, muxes, etc. The on-chip PLD eliminates the need for small external PLDs and logic devices. Configuration of PLD, I/O, and Flash memory mapping are easily entered in a point-and-click environment using the software development tool, PSDsoft Express. The software is available to download from www.st.com/psd.

The two-chip combination of a DSP and a DSM device is ideal for systems which have limitations on size, EMI levels, and power consumption. DSM memory and logic are "zero-power", meaning they automatically go to standby between memory accesses or logic input changes, producing low active and standby current consumption, making them ideal for battery powered products.

Figure 2. System Block Diagram, Two Chip Solution

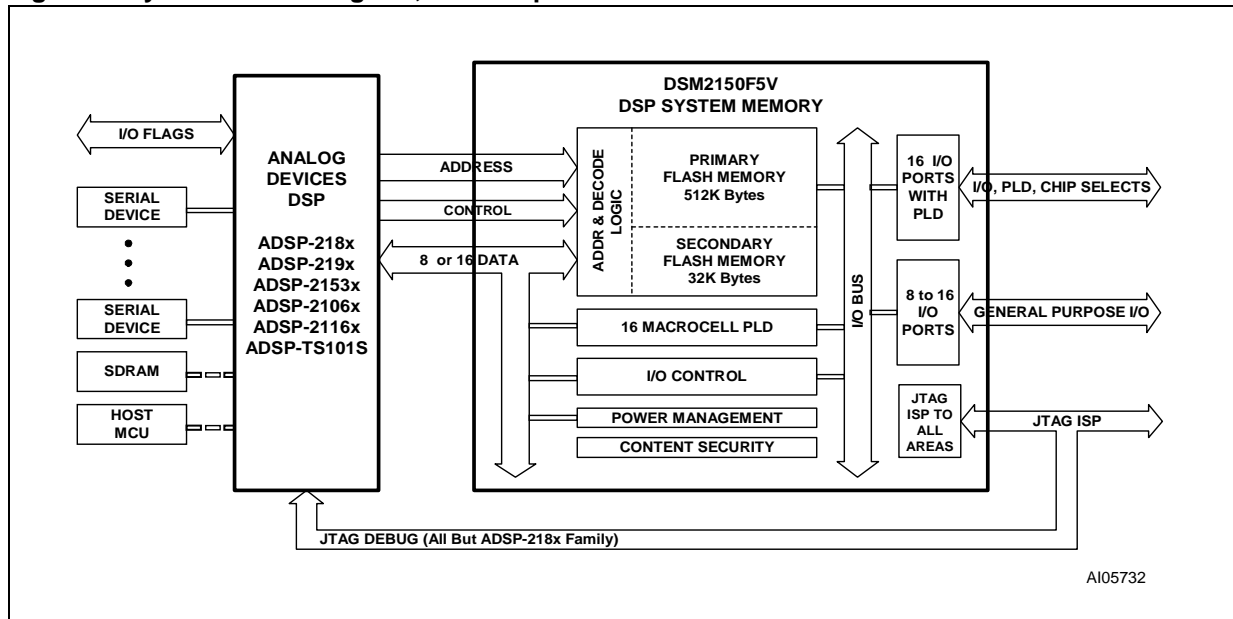
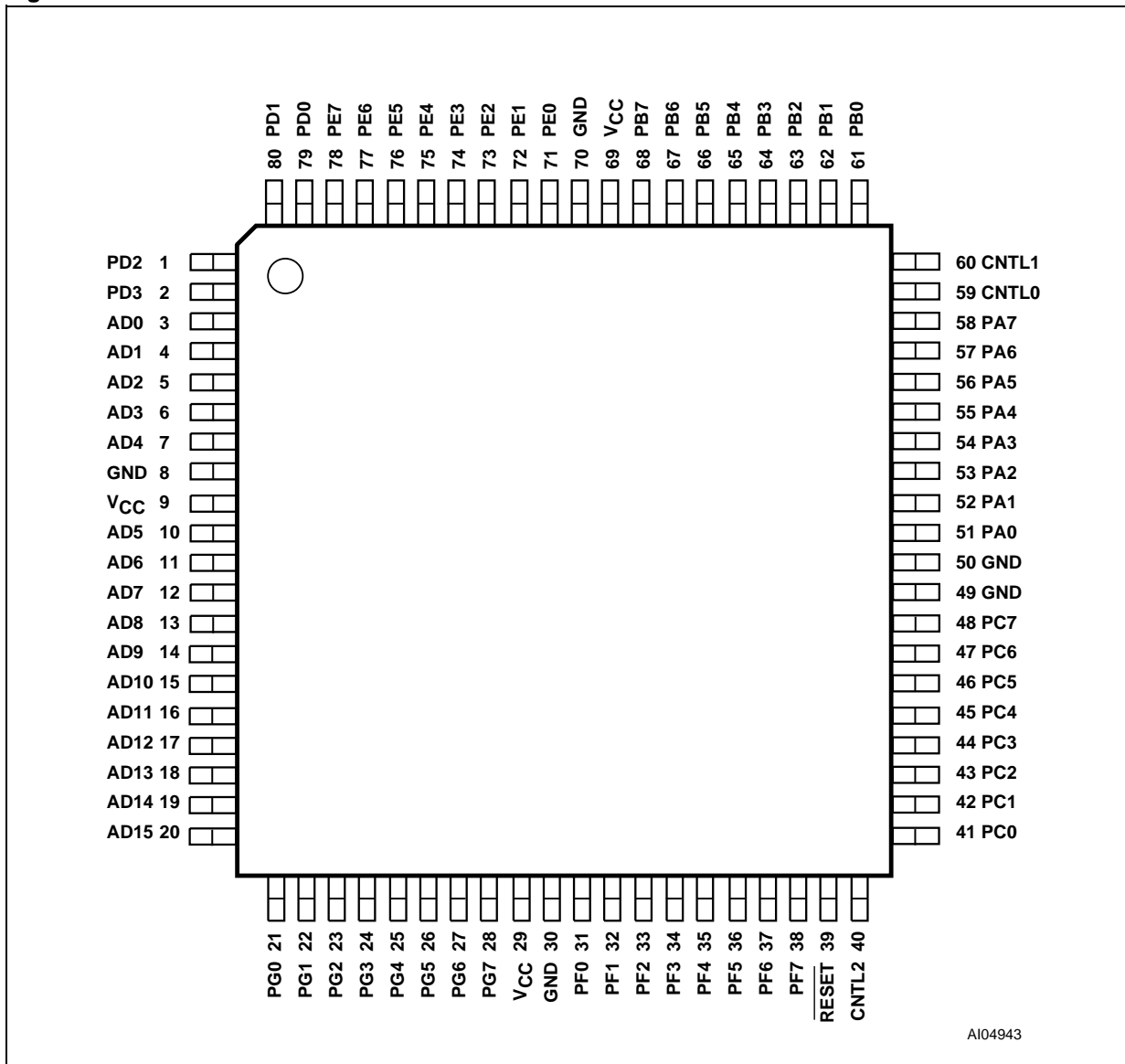


Figure 3. TQFP Connections

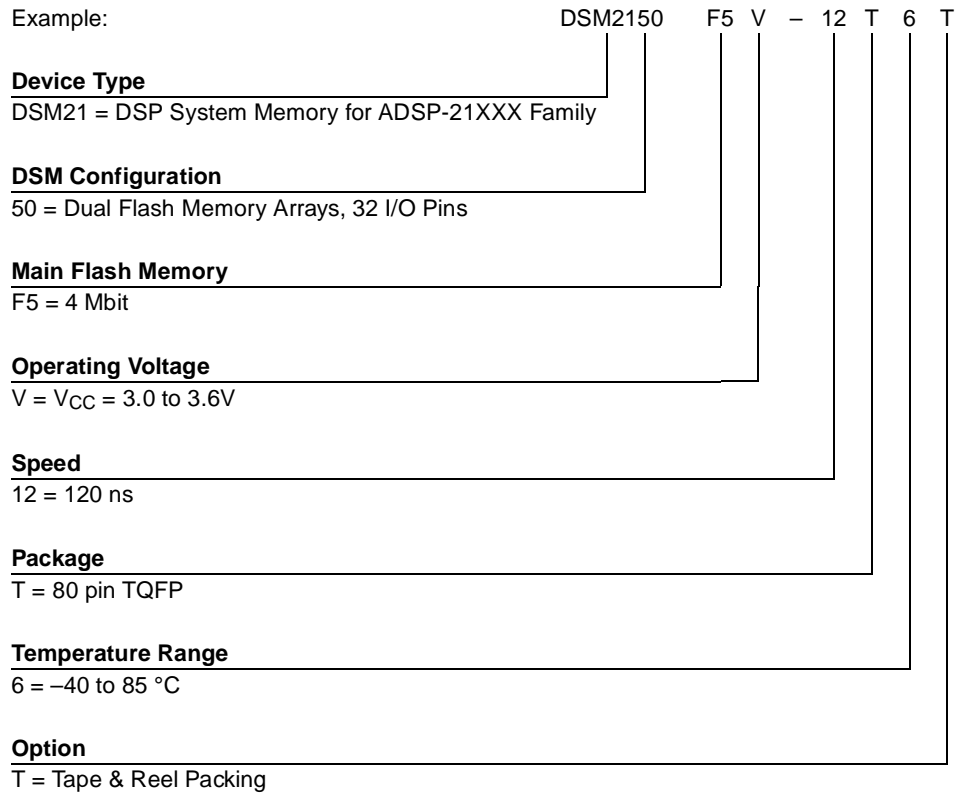


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Table 1. Pin Assignments – TQFP80

Pin No.	Pin Assignments	Pin No.	Pin Assignments	Pin No.	Pin Assignments	Pin No.	Pin Assignments
1	PD2	21	PG0	41	PC0	61	PB0
2	PD3	22	PG1	42	PC1	62	PB1
3	AD0	23	PG2	43	PC2	63	PB2
4	AD1	24	PG3	44	PC3	64	PB3
5	AD2	25	PG4	45	PC4	65	PB4
6	AD3	26	PG5	46	PC5	66	PB5
7	AD4	27	PG6	47	PC6	67	PB6
8	GND	28	PG7	48	PC7	68	PB7
9	V _{CC}	29	V _{CC}	49	GND	69	V _{CC}
10	AD5	30	GND	50	GND	70	GND
11	AD6	31	PF0	51	PA0	71	PE0
12	AD7	32	PF1	52	PA1	72	PE1
13	AD8	33	PF2	53	PA2	73	PE2
14	AD9	34	PF3	54	PA3	74	PE3
15	AD10	35	PF4	55	PA4	75	PE4
16	AD11	36	PF5	56	PA5	76	PE5
17	AD12	37	PF6	57	PA6	77	PE6
18	AD13	38	PF7	58	PA7	78	PE7
19	AD14	39	$\overline{\text{RESET}}$	59	CNTL0	79	PD0
20	AD15	40	CNTL2	60	CNTL1	80	PD1

Table 2. Ordering Information Scheme



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