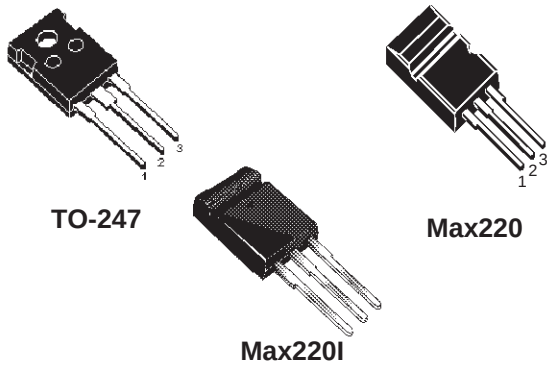
STW26NM50
STU26NM50, STU26NM50I

N-CHANNEL 500V - 0.10Ω - 26A TO-247,Max220,Max220I
Zener-Protected MDmesh™ Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STW26NM50	500 V	< 0.120 Ω	30 A
STU26NM50	500 V	< 0.120 Ω	26 A
STU26NM50I	500 V	< 0.120 Ω	26 A

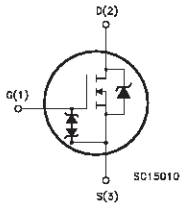
- TYPICAL $R_{DS}(on)$ = 0.10Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE



DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW26NM50	W26NM50	TO-247	TUBE
STU26NM50	U26NM50	Max220	TUBE
STU26NM50I	U26NM50I	Max220I	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STW26NM50	STU26NM50	STU26NM50I	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500			V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	500			V
V_{GS}	Gate- source Voltage	± 30			V
I_D	Drain Current (continuos) at T_C = 25°C	30	26	26 (*)	A
I_D	Drain Current (continuos) at T_C = 100°C	18.9	16.38	16.38 (*)	A
I_{DM} (ι)	Drain Current (pulsed)	120	104	104 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	313	192	73	W
	Derating Factor	2.5	1.54	0.58	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000			V
dv/dt (1)	Peak Diode Recovery voltage slope	15			V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150			°C °C

(ι) Pulse width limited by safe operating area
(1) I_{SD} ≤26A, di/dt ≤200A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.
(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-247	Max220	Max220I	
Rthj-case	Thermal Resistance Junction-case Max	0.4	0.65	1.7	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5			°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300			°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	13	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	740	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igss=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to souce. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			10 100	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 13 A		0.1	0.12	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 13 A		20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		3000 700 50		pF pF pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 250 V, I_D = 13 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		28 25		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400V, I_D = 26 A, V_{GS} = 10V		76 20 36	106	nC nC nC

SWITCHING OFF

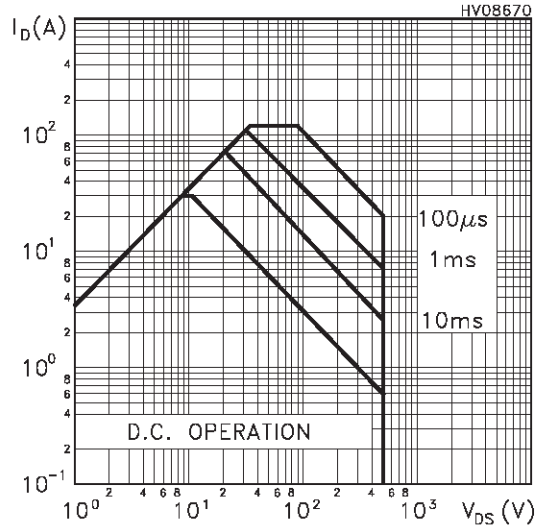
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 400V, I_D = 26 A, R_G = 4.7Ω, V_{GS} = 10V (Inductive Load see, Figure 5)		13 19 36		ns ns ns

SOURCE DRAIN DIODE

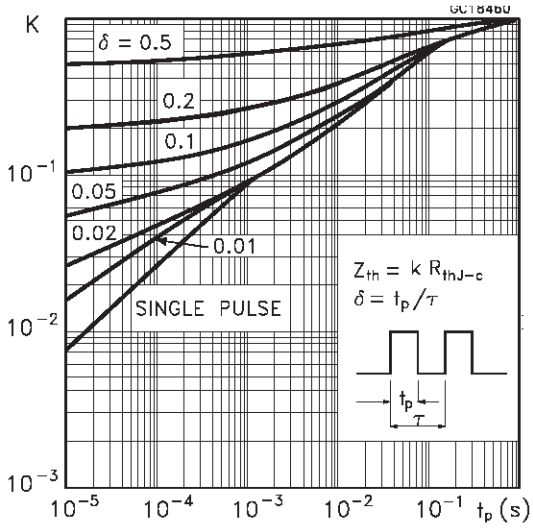
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				26 104	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 26 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 26 A, di/dt = 100A/µs V_{DD} = 60V, T_j = 150°C (see test circuit, Figure 5)		400 5.5 27		ns µC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

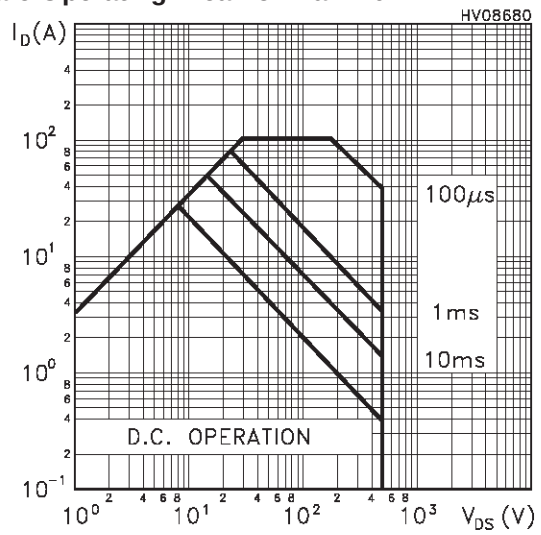
Safe Operating Area For TO-247



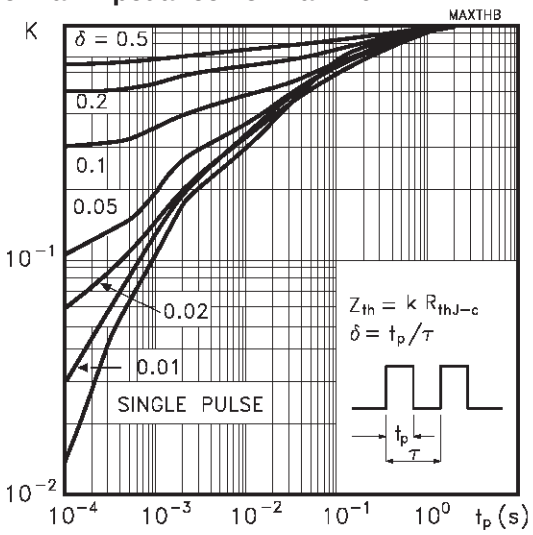
Thermal Impedance For TO-247



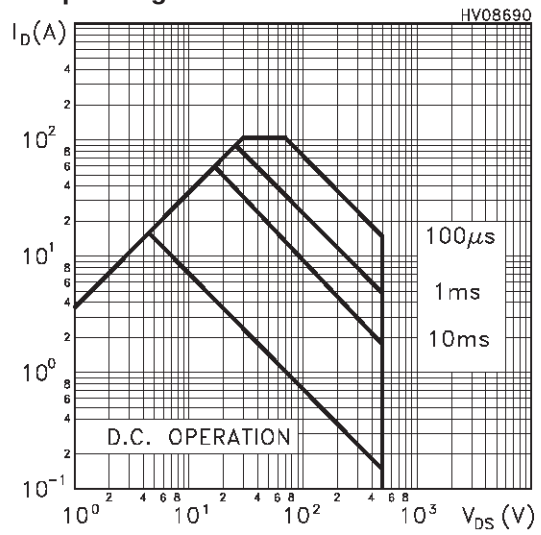
Safe Operating Area For Max220



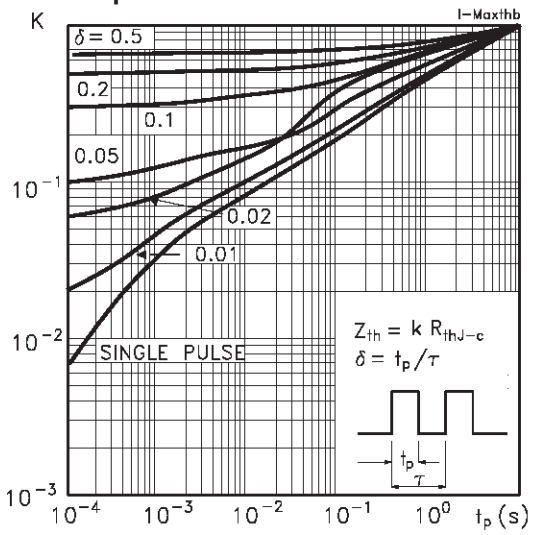
Thermal Impedance For Max220



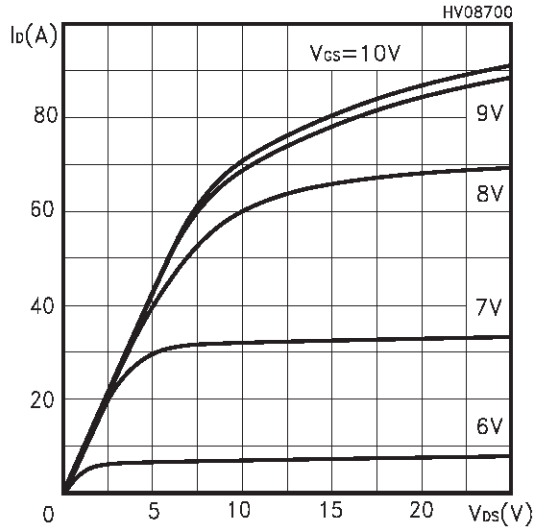
Safe Operating Area For Max220I



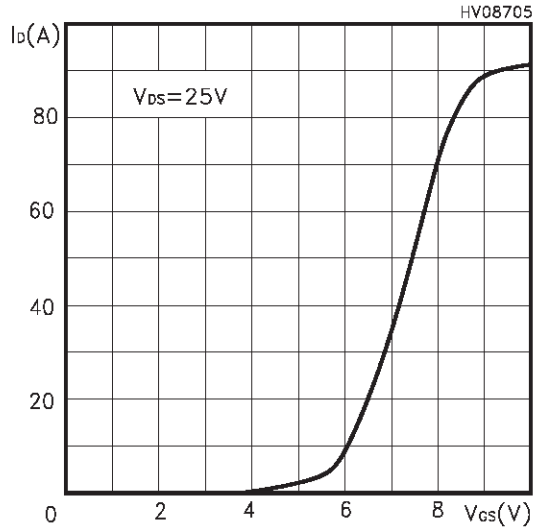
Thermal Impedance For Max220I



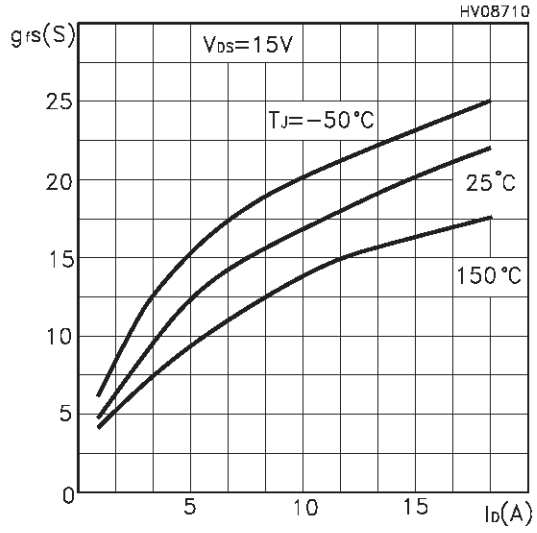
Output Characteristics



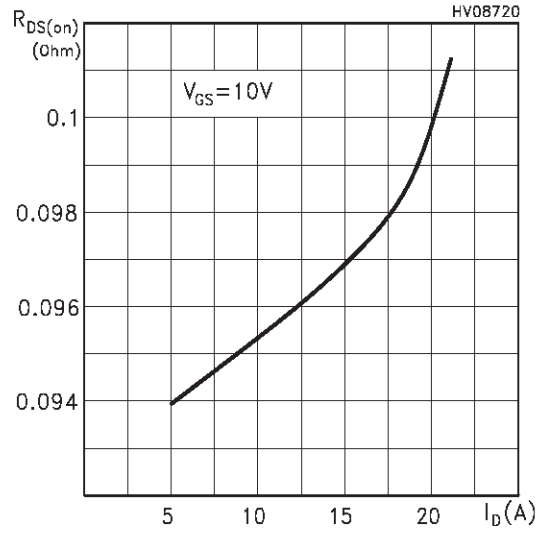
Transfer Characteristics



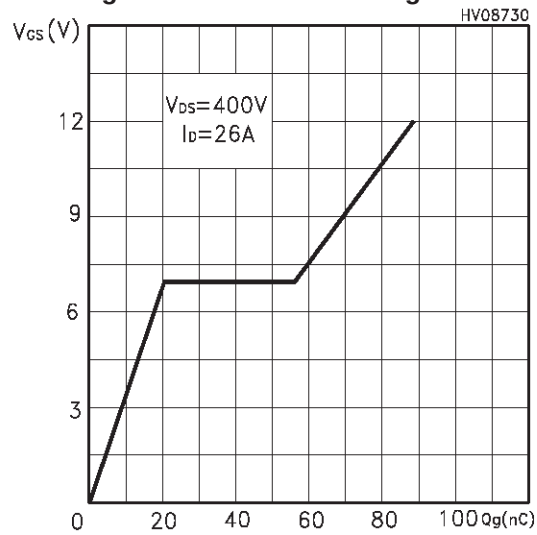
Transconductance



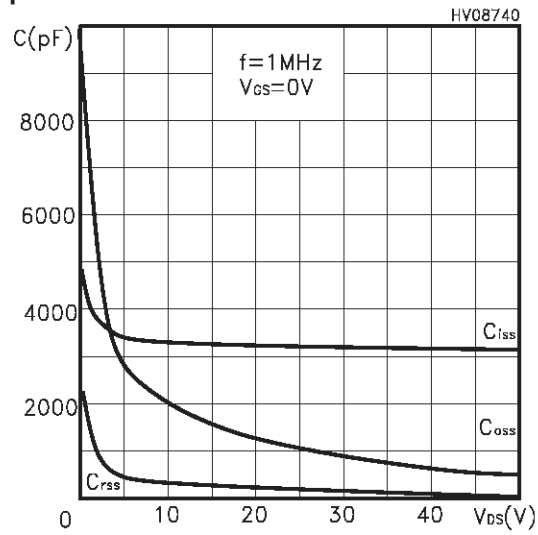
Static Drain-source On Resistance



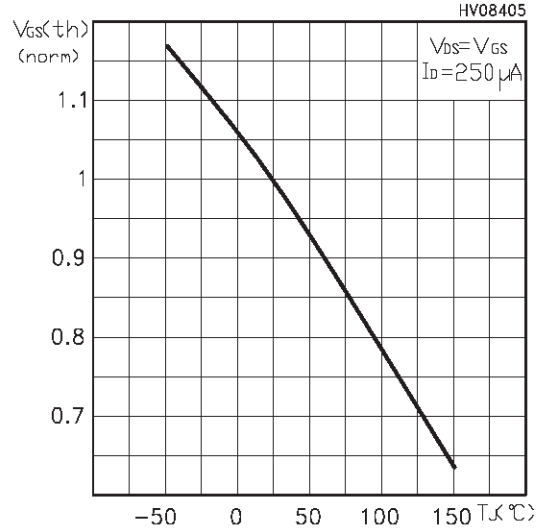
Gate Charge vs Gate-source Voltage



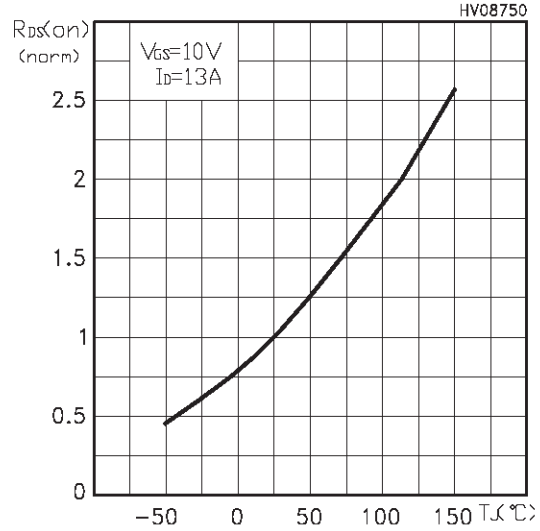
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

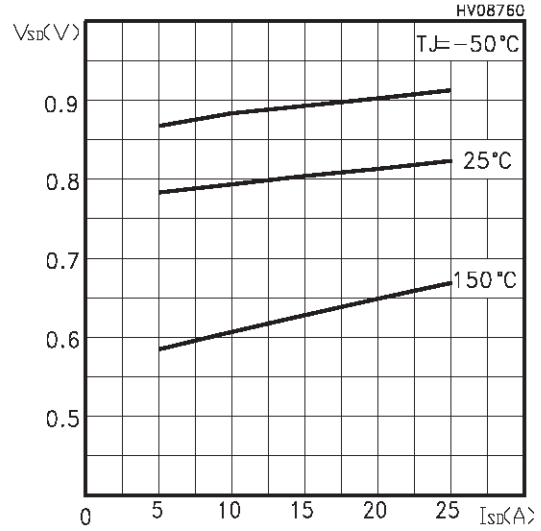


Fig. 1: Unclamped Inductive Load Test Circuit

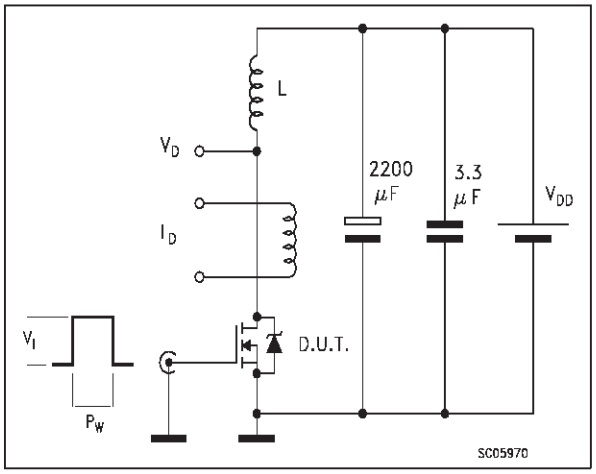


Fig. 2: Unclamped Inductive Waveform

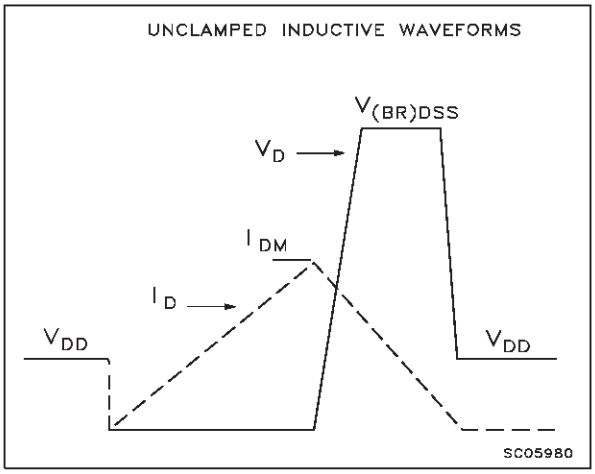


Fig. 3: Switching Times Test Circuit For Resistive Load

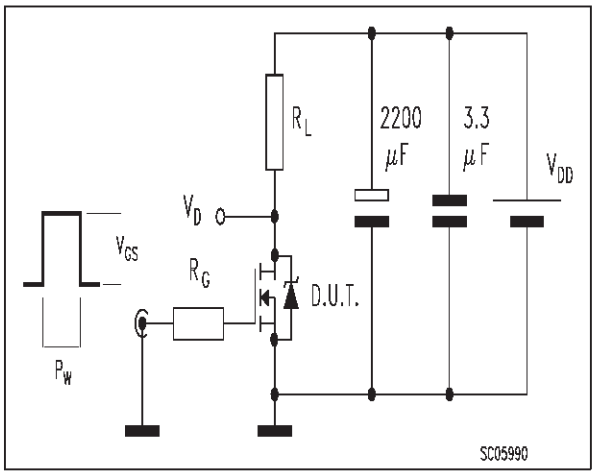


Fig. 4: Gate Charge test Circuit

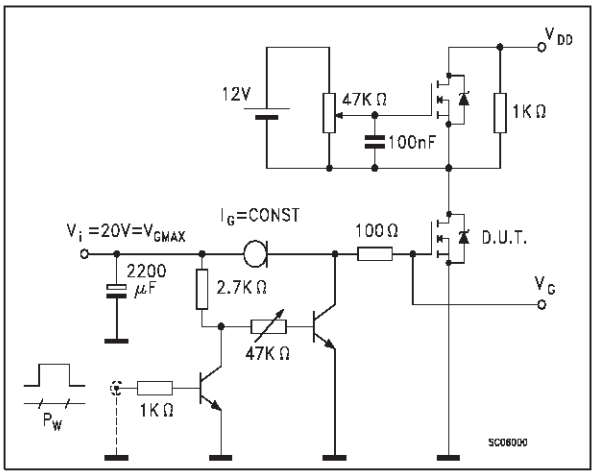
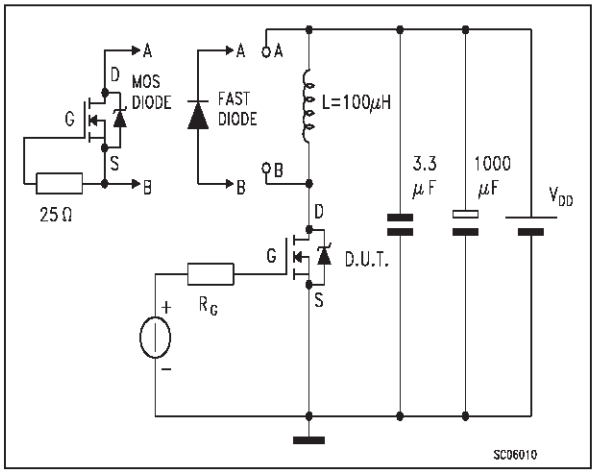
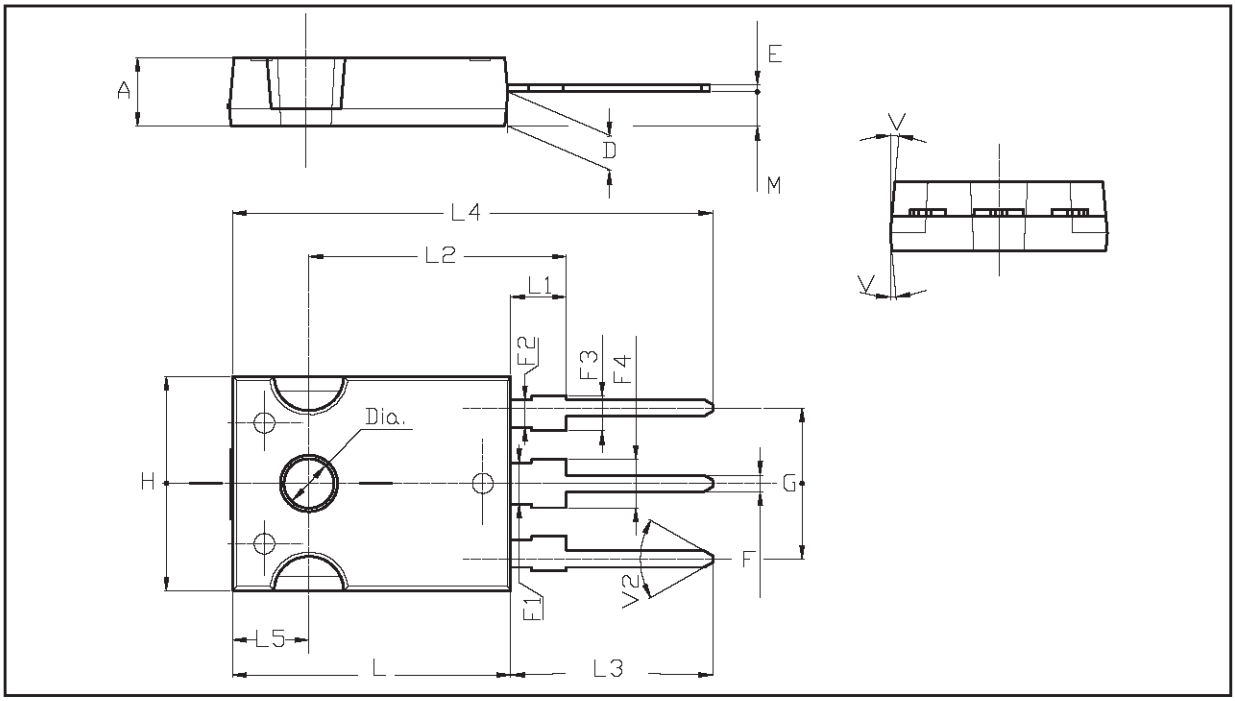


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



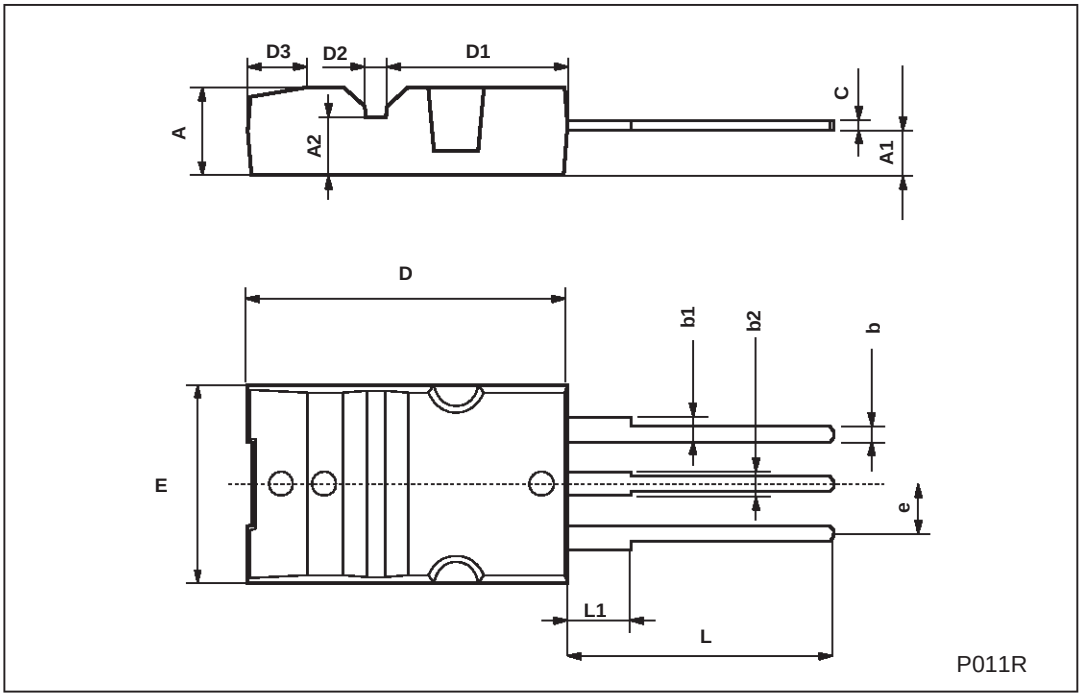
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
E	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
H	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
M	2		3	0.07		0.11
V		5º			5º	
V2		60º			60º	
Dia	3.55		3.65	0.14		0.143



Max220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.3		4.6	0.169		0.181
A1	2.2		2.4	0.087		0.094
A2	2.9		3.1	0.114		0.122
b	0.7		0.93	0.027		0.036
b1	1.25		1.4	0.049		0.055
b2	1.2		1.38	0.047		0.054
c	0.45		0.6		0.18	0.023
D	15.9		16.3		0.626	0.641
D1	9		9.35	0.354		0.368
D2	0.8		1.2	0.031		0.047
D3	2.8		3.2	0.110		0.126
e	2.44		2.64	0.096		0.104
E	10.05		10.35	0.396		0.407
L	13.2		13.6	0.520		0.535
L1	3		3.4	0.118		0.133



I-Max220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.3		4.6	0.169		0.181
A1	2.6		2.75	0.102		0.108
A2	1.95		2.15	0.077		0.084
b	0.7		0.93	0.027		0.036
b1	1.25		1.4	0.049		0.055
b2	1.2		1.38	0.047		0.054
c	0.45		0.6	0.017		0.023
D	15.9		16.3	0.626		0.641
D1	12.5		12.9	0.492		0.508
D2	0.6		1	0.023		0.039
D3	1.75		2.15	0.069		0.084
e	2.44		2.64	0.096		0.104
E	10.05		10.35	0.396		0.407
L	13.2		13.6	0.520		0.535
L1	3		3.4	0.118		0.133