Evaluation Board for the ADV7195/96a/97 HD Encoders

Eval-ADV7195/96a/97 Rev C

FEATURES
On-Board Reference
On-Board Clock
On-Board Output Buffer and LPF
3 x 10Bit Pixel Data Input
Progressive Scan or HDTV component YPrPb Output
ADuC812 Microconverter + Switch Control
Direct Hook-Up to Printer Port of PC
PC Software for Control for the evaluation board

INTRODUCTION

This Application Note describes the ADV7195/96A/97 RevC evaluation board which supports the ADV7195/96A/97 High Definition Encoders.

Full data on the ADV7195/96A/97 is available in the ADV7195/96A/97 data sheets, available from Analog Devices and should be consulted in conjunction with this note when using the Evaluation Board.

REQUIREMENTS

The ADV7195/96A/97 requires a DC power supply which is able to deliver a minimum of 3.3V. Ideal operating voltage for the Eval-ADV7195/96A/97 RevC is 3.3V.Current requirements are approx. 0.5 A**.**
To run the software which is supplied with the ADV7195/96A/97 it is necessary to connect the printer port LPT1 of the PC to the boards 36pin Centronics connector.
In order to run the software on a PC the operating system needs to be Windows 95 or Windows 98. The system requirements ask for any Pentium I, PMMx or Pentium II PC.

GENERAL DESCRIPTION

The Eval-ADV7195/96A/97RevC provides a 96-pin input port over which pixel data at TTL level is accepted to the ADV7195/96A/97. Otherwise pixel data can be input
over the headers P4,P5,P6 and P8. All input data must be at TTL level.
There is an additional evaluation board available from Analog Devices specifically designed to interface to the Eval-ADV7195/96A/97RevC which converts ECL data to TTL level.
This converter board interfaces to the 96-pin input port.
If a different clock source as that provided by the pixel data in EAV/SAV input mode is required, the ADV7195/96A/97 a 27Mhz oscillator (Y1) for Progressive Scan Mode. In HDTV Mode Y1 must be exchanged with a 74.25MHz or 74.1758MHz oscillator.
The ADV7195/96A contains an internal PLL which synchronizes 27MHz operation with 54 MHz operation in Progressive Scan Mode.
An on-board push-button provides control over the RESET pin. When RESET (PB1) is pressed the internal registers of the ADV7195/96A/97 reset to default register settings and all internal counters are reset.
The Eval-ADV7195/96A/97RevC also features an external Voltage Reference (U4) which provides 1.235V Output Voltage.Alternatively the internal Vref can be used in changing the settings of jumper J9.

The DAC outputs are fed to a LPF and buffer circuit.The analog component Y, Pr, Pb signals are finally output over 3 BNC connectors.

Two testpoints are available to monitor signals on pin 27 (TP1) and pin 25 (TP2).

The Eval-ADV7195/96A/97RevC is fitted with the ADuC812 Microconverter.
The ADuC812 is optional and is not required to make full use of the Eval-ADV7195/96A/97RevC board.

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Eval-ADV7195/96A/97EB REVC

DATA INPUT

1.Progressive Scan data (ADV7195/96a)

a) 3x10Bit 4:4:4 or 2x10Bit 4:2:2 (525p) YCrCb format or 3x10Bit 4:4:4 RGB format accompanied by seperate horizontal, vertical and blanking signals complying to SMPTE293M (525p).
There a several methods to input this data to the ADV7195/96A:

1. using a direct hook-up over the 96pin input port, P1. Either interfaced from the Genesis gmVLX1AMD De-Interlacing IC evalboard or the ECL to TTL converter board from Analog Devices used with an appropriate signal source.

2. using the input headers P4, P5,P6 and P8. Pixel data must be at TTL level.

b) 3x10Bit 4:4:4 or 2x10Bit 4:2:2 (625p) YCrCb format or 3x10Bit RGB 4:4:4 format accompanied by seperate horizontal, vertical and blanking signals complying to or ITU-R.1358 (625p).

1. using a direct hook-up over the 96pin input port, P1and the ECL to TTL converter board from Analog Devices used with an appropriate signal source.

2. using the input headers P4, P5, P6 and P8. Pixel data must be at TTL level.

c) EAV/SAV format complying to ITU-R.1358 (625p) or SMPTE293M (525p) using input port P1 and the ECL to TTL converter board from Analog Devices used with an appropriate signal source.

2. HDTV data (aDV7195/96a/97)

a) 3x10Bit 4:4:4 or 2x10Bit 4:2:2 YCrCb format or 3x10bit 4:4:4 RGB accompanied by seperate horizontal, vertical and blanking signals complying to SMPTE274M (1080i):

1.using input pixel port P1 and the ECL to TTL converter board from Analog Devices in conjunction with a suitable signal generator (eg TG2000 signal generator from Tektronix with HDTV expansion card).

2. using the input headers P4, P5, P6 and P8.All input data must be at TTL level.

b) in 3x10Bit 4:4:4 or 2x10Bit 4:2:2 YCrCb format or 3x10Bit 4:4:4 RGB accompanied by seperate horizontal, vertical, blanking_signals complying to SMPTE296M (720p).
Data input is as under 2.a.1 and 2.a.2.

c) EAV/SAV format complying to SMPTE274M (1080i) or SMPTE296M (720p) using pixel input port P1and the ECL to TTL converter board from Analog Devices in conjunction with a suitable signal generator (eg TG2000 signal generator from Tektronix with HDTV expansion card).

3. Any other High Definition Standard

3x10Bit 4:4:4 or 2x10Bit 4:2:2 YCrCb format or 3x10Bit 4:4:4 RGB accompanied by seperate horizontal, vertical, blanking signals. These signals are input on pins $\overline{\text{SYNC}}$, TSYNC and $\overline{\text{BLNK}}$ signals using Async Timing Mode and input headers P4, P5, P6 and P8.
All input data must be at TTL level.

SIGNAL OUTPUT:

Using the ADV7195/96A/97 software the following output standards can be selected. For output signal levels refer to the ADV7195/96A/97 datasheet.

1. YPrPb analog component progressive scan complying to EIA770.2 (ADV7195/96A only).
2. YPrPB analog component progressive scan complying to EIA770.1 (ADV7195/96A only).
3. YPrPb HDTV component complying to EIA770.3.
4. RGB output compliant to RS-170/RS-343A.

DEFAULT REGISTER SETTINGS ON POWER-UP AND ON RESET:

After pressing the reset button PB1 on the evaluation board or powering up the device, the register settings of the ADV7195/96A/97 will set up as follows:

	Address	Register Value
MR00	00HEX	80HEX
MR01	01HEX	00HEX
MR02	02HEX	00HEX
MR03 (ADV7195/96A)	03HEX	38HEX
MR03 (ADV7197)	03HEX	39HEX
MR04	04HEX	00HEX
MR05	05HEX	00HEX
COLORY	06HEX	A0HEX
COLORCR	07HEX	80HEX
COLORCB	08HEX	80HEX

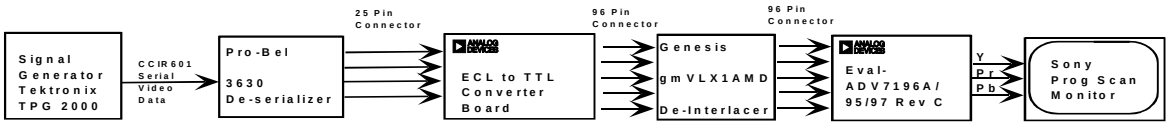
All other registers read 00HEX.
The ADV7195/96A/97 S2 powers-up with MR00= 00hex.

LED INDICATORS:

D1 on: n.d.
D1 off: n.d.
D2 on: n.d.
D2 off: n.d.
D3 on: ADV7195/96A/97 is controlled by PC
D3 off: ADV7195/96A/97 is controlled by SW1
D4 on: PC connection check : o.k.
D4 off: PC connection check: failure
D5 on: ADV7195/96A/97 EB Rev1 power o.k.
D5 off: ADV7195/96A/97 EB Rev1 power failure

HDTV Application Setup Example

Progressive Scan Application Setup Example



Note: There are two different ECL to TTL converter boards available from Analog Devices. Each of the above applications requires a different type of ECL to TTL converter board as demonstrated in the above figures.

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EVALUATION SOFTWARE

In order to give the user complete control over the ADV7195/96A/97, a computer program is supplied with the board.

Setting Up:
Insert DISK 1 into the floppy drive and double click on "SETUP.EXE" and you will be prompted for all other necessary information.

Running the Software:
It is recommended to power-up the board before running the software.
After installing the software successfully, double clicking the ADV7195/96A/97 icon will run the software for the evaluation board.

ADV7195/96A/97 Software User Interface:
After starting the software it is possible to load a preset as shown in the figure below.

When the message is accepted, the ADV7195/96A/97 is configured in such a way that it will output
a test pattern signal.
For this to work the jumpers have to be set as displayed in the message and a 27MHz clock must be supplied for Y1. The three BNC outputs must be connected to a Progressive Scan display device.
For this configuration it is not necessary to provide an input signal because the internal test pattern generator is enabled.
It is recommended to consult the datasheet for information about each control.

OPEN FILE icon:
Register settings as used with the ADV7195/96A/97 software can be saved as .ini files and reloaded at a later stage.

SUN, ICE, CLOUD icon:
Loads the presets as displayed in the tooltip message
box.

BLUE FILE OPEN:
Opens the Software Settings/Options form. 'ACKcheck' allows for an automatic acknowledge check. 'Auto Configure'

GREEN FILE OPEN:
Opens the Register Access form.
When any register value is changed, it can be automatically read back using the 'Not Continuous/Continuous' command.
'No Update/Auto Update' will automatically set the commands in the Mode Registers and all other registers according to the settings in the Register Access form.

CAMERA icon:
Displays all present register settings at once.

B icon:
Displays the register settings in binary format.

I²C Compatible Programming:
This version of software does not take into account the ability of the ADV7195/96A/97 to accept continuous streams of data. Instead, for every register write or read, it completely re-initiates a start sequence (see the ADV7195/96A/97 datasheet for information on different ways registers can be written to). This means that more information has to be written to the MPU port extending the time required to program the ADV7195/96A/97.This, while being a valid way of writing to the ADV7195/96A/97 is not the optimum method of writing

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ADV7195/96A/97 LINKS

These links are used for operating the ADV7195/96A/97 encoder:

J1: Insert this link if an external reset signal is provided. For example from the gmVLX1AMD board.

J2: Connect DV pin to Ground.

J4: This link controls the value of Rset and therefore the output levels of the DACs.

J4A: Rset = 2820 Ohms. Used for RS170/ 343A output standards.

J4B: Rset = 2470 Ohms. Used for EIA770.1, EIA770.2 and EIA770.3 output standards.

J5: Connect $\overline{\text{VSYNC}}$ pin to Ground to disable this input.

J6: Connect $\overline{\text{HSYNC}}$ pin to Ground to disable this input.

J8: Connect ALSB to Ground. Selects ALSB to be low.

J9: Insert this link if the on-board external Vref is prefered to the internal Vref.

J105: Clock source

J105A:ADV7195/96A/97 is clocked from the on-board oscillator. This setting is required for internal test pattern generation and all other input modes but EAV/SAV.

J105B :ADV7195/96A/97 is clocked from the clock contained in the pixel input data. This setting must be used for EAV/SAV input codes.

MICROCONVERTER ADuC812 LINKS

These links are required in conjunction with the ADuC812 Microconverter:

J10: Connect $\overline{\text{HSYNC}}$ signals to Interrupt.

J11: When this link is set, serial download on power-up or external Reset is enabled. After downloading the ADuC program code, this jumper must never be inserted, otherwise the ADuC program will be lost forever.

J12A: Connect DV to Interrupt.

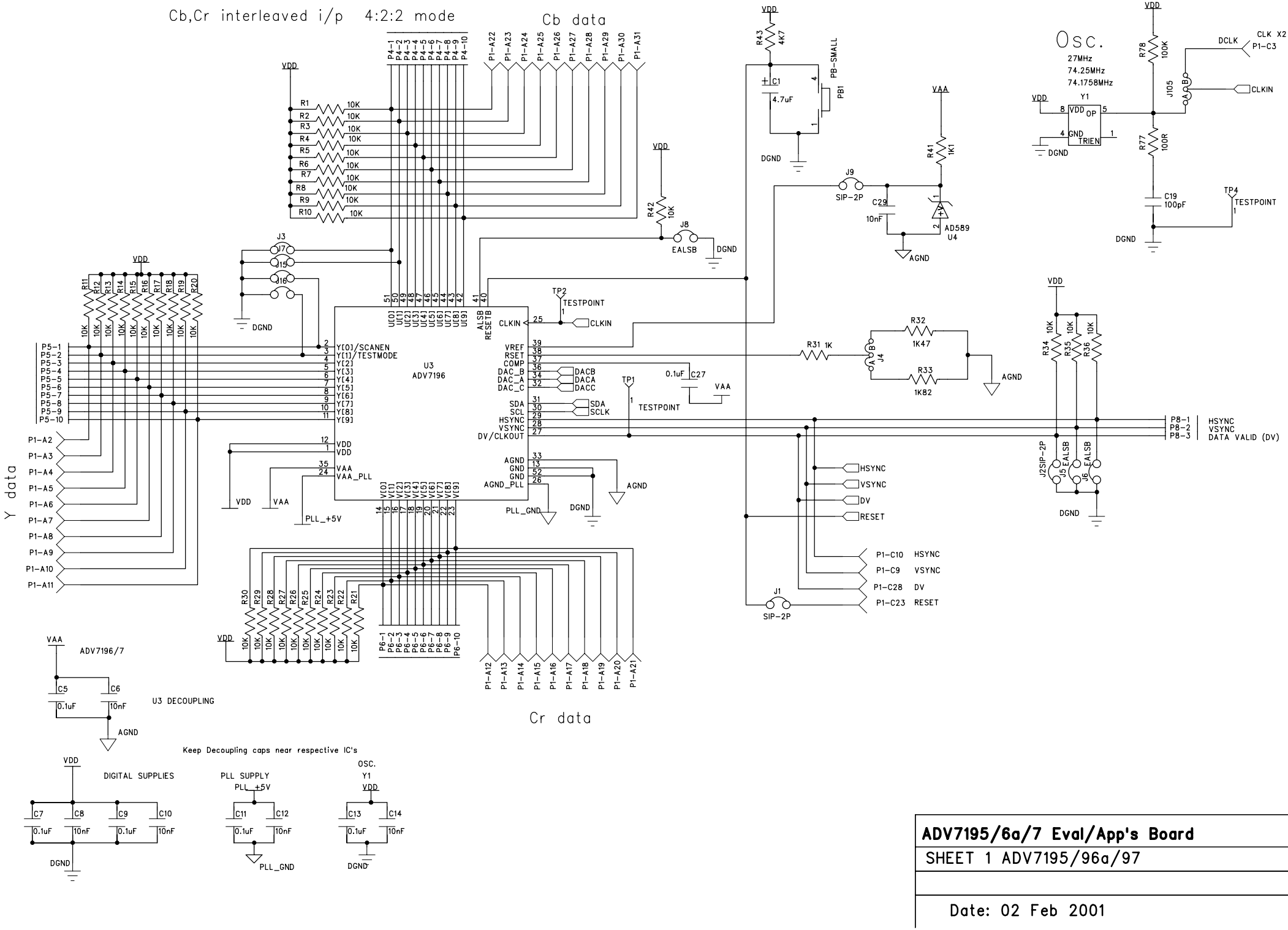
J12B: Connect $\overline{\text{VSYNC}}$ to Interrupt.

J13: If the ADuC is to be used with the ADV7195/96A/97 this link sets the SDA of the I2C interface. This link must be set whenever the Microconverter is to be used with the ADV7195/96A/97.

J14: If the Microconverter is to be used with the ADV7195/96A/97 this link sets the SCL of the I2C interface. This link must be set whenever the Microconverter is to be used with the ADV7195/96A/97.

J110: If the ADuC is to be used with the Genesis gmVLX1A-X this link sets the SDA of the I2C interface. This link must be set whenever the Microconverter is to be used with the Genesis gmVLX1A-X.

J111: If the ADuC is to be used with the Genesis gmVLX1A-X this link sets the SCL of the I2C interface. This link must be set whenever the Microconverter is to be used with the SGenesis gmVLX1A-X.



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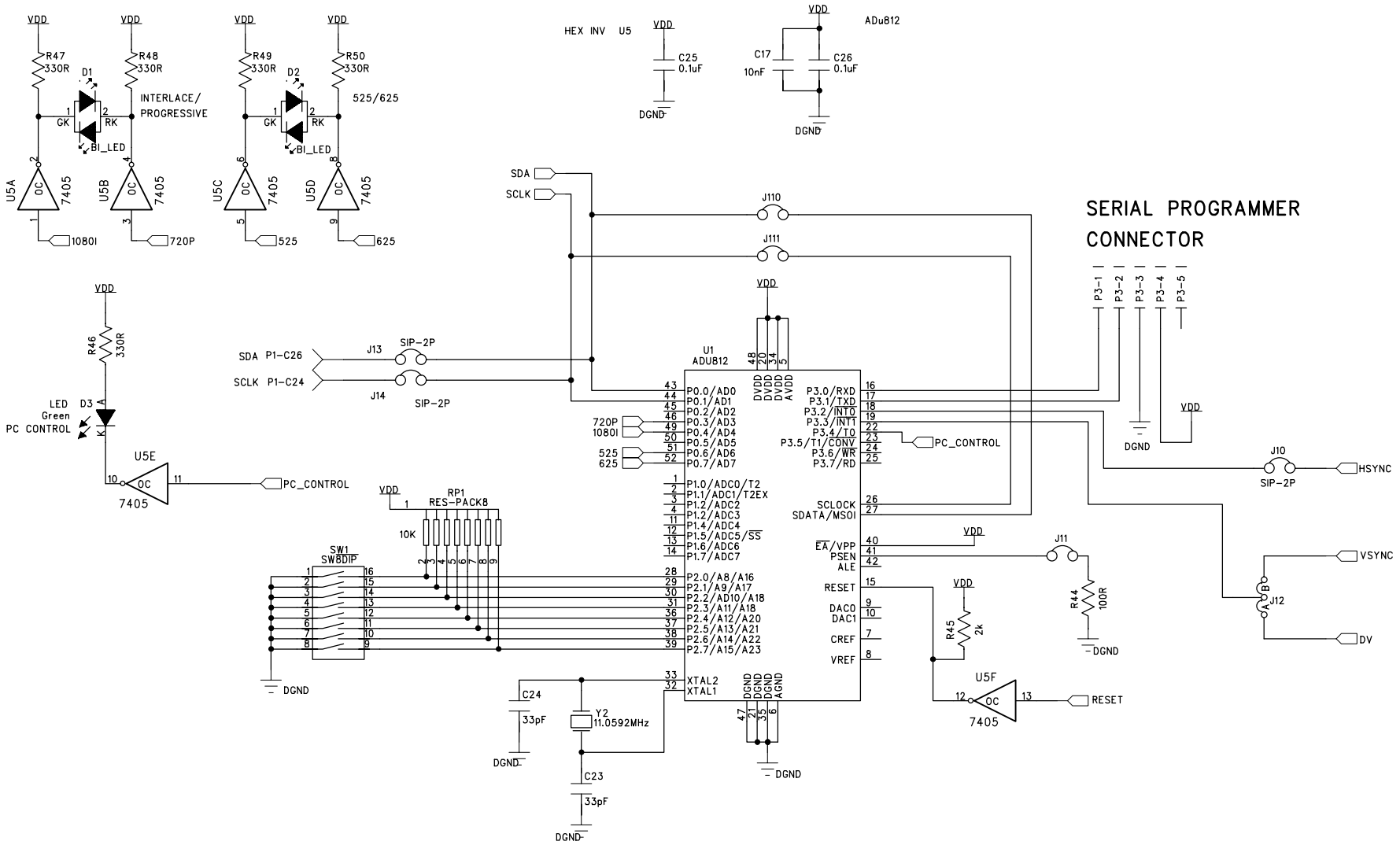

ADV7195/6a/7 Eval/Apps BOARD
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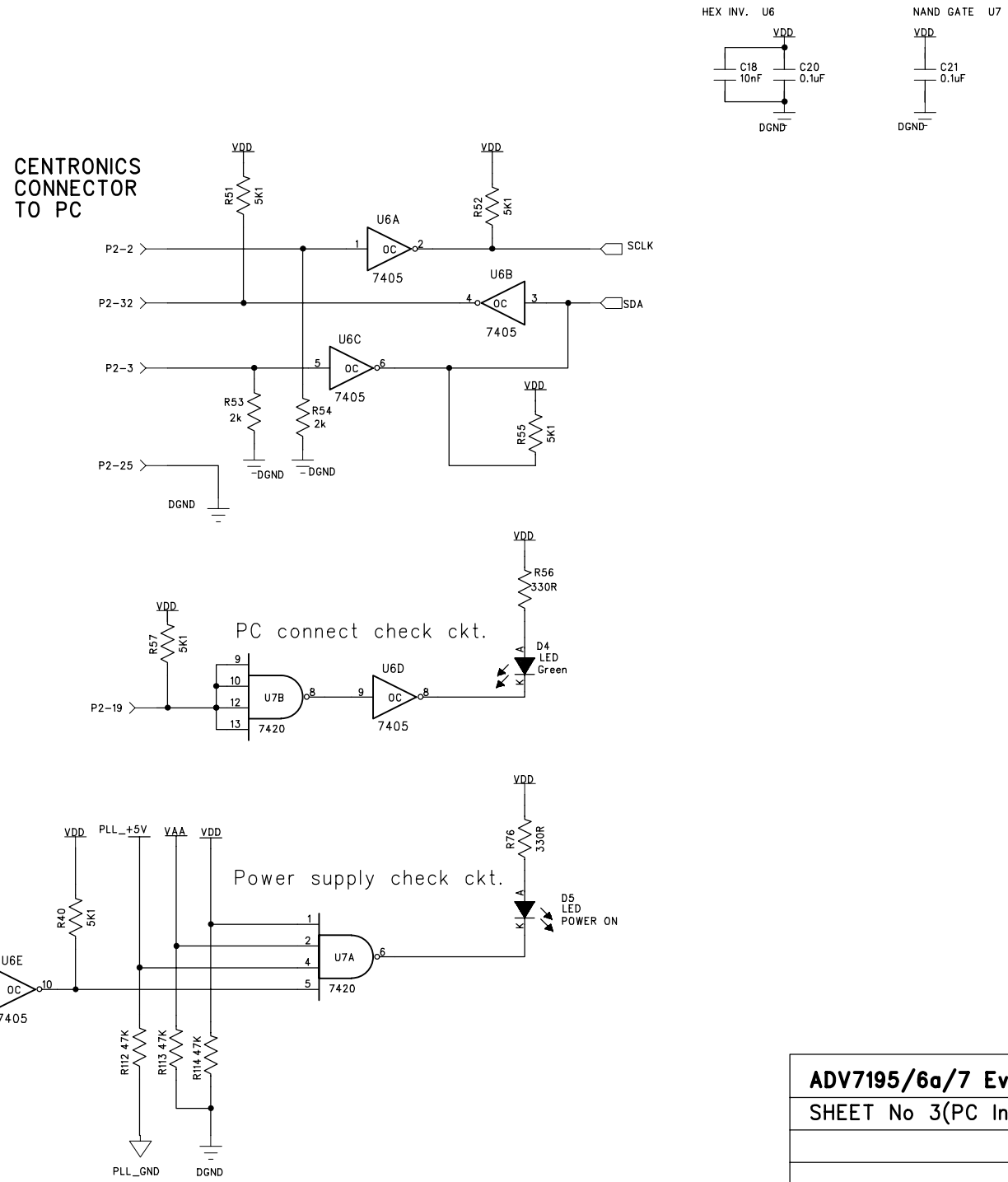

ADV7195/6a/7 Eval/Apps BOARD

SHEET No 3(PC Interface + VID Bus)

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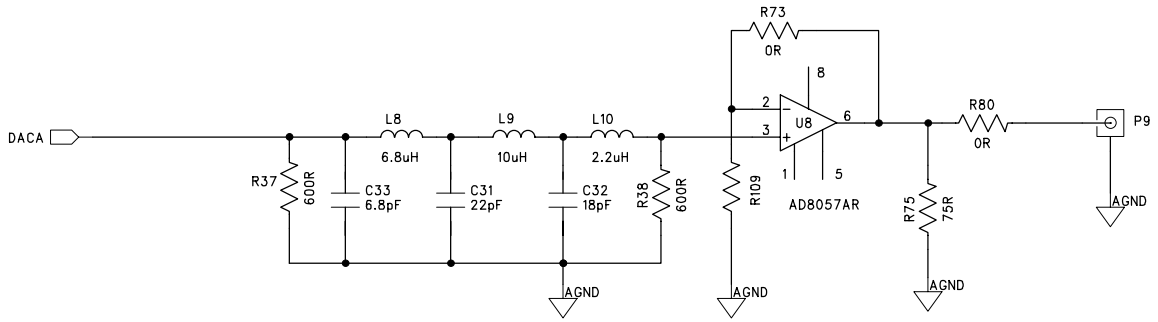

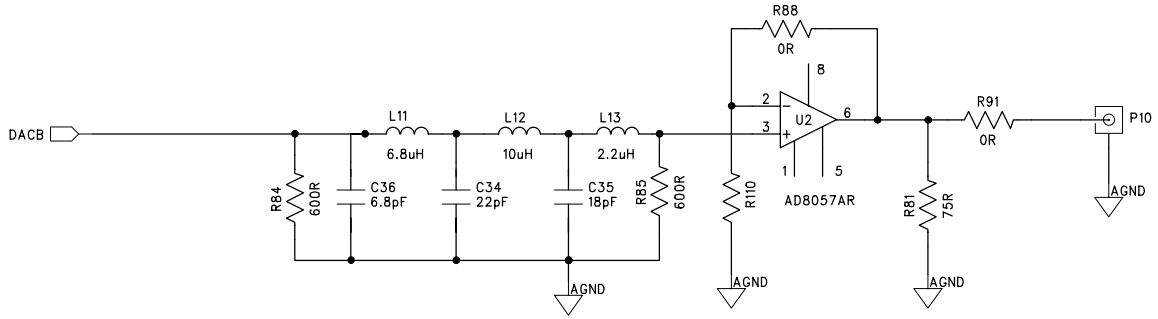

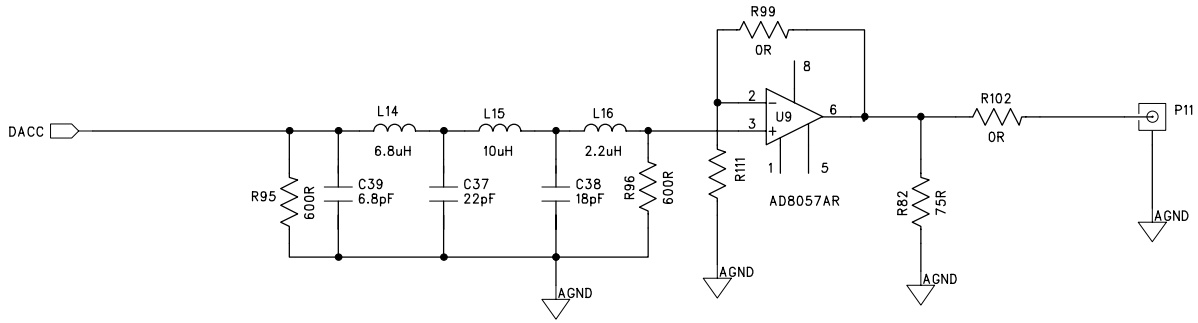

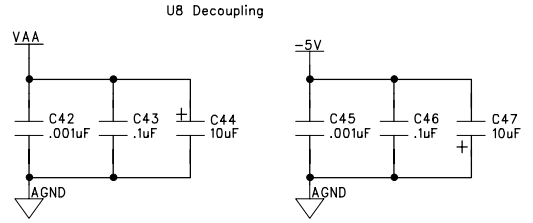

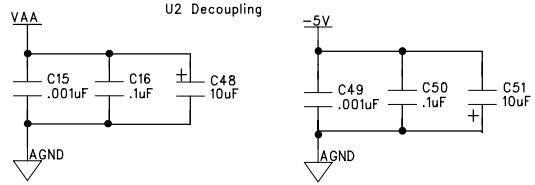

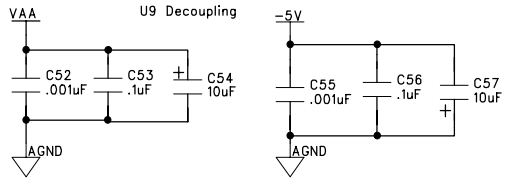

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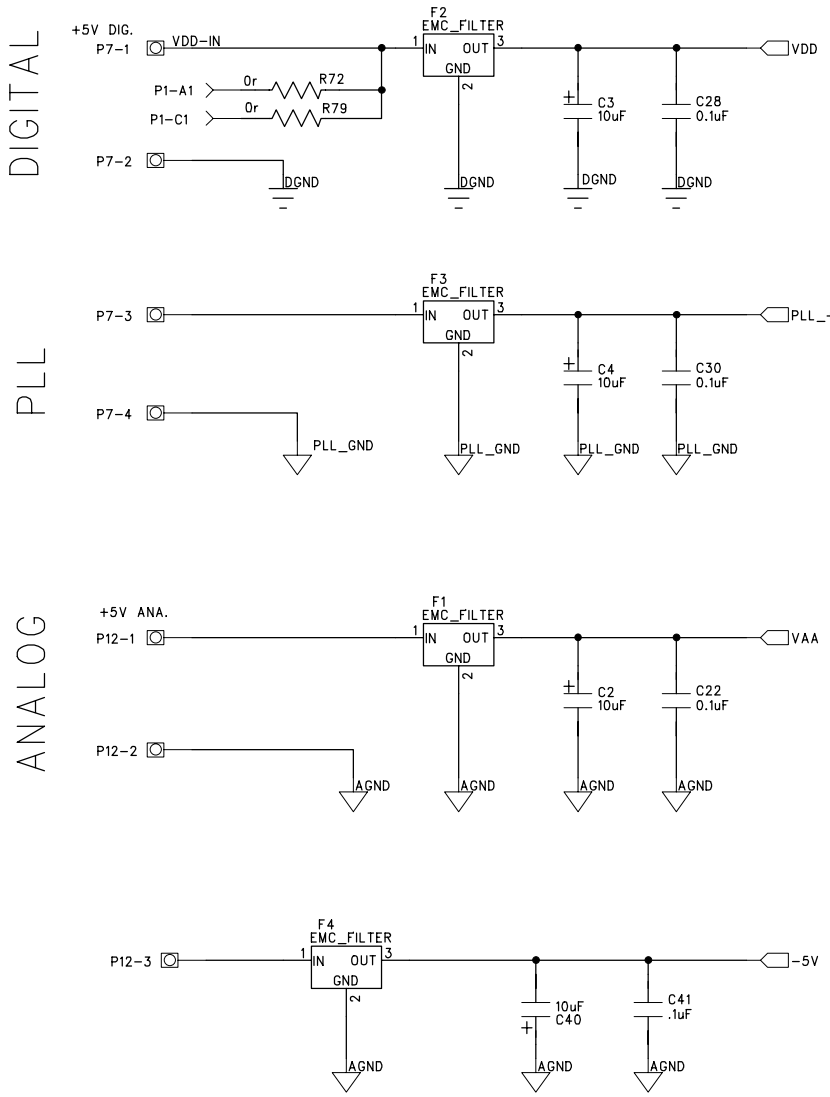

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ADV7195/6a/7 EVAL/APPS BOARD

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