
Code Hopping Decoder Using a PIC16C56

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OVERVIEW

This application note fully describes the working of a code hopping decoder implemented on a Microchip PIC16C56 microcontroller. Background is given on the various KEELOQ[®] code hopping encoders that can be used with the decoder, the decoder hardware described, and descriptions of the various software modules comprising the system. The software can be used to implement a stand-alone decoder or integrated with full function security systems. The decoder supports the Microchip HCS200, HCS201, HCS300, HCS301, HCS360, HCS361 and HCS410 KEELOQ Code Hopping Encoders.

KEY FEATURES

- Stand-alone decoder
- Compatible with Microchip HCS200, HCS201, HCS300, HCS301, HCS360, HCS361 and HCS410 encoders
- Automatic baud rate detection
- Automatic encoder type detection
- Four function outputs
- Six learnable transmitters
- RC Oscillator

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INTRODUCTION TO KEELOQ ENCODERS

All KEELOQ encoders use the KEELOQ code hopping technology to make each transmission by an encoder unique. The encoder transmissions have two parts. The first part changes each time the encoder is activated and is called the hopping code part. The second part is the serial number of the encoder, identifying it to a decoder.

Hopping Code

The Hopping Code contains function information, a discrimination value, and a synchronization counter. This information is encrypted by an encryption algorithm before being transmitted. A 64-bit encryption key is used by the encryption algorithm. If one bit in the data that is encrypted changes, the result is that an average of half the bits in the output will change. As a result, the hopping code changes dramatically for each transmission and can not be predicted.

Function Information

The encoder transmits up to four bits of function information. Up to 15 different functions are available (0000 is related to the reset condition in all the current encoders, and can never be transmitted).

Discrimination Value

Stored in the encoder EEPROM, this information is used to check integrity of decryption operation in the decoder. If known information is inserted into the transmitted string before encryption, the same information can be used at the decoder to check whether the information has been decrypted correctly. In the Microchip HCS encoders, up to 12 bits (including overflow bits) are available.

Synchronization Counter

The transmitted word contains a 16-bit synchronization counter. The synchronization information is used at the decoder to determine whether a transmission is valid, or a repetition of a previous transmission. Previous codes are rejected to safeguard against code grabbers. The HCS300/301 encoder transmits two overflow bits which may be used to extend the range of the synchronization counter from 65,536 to 196,608 button operations.

Fixed Code

Serial Number

The encoder's serial number is transmitted every time the button is pressed. The serial number is transmitted unencrypted as part of the transmission, and serves to identify the encoder to the decoder. The number can be used during learning operations to calculate the key to be used for decrypting the transmissions.

Other Status and Function Information

The HCS300/301 encoders include provision for four bits of function information and two status bits in the fixed code portion of its transmission. The two status bits indicate whether a repeated transmission is being sent, and whether the battery voltage is low. The HCS200/201 does not send repeated transmission information and the bit is permanently set to '0'.

Transmission Format

Table 1 contains a summary of the information contained in transmissions from each of the KEELOQ encoders that can be learned by the Microchip decoder.

FIGURE 1: BLOCK DIAGRAM

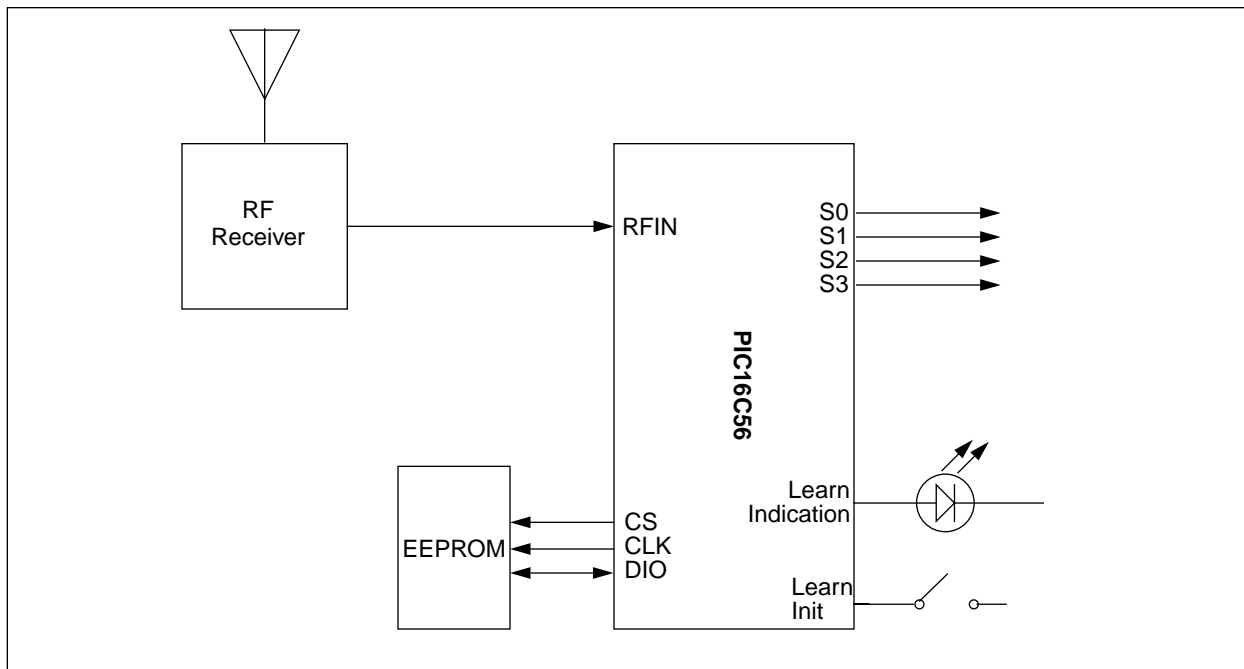


TABLE 1: KEELOQ ENCODER TRANSMISSION SUMMARY

| | HCS200/201 # of bits | HCS300/301 # of bits | HCS360/361 # of bits | HCS410 # of bits |
|---------------------------|-------------------------|-------------------------|-------------------------|---------------------|
| Total Transmission Length | 66 | 66 | 67 | 69 |
| Code Hopping Portion | 32 | 32 | 32 | 32 |
| Sync Counter | 16 | 16 | 16 | 16 |
| Discrimination bits | 12 | 10 | 8 | 10 |
| User Bits | 0 | 0 | 2 | 0 |
| Overflow Bits | 0 | 2 | 1 | 2 |
| Independent Mode | 0 | 0 | 1 | 0 |
| Function Code | 4 | 4 | 4 | 4 |
| Fixed Portion | 34 | 34 | 35 | 37 |
| Serial number | 28 | 28 | 28/32 | 28/32 |
| Function Code | 4 | 4 | 4/0 | 4/0 |
| Low Voltage Indicator | 1 | 1 | 1 | 1 |
| Repeat Bit | 1 | 1 | 0 | 0 |
| CRC | 0 | 0 | 2 | 2 |
| Queue Bits | 0 | 0 | 0 | 2 |

TABLE 2: HCS200/201 AND HCS300/301 CODE HOPPING TRANSMISSION FORMAT

| Code Hopping Portion | | | Fixed Portion | | |
|----------------------|----------------|------|---------------|------|-----------|
| Sync Counter | Discrimination | Func | Serial Number | Func | VLOW REPT |

TABLE 3: HCS200/201 AND HCS300/301 SEED TRANSMISSION FORMAT

| Seed Portion | | Fixed Portion | | |
|--------------|--|---------------|------|-----------|
| Seed | | Serial Number | Func | VLOW REPT |

TABLE 4: HCS360/361 CODE HOPPING TRANSMISSION FORMAT

| Code Hopping Portion | | | Fixed Portion | | |
|----------------------|----------------------------|------|-------------------------------|--------------------|-----------|
| Sync Counter | Discrimination OVR, IND | Func | Serial Number (28/32 bits) | Func (4/0 bits) | VLOW REPT |

TABLE 5: HCS360/361 SEED TRANSMISSION FORMAT

| Seed Portion | | Fixed Portion | | |
|-------------------|--|----------------------------------|--------------------|-----------|
| Seed (48 bits) | | Serial Number (12/16 MS bits) | Func (4/0 bits) | VLOW REPT |

TABLE 6: HCS410 CODE HOPPING TRANSMISSION FORMAT

| Code Hopping Portion | | | Fixed Portion | | |
|----------------------|-----------------------|------|-------------------------------|--------------------|--------------------|
| Sync Counter | Discrimination OVR | Func | Serial Number (28/32 bits) | Func (4/0 bits) | VLOW CRC QUE |

TABLE 7: HCS410 SEED TRANSMISSION FORMAT

| Seed Portion | | Fixed Portion | |
|-------------------|--|--------------------|--------------------|
| Seed (60 bits) | | Func (4/0 bits) | VLOW CRC QUE |

PWM Format

In general, all KEELOQ encoders share a common transmission format.

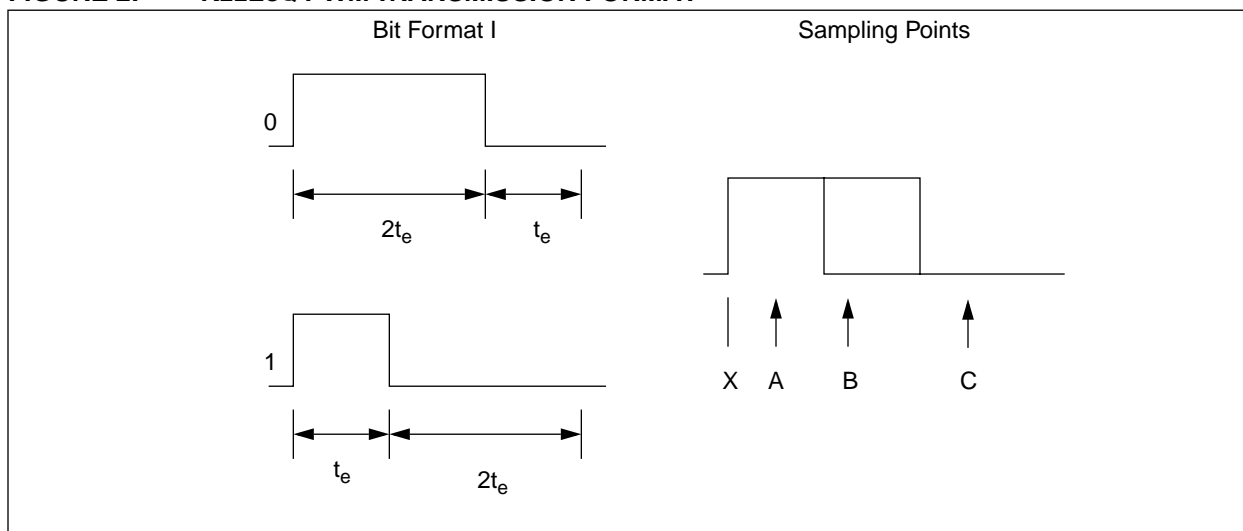
- A preamble to improve biasing of decision thresholds in super-regenerative receivers. The preamble consists of alternate on and off periods, each lasting as long as a single elemental period.
- A calibration header, consisting of a low period of 10 elemental periods. Calibration actions should be performed on the low period of the header to ensure correct operation with header chopping.
- A string of 66 pulse width modulated bits, each consisting of three elements. The first element is high, the second contains the data transmitted and is either high or low, the third element is always low.
- A guard period is usually left between the transmissions. During this period nothing is transmitted by the encoder.

Figure 2 shows the sampling points when sampling data. The first and last elements are used exclusively to verify the integrity of the received signal. The first element (sample point A) is always high, the second (sample point B) is the complement of the data bit being sent, and the final element (sample point C) is always low. Because the period between the low portion of a bit (sample point C) and the rising edge of the following bit (sample point X) can vary somewhat, the rising edge of the first element (sample point X) is used to resynchronize the receiving routine to each incoming bit.

If random noise is being received, the probability of a set of three samples producing a valid combination is only $2^{-2} = 1/4$. For a string of 56 bits, the corresponding figure is 2^{-134} . For longer strings, the probability is considerably less.

Integrity checking on incoming signals is important. Code hopping signals require significant processing, as well as EEPROM access, to decrypt. Unnecessary processing can be avoided by not attempting to decrypt incoming codes that have bit errors.

FIGURE 2: KEELOQ PWM TRANSMISSION FORMAT



IMPLEMENTATION

The Microchip decoder's primary hardware components are a PIC16C56 RISC microcontroller and a 93LC46B EEPROM. However, this solution can be implemented in any PICmicro[®] microcontroller with at least 1K words of programming. The operating frequency of the controller is 4 MHz. The microcontroller is used to capture transmissions from the various encoders, decrypt transmissions captured, and check the validity of the transmission based on the information in the decrypted transmission and information stored in the EEPROM. If a transmission from a valid encoder is received, the Microchip decoder activates the outputs dictated by the transmission.

Encoder information, such as serial number, synchronization information, and decryption key are stored externally in an EEPROM. The EEPROM used is a Microchip 93LC46B CMOS serial EEPROM. The information stored in the EEPROM is encrypted to protect the decoders from cloning. The EEPROM encryption is less secure than the KEELOQ code hopping algorithm.

A more secure implementation of the decoder would be to modify the software in the application note and use a PIC16CXX with an internal EEPROM such as a PIC16C84. In this way communication between the PIC16C56 and EEPROM cannot be monitored.

As can be seen from the section on encoder transmissions there are differences in the transmission formats of the different encoders that are compatible with the system. The following section summarizes how the differences in transmitted data are dealt with by the decoder.

As the **serial number** information follows after the code hopping portion of the transmission, any number of serial number bits can be received and processed. In the Microchip decoder described 28 bits of the serial number are stored.

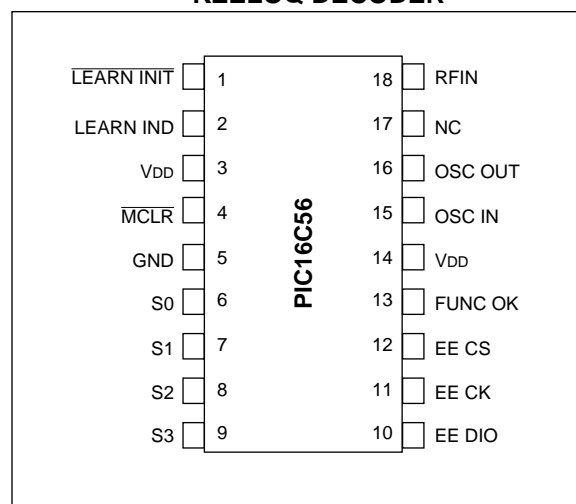
The serial number is used to identify the memory block used to store the 64-bit decryption key for a particular encoder because of the relationship between serial num-

ber and decryption key. In other words, the serial number is stored with the key. When a transmission is received, the decoder finds the correct memory block by checking all blocks until a matching serial number is found. The key is then retrieved from that particular memory block. A serial number of 0000000₁₆ is considered invalid.

Validation of a received transmission consists of two parts. The first includes checking the integrity of the decryption operation. Here the decoder compares the 12-bit discrimination value received with the stored discrimination value. The discrimination value stored for the HCS300/301 includes the overflow bits.

The second portion of validation involves checking **synchronization** information for that particular encoder. The synchronization counter transmitted by all encoders is 16 bits long. Two copies of the full synchronization counter are stored for all valid encoders. The storing of two copies of the synchronization information protects the decoder from losing synchronization with an encoder if one of the counters is corrupted.

FIGURE 3: PINOUTS OF MICROCHIP KEELOQ DECODER



FUNCTIONAL INPUTS AND OUTPUTS

TABLE 8: MICROCHIP DECODER FUNCTIONAL INPUTS AND OUTPUTS

| Mnemonic | Pin Number | Input / Output | Function |
|------------------|------------|----------------|--|
| RF IN | 18 | I | Demodulated PWM signal from RF receiver. The decoder uses this input to receive encoder transmissions. |
| LEARN INIT | 1 | I | Input to initiate learning. |
| LEARN INDICATION | 2 | O | Output to show the status of the learn process (in an integrated system this will be combined with the system status indicator). |
| FUNC OK | 13 | O | Indication that the received button code matches the learned button code. |
| S0, S1, S2, S3 | 6, 7, 8, 9 | O | Function outputs, correspond to encoder input pins. |
| EE DIO | 10 | I/O | EEPROM Data. |
| EE CK | 11 | O | EEPROM Clock. |
| EE CS | 12 | I | EEPROM Chip Select. |

PROGRAM FLOW

The software for the Microchip decoder has been written for the PIC16C56 microcontroller. The compiler used is MPASM. The operating frequency of the PIC16C56 is 4 MHz. The clock speed is important as the reception routine (RECEIVE) has some critical timing specifications. Other decoder functions that rely on a 4 MHz clock speed are the hold times of the various outputs, time-outs, etc.

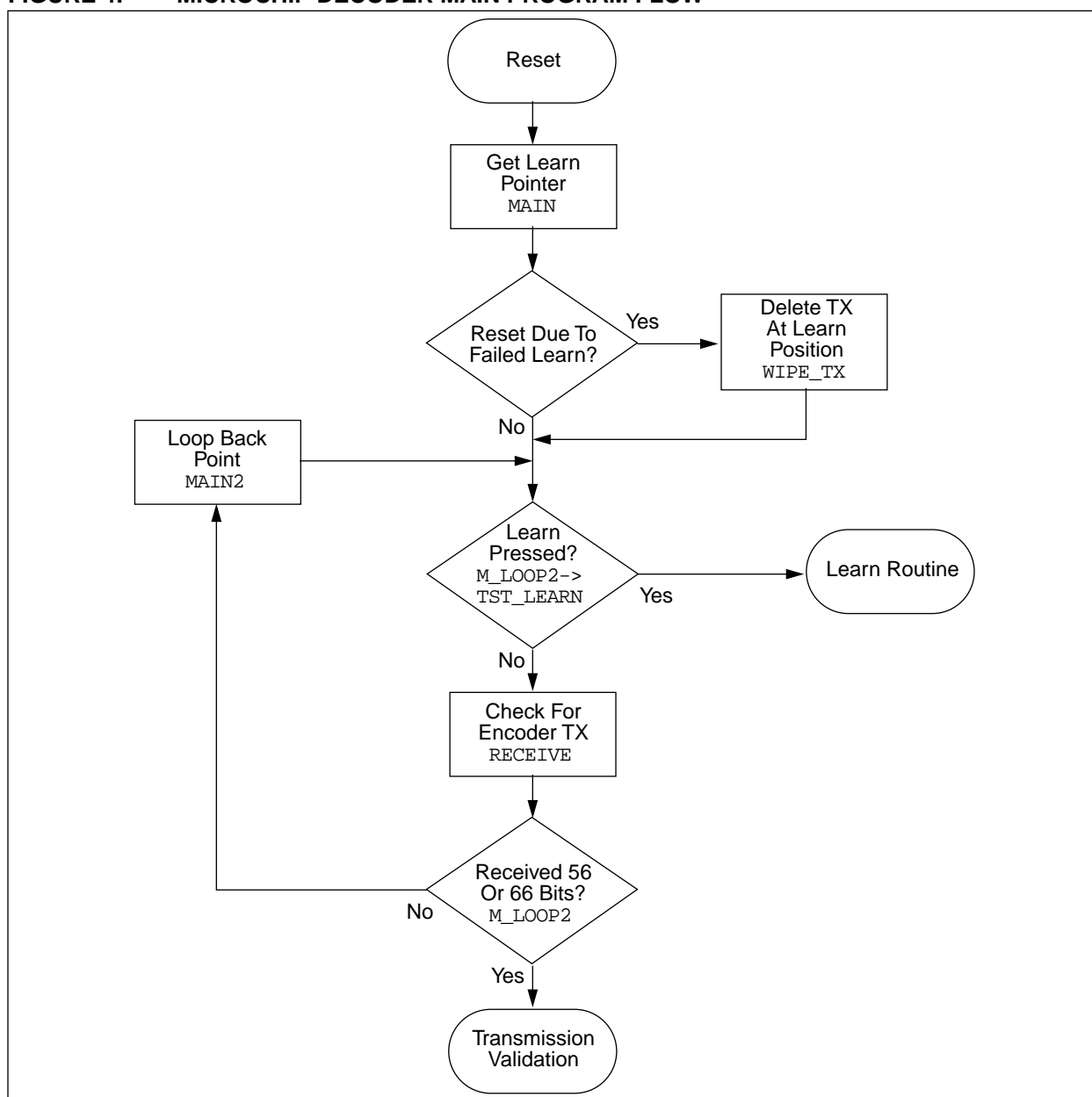
The main program flow is described here. More detailed descriptions of the modules can be found further in the application note. On power-up the decoder reads the learn indicator from the external EEPROM. The status flags are checked to see if a learn routine was interrupted when the microcontroller was reset. If

so, it is assumed the learn cycle was not successfully completed and the encoder at the learn indicator subsequently deleted (WIPE_TX).

The encoder then enters the main loop where it spends most of its time. The main loop checks to see if the learn button is being activated (TST_LEARN). If so, the decoder enters the learn mode.

If learn has not been initiated, the microcontroller then checks for transmissions from encoders (RECEIVE). If 64 bits (HCS encoders) are received, the microcontroller validates the transmission received. If the transmission received is a valid transmission from an encoder learned into the system, the system sets the appropriate outputs (M_BUT).

FIGURE 4: MICROCHIP DECODER MAIN PROGRAM FLOW



FUNCTIONAL MODULES

Reception

The reception routine (`RECEIVE`) is based on a reliable algorithm which has successfully been used in previous implementations of KEELOQ decoders. Automatic baud rate detection is used to compensate for variations in baud rate of different encoders of a specific type, as well as the difference in baud rate between different encoders (HCS200 and HCS300). The reception routine is able to handle 64-bit transmissions. This is easily extended to receive more bits. The reception routine is able to determine the type of encoder by the number of bits in the transmission.

The reception algorithm performs the following functions when an output is detected from the receiver:

1. Calibrate on the header low period to determine the actual elemental period for the transmission being received. The required elemental period is 10% of the low header period. In the diagram below (Figure 5) the header calibration sample points are marked 1 through 3. The calibration flow chart (Figure 6) shows at what points in the source code samples 1, 2, and 3 are taken.
Elemental periods outside the capture range of the algorithm (either too long or too short) should be rejected, since they would be due either to noise or to reception of an incomplete signal.
2. Using the determined elemental period, three samples after the first rising edge following the header are taken. The first sample is taken half an elemental period after the rising edge (Sample 4); the second, one elemental period later (Sample 5), and the third, another one elemental period later (Sample 6). The first sample must be high, the second could be either high or low, and the third sample must be low. If either the first or the third sample is not as expected, the attempt at capturing a transmission is abandoned. In the diagram below (Figure 5), the data sample points are points 4 through 6. The flow chart describing data reception (Figure 7) shows where in the code the samples are taken.
3. If all 64 bits have been captured, each with the correct first and third elements, the transmission can be assumed to be correct, and decryption can commence.

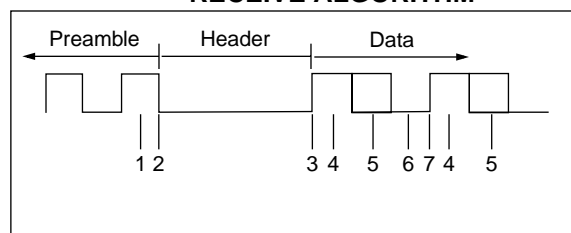
The receiving routine should be called often enough to ensure that the high portion in the header is not missed (Sample 1, Figure 5).

In systems where the receive routine is called to check if there is activity on the receiver input, the routine should poll the input for a valid transmission for at least the time taken to complete one transmission if activity is detected on the input line. This makes provision for the receive routine being called while a transmission is in progress. Having missed the first header, the first transmission will be invalid and be discarded. The decoder should continue sampling the input through the guard time in order to catch the next header and transmission (i.e., for a decoder designed to capture HCS300 transmissions the time spent polling for a valid transmission should be at least 100 ms if activity is detected in the input line).

The diagram below (Figure 5) gives all the major sampling points in the receive algorithm.

Note: The sample points are labeled in the receive routine flow diagrams that follow.

FIGURE 5: SAMPLING POINTS USED IN RECEIVE ALGORITHM



Flow Diagrams

The first flow diagram (Figure 6) describes the calibration routine which is used to determine the actual transmission rate of the encoder so that the decoder can compensate for deviations from nominal timing. There are four different exit points, each of which should branch to a point in the program where housekeeping and input monitoring can be resumed. There is only one exit point for a valid calibration operation (RCV7). At this point, it is assumed that a valid header has been received and that a string of data bits will follow.

The second flow diagram (Figure 7) handles the reception of bits once the calibration routine has been successfully completed. The data bits are all sampled three times each to ensure that a noise free transmission has been received. The receive routine uses the calibrated elemental period, determined in the calibration routine, to ensure that the samples are spaced correctly. The routine resynchronizes itself on the rising flank of each bit. Provision for identification of the encoder type, based on the number of bits received, is included. Keeloq encoders transmit at least 66 bits. The decoder only receives 64 bits of the transmission, the remaining status bits aren't used by the decoder.

If all of the control samples in all of the bits are sampled correctly (i.e., the first element is high and the last element is low), the routine checks whether 56 bits have been received correctly. If not, the routine returns to the calling procedure.

FIGURE 6: CALIBRATION FLOW CHART

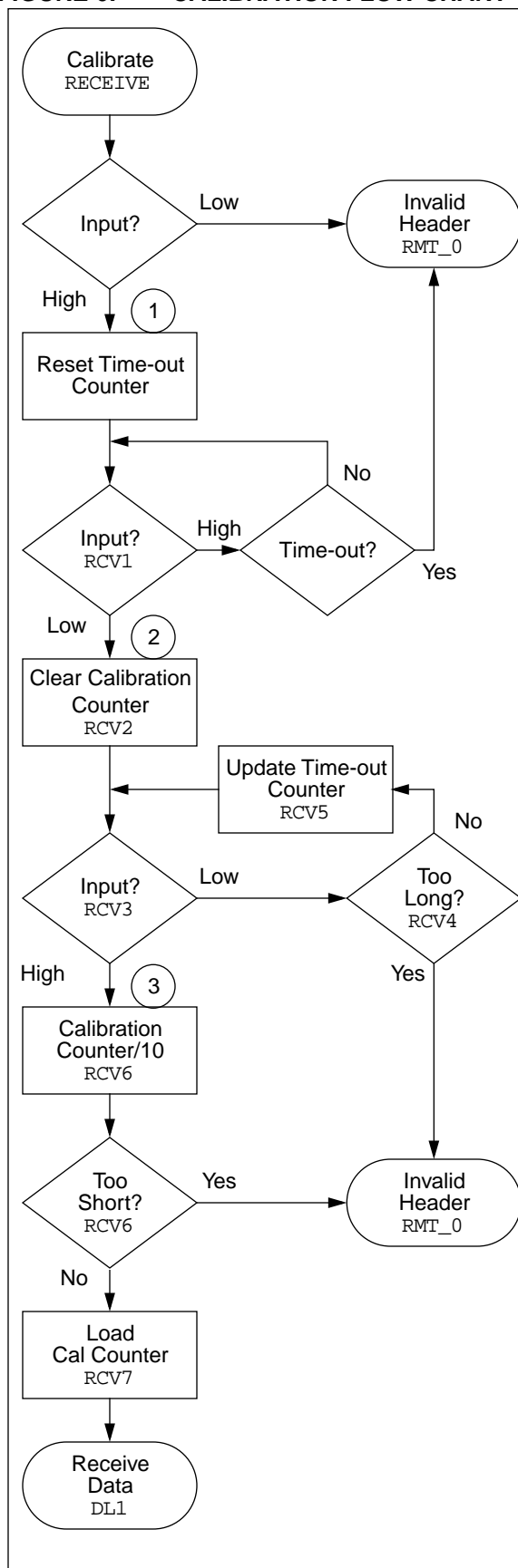
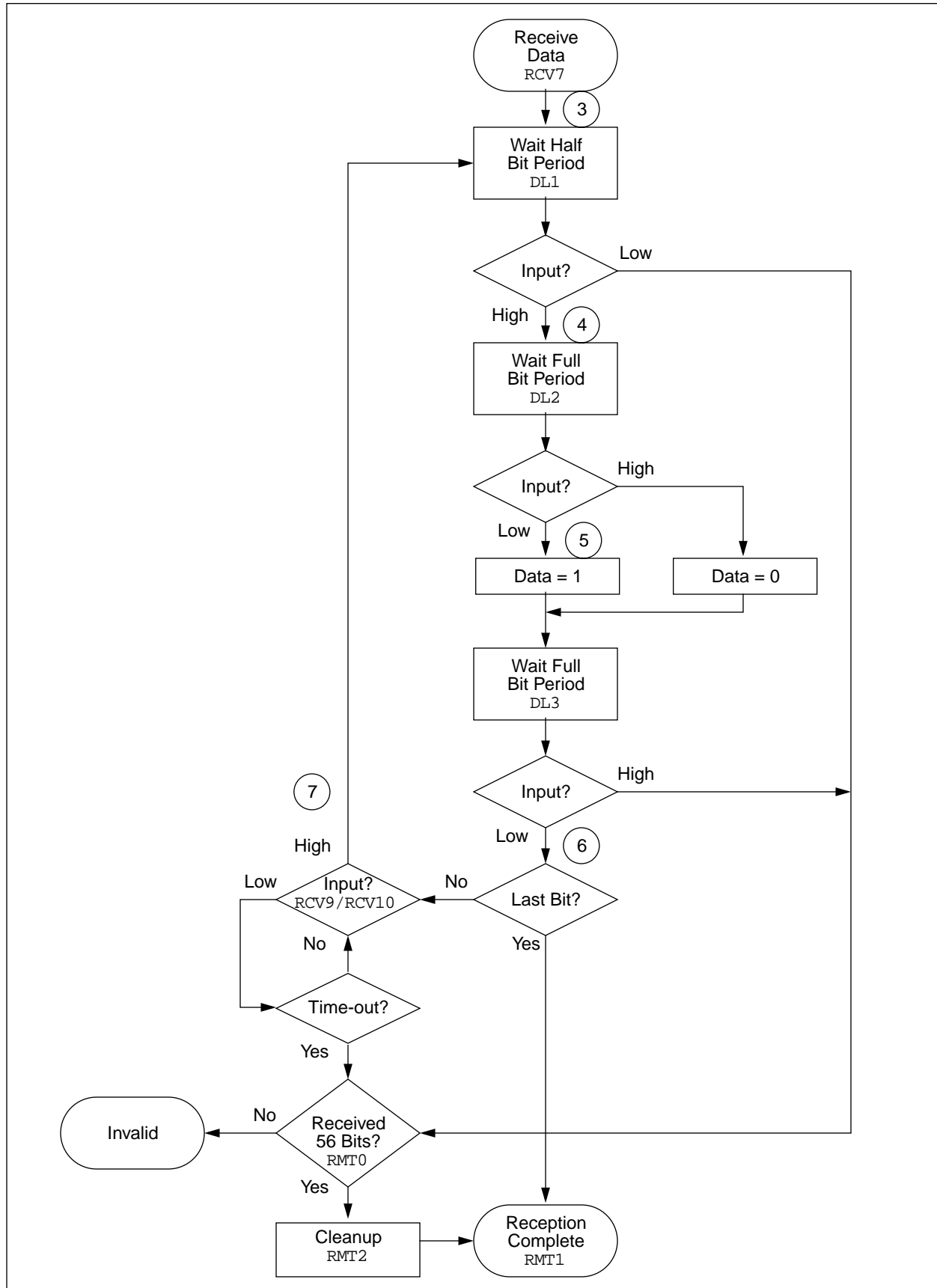


FIGURE 7: DATA RECEPTION IN RECEIVE



AN661

VALIDATION

SYNCHRONIZATION

FUNCTION INTERPRETATION

OUTPUT ACTIVATION

KEY GENERATION

DECRYPTION

LEARN

ROM MEMORY MAP

EEPROM MEMORY MAP

RAM MEMORY MAP

The confidential and proprietary information contained in this section of AN642 has been removed. The full application note is available under a license agreement and can be ordered as DS40149 from Microchip Technology Inc.

DEVICE PINOUTS

The device used in the application note is a PIC16C56 PDIP.

TABLE 9: DEVICE PINOUTS

| PIN | PIC16C56 Function | Decoder Function | PIN | PIC16C56 Function | Decoder Function |
|-----|-------------------|----------------------------|-----|-------------------|------------------|
| 1 | PORTA Bit2 | LEARN Input Active Low | 18 | PORTA Bit1 | RF Input |
| 2 | PORTA Bit3 | LRN IND Output Active High | 17 | PORTA Bit0 | Not used |
| 3 | TIME | Connect to VDD | 16 | Osc In | RC osc (4 MHz) |
| 4 | MCLR | Brown out detect | 15 | Osc Out | |
| 5 | GND | Ground | 14 | VDD | +5V supply |
| 6 | PORTB Bit0 | S0 | 13 | PORTB Bit7 | FUNC OK |
| 7 | PORTB Bit1 | S1 | 12 | PORTB Bit6 | EEPROM CS (1) |
| 8 | PORTB Bit2 | S2 | 11 | PORTB Bit5 | EEPROM CLK (2) |
| 9 | PORTB Bit3 | S3 | 10 | PORTB Bit4 | EEPROM DIO (3+4) |

TIMING PARAMETERS

TABLE 10: TIMING PARAMETERS

| Parameter | Typical | Unit |
|---|---------|------|
| Output activation duration | 524 | ms |
| Output pause if new function code received | 131 | ms |
| Erase all duration | 8.4 | s |
| Learn mode time-out | 33.6 | s |
| Learn successful $\overline{\text{LED}}$ flash duration | 4.2 | s |
| Learn successful $\overline{\text{LED}}$ flash rate | 3.8 | Hz |
| Learn failure $\overline{\text{LED}}$ on duration | 1 | s |

SOURCE CODE LISTING

A diskette is supplied containing source code for the Microchip decoder in the file `mddec12.asm`. The code has been compiled using MPASM v02.13.00. Certain functions are dependent on the oscillator speed for correct functioning. Examples of time dependent functions include `RECEIVE` and `TST_RTCC`. The PIC16C56 Microcontroller should run at 4 MHz.

LIST OF IMPORTANT FUNCTIONS

| Function Name | Description | Function Length |
|---------------|---|-----------------|
| CALC_KEY | Key generation routine. | 62 |
| DECRYPT | Decryption routine for Code Hop. | 61 |
| EEREAD | The data in the EEPROM at ADDRESS is read and decrypted to TMP1 and TMP2. Note that TMP1, TMP2 and ADDRESS are user defined registers. | 31 |
| EEWRITE | The data in TMP1 and TMP2 is encrypted and written to the EEPROM at ADDRESS. Note that TMP1, TMP2 and ADDRESS are user defined registers. | 48 |
| M_DIS | Check discrimination value. | 19 |
| M_CNT | Check synchronization (counter) values. | 69 |
| RECEIVE | Start of the RF receive routine. | 121 |
| TST_LEARN1 | Check for learn mode and entry to learn. | 21 |
| TST_RTCC | Check TIMER0 and do whatever real time tasks are required. | 38 |

APPENDIX A: APPENDIX SCHEMATIC DIAGRAMS

FIGURE A1: SCHEMATIC DIAGRAM OF MICROCHIP KEELoQ DECODER

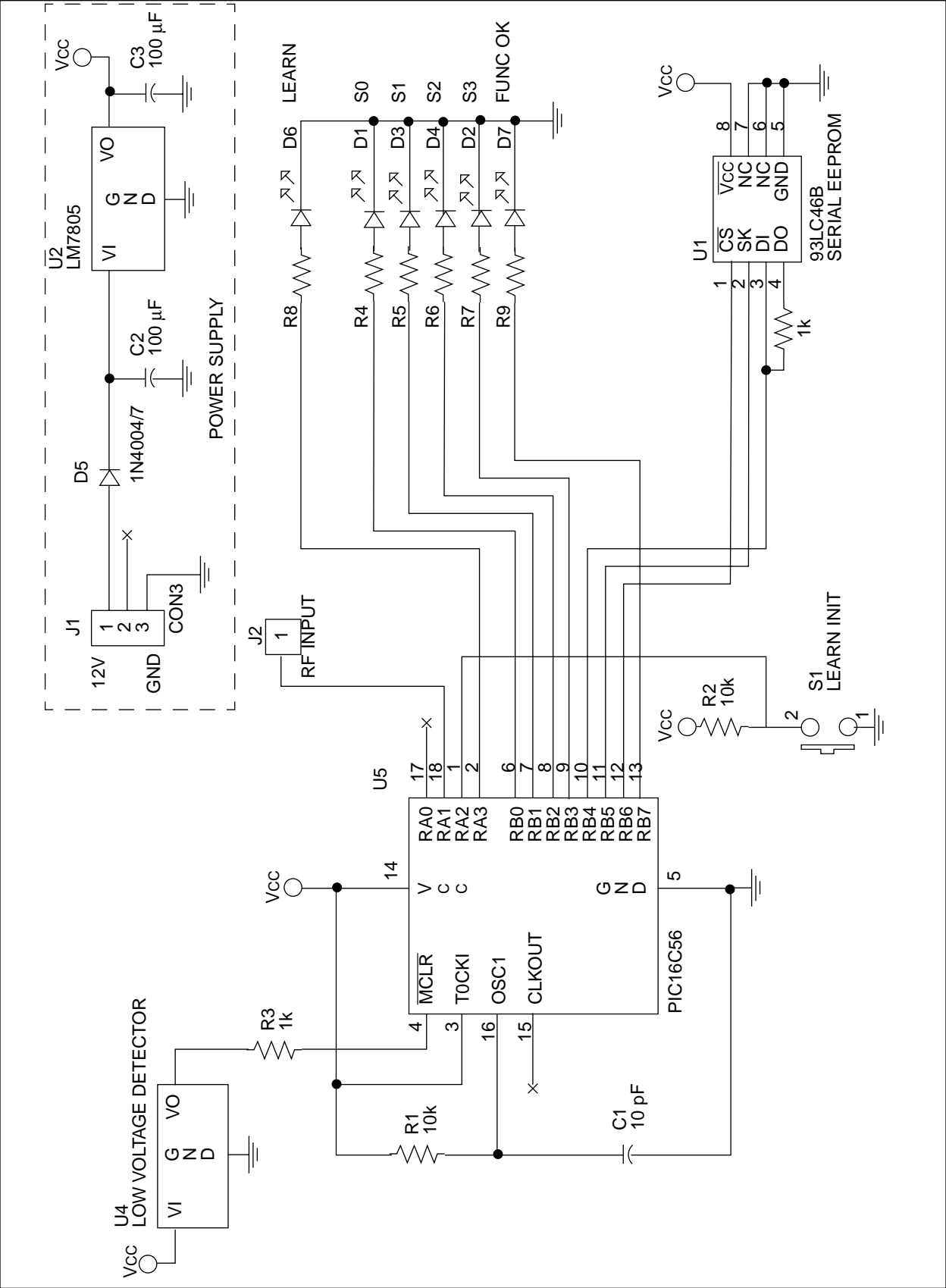
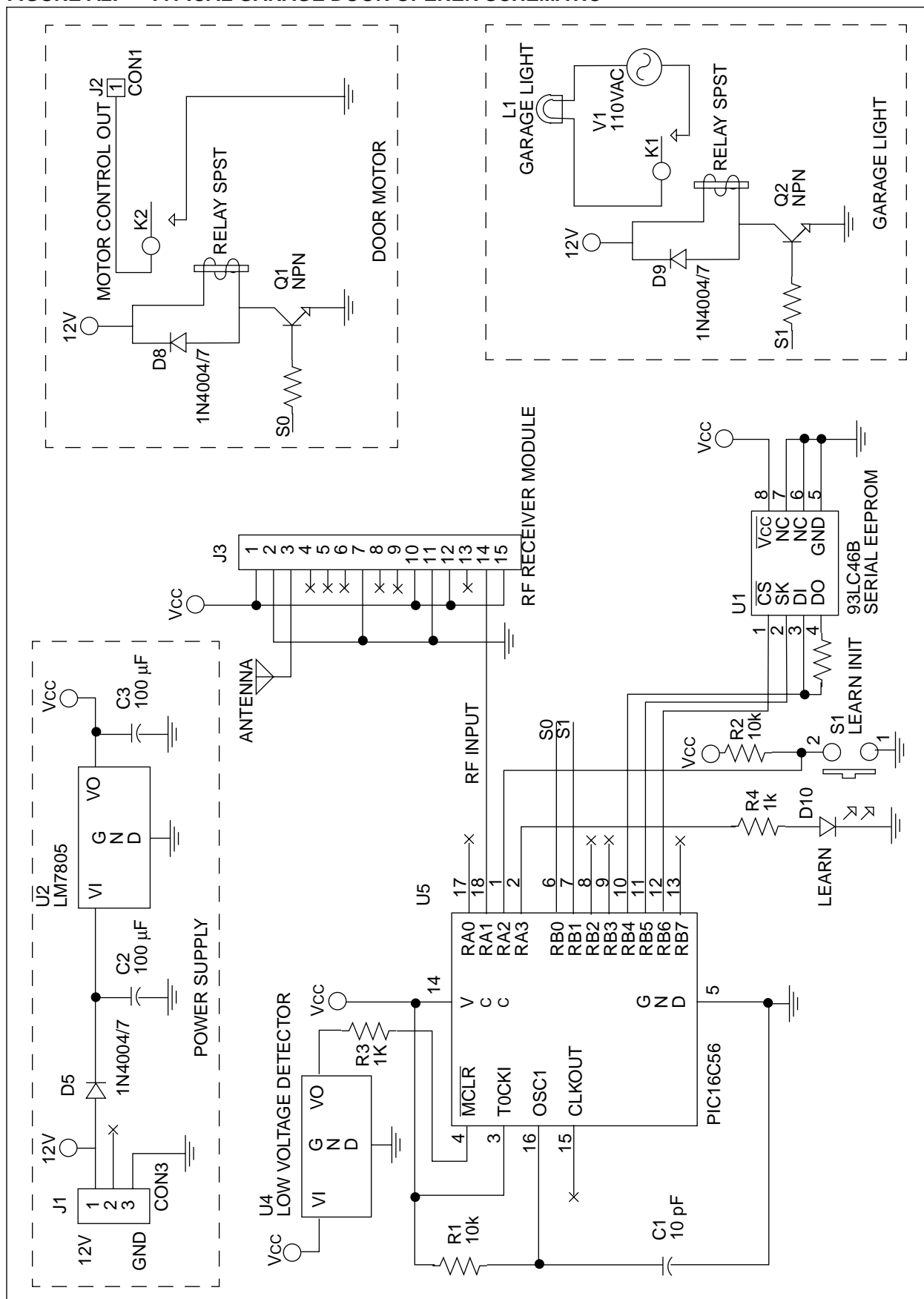


FIGURE A2: TYPICAL GARAGE DOOR OPENER SCHEMATIC



NOTES:

NOTES:

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