CDP6872

January 1996

Low Power Crystal Oscillator

Features

- **Single Supply Operation at 32kHz . . . . . 2.0V to 7.0V**
- **Operating Frequency Range. . . . . 10kHz to 10MHz**
- **Supply Current at 32kHz 5μA**
- **Supply Current at 1MHz 130μA**
- **Drives 2 CMOS Loads**
- **Only Requires an External Crystal for Operation**

Applications

- **Battery Powered Circuits**
- **Remote Metering**
- **Embedded Microprocessors**
- **Palm Top/Notebook PC**

Description

The CDP6872 is a very low power crystal-controlled oscillators that can be externally programmed to operate between 10kHz and 10MHz. For normal operation it requires only the addition of a crystal. The part exhibits very high stability over a wide operating voltage and temperature range.

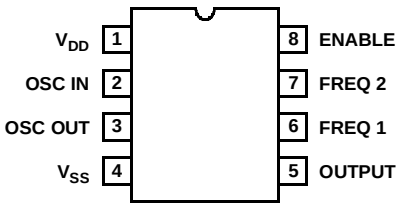
The CDP6872 also features a disable mode that switches the output to a high impedance state. This feature is useful for minimizing power dissipation during standby and when multiple oscillator circuits are employed.

Ordering Information

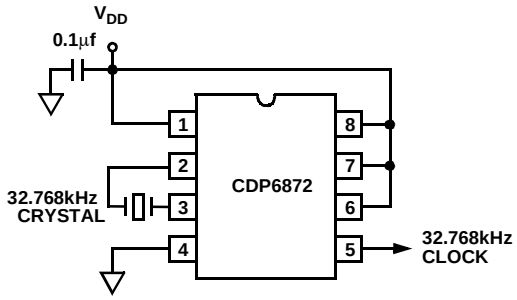
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CDP6872E	-40°C to +85°C	8 Lead Plastic DIP
CDP6872M	-40°C to +85°C	8 Lead Plastic SOIC (N)
CDP6872H	-40°C to +85°C	DIE

Pinout

CDP6872 (PDIP, SOIC)
TOP VIEW

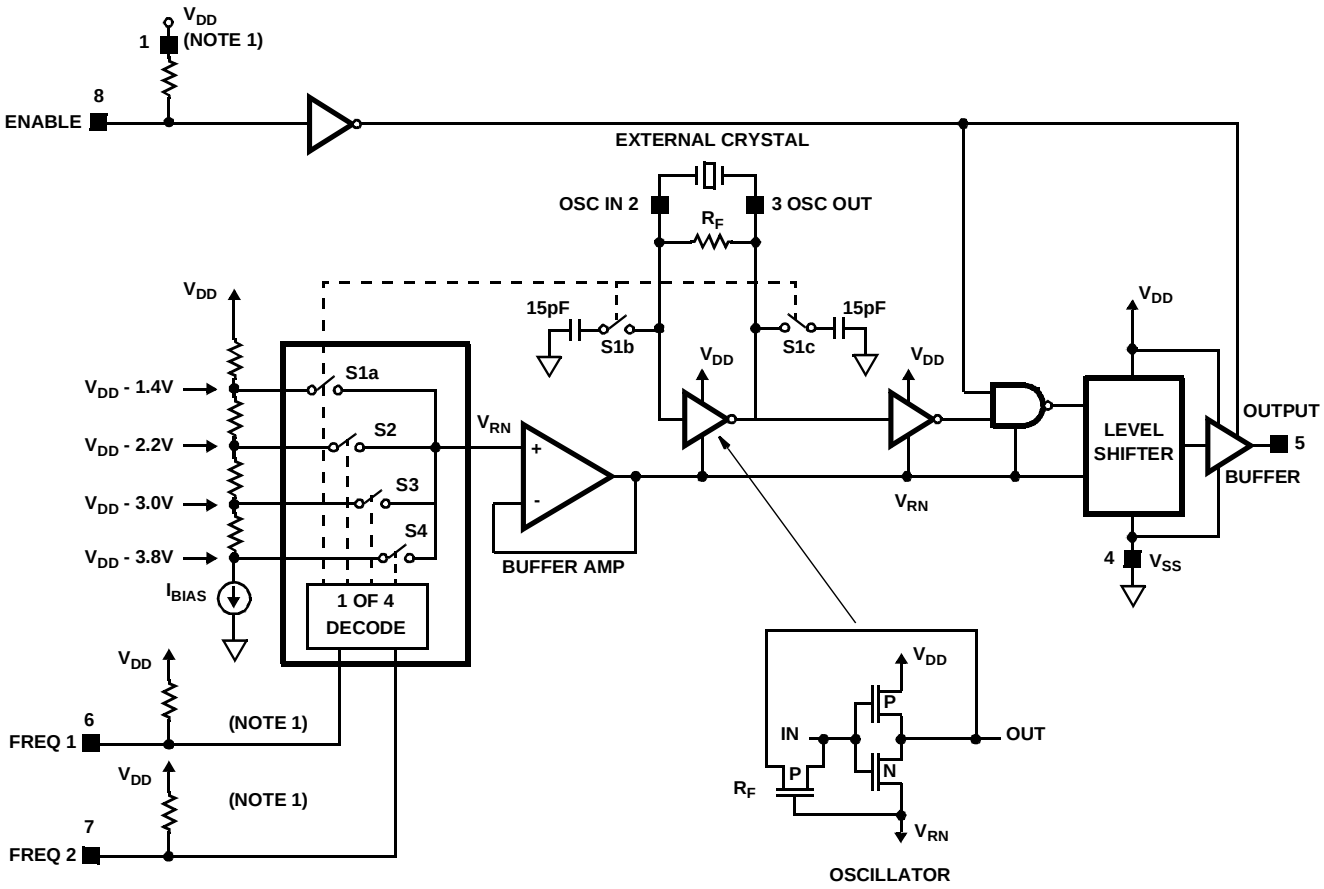


Typical Application Circuit



32.768kHz MICROPOWER CLOCK OSCILLATOR

Simplified Block Diagram



FREQUENCY SELECTION TRUTH TABLE

ENABLE	FREQ 1	FREQ 2	SWITCH	OUTPUT RANGE
1	1	1	S1a, b, c	10kHz - 100kHz
1	1	0	S2	100kHz - 1MHz
1	0	1	S3	1MHz - 5MHz
1	0	0	S4	5MHz - 10MHz+
0	X	X	X	High Impedance

NOTE:

1. Logic input pull-up resistors are constant current source of 0.4µA.

Absolute Maximum Ratings

Supply Voltage 10.0V
Voltage (any pin) . . . . . V_{SS}-0.3V to V_{DD}+0.3V
Junction Temperature (Plastic Package) . . . . . +150^{o}C
ESD Rating (Note 2) . . . . . >4000V
Lead Temperature (Soldering 10s) . . . . . +300^{o}C
(SOIC - Lead Tip Only)

Operating Conditions

Operating Temperature (Note 3) . . . . . -40^{o}C to +85^{o}C
Storage Temperature Range . . . . . -65^{o}C to +150^{o}C

Thermal Information (Typical)

Thermal Resistance (^{o}C/W)	θ_{JA}
8 Lead Plastic DIP	125
8 Lead Plastic SOIC	170

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SS} = GND, T_A = +25^{o}C, Unless Otherwise Specified

PARAMETER	V_{DD} = 5V			V_{DD} = 3V			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{DD} Supply Range (f_{OSC} = 32kHz)	2	5	7	-	-	-	V
I_{DD} Supply Current							
f_{OSC} = 32kHz, EN = 0 Standby	-	5.0	9.0	-	-	-	µA
f_{OSC} = 32kHz, C_L = 10pF (Note 1), EN = 1, Freq1 = 1, Freq2 = 1	-	5.2	10.2	-	3.6	6.1	µA
f_{OSC} = 32kHz, C_L = 40pF, EN = 1, Freq1 = 1, Freq2 = 1	-	10	15	-	6.5	9	µA
f_{OSC} = 1MHz, C_L = 10pF (Note 1), EN = 1, Freq1 = 0, Freq2 = 1	-	130	200	-	90	180	µA
f_{OSC} = 1MHz, C_L = 40pF, EN = 1, Freq1 = 0, Freq2 = 1	-	270	350	-	180	270	µA
V_{OH} Output High Voltage (I_{OUT} = -1mA)	4.0	4.9	-	-	2.8	-	V
V_{OL} Output Low Voltage (I_{OUT} = 1mA)	-	0.07	0.4	-	0.1	-	V
I_{OH} Output High Current ($V_{OUT} \geq$ 4V)	-	-10	-5	-	-	-	mA
I_{OL} Output Low Current ($V_{OUT} \leq$ 0.4V)	5.0	10.0	-	-	-	-	mA
Three-State Leakage Current							
(V_{OUT} = 0V, 5V, T_A = 25^{o}C, -40^{o}C)	-	0.1	-	-	-	-	nA
(V_{OUT} = 0V, 5V, T_A = 85^{o}C)	-	10	-	-	-	-	nA
I_{IN} Enable, Freq1, Freq2 Input Current (V_{IN} = V_{SS} to V_{DD})	-	0.4	1.0	-	-	-	µA
V_{IH} Input High Voltage Enable, Freq1, Freq2	2.0	-	-	-	-	-	V
V_{IL} Input Low Voltage Enable, Freq1, Freq2	-	-	0.8	-	-	-	V
Enable Time (C_L = 18pF, R_L = 1kΩ)	-	800	-	-	-	-	ns
Disable Time (C_L = 18pF, R_L = 1kΩ)	-	90	-	-	-	-	ns
t_R Output Rise Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	12	25	-	12	-	ns
t_F Output Fall Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	12	25	-	14	-	ns
Duty Cycle (C_L = 40pF) f_{OSC} = 1MHz, Packaged Part Only (Note 4)	40	54	60	-	-	-	%
Duty Cycle (C_L = 40pF) f_{OSC} = 32kHz, (See Typical Curves)	-	41	-	-	44	-	%
Frequency Stability vs. Supply Voltage (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	1	-	-	-	-	ppm/V
Frequency Stability vs. Temperature (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.1	-	-	-	-	ppm/^{o}C
Frequency Stability vs. Load (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.01	-	-	-	-	ppm/pF

NOTES:

1. Calculated using the equation I_{DD} = I_{DD} (No Load) + (V_{DD}) (f_{OSC})(C_L)
2. Human body model.
3. This product is production tested at +25^{o}C only.
4. Duty cycle will vary with supply voltage, oscillation frequency, and parasitic capacitance on the crystal pins.

Test Circuits

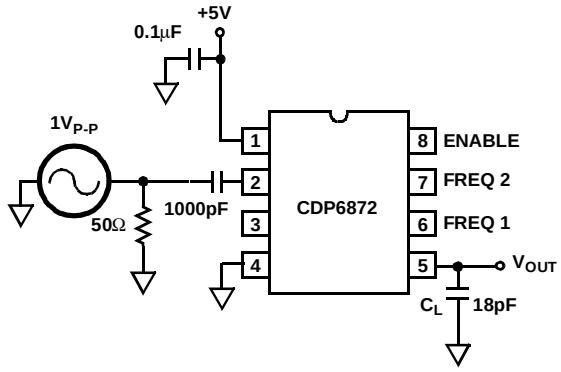


FIGURE 1.

In production the CDP6872 is tested with a 32kHz and a 1MHz crystal. However for characterization purposes data was taken using a sinewave generator as the frequency determining element, as shown in Figure 1. The $1V_{P-P}$ input is a smaller amplitude than what a typical crystal would generate so the transitions are slower. In general the Generator data will show a "worst case" number for I_{DD}, duty cycle, and rise/fall time. The Generator test method is useful for testing a variety of frequencies quickly and provides curves which can be used for understanding performance trends. Data for the CDP6872 using crystals has also been taken. This data has been overlaid onto the generator data to provide a reference for comparison.

Theory of Operation

The CDP6872 is a Pierce Oscillator optimized for low power consumption, requiring no external components except for a bypass capacitor and a Parallel Mode Crystal. The Simplified Block Diagram shows the Crystal attached to pins 2 and 3, the Oscillator input and output. The crystal drive circuitry is detailed showing the simple CMOS inverter stage and the P-channel device being used as biasing resistor R_F. The inverter will operate mostly in its linear region increasing the amplitude of the oscillation until limited by its transconductance and voltage rails, V_{DD} and V_{RN}. The inverter is self biasing using R_F to center the oscillating waveform at the input threshold. Do not interfere with this bias function with external loads or excessive leakage on pin 2. Nominal value for R_F is 17MΩ in the lowest frequency range to 7MΩ in the highest frequency range.

The CDP6872 optimizes its power for 4 frequency ranges selected by digital inputs Freq1 and Freq2 as shown in the Block Diagram. Internal pull up resistors (constant current 0.4μA) on Enable, Freq1 and Freq2 allow the user simply to leave one or all digital inputs not connected for a corresponding "1" state. All digital inputs may be left open for 10kHz to 100kHz operation.

A current source develops 4 selectable reference voltages through series resistors. The selected voltage, V_{RN}, is buffered and used as the negative supply rail for the oscillator section of the circuit. The use of a current source in the reference string allows for wide supply variation with minimal effect on performance. The reduced operating voltage of the oscillator section reduces power consumption and limits transconductance and bandwidth to the frequency range selected. For frequencies at the edge of a range, the higher range may provide better performance.

The OSC OUT waveform on pin 3 is squared up through a series of inverters to the output drive stage. The Enable function is implemented with a NAND gate in the inverter string, gating the signal to the level shifter and output stage. Also during Disable the output is set to a high impedance state useful for minimizing power during standby and when multiple oscillators are OR'd to a single node.

Design Considerations

The low power CMOS transistors are designed to consume power mostly during transitions. Keeping these transitions short requires a good decoupling capacitor as close as possible to the supply pins 1 and 4. A ceramic 0.1μF is recommended. Additional supply decoupling on the circuit board with 1μF to 10μF will further reduce overshoot, ringing and power consumption. The CDP6872, when compared to a crystal and inverter alone, will speed clock transition times, reducing power consumption of all CMOS circuitry run from that clock.

Power consumption may be further reduced by minimizing the capacitance on moving nodes. The majority of the power will be used in the output stage driving the load. Minimizing the load and parasitic capacitance on the output, pin 5, will play the major role in minimizing supply current. A secondary source of wasted supply current is parasitic or crystal load capacitance on pins 2 and 3. The CDP6872 is designed to work with most available crystals in its frequency range with no external components required. Two 15pF capacitors are internally switched onto crystal pins 2 and 3 to compensate the oscillator in the 10kHz to 100kHz frequency range.

The supply current of the CDP6872 may be approximately calculated from the equation:

$$I_{DD} = I_{DD}(\text{Disabled}) + V_{DD} \times F_{OSC} \times C_L$$

where: I_{DD} = Total supply current
V_{DD} = Total voltage from V_{DD} (pin1) to V_{SS} (pin4)
F_{OSC} = Frequency of Oscillation
C_L = Output (pin5) load capacitance

Example #1:

V_{DD} = 5V, F_{OSC} = 100kHz, C_L = 30pF
I_{DD}(Disabled) = 4.5μA (Figure 10)
I_{DD} = 4.5μA + (5V)(100kHz)(30pF) = 19.5μA
Measured I_{DD} = 20.3μA

Example #2:

V_{DD} = 5V, F_{OSC} = 5MHz, C_L = 30pF
I_{DD}(Disabled) = 75μA (Figure 9)
I_{DD} = 75μA + (5V)(5MHz)(30pF) = 825μA
Measured I_{DD} = 809μA

Crystal Selection

For general purpose applications, a Parallel Mode Crystal is a good choice for use with the CDP6872. However for applications where a precision frequency is required, the designer needs to consider other factors.

Crystals are available in two types or modes of oscillation, Series and Parallel. Series Mode crystals are manufactured to operate at a specified frequency with zero load capacitance and appear as a near resistive impedance when oscillating. Parallel Mode crystals are manufactured to operate with a specific capacitive load in series, causing the crystal to operate at a more inductive impedance to cancel the load capacitor. Loading a crystal with a different capacitance will "pull" the frequency off its value.

The CDP6872 has 4 operating frequency ranges. The higher three ranges do not add any loading capacitance to the oscillator circuit. The lowest range, 10kHz to 100kHz, automatically switches in two 15pF capacitors onto OSC IN and OSC OUT to eliminate potential start-up problems. These capacitors create an effective crystal loading capacitor equal to the series combination of these two capacitors. For the CDP6872, in the lowest range, the effective loading capacitance is 7.5pF. Therefore the choice for a crystal, in this range, should be a Parallel Mode crystal that requires a 7.5pF load.

In the higher 3 frequency ranges, the capacitance on OSC IN and OSC OUT will be determined by package and layout parasitics, typically 4 to 5pF. Ideally the choice for crystal should be a Parallel Mode set for 2.5pF load. A crystal manufactured for a different load will be "pulled" from its nominal frequency (see Crystal Pullability).

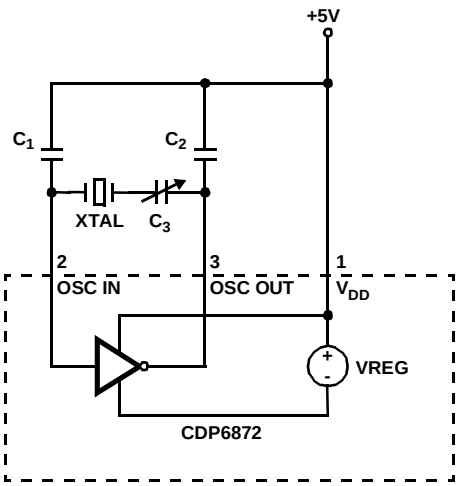


FIGURE 2.

Frequency Fine Tuning

Two Methods will be discussed for fine adjustment of the crystal frequency. The first and preferred method (Figure 2), provides better frequency accuracy and oscillator stability than method two (Figure 3). Method one also eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

For best oscillator performance, two conditions must be met: the capacitive load must be matched to both the inverter and crystal to provide ideal conditions for oscillation, and the frequency of the oscillator must be adjustable to the desired frequency. In Method two these two goals can be at odds with each other; either the oscillator is trimmed to frequency by de-tuning the load circuit, or stability is increased at the expense of absolute frequency accuracy.

Method one allows these two conditions to be met independently. The two fixed capacitors, C_1 and C_2, provide the optimum load to the oscillator and crystal. C_3 adjusts the frequency at which the circuit oscillates without appreciably changing the load (and thus the stability) of the system. Once a value for C_3 has been determined for the particular type of crystal being used, it could be replaced with a fixed capacitor. For the most precise control over oscillator frequency, C_3 should remain adjustable.

This three capacitor tuning method will be more accurate and stable than method two and is recommended for 32kHz tuning fork crystals; without it they may leap into an overtone mode when power is initially applied.

Method two has been used for many years and may be preferred in applications where cost or space is critical. Note that in both cases the crystal loading capacitors are connected between the oscillator and V_{DD}; do not use V_{SS} as an AC ground. The Simplified Block Diagram shows that the oscillating inverter does not directly connect to V_{SS} but is referenced to V_{DD} and V_{RN}. Therefore V_{DD} is the best AC ground available.

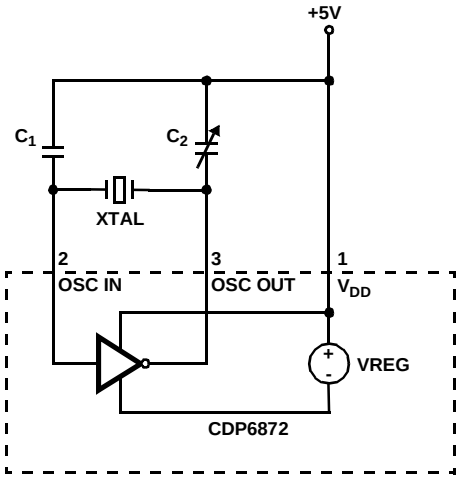


FIGURE 3.

Typical values of the capacitors in Figure 2 are shown below. Some trial and error may be required before the best combination is determined. The values listed are total capacitance including parasitic or other sources. Remember that in the 10kHz to 100kHz frequency range setting the CDP6872 switches in two internal 15pF capacitors.

CRYSTAL FREQUENCY	LOAD CAPS C1, C2	TRIMMER CAP C3
32kHz	33pF	5-50pF
1MHz	33pF	5-50pF
2MHz	25pF	5-50pF
4MHz	22pF	5-100pF

Crystal Pullability

Figure 4 shows the basic equivalent circuit for a crystal and its loading circuit.

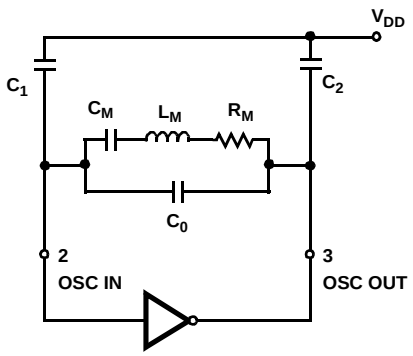


FIGURE 4.

Where: C_M = Motional Capacitance
L_M = Motional Inductance
R_M = Motional Resistance
C_0 = Shunt Capacitance

$$C_{CL} = \frac{1}{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} = \text{Equivalent Crystal Load}$$

If loading capacitance is connected to a Series Mode Crystal, the new Parallel Mode frequency of resonance may be calculated with the following equation:

$$F_P = F_S\left[1 + \frac{C_M}{2(C_0 + C_{CL})}\right]$$

Where: F_P = Parallel Mode Resonant Frequency
F_S = Series Mode Resonant Frequency

In a similar way, the Series Mode resonant frequency may be calculated from a Parallel Mode crystal and then you may calculate how much the frequency will “pull” with a new load.

Layout Considerations

Due to the extremely low current (and therefore high impedance) the circuit board layout of the CDP6872 must be given special attention. Stray capacitance should be minimized. Keep the oscillator traces on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential source of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Further Reading

Al Little “HA7210 Low Power Oscillator: Micropower Clock Oscillator and Op Amps Provide System Shutdown for Battery Circuits”. Intersil Application Note AN9317.

Robert Rood “Improving Start-Up Time at 32KHz for the HA7210 Low Power Crystal Oscillator”. Intersil Application Note AN9334.

S. S. Eaton “Timekeeping Advances Through COS/MOS Technology”. Intersil Application Note ICAN-6086.

E. A. Vittoz et. al. “High-Performance Crystal Oscillator circuits: Theory and Application”. IEEE Journal of Solid-State Circuits, Vol. 23, No3, June 1988, pp774-783.

M. A. Unkrich et. al. “Conditions for Start-Up in Crystal Oscillators”. IEEE Journal of Solid-State Circuits, Vol. 17, No1, Feb. 1982, pp87-90.

Marvin E. Frerking “Crystal Oscillator Design and Temperature Compensation”. New York: Van Nostrand-Reinhold, 1978. Pierce Oscillators Discussed pp56-75.

Die Characteristics

DIE DIMENSIONS:
68 x 64 x 14 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 10kÅ ± 1kÅ

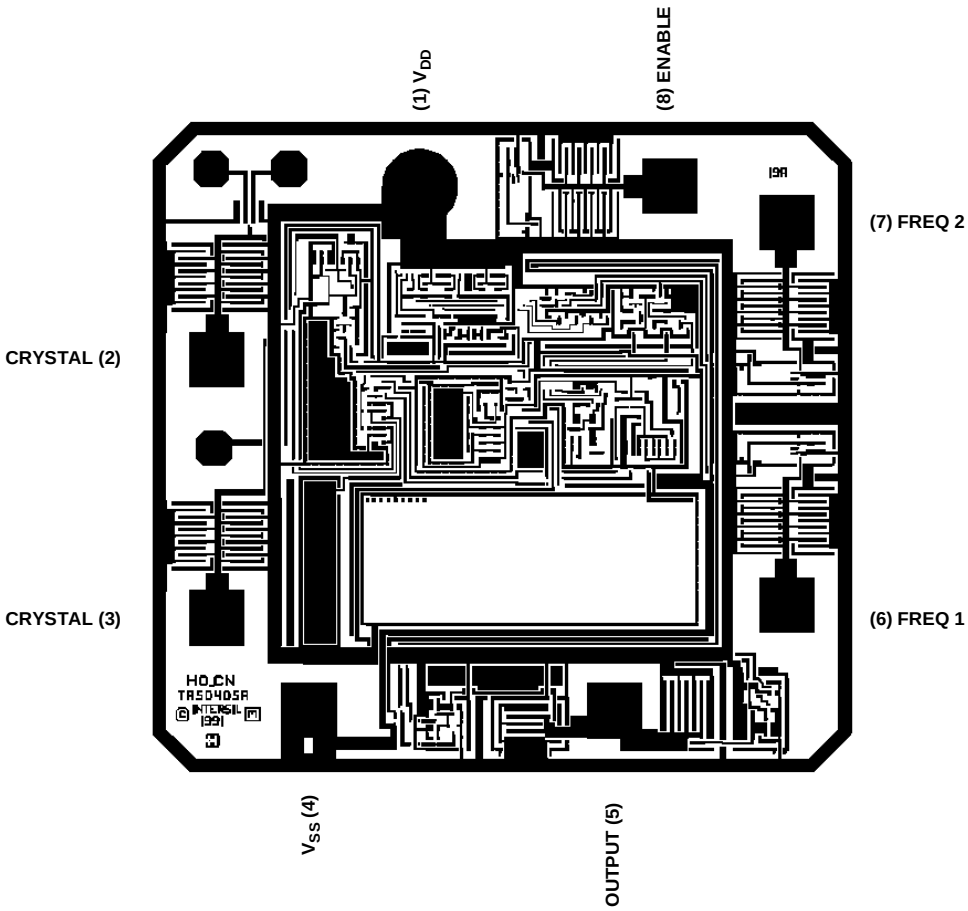
GLASSIVATION:
Type: Nitride (Si_3N_4) Over Silox (SiO_2, 3% Phos)
Silox Thickness: 7kÅ ± 1kÅ
Nitride Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Epoxy - Plastic DIP and SOIC

SUBSTRATE POTENTIAL: V_{SS}

Metallization Mask Layout

CDP6872



Typical Performance Curves

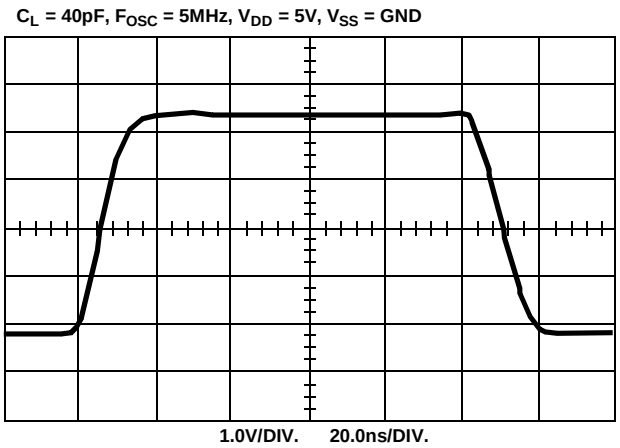


FIGURE 5. OUTPUT WAVEFORM (C_L = 40pF)

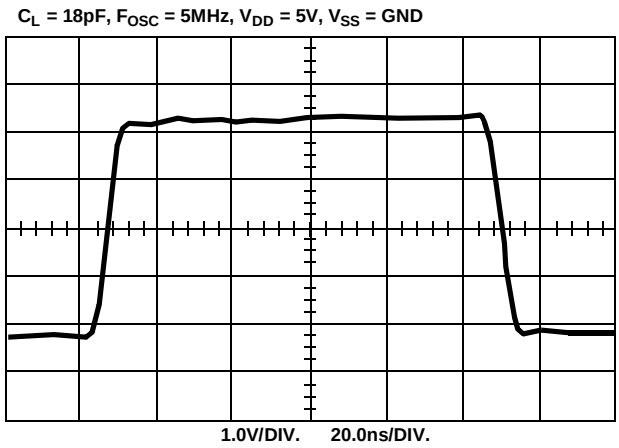


FIGURE 6. OUTPUT WAVEFORM (C_L = 18pF)

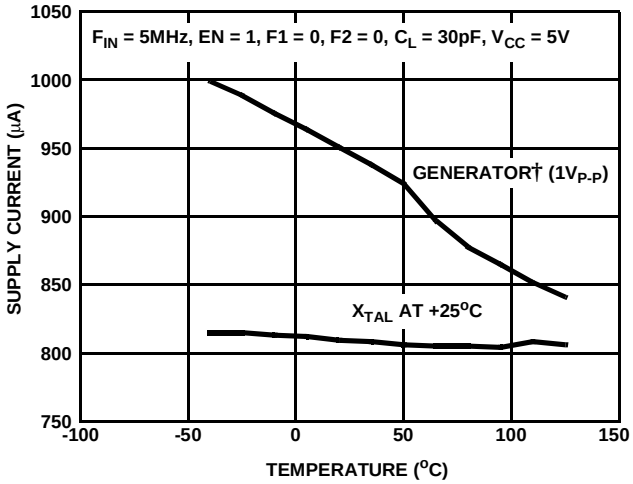


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

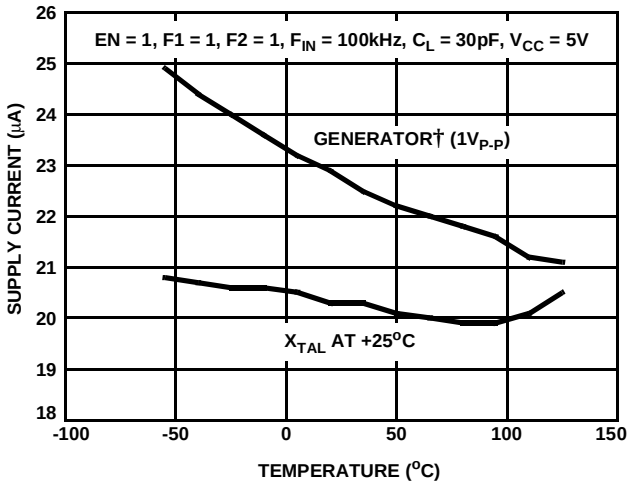


FIGURE 8. SUPPLY CURRENT vs TEMPERATURE

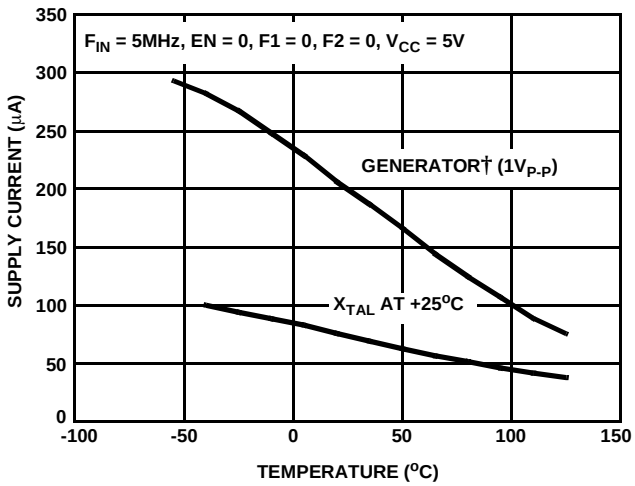


FIGURE 9. DISABLE SUPPLY CURRENT vs TEMPERATURE

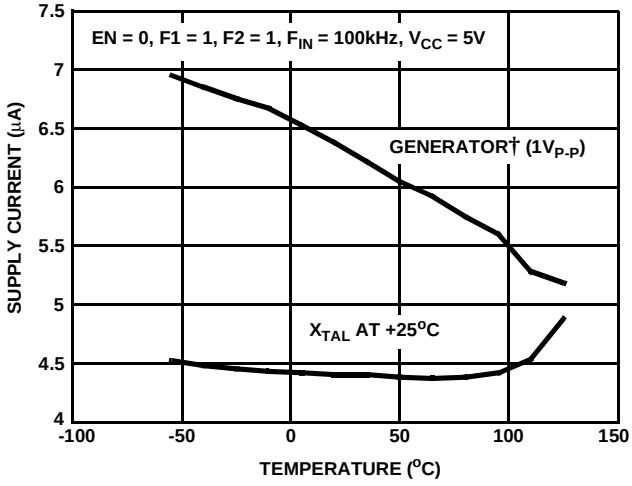


FIGURE 10. DISABLE SUPPLY CURRENT vs TEMPERATURE

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

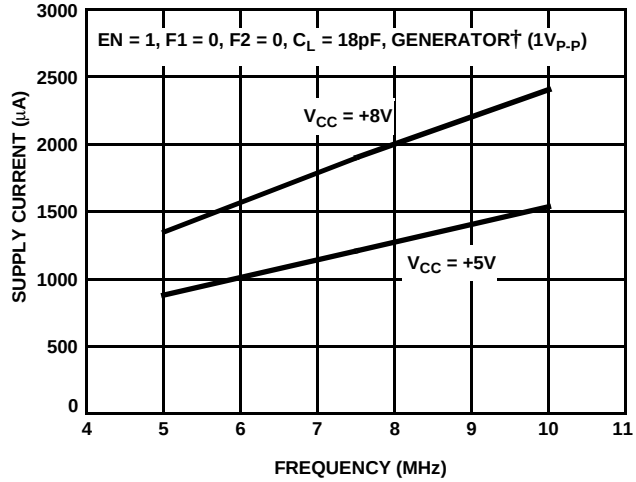


FIGURE 11. SUPPLY CURRENT vs FREQUENCY

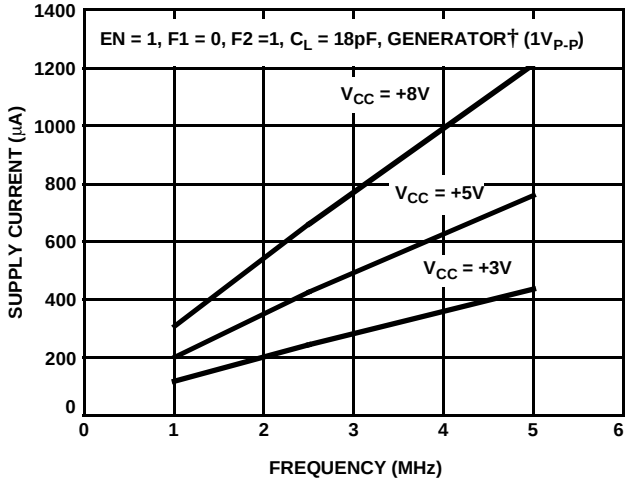


FIGURE 12. SUPPLY CURRENT vs FREQUENCY

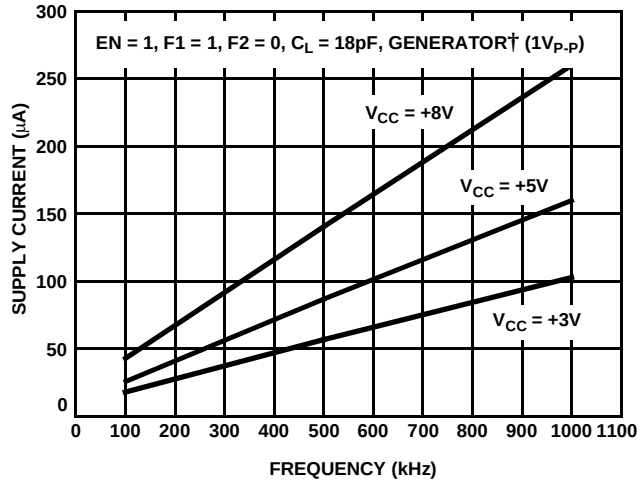


FIGURE 13. SUPPLY CURRENT vs FREQUENCY

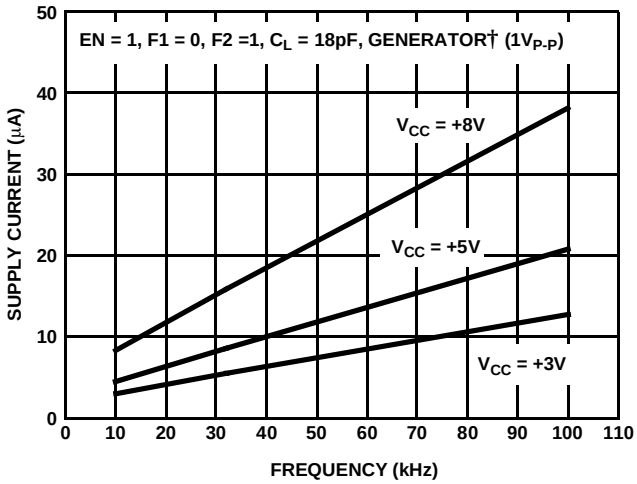


FIGURE 14. SUPPLY CURRENT vs FREQUENCY

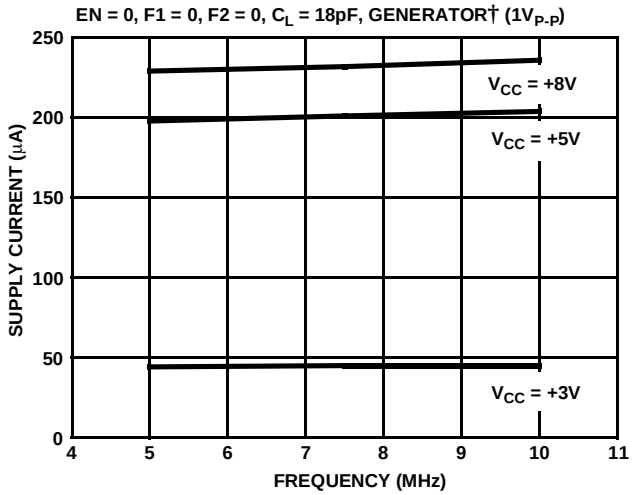


FIGURE 15. DISABLED SUPPLY CURRENT vs FREQUENCY

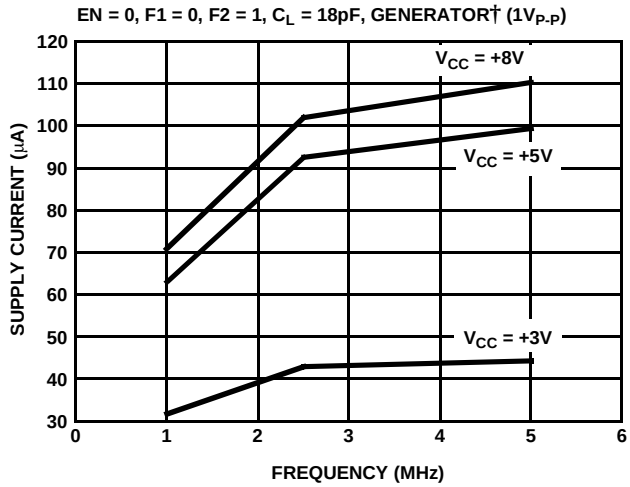


FIGURE 16. DISABLE SUPPLY CURRENT vs FREQUENCY

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

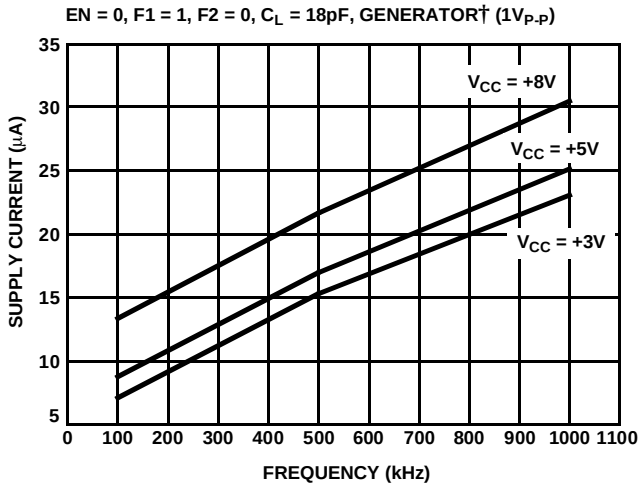


FIGURE 17. DISABLE SUPPLY CURRENT vs FREQUENCY

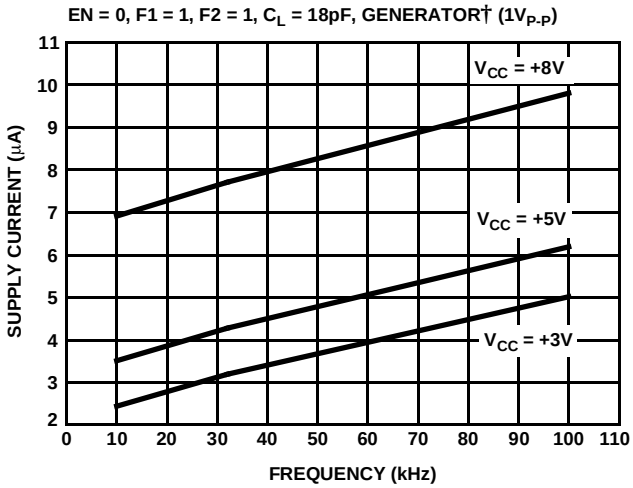


FIGURE 18. DISABLE SUPPLY CURRENT vs FREQUENCY

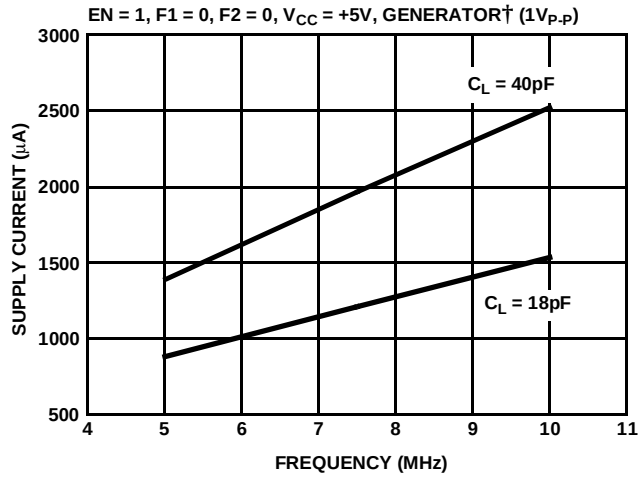


FIGURE 19. SUPPLY CURRENT vs FREQUENCY

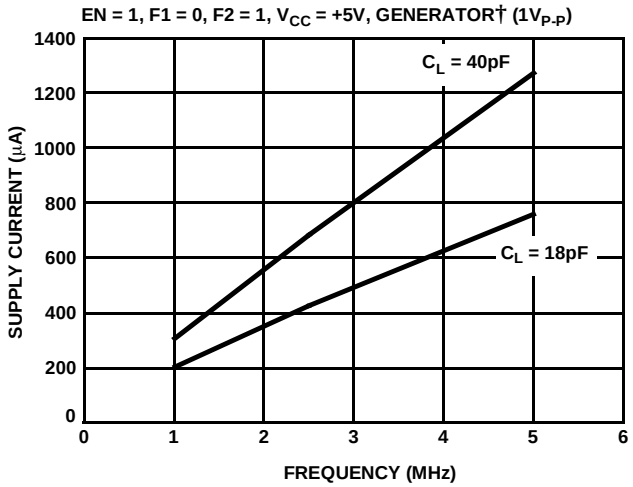


FIGURE 20. SUPPLY CURRENT vs FREQUENCY

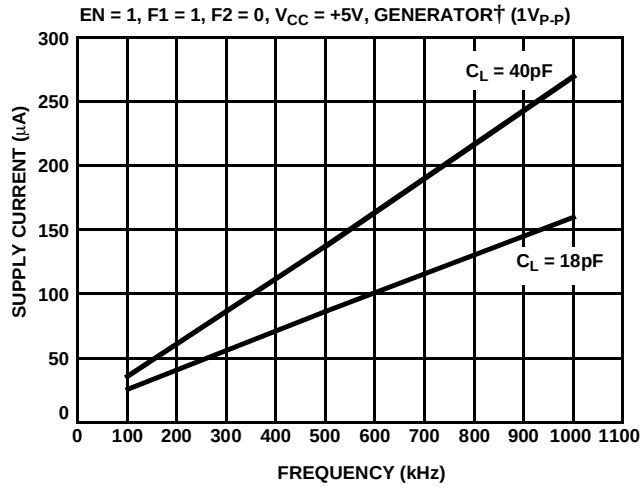


FIGURE 21. SUPPLY CURRENT vs FREQUENCY

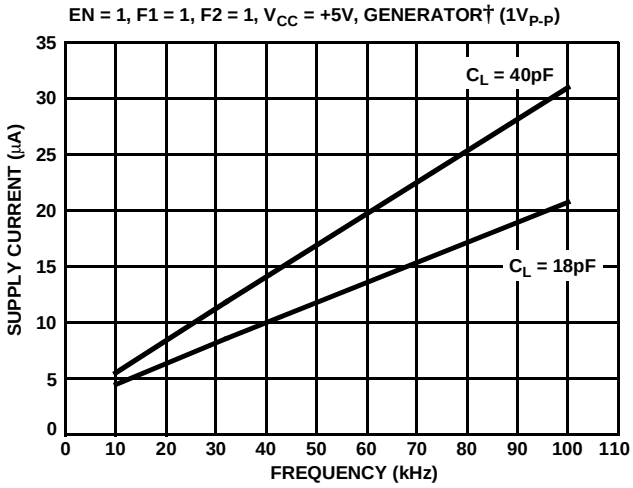


FIGURE 22. SUPPLY CURRENT vs FREQUENCY

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

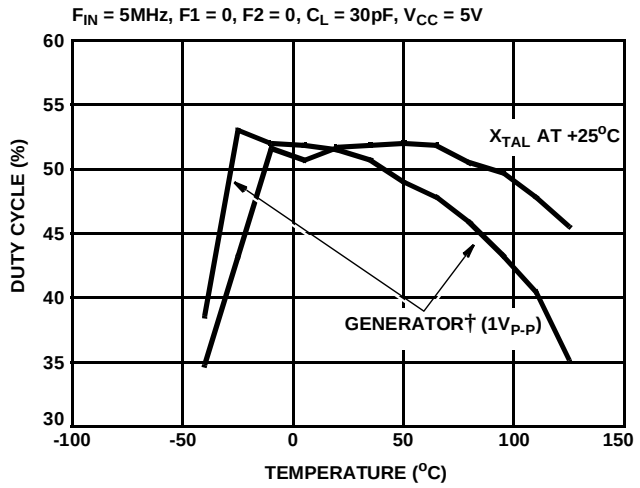


FIGURE 23. DUTY CYCLE vs TEMPERATURE

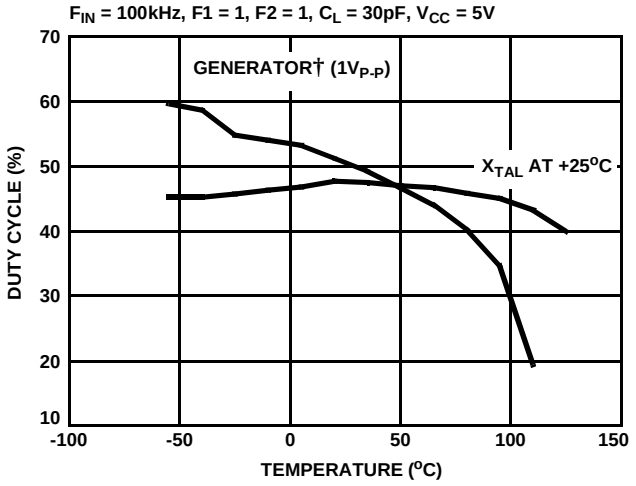


FIGURE 24. DUTY CYCLE vs TEMPERATURE

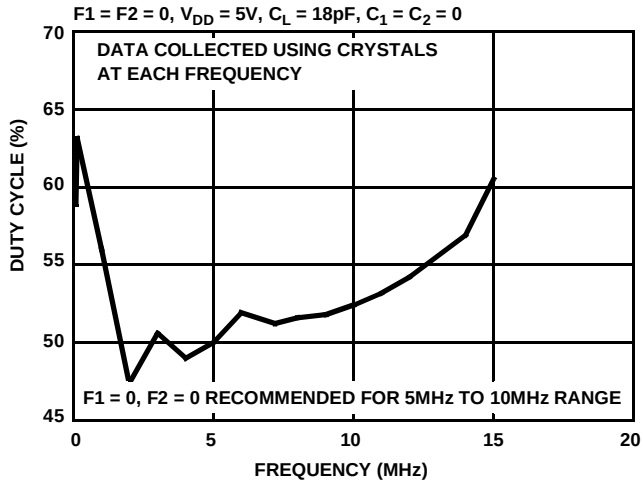


FIGURE 25. DUTY CYCLE vs FREQUENCY

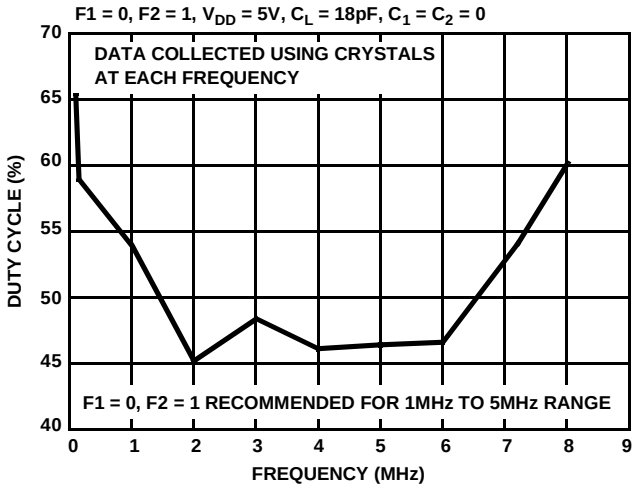


FIGURE 26. DUTY CYCLE vs FREQUENCY

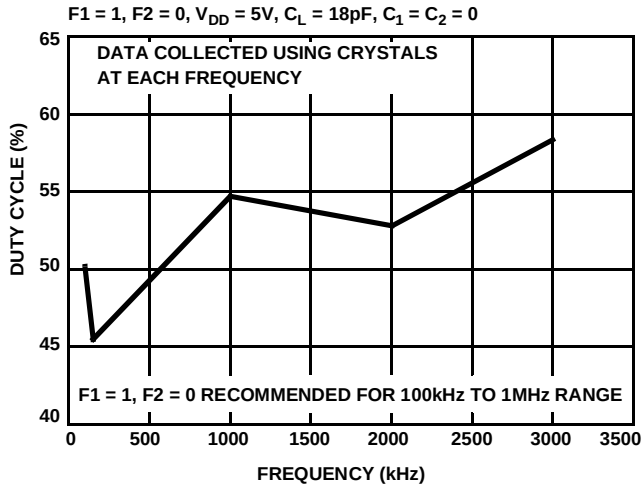


FIGURE 27. DUTY CYCLE vs FREQUENCY

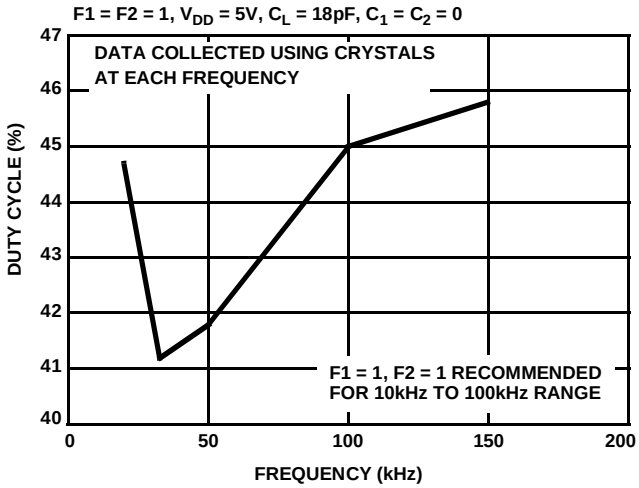


FIGURE 28. DUTY CYCLE vs FREQUENCY

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

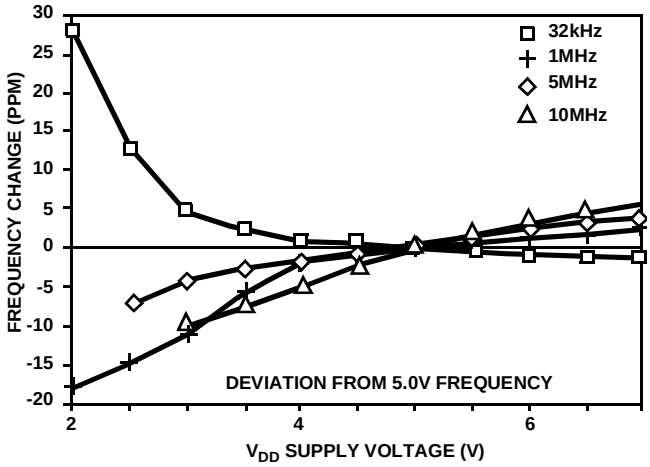


FIGURE 29. FREQUENCY CHANGE vs V_{DD}

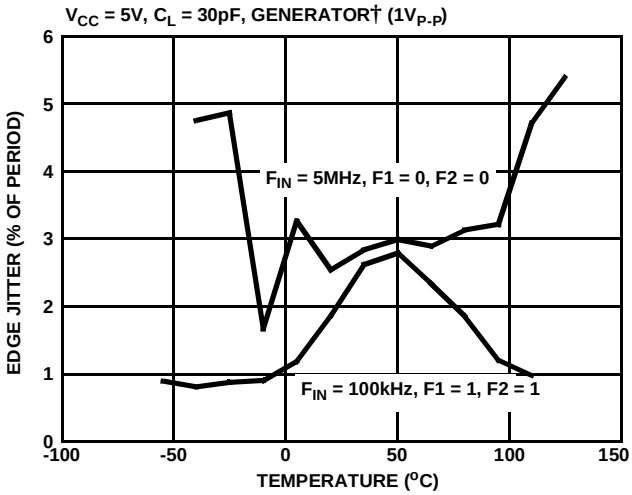


FIGURE 30. EDGE JITTER vs TEMPERATURE

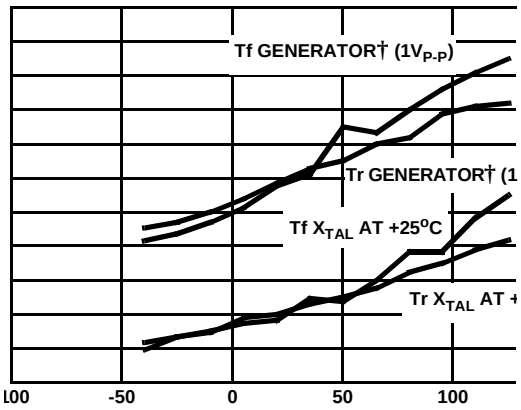


FIGURE 31. RISE/FALL TIME vs TEMPERATURE

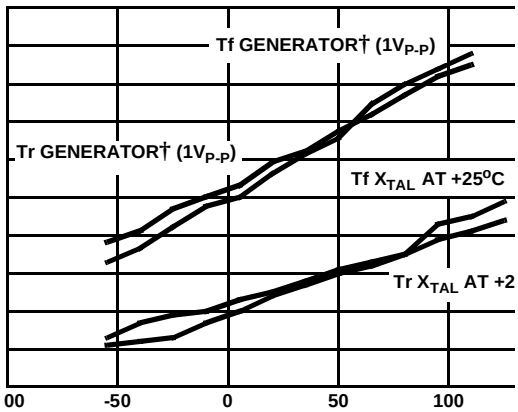


FIGURE 32. RISE/FALL TIME vs TEMPERATURE

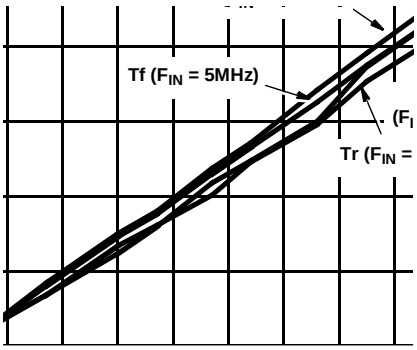


FIGURE 33. RISE/FALL TIME vs C_L

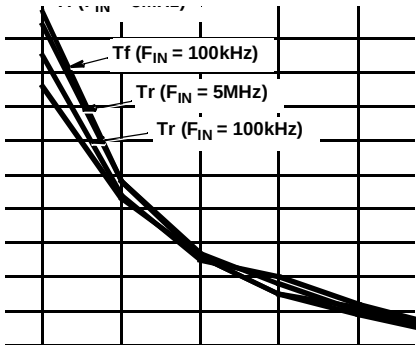


FIGURE 34. RISE/FALL TIME vs V_{CC}

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

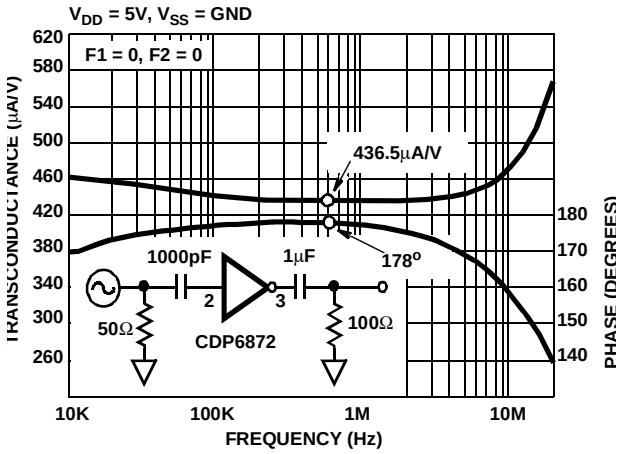


FIGURE 35. TRANSCONDUCTANCE vs FREQUENCY

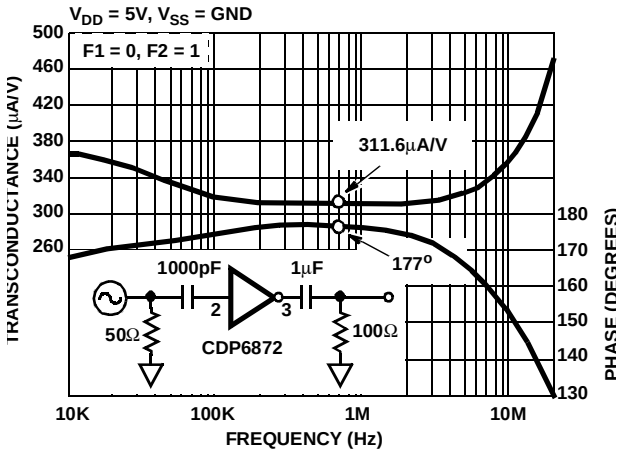


FIGURE 36. TRANSCONDUCTANCE vs FREQUENCY

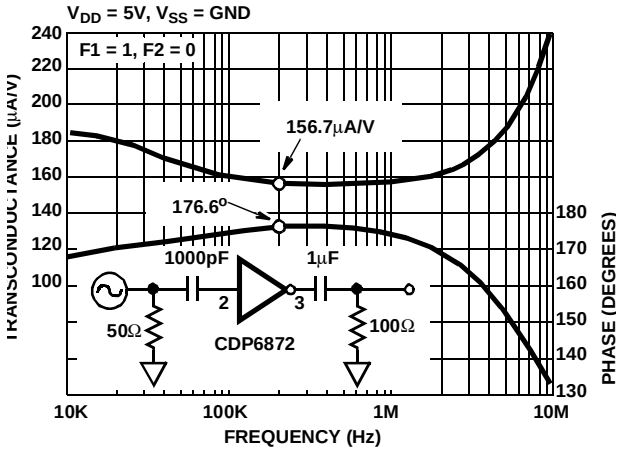


FIGURE 37. TRANSCONDUCTANCE vs FREQUENCY

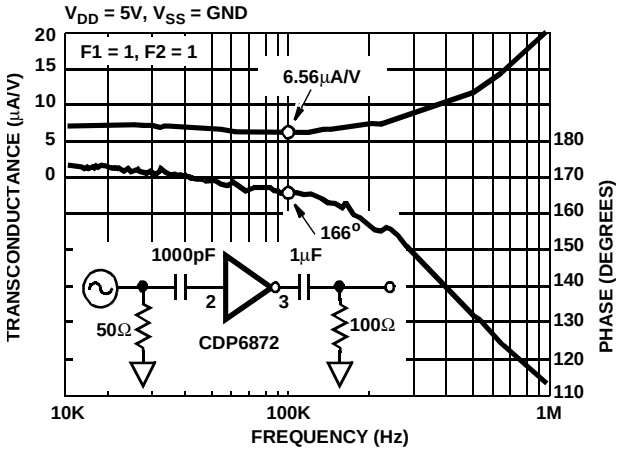


FIGURE 38. TRANSCONDUCTANCE vs FREQUENCY

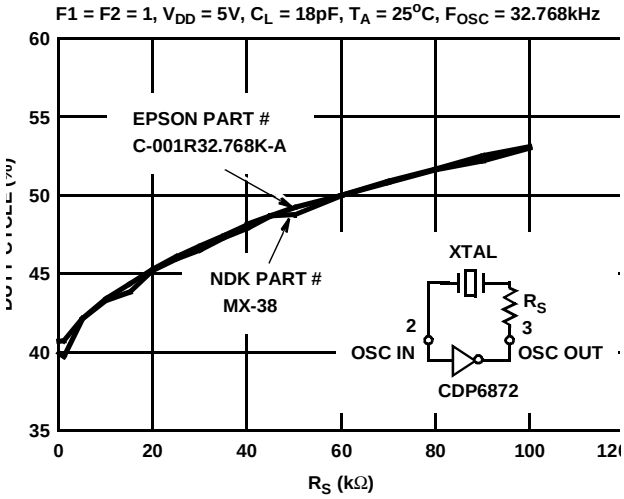
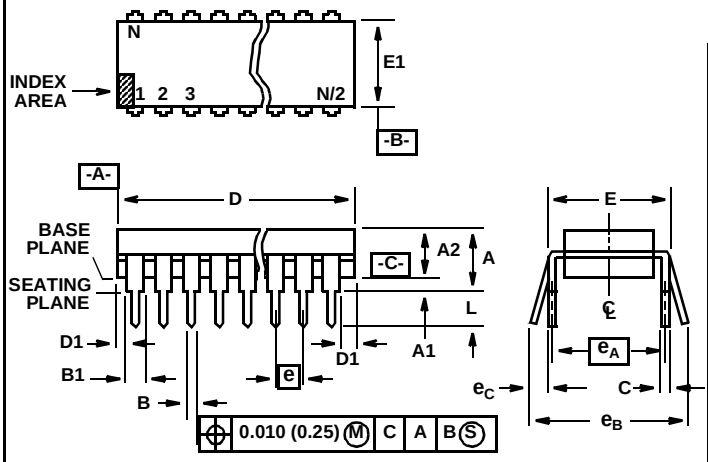


FIGURE 39. DUTY CYCLE vs R_S at 32kHz

NOTE: Figure 39 (Duty Cycle vs R_S at 32kHz) should only be used for 32kHz crystals. R_S may be used at other frequencies to adjust Duty Cycle but experimentation will be required to find an appropriate value. The R_S value will be proportional to the effective series resistance of the crystal being used.

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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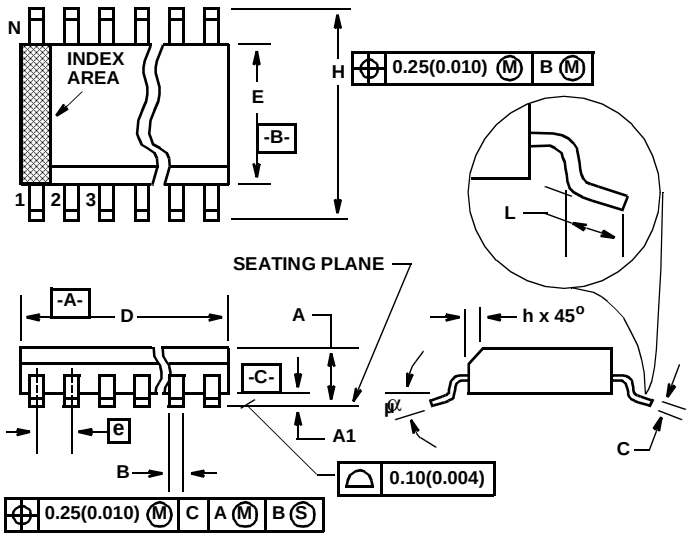
NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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