The CA1523 Variable Interval Pulse Regulator (VIPUR) For Switch Mode Power Supplies

Application Note | April 1994 | AN8614.1

The CA1523, Variable Interval, Pulse Interval Regulator (VIPUR) is a monolithic integrated circuit designed for use in switch mode power supply (SMPS) systems. The advantages of both pulse interval modulation (PIM) and pulse width modulation (PWM) are combined in the VIPUR circuit. Figure 1 shows the block diagram and external circuit used in a typical CA1523 switching regulator circuit.

The special features of the CA1523, including a slow-start controlled power-up and mode sensitive logic control of the output pulse, provide several advantages in power supply applications. Intrinsic controls for adjustment of the pulse and frequency modulation range allow easy use of the CA1523 in a variety of SMPS systems, but especially those where line isolation is required.

Systems that require line-isolated power supply voltages may be powered with the CA1523 regulator in a transformer flyback-converter system like the one shown in Figure 2(a). This system is particularly useful in meeting rigid safety standards when interfacing between workstation equipment or modular consumer audio and video instruments is required. Less stringent interface requirements may permit the use of regulators with a common ground for both the switching controller and power supply outputs; examples of these regulators are the flyback converter of Figure 2(B) or the buck converter regulator of Figure 2(C). However, the application of most interest is the line isolated type shown in Figure 2(A).

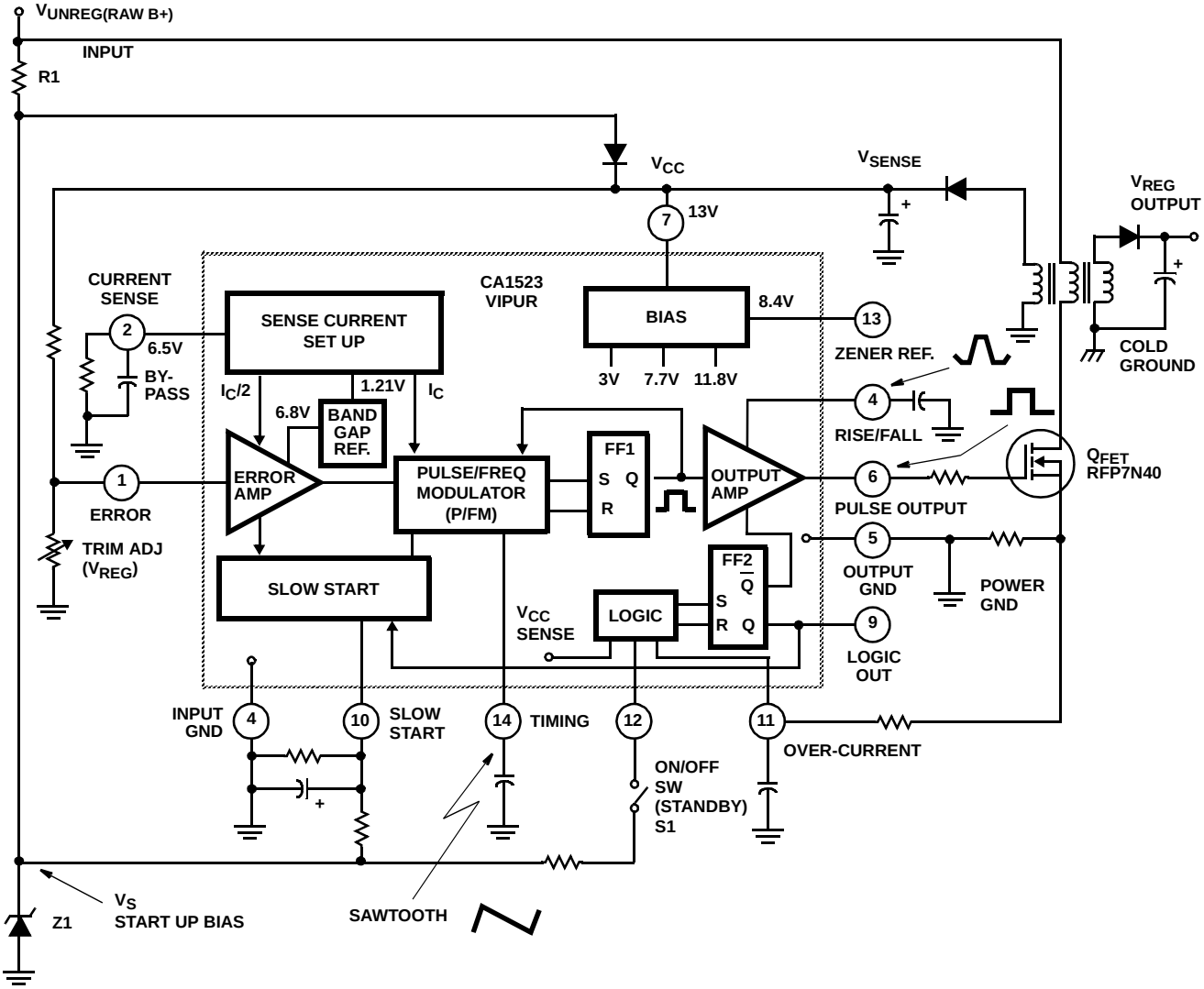

FIGURE 1. BLOCK DIAGRAM OF THE CA1523

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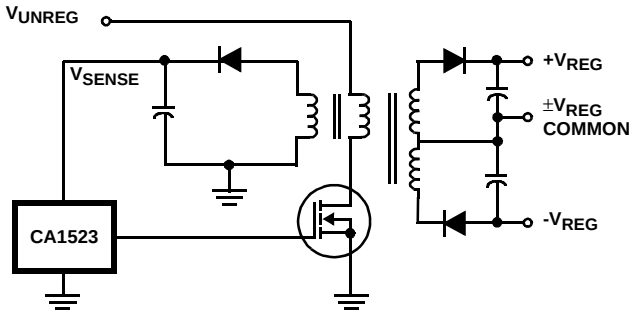


.FIGURE 2A. LINE ISOLATED FLYBACK CONVERTER

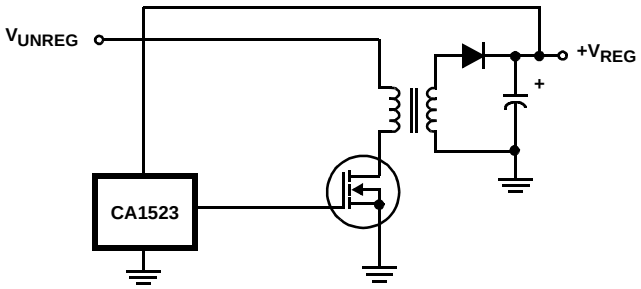


FIGURE 2B. NON-ISOLATED FLYBACK CONVERTER

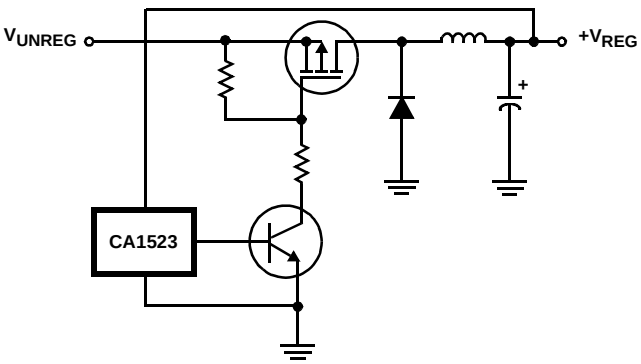


FIGURE 2C. BUCK CONVERTER REGULATOR

FIGURE 2. THE CA1523 IN SWITCH MODE POWER SUPPLY SYSTEMS

The PWM system is a popular mode of control in switching power supplies, as noted in the wide use of the CA1524. The counterpart of this mode of control, the PM system, was used extensively in the early period of switching power supply development. Both methods of control have their advantages and disadvantages. PWM offers effective control over a wide range of power supply loads. However, at the lower end of the load range, the PWM becomes limited because of the minimum pulse width, T_{ON}, required. In addition, the rise and fall time of the drive pulse of the power switching transistor must be slowed down to meet RFI and EMI requirements. On the other hand, the PIM can handle low loads better because the duty cycle is reduced by increasing the pulse interval. However, the low range of the operating frequency may cause filtering-related problems in audio or other sensitive instruments. Another problem with PIM at the low-frequency end is the related conversion losses.

The CA1523 is primarily a PIM controller with built-in PWM correction over a 2-to-1 pulse width range. For a frequency f and an associated period T, the pulse width reduces from a maximum width of T/2 (50% duty cycle), corresponding to the highest frequency at the maximum load limit, and approaches T/4 at the lowest frequency and minimum load.

The combination of both PIM and PWM control effectively compresses the operating frequency range over that of a pure PIM control for a given range of load. The combined CA1523 VIPUR advantages at minimum frequency include reduced losses and low ripple with improved efficiency and regulation. Pulse-width correction done simultaneously with pulse-interval correction produces an inherent gain magnitude of approximately 2 at 50% duty cycle under high-load conditions. This feature helps in keeping the error-amplifier gain low, and improves stability without the addition of expensive external components.

Features of the CA1523

As shown in Figure 1, the output drive pulse of the CA1523 is modulated and mode-controlled by several system features:

1. The output drive pulse has a maximum continuous ±50mA capability into an 1800pF load.
2. The peak transient load is +300mA and -200mA for a maximum of 1µs.
3. The maximum pulse width can be controlled by choice of the timing capacitance at pin 14 and the current-sense resistance at pin 2.
4. The output-pulse rise and fall time can be controlled by choice of the rise/fall-time capacitor at pin 4.
5. The slow-start threshold of the pulse output is controlled by choice of the resistance at pin 2.
6. The output-pulse interval is rate controlled during power-up by the slow-start RC-charge time constant at pin 10.
7. Maximum output frequency is in excess of 200kHz, and is user controlled.
8. Output pulse interval and width corrections are maintained by the error voltage feedback to pin 1.
9. The standby on/off switch between pins 7 (V_{CC}) and 12 controls the output pulse. As an option, the on/off function may be controlled by logic-level switching at pin 12 or by line-isolated switching using an optical coupler.
10. Overcurrent shutdown may be controlled by using a sense resistor in the load circuit to shut down the output drive pulse.

Other Features of the CA1523 Include:

1. A substantial level of ESD (electrostatic discharge) protection designed into the interfacing pin terminals of the chip.
2. An 8.4V internal zener voltage reference for the on-chip bias circuits.
3. A 1.21V bandgap that provides a stable voltage reference for bias to the timing circuit and error amplifier.
4. NOR logic control of shutdown of the output pulse under fault conditions for low V_{CC}, on/off, and overcurrent. Pin 9 is a monitor or output indicator of a fault condition.
5. Availability in an economical 14 pin DIP package.

Control Structure of the CA1523

The CA1523 has five primary circuit functions:

1. Error amplification
2. Pulse/frequency modulation
3. Pulse driver/output amplification
4. Slow-start power-up control
5. System logic control

The block diagram of Figure 1 shows the interrelated functions of the circuit. When the system raw B+ is switched on, the slow-start function controls the pulse/frequency modulator, P/FM, until the voltage at pin 10 is greater than 7V.

Standby conditions then exist until switch S1 is closed. In the standby mode, the P/FM maintains a maximum frequency output with a 50% duty cycle. After switch S1 is turned on, the output amplifier is enabled and the P/FM response is a function of the error voltage at pin 1. The error amplifier accepts error-correction inputs and controls the pulse and frequency modulation. The P/FM output pulse is then amplified in the driver and output stage.

Figure 3 shows the timing-circuit schematic of the CA1523. For a given timing capacitance, C_T, the maximum frequency of the P/FM circuit is determined by the current-sense bias at pin 2. The current-sense level, I_S, is set by the fixed resistor at pin 2, R_S, which goes to ground. A resistor divider reference at the base of Q92 of differential amplifier Q91, Q92, is approximately $V_{CC}/2$. The differential amplifier feeds back, via Q17C, any error in the balance of Q91 and Q92, while holding the pin 2 voltage at the $V_{CC}/2$ reference level. The differential emitter current is supplied by Q93, and is determined by the bandgap bias voltage of 1.21V at the base of Q93.

The differential emitter current is approximately equal to the collector current of Q17C; the collector currents of Q17A and Q17B are current mirrors to the collector current of Q17C. The currents $I_C/2$ and I_C provide the P/FM charge and discharge timing, and are, respectively, the collector currents of Q17A and Q17B. The current ratio is $^1/_2$-to-1 to accommodate a 50% duty cycle at maximum frequency and load conditions. When start-up conditions exist, and the pin 1 error voltage is low, Q6 passes all of the $I_C/2$ current to Q11. Since Q11 and Q18 are current mirrors, the collector of Q18 discharges the timing capacitor, C_T, at pin 14. The state of the flip-flop, FF1, determines whether Q15 will conduct current I_C from Q17B into the timing capacitor.

When Q18 is discharging current from C_T at an $I_C/2$ rate, and Q15 is charging C_T at an I_C rate, the net charge current is $I_C/2$. This is an FF1 high state for the Q output, and Q16 is cut off while Q15 is conducting current I_C. The positive voltage ramp at pin 14 increases until the V_H comparator toggles at the 5V reference to the inverting input, resetting FF1, with the Q output going low. When Q is low, Q15 is cut off, and no charge current passes to C_T. Timing capacitor C_T is then discharged by Q18 at a maximum rate of $I_C/2$. The discharge ramp continues until the voltage at pin 14 reaches 2.5V, when the V_L comparator toggles the S input of FF1 to a high state. The cycle of charge/discharge to timing capacitor C_T is complete when the Q output of FF1 goes high in response to the high at the S input.

The above operation occurs when the error voltage is lower than the 6.8V differential input reference, a condition that allows the full $I_C/2$ discharge of C_T by the Q11 and Q18 current mirror. After being turned on from the line power source, the slow-start function shunts Q6 collector current through Q2. As a result, the Q11,Q18 current mirror initially receives little or no forward bias current, and C_T cannot be discharged. As the slow-start voltage increases, the current in Q2 decreases, allowing Q11 and Q18 to discharge C_T at an increasing rate. As long as the error voltage at pin 1 remains below the 6.8V reference level, the charge and discharge rate is at the 50% duty cycle condition.

In reference to the slow-start circuit of Figure 3, an increase of the slow-start bias on capacitor C2 at start-up exercises a decreasing degree of control over the discharge timing. If the current-sense adjustment at pin 2 is typically less than 100µA, there will be a full frequency range of slow-start control, and the range of increasing pulse width will be 2 to 1. Higher pin 2 bias currents will reduce the range of frequency control. The input to pin 10 drives the base of p-n-p transistor Q34. A 30kΩ emitter resistor, R22, is returned from Q34 to an internal 7.7V bias source. Transistors Q1 and Q2 mirror the Q34 collector current and shunt the Q6 collector current away from Q11, reducing the discharge current in the timing control circuit. As an example, with 4V at pin 10, there are approximately 3V across emitter resistor R22. This arrangement allows the discharge current to be controlled over a range of 100µA. A bias resistor in the range of 56kΩ to 68kΩ between pin 2 and ground is suggested for a full range of slow-start control. Higher levels of pin 2 sense current increase the $I_C/2$ current beyond the full range of the slow-start bias control at pin 10.

When a power-on condition has been established, slow-start completed, and S1 switched on, the CA1523 begins normal regulation through error-voltage control as follows. When S1 is switched on, maximum energy conversion occurs in the switched transformer. The supply voltage approaches normal regulation level, and the error voltage increases toward the 6.8V reference level. The error voltage is set by a resistive divider ratio determined from the rectified voltage of the transformer sense winding. The Q5, Q6, Q7, and Q8 differential controls the Q6 current to the Q11, Q18 current

mirror, decreasing Q6 current as the error voltage increases. A portion of the $I_C/2$ current from Q17A is passed by Q6. This current controls the P/FM output pulse and maintains regulation at the desired level, as determined by adjustment of the divider at pin 1. Pulse output continues from FF1 during regulation, but at a reduced rate and with reduced pulse width. The Q output of FF1 is always high during the positive ramp at pin 14, a condition of maximum charge current to C_T. At minimum load, the pin 1 voltage increases, and the net charge current for the positive ramp is higher because Q18 is discharging less current. For example, if the error voltage at pin 1 is forcing half of the $I_C/2$ current to Q7, the Q6 current is $I_C/4$, and the net positive ramp charge current at pin 14 is:

$$I_C - I_C/4 = 3I_C/4$$

The net negative-ramp discharge current is then $I_C/4$. What had been a maximum charge and discharge rate of $I_C/2$ at start-up is now pulse-interval and pulse-width modulated to provide a 3 to 1 charge/discharge ratio.

To generalize, we can establish the range of error correction by assigning a k factor to the decimal portion of the Q17A collector current that is shifted from Q6 to Q7. Let k = 0 when V_1 (pin 1 voltage) is low and all Q17A current ($I_C/2$) flows through Q6 to discharge pin 14. k = 1 when all Q17A current is shifted to Q7 and there is no discharge current to pin 14. The maximum rate of charge and discharge is established by the sense current, I_S at pin 2; I_S is approximately $I_C/2$.

Since:

$$V = (1/C) \times \int idt$$

For a constant rate of charge (or discharge) current:

$$V_H - V_L = I_{CHARGE} \text{ (or } I_{DISCHARGE}) \times (T_2 - T_1)/C.$$

And:

$$T_{ON(MAX)} = (V_H - V_L)C_T/I_S.$$

From Figure 3, the range of $(V_H - V_L)$ is approximately (5.0 - 2.5), or 2.5V, and I_S is approximately equal to $V_{CC}/2$ divided by R_S.

The above information is used to establish the pulse interval or system frequency. The frequency is the reciprocal of T_{ON}(charge) plus T_{OFF}(discharge). As V_1 increases, k increases. The positive ramp charge current to pin 14 and C_T is:

$$I_{CHARGE} = I_C - (I_C/2)(1 - k) = 2I_S - I_S(1 - k) = I_S(1 + k).$$

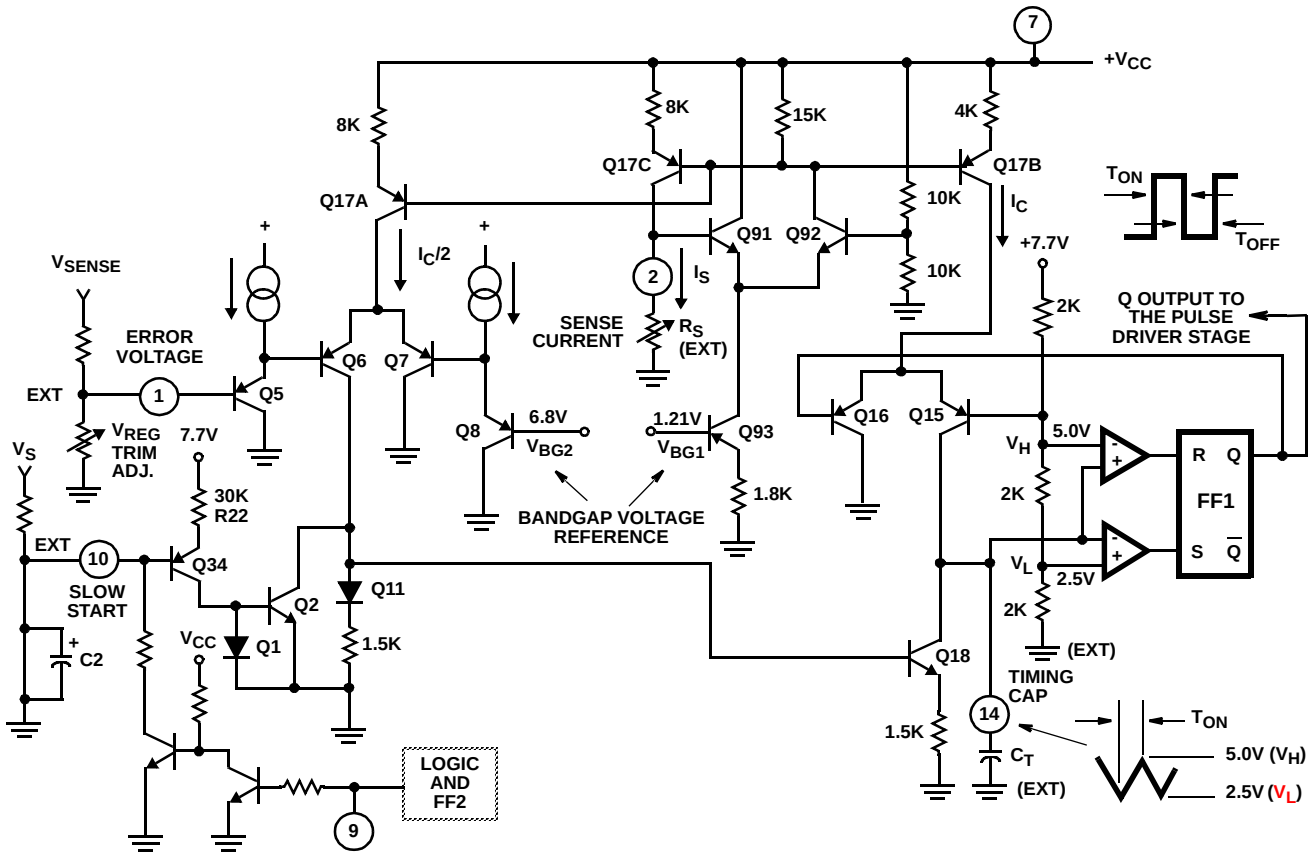


FIGURE 3. PULSE/FREQUENCY MODULATION AND TIMING CIRCUIT FOR THE CA1523

Since I_C is cut off during discharge:

$I_{DISCHARGE} = I_S(1 - k)$

Therefore, during charge:

$T_{ON} = [(V_H - V_L)C_T]/[I_S(1 + k)] = T_{ON}(max)/(1 + k)$

and, during discharge:

$T_{OFF} = [(V_H - V_L)C_T]/[I_S(1 - k)] = T_{ON}(max)/(1 - k)$

Note that T_{ON} approaches $T_{ON}(max)/2$ as k approaches 1. This is the condition of minimum power supply load. With the time conditions for T_{ON} and T_{OFF}, established, the frequency, f, can be defined as:

$f = 1/(T_{ON} + T_{OFF}) = (1 - k^2)/2T_{ON}(Max)$

Since the maximum frequency occurs at k = 0:

$f_{MAX} = 1/2T_{ON}(Max)$ and

$f = f_{MAX}(1 - k^2) = (1 - k^2)/2T_{ON}(Max)$.

The duty cycle is $T_{ON}/(T_{ON} + T_{OFF})$ which, by substitution, is:

$D = (1 - k)/2$

Since k is the current split ratio of the input differential amplifier, the differential equation applies, that is:

$k \cong 1/(1 + e^{\Delta V/h})$

where e is the natural log value of 2.718, h is KT/q (≅26mV), and ΔV is V_1-V_{REF}. The equation for k is approximate, but provides a reasonably accurate transfer function for the CA1523 when output pulse width, frequency, and duty cycle may be calculated for given values of (V_1 - V_{REF}).

As k goes to 1, the frequency goes to zero, implying a no-load condition on the power supply. This is an improbable condition; however, the lowest system frequency is always determined by the minimum power supply load.

The timing circuit of the VIPUR is a stand-alone pulse generator in which the Q output of FF1 is amplified by the driver output circuit of Figure 4, subject to the logic control of transistor Q33 and the proper logic-state control for the slow start (SST), ON, V_{CC}, and overcurrent (OC) inputs shown in Figure 5.

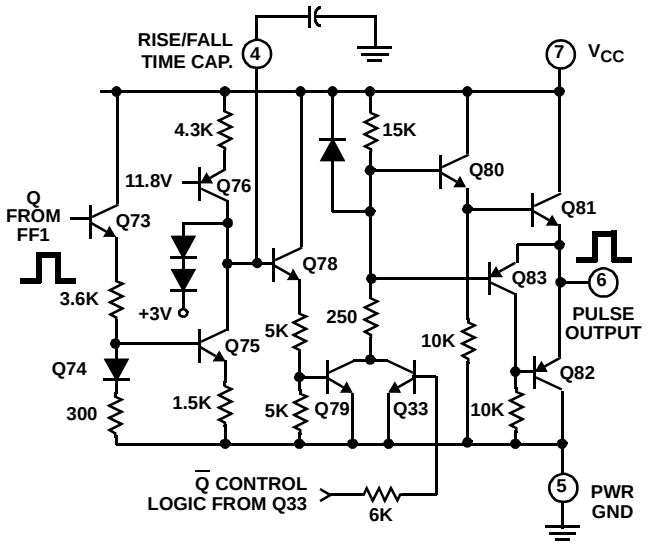


FIGURE 4. CA1523 DRIVER AND OUTPUT STAGE

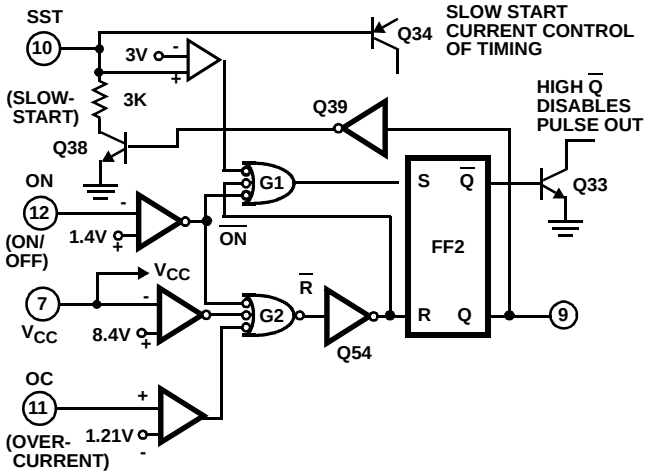


FIGURE 5. CA1523 LOGIC CONTROL DIAGRAM

The test circuit of Figure 6 demonstrates the pin 2 current sense (I_S) range using timing capacitance values of 100pF, 240pF, and 470pF. Figure 7 shows the frequency versus I_S current at pin 2. Figures 8 and 9 show the range of pin 6 pulse width and duty cycle. Since the curves of Figures 7, 8, and 9 were determined with V_1 at approximately 5.9V (much less than the 6.8V reference) maximum frequency conditions apply to all Figure 6 curves. With the rise/fall-time capacitance of 68pF at pin 4, the rise/fall delay will affect the duty cycle when the frequency is greater than 120kHz. Removing the pin 4 capacitance will extend the maximum frequency to well above 200kHz. However, use of the rise/fall-time delay function is important to the control of EMI and RFI. The optimum rise/fall capacitance value is chosen to assure a 50% duty cycle at the maximum frequency with a reasonable margin in design tolerance and, for the system requirements, to ensure compliance with EMI and RFI requirements.

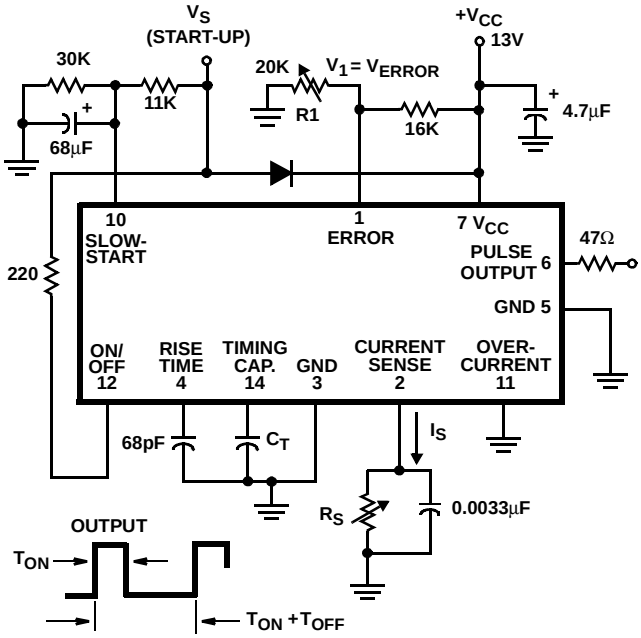


FIGURE 6. VARIABLE-INTERVAL SWITCHING-REGULATOR TEST CIRCUIT USED TO OBTAIN TIMING CURVES OF FIGURES 7, 8, AND 9

Where there are no external system restrictions on the operation of the CA1523, and the function is that of a pulse generator, very large values of capacitance may be used at pin 14 to achieve very low pulse frequencies. External resistor loading at pin 14 will contribute a nonlinear slope to the otherwise linear sawtooth there. This nonlinear contribution can also be noted in the waveform at pin 14 if the timing capacitor has less than 10MΩ leakage. Very low values of I_S are not recommended because the balance of charge and discharge currents is, to some degree, affected by base bias and junction leakage currents. As noted by the degradation of duty cycle balance in Figure 9, and for practical reasons, I_S should be greater than 20µA. The upper limit for I_S is determined by the maximum available collector current from Q17C, which is typically 350µA.

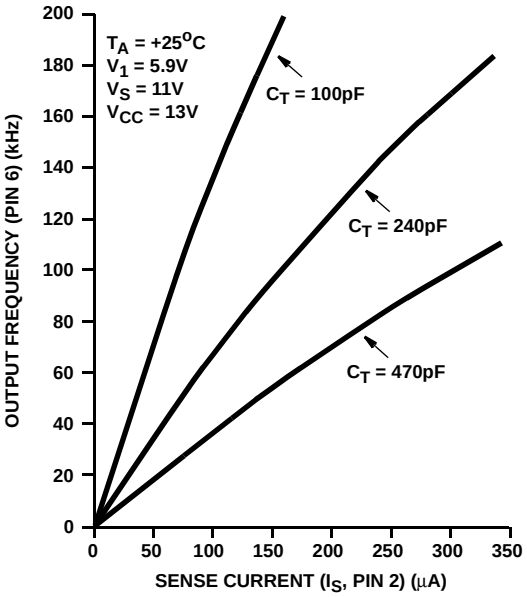


FIGURE 7. PULSE/FREQUENCY MODULATOR CHARACTERISTIC OF FREQUENCY vs. TIMING CAPACITOR C_T AND SENSE CURRENT I_S (T_A = +25°C, V_1 = 5.9V, V_5 = 11V, V_{CC} = 13V.)

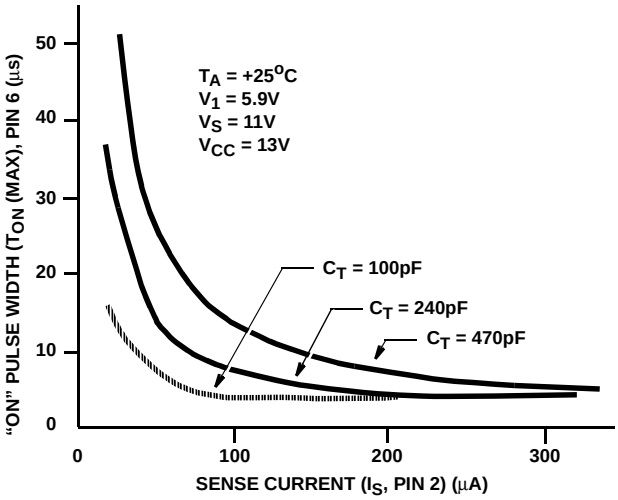


FIGURE 8. PULSE/FREQUENCY MODULATOR CHARACTERISTIC T_{ON}(MAX) OUTPUT PULSE WIDTH (PIN 6) vs. CURRENT SENSE (PIN 2). (T_A = 25°C, V_1 = 5.9V, V_5 = 11V, V_{CC} = 13V.)

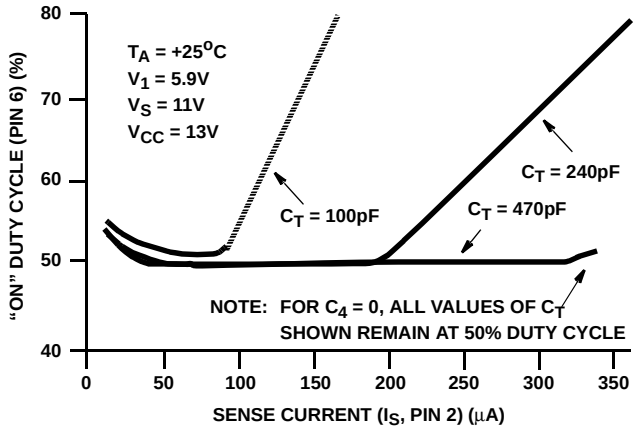


FIGURE 9. PULSE/FREQUENCY MODULATOR CHARACTERISTIC "ON" DUTY CYCLE (PIN 6) vs. CURRENT SENSE (PIN 2).

CA1523 Generated Waveforms And Delays

The signal waveforms of the CA1523 are shown in Figure 10, and are based on the test circuit of Figure 6, where R_S is adjusted for a maximum frequency of 100kHz. Because the sink and source current drivers of the timing capacitor, C_T, are constant current generators, the waveform at pin 14 is a very linear sawtooth. As noted in Figure 4, the waveform at pin 4 is derived from the Q75 sink and Q76 source drive currents, but is normally clipped at the top and bottom. The positive tip of the pin 4 signal is set by a positive clamp from two series diodes to an internal 3V bias source, providing a clamp level of approximately 4.5V. The bottom, or negative, truncation is the result of a current sink depletion of the charge on the rise/fall-time capacitor at pin 4. The degree of waveform clipping is determined by the maximum operating frequency and the value of the rise/fall time capacitor at pin 4.

In Figure 4, the rise, delay, and fall times of the input drive signal, Q, are controlled by the capacitance at pin 4, amplified, and output at pin 6. The Q input, a square wave output pulse from the timing generator (Figure 3), drives the rise/fall capacitor via the Q73 buffer and the Q74, Q75 current mirror. Rise time is determined by the Q76 constant current source. As such, the sink and source currents control the voltage at pin 4. Capacitance loading at pin 4 provides a controlled rise and fall delay time. With the 68pF capacitance shown in Figure 6, plus 10.5pF probe capacitance, the waveforms are as shown in Figure 10. A rise-time delay of 1.6µs is noted at the 2.1V point on the pin 4 waveform. The signal at pin 4 drives the base of Q78 and, through a resistor divider, Q79. Approximately 2.1V is required at pin 4 to switch Q79 and set the delay, which can be calculated from the rise time equation for constant currents. The source current from Q76 is approximately 100µA, and the delay, T_D, is:

$$T_D = VC/I = [(2.1V)(68 + 10.5pF)]/(100\mu A) = 1.6\mu s$$

If the rise time capacitor at pin 4 is too large, the peak voltage will be reduced below the positive clamp level. This condition will cause the on-time duty cycle at pin 6 to be increased. The rise time capacitor at pin 4 must be adjusted

to restore the duty cycle to 50% at the maximum frequency condition. When no external capacitor is used at pin 4, maximum operating frequencies in excess of 300kHz are possible. An example of the typical CA1523 pulse output capability at high frequency conditions is provided below.

Using the circuit conditions of Figure 6 with no pin 4 capacitor, I_S = 160µA, and C_T = 50pF, the pin 6 output pulse is:

$$t_R = 250ns$$

$$f_{(MAX)} = 312kHz$$

$$T_{0N}(Max) = 1.6\mu s$$

$$T_{0N}(Min) = 0.8\mu s$$

Additional delay in the pin 6 output drive pulse may result from the conditions of loading. The normal specifications for the CA1523 are given for a 68pF rise/fall-time capacitance at pin 4 and an 1800pF output capacitance loading to reflect typical drive requirements for a power-FET switch transistor. The rise and fall times for 1.8V and 10V thresholds at the V6 output are typically t_R = 600ns and t_F = 200ns.

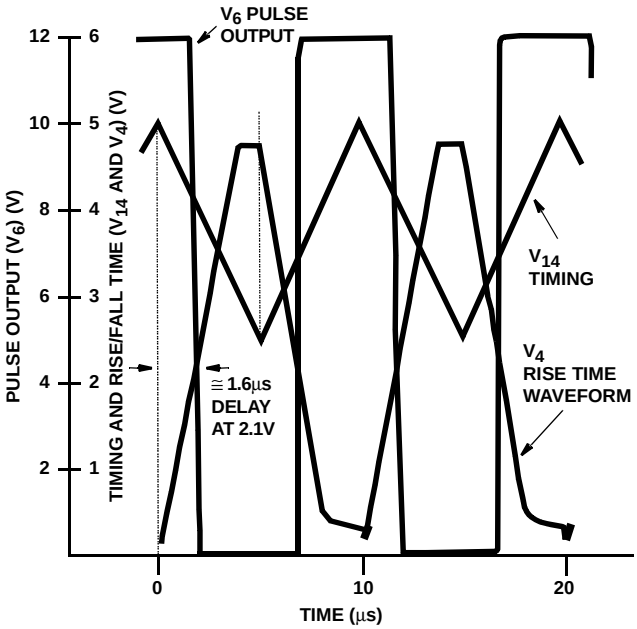


FIGURE 10. SIGNAL WAVEFORMS OF THE CIRCUIT OF FIGURE 4 (WITH 10.5pF TEST-PROBE LOADING). (C_T = 240pF, R_S APPROXIMATELY 39kΩ, $F_{(MAX)}$ = 200kHz.)

Application Circuits

TV Monitor Flyback Converter

Figure 11 shows a typical television receiver application of the CA1523. Line isolation permits use of the TV receiver as an RGB or composite-video DC-coupled monitor. In this system, the switching transformer isolates the power line from the signal circuits of the TV receiver. As shown in the block diagram of Figure 11, $120V_{AC}$ is connected through a fuse to the bridge rectifier and a step-down transformer, T2. The rectified output of the step-down transformer is used as a 16V standby power supply for the TV control module. The control module, in response to the user input control, switches Q2 on and off to control turn-on of the VIPUR regulator through the optoisolator. The bridge rectifier supplies a +150V raw B+ to the VIPUR start-up circuit and to the primary of the switching transformer, T1. After start-up, the run supply provides a regulated $+V_{CC}$ for the CA1523 from the sense feedback circuit. In normal regulation, the VIPUR drives the Q1 power MOSFET, which switches the primary of T1. T1 converts regulated power to the cold 20V, 25V, and 150V levels required for the power supply outputs and the run-supply circuit.

Figure 12 explains the on/off operation of the switching power-supply portion of the converter application. The logic function maintains control of the on/off operation of the system. In the off state, the system remains in a standby mode as long as the $120V_{AC}$ is connected. Standby power is supplied via the start-up circuit, which consists of R2 and the 11V zener diode CR3. Continuous start-up bias is supplied to the $+V_{CC}$ function at pin 7, the on/off input at pin 12 via the optoisolator, and the slow-start circuit at pin 10. The 11V source is connected to the pin 7 $+V_{CC}$ function via the forward biased diode, CR13. The logic function inputs (as previously noted in Figure 5) are the B+ sense from pin 7, the slow-start function at pin 10, the on/off function at pin 12, and the overcurrent function at pin 11. The logic function responds to a voltage level for each input and, if the voltage range of a required input is not met, shuts down the output amplifier, so that no pulses appear at pin 6. After start-up, normal operation is resumed when the on/off input is greater than 2.5V, the peak overcurrent input is less than 1.2V, and the B+ sense has determined that $+V_{CC}$ is greater than 8.4V. The slow-start function controls the gradual start-up of the pulse and frequency modulation functions such that a slow RC rise time at pin 10 is synonymous with a slow decrease of the pulse interval. As the pin 10 voltage increases, the slow-start allows a gradual increase of the $I_C/2$ discharge current. As the voltage at pin 10 increases from 3V to 7V, the full range of slow-start control over the P/FM changes from zero to maximum frequency. The RC time constant consisting of R1, C7, and R3 controls the slow-rise voltage at pin 10. The slow increase controls the power-up rate and limits the start-up dissipation in power MOSFET Q1.

The on/off function could be controlled by an insulated manual switch or a relay. However, the optoisolator has the advantage in that it can be remotely controlled with low standby power. The overcurrent shutdown voltage is sampled from the source terminal of the power MOSFET, Q1, to assure that peak currents in the transformer primary circuit will be fault-mode limited. When start-up is complete, the run B+ is greater than the start-up supply voltage from the 11V zener diode, and CR13 is reverse biased. The on/off and slow-start input circuits remain under the control of the 11V start-up source, but the VIPUR power supply is transferred to the well-regulated run B+ supply derived from the sense winding of the transformer.

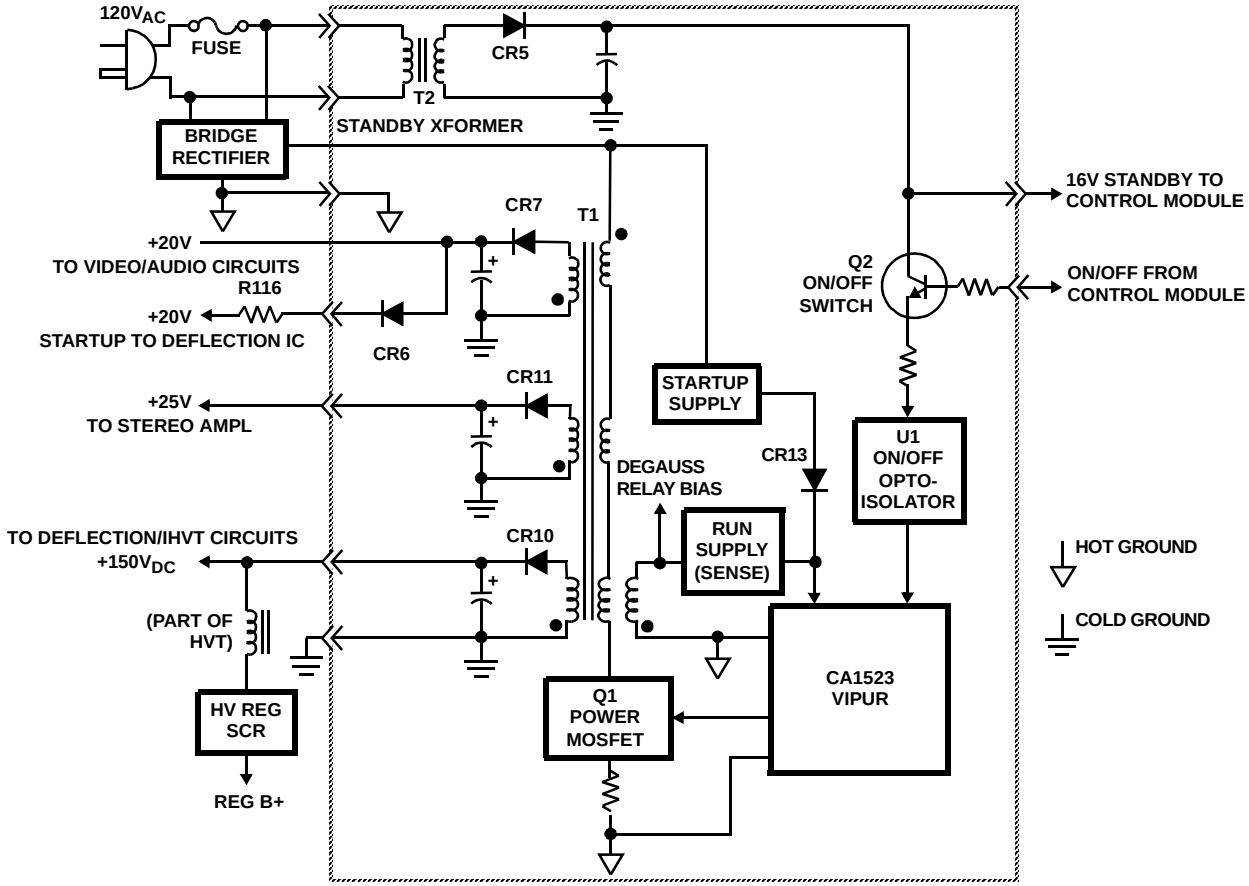


FIGURE 11. GENERAL TV MONITOR APPLICATION OF THE CA1523

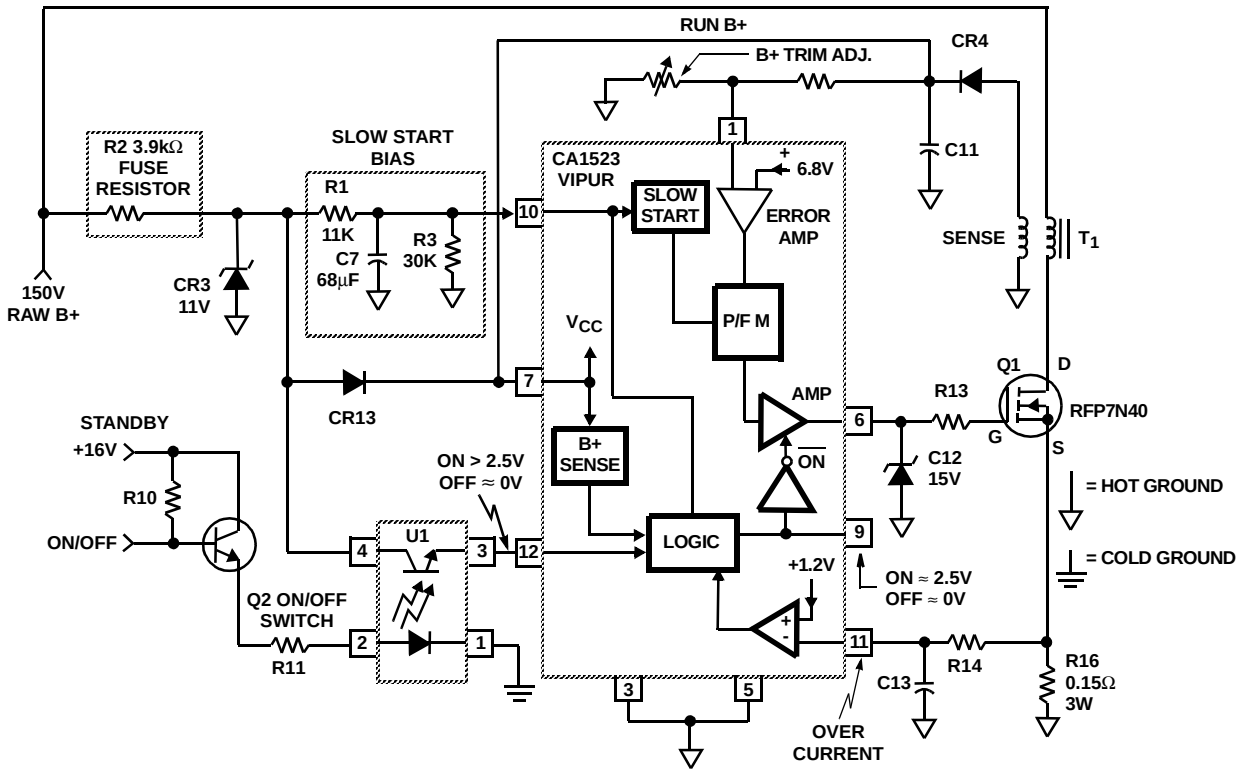


Figure 13 shows the VIPUR switching-regulator output operation as it functions in a normal feedback mode. As explained above, the error amplifier at pin 1 is differentially compared to a 6.8V internal reference. The error amplifier supplies the correction signal for the P/FM. Pulse and frequency modulation is controlled by timing-capacitor C15 and sense-current resistor R9. The output amplifier is controlled by the logic input; its rise time is controlled by capacitor C14. Zener-diode CR12 and resistor R13 are used to protect the gate of power MOSFET Q1. As Q1 switches the raw B+ current through the primary of the ferrite transformer, T1, power is supplied to the output windings and the sense winding. The pulse in the sense winding is rectified, and supplies run power to the CA1523 and error feedback to pin 1 through the resistor divider. The ratio of resistor R8 to the parallel trim resistors R4, R5, R6 and R7 sets the output voltage of the CA1523. The required output voltage of the regulator is determined by clipping resistors from the PC board.

A limited-range potentiometer adjustment may be used to control the regulator output, but this approach can be potentially dangerous if the high voltage of the CRT is not limited in some way. The fixed resistor-divider network is preferred for safety reasons. Because of the tight coupling of the transformer windings, the sense winding reflects the input-voltage changes and output-loading conditions. The preferred run B+ is 12V to 13V. The product of the resistor-divider ratio and the run B+ voltage should be, typically, 6.8V. When working with direct AC line power supplies, an isolation transformer must be used for hot AC line protection. Figure 14 joins together the circuits referenced in Figures 11, 12, and 13. The parts of the circuit connected to the “hot” line are identified at the center of the schematic. In addition to the circuitry discussed above, Figure 14 shows various chokes, bypass capacitors, and ferrite beads used in conjunction with the diode-rectifier filtering. These components are normally required to improve filtering and to reduce EMI and RFI.

CA1523 Buck Converter Switching Regulator

Figure 15 is the circuit schematic of a buck-type regulator useful in lower-voltage applications with a nominal raw B+ of 28V and an input tolerance range of 18V to 38V. This circuit has been chosen to illustrate some of the special capabilities of the VIPUR circuit; but, for the most part, these features are applicable to any other circuit controlled by the CA1523. The circuit of Figure 15 has special start-up features that minimize standby current in zener diode Z1 and make use of the internal zener diode for slow-start control. As shown, the error feedback voltage has been made adjustable over a typical range of 6.8V to 13.5V. The pulse frequency range is typically 25kHz to 75kHz, and the regulation at a nominal 12V output is typically 0.3%.

This circuit normally requires an output transformer only when it is desirable to isolate the output from the input. The pulse output of the CA1523 is inverted in a 2N2102 and used to drive an RFP8P10 p-channel enhancement mode power FET. The power FET is driven by the 2N2102 through a resistive divider that limits the maximum source-to-gate voltage. In the drain circuit of the power-FET output there is a shunt RUR-820 fast-switching catch diode followed by a filtering circuit comprising a 0.5mH choke and a 470µF capacitor.

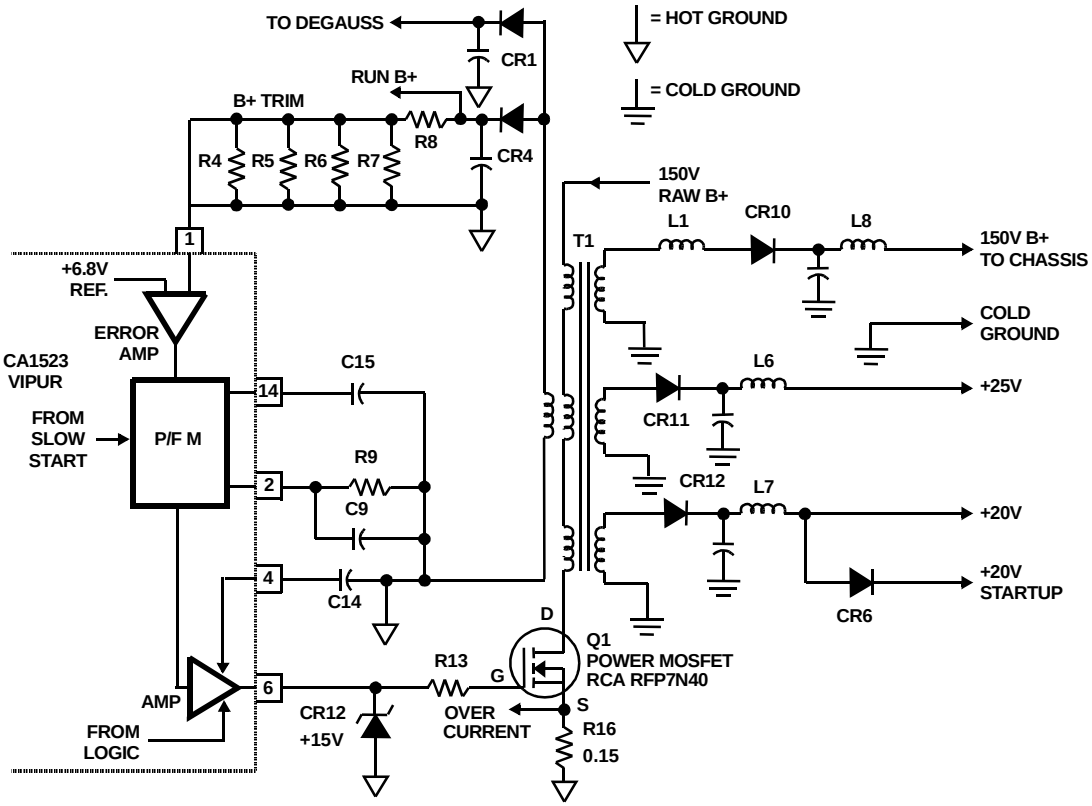
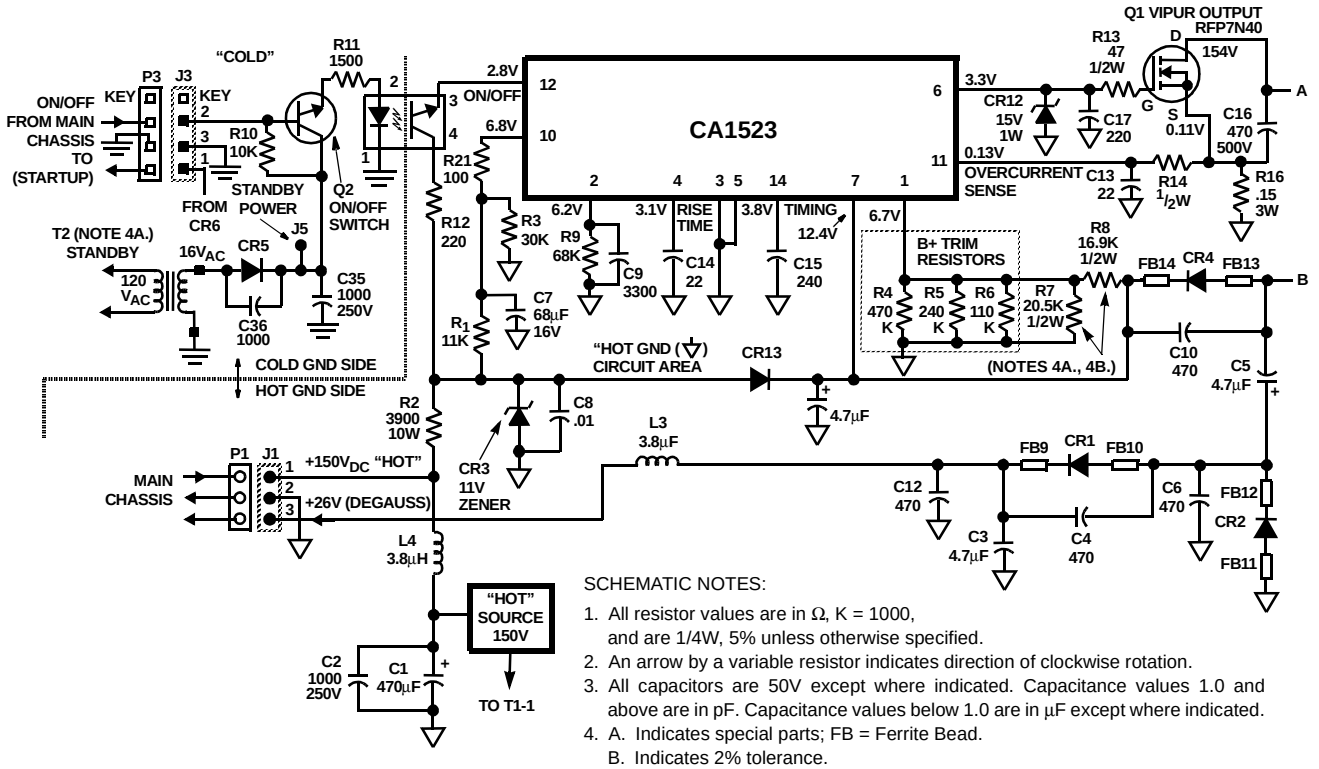


FIGURE 13. SWITCHING REGULATOR OUTPUT OPERATION



SCHEMATIC NOTES:

1. All resistor values are in Ω, K = 1000, and are 1/4W, 5% unless otherwise specified.
2. An arrow by a variable resistor indicates direction of clockwise rotation.
3. All capacitors are 50V except where indicated. Capacitance values 1.0 and above are in pF. Capacitance values below 1.0 are in µF except where indicated.
4. A. Indicates special parts; FB = Ferrite Bead.
   B. Indicates 2% tolerance.
   C. Indicates 1% tolerance.
5. ⏚ Cold chassis ground. ⏚ "Hot" ground.

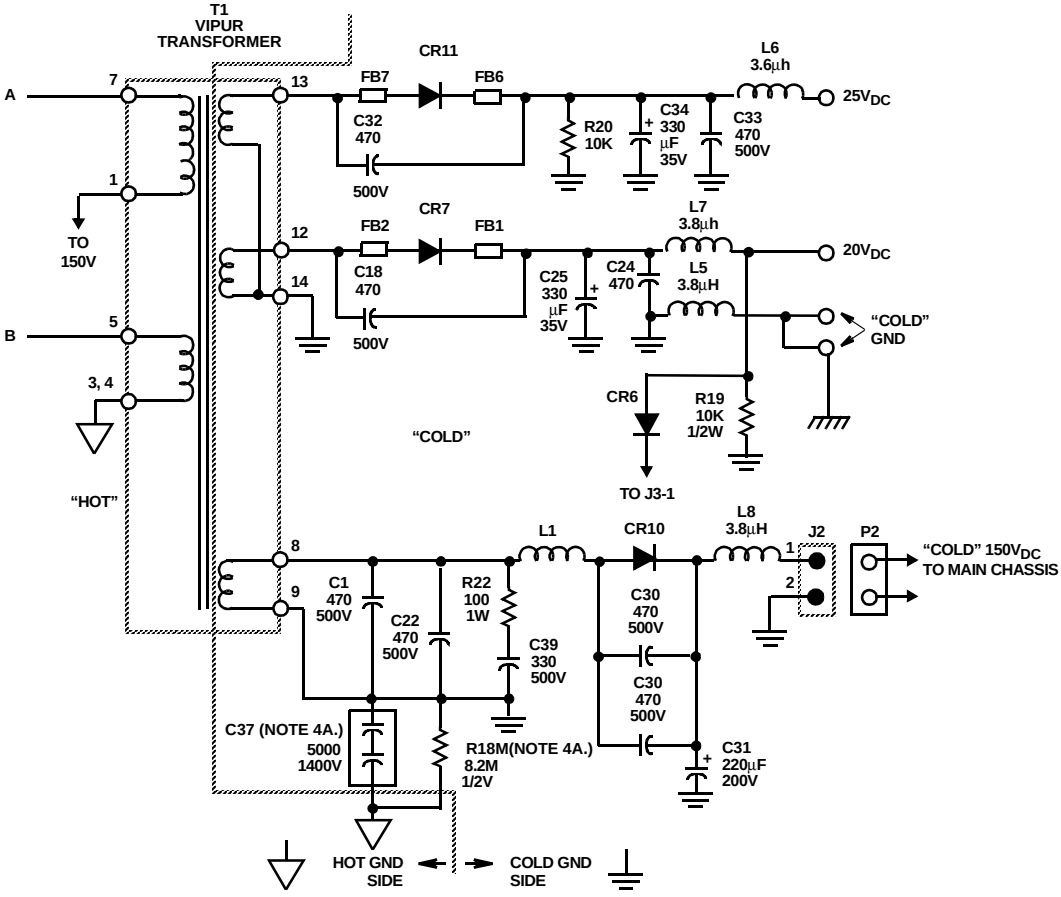


FIGURE 14. APPLICATION OF THE CA1523 VIPUR IN RCA CTC-130 TELEVISION CHASSIS POWER SUPPLY MODULE

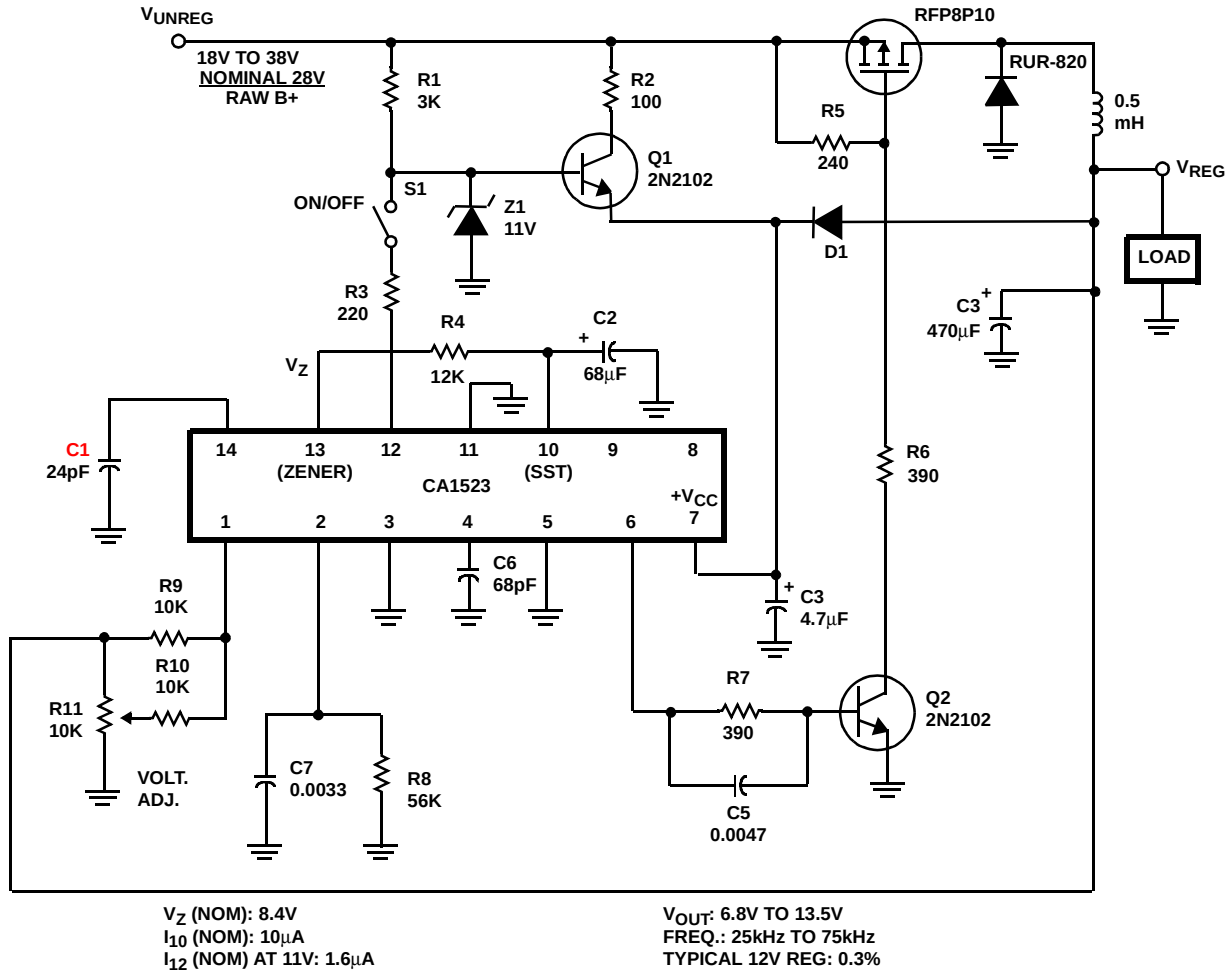


FIGURE 15. BUCK REGULATOR FEATURING ADJUSTABLE OUTPUT VOLTAGE AND SLOW START USING CA1523 ZENER

The raw B+ input may be a 28V battery source or the filtered output of a bridge rectifier supplied from a line isolated step-down transformer. The start-up components are substantially different from those shown in the transformer-isolated fly-back-converter circuit, although, as noted, the start-up circuit shown here may be applied in either system. If the output voltage range of the regulator is chosen, as it is typically, to be 11V to 13V, transistor Q1 conducts only for a brief period after S1 is closed. The run B+ is supplied through diode D1 to $+V_{CC}$ at pin 7, and the emitter of Q1 is reverse biased after the power-up cycle is complete. This situation substantially reduces the continuous running dissipation of zener Z1 and resistor R1.

Even when the V_{REG} voltage is less than the zener voltage level, the base current to Q1 is a fraction of a milliampere in a normal run mode. However, more base current is required to charge C4 at line turn on. After start-up is complete and the standby on/off switch is closed, approximately 1.6mA of current is supplied to pin 12. Typically, less than 2mA are needed to sustain idle current to zener Z1. The difference in these losses for the circuit conditions shown in Figure 15 versus those shown in Figure 14 is approximately 2mA versus 35mA. A number of bias options are available for implementing the error-voltage feedback; most of the options are adaptable to either the buck regulator or the transformer flyback-converter system. Either system must feed back a sense return voltage of approximately 6.8V to pin 1. It is not required that the CA1523 be powered by the sense return voltage, but if it is, the voltage should be approximately 11V to 13V. The CA1523 will operate over a supply-voltage range of 9.5V to 15V.

The buck regulator circuit of Figure 15 shows an output voltage adjustment range ratio of 2 to 1. The adjustment range is from the typical 6.8V error-reference level to 2 times the error-reference level. If diode D1 is removed and Q1 used with zener Z1 to supply the run B+ for regulated $+V_{CC}$, higher levels of output can be set by reducing the divider ratio, R10 (R9 + R10). With a ratio of 3 to 1, the typical output voltage will be 3 times 6.8V or 20.4V. Of course, under this condition, the V_{UNREG} input voltage must be higher than 20.4V by the amount of the saturated voltage drop in the power FET. If the error input to pin 1 is directly connected to the V_{REG} output, the typical output voltage is 6.8V. V_{REG} output voltage levels less than 6.8V cause two concerns. First, the return resistor divider that sets the output voltage level must be referenced to a positive voltage greater than 6.8V. Although a concern, this condition is feasible. The second concern, that of using the 11V zener supply, is more serious. When the Z1 reference is used, a power-down condition may allow the V_{REG} output

voltage to increase when zener voltage collapses. When that happens, pin 1 voltage will decrease and the error voltage will increase the pulse output drive, increasing V_{REG}. A proper choice of components can avoid the turn off output voltage peaking problem when the raw B+ collapses, and even extend the low voltage regulation range.

The circuit of Figure 16 shows the use of the internal zener diode at pin 13 as a reference for the return divider from the output V_{REG} voltage source. An optional adjustment method using the start-up zener, Z_1, is also shown. For the circuit of Figure 16, the range of this adjustment is 2V to 13V.

Using the CA1523 as a VCO Pulse Generator and Driver

The uses of the CA1523 VIPUR discussed above are application specific to a switch-mode controller for power supplies. Figure 17 shows the CA1523 as a general-purpose V_{CO} pulse generator and driver circuit with a minimum of external components. The V_{CO} control input is at the base of the external transistor Q1, which provides a linear current drive to the current sense, pin 2. For a given timing capacitance at pin 14, a 50% duty cycle pulse frequency at pin 6 is controlled by the pin 2 current. The frequency is linear, with the V_{CO} input to Q1. The pin 1 error voltage is biased low, but may be gated to provide synchronous burst control of the V_{CO} output. Some of the typical characteristics and features of this circuit are listed in Table 1. The drive capability of the pulse output from pin 6 has been noted to be as much as +50mA continuous for an 1800pF load. The internal zener bias and bandgap reference sources keep the frequency output very stable over a power-supply range of 10V to 15V.

TABLE 1. TYPICAL CHARACTERISTICS AND FEATURES OF VCO PULSE GENERATOR AND DRIVER CIRCUIT

CHARACTERISTIC	VALUE
V_{CC}	12V
V_{CC} Range	10V to 15V
I_{CC}	23mA
V_{CO} Input Range	1V to 4V
V_{CO} Sensitivity	53.3kHz/V
$f_{(MAX)}$	200kHz (for C14 = 240pF)
$f_{(MAX)}$	500kHz (C14 = Stray Capacitance)
V_O Output	11V
t_R	300ns (0V to 8V)
t_F	100ns (11V to 2V)

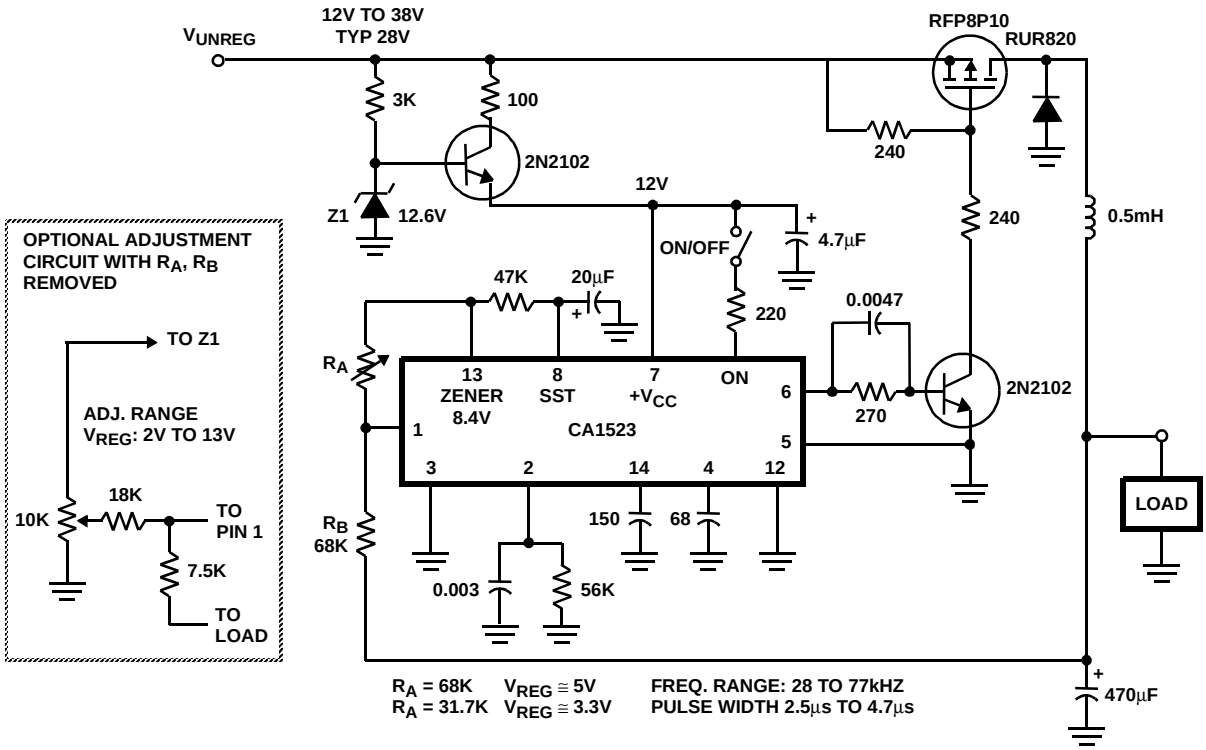


FIGURE 16. LOW VOLTAGE SUPPLY VARIATION IN THE BUCK CONVERTER CIRCUIT

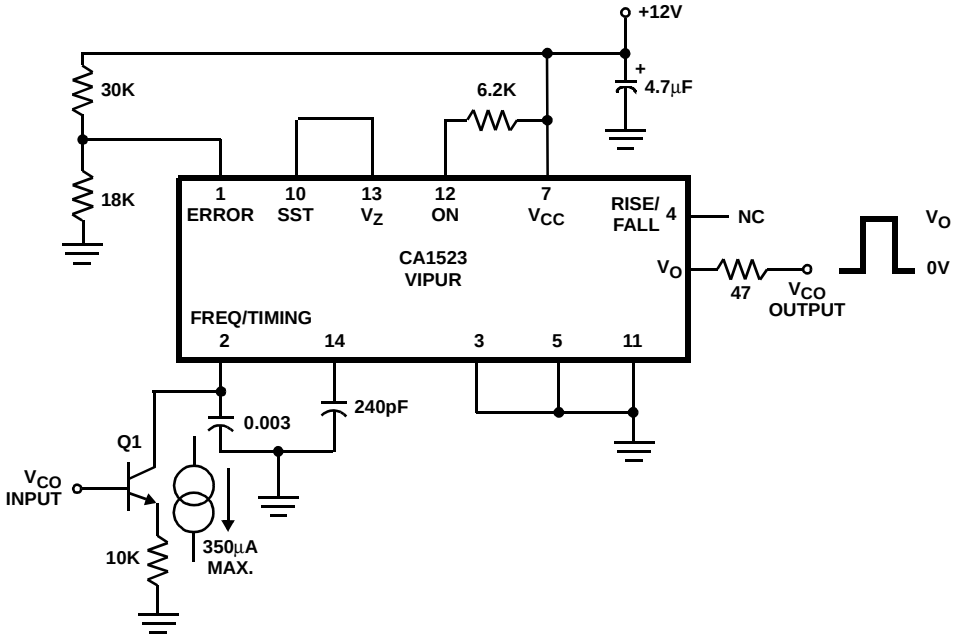


FIGURE 17. V_{CO} PULSE GENERATOR AND DRIVER CIRCUIT

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