SH7490

DAB Digital Baseband Decoder

ADE-202-077A

Rev. 1.0
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Overview

The SH7490 is a digital audio broadcasting (DAB) digital baseband decoder providing a low cost, highly integrated solution for consumer DAB receivers, according to the ETS 300 401 standard [1].

It offers a flexible design approach for both audio and multimedia applications.

Features

- Complete COFDM demodulator supporting single or dual sub-channel demodulation
- Supports DAB transmission modes I, II, III, and IV with automatic detection of mode
- Internal digital AFC to simplify RF tuner design
- On chip carrier, and symbol synchronisation and tracking
- Extended acquisition range to shorten receiver scanning time in search mode
- Disturbance-free operation during multiplex sub-channel re-configuration
- On chip MPEG audio decoding supports both 48kHz and 24 kHz audio sampling frequency
- On chip digital volume, and dynamic range control (DRC) for audio output data
- Controlled using a serial controller interface protocol (CIP)
- Easy extraction of transmitter identification information (TII), fast information channel (FIC), and programme associated data (PAD) using CIP commands
- Parallel port for easy connection to PC or host microcontroller
- Receiver data interface (RDI) based on IEC 958 physical interface, high capacity mode
- 176-pin plastic LQFP package
- Wide operating temperature range -40°C to +85°C
- 3.3 volt operation

Hitachi semiconductor

Functional Description

Figure 1 shows an overview of the SH7490 functions:

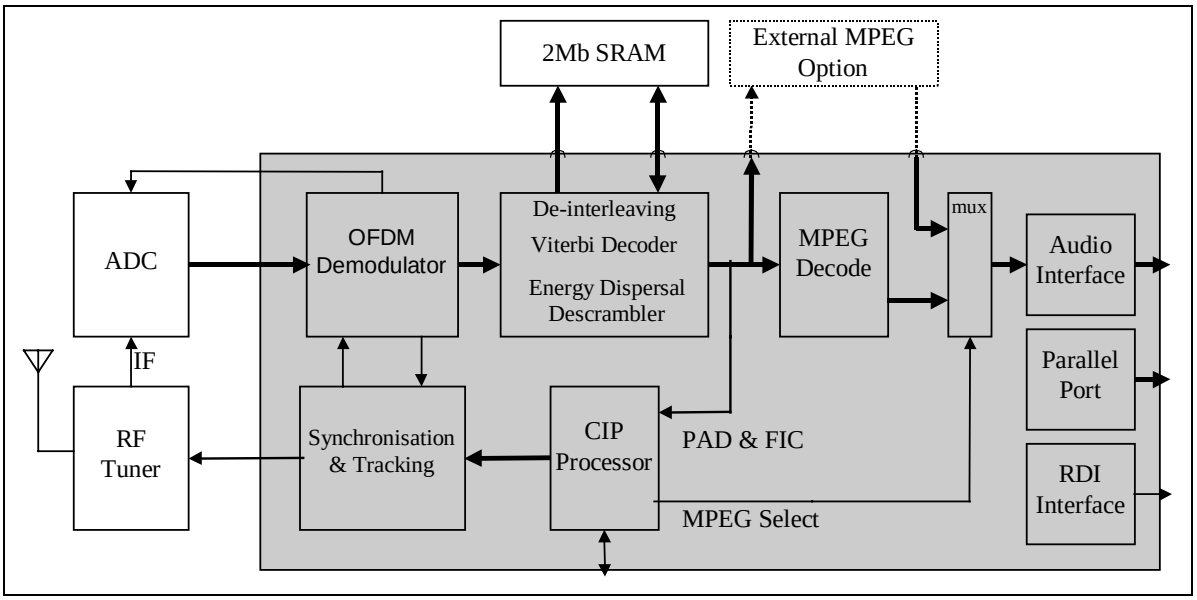


Figure 1 SH7490 Functional Block Diagram

Decoding Capacity

The decoding capacity of the SH7490 is dependent on the use of internal or external MPEG decoding and the use of single or dual sub-channel decoding. The configurations supported by the SH7490 are defined below:

a. Configuration 1

   One sub-channel of MSC including MPEG Audio decoding on chip where the total number of capacity units (CU) of the sub-channel does not exceed 192, although the maximum bit rate may not exceed 256 kbits/s.

   e.g. Maximum output rate: 256 kbit/s at r= 0.5. The supported bit rate and protection profiles matrix is defined in the Internal MPEG section of the table in Appendix B.

b. Configuration 2

   Two sub-channels of MSC including MPEG decoding of one sub-channel on chip where the total number of CUs in each channel does not exceed 48.

   e.g. Each sub-channel must have an output rate of 64kbits/s at r=0.5 or lower.

c. Configuration 3

   Two sub-channels of MSC with external MPEG Audio decoder. This allows decoding of 2 individual channels of MSC where the total number of combined CUs does not exceed 192. But each sub-channel will use at least 48 CU from the total of capacity of 192 CU.
   e.g. 1 Audio channel at 192 kbit/s and 1 data channel at 64 kbit/s

d. Configuration 4

   One sub-channel of MSC with external MPEG Audio decoder where the total number of capacity units in the sub-channel does not exceed 280. e.g. Maximum output rate: 384 kbit/s at r= 0.5. The supported bit rate and protection profiles matrix is defined in the External MPEG section of the table in Appendix B.

Notes: a. In all cases, FIC is fully decoded. Full synchronisation is provided. The decodable output rates are guaranteed in all modes,

b. r = Viterbi protection rate ; r=0.5 equals to DAB protection profile 3 (UEP).

OFDM Demodulator

The 8-bit A/D input data is digitally mixed and filtered to produce a data stream of in-phase and quadrature (I/Q) pairs each with an 8-bit resolution at 2.048 MSPS. The transfer function of the digital filter is dependent on the selected sampling rate. Figure 2 and Figure 3 show the transfer function for 8.192 MHz and 4.096 MHz respectively. Fs is the A/D converter sampling frequency and Fc is the centre frequency of the filter.

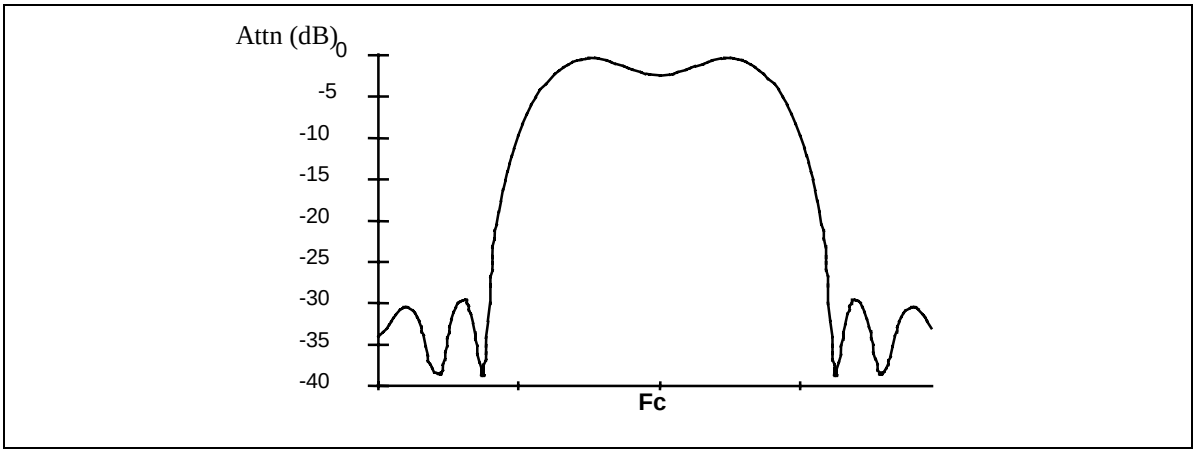


Figure 2 Transfer Function of Digital I/Q - Down-Sampling Filter;
Fc = 2.048 MHz for Operation with Fs = 8.192 MHz

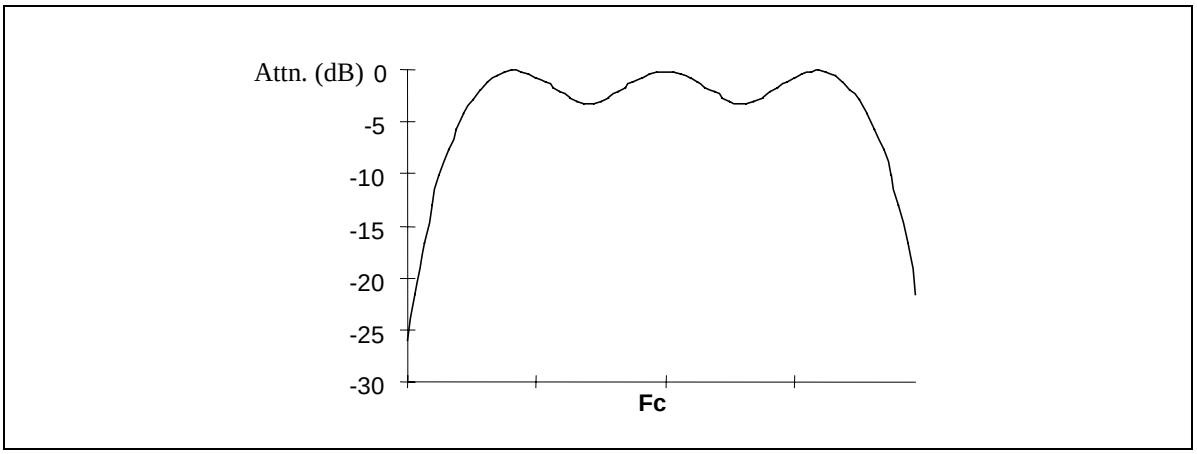


Figure 3 Transfer Function of Digital I/Q – Down-Sampling Filter ;
Fc = 3.072 MHz for Operation with Fs = 4.096 MHz

A digital rotator is used to perform an automatic frequency control (AFC) function on the I/Q data stream.

The range of frequency offsets which can be applied to the baseband I/Q data stream is -16 kHz to +16 kHz.

When the SH7490 has direct control of the tuning synthesiser using synthesiser controls signals (SY_EN1, SY_DATA and SY_CLK), the internal control algorithm automatically re-programs the synthesiser for AFC ranges of wider than +/-16 kHz.

The SH7490 performs a fast Fourier transform (FFT) on the I/Q samples; internal algorithms control the FFT window positioning without the aid of an external null symbol detector. The SH7490 can also have the FFT window position adjusted externally using a CIP command. The FFT result is then demodulated and the result is stored as soft-decisions.

Synchronisation and Tracking

The SH7490 has internal synchronisation and tracking algorithms that control the following:

a. Amplitude of the incoming data to the A/D Converter (AGC Control output)
b. FFT window position
c. Digital AFC
d. VHF synthesiser frequency (SY_EN1, SY_DATA and SY_CLK outputs)
e. Sampling rate control (VCXO control output)

The null symbol, phase reference symbol and half of the channel impulse response are available from the parallel port. If needed, this information can be used by an optional external synchronisation and tracking processor.

De-Interleaving, Viterbi Decoder and Energy Dispersal De-scrambler

The SH7490 requires 2M bit of external SRAM, arranged as two 128k by 8-bit wide devices, for de-interleaving and buffering. The de-interleaving function gives disturbance free operation during multiplex re-configurations. After de-interleaving, the internal Viterbi decoder error corrects the soft-decision data.

MPEG Decoding

The SH7490 has an internal MPEG decoder providing support for 48kHz and 24 kHz audio sampling frequencies. This internal MPEG decoder can be used when decoding a single sub-channel of MSC up to a data rate of 256kbits/s at r=0.5, or 2 sub-channels of MSC of 64kbits/s each, or lower. With an external MPEG decoder the following decoding configurations are supported:

a. Two sub-channels of MSC at combined bit rates of up to 256kbits/s,
b. A single sub-channel of MSC with bit rates greater than 256kbits/s but less than 384kbits/s (r=0.5).

The SH7490 does not support decoding capacity greater than 384kbits/s at r=0.5, or 256kbits/s at r=0.3.

Audio Interface

The audio interface allows direct connection to a wide range of stereo audio digital-to-analogue converters (DAC). The audio interface allows dynamic range control (DRC) and volume control to be applied by CIP commands.

Command Interface Protocol Processor

The SH7490 uses a command interface protocol (CIP) that operates over an asynchronous serial interface. This protocol provides all of the required functions for selection of DAB ensembles and services and controlling and monitoring the facilities and features of the device. The contents of the fast information channel (FIC) and programme associated data (PAD) are available through the CIP. DAB applications may require a large amount of memory for storing data such as service information. The SH7490 can offer up to 27k byte of storage, accessible by the host microcontroller using CIP commands.

RDI Port

The SH7490 offers an RDI port conforming to the high capacity mode defined in Specification of the Receiver Data Interface (RDI) Issue 1.4, November 1996 [2]. Only the actual decoded data is included in the RDI output bit stream. This includes the selected sub-channel(s) of MSC, FIC, and TII data.

Parallel Port

The SH7490 provides an IEEE-1284 compliant parallel port supporting compatibility mode (output only). This allows easy access to the FIC data, decoded MSC data, FFT window offset, null and phase reference symbols samples, and the channel impulse response. It allows connection to a host microcontroller parallel port or an extended capabilities port (ECP) compliant PC parallel port.

Applications Block Diagram

Figure 4 shows an example application block diagram using the SH7490.

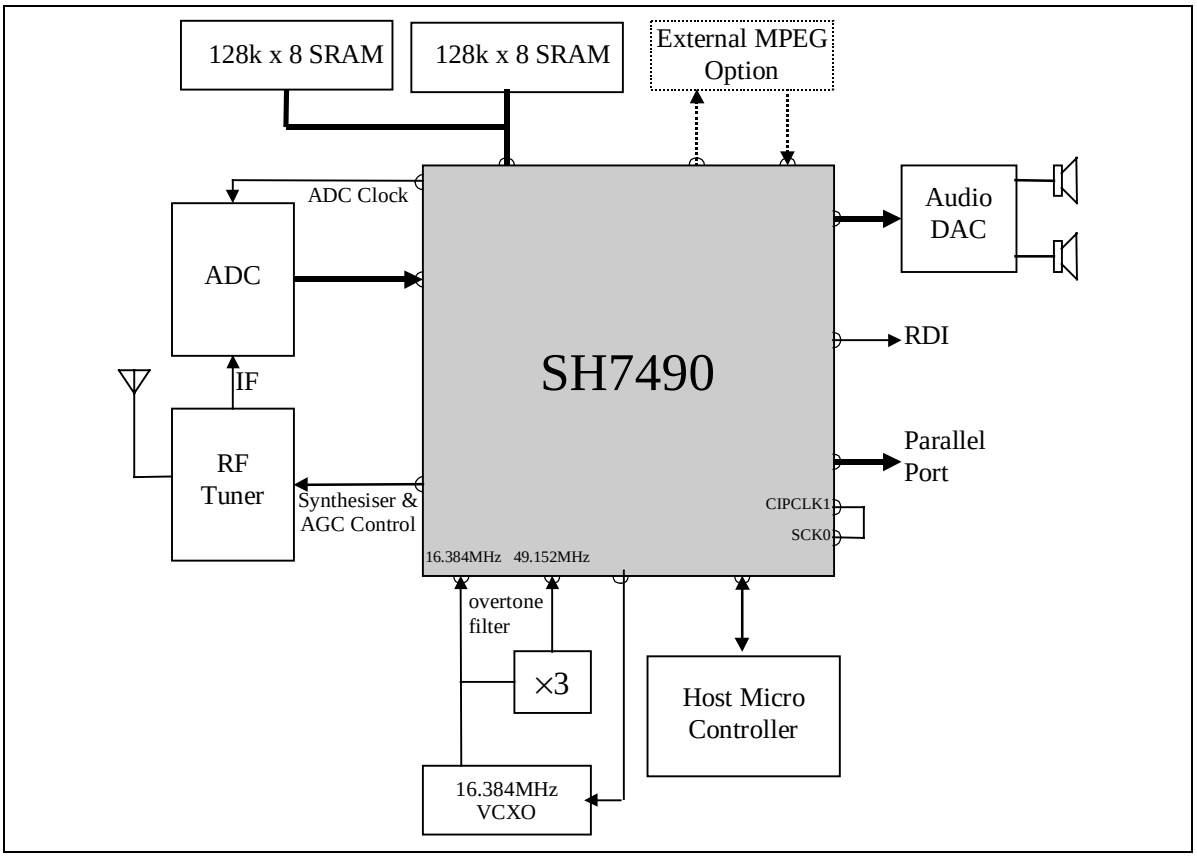


Figure 4 Applications Block Diagram

Pin Functions

A/D Converter Interface

The SH7490 provides the sampling clock for an external A/D converter. The parallel 8-bit conversion result from the external A/D converter drives ADC (7) to ADC (0). The interface is designed to serve various tuner designs. The mode selection is performed by the RFMODE1 pin as follows:

PINS:

RFMODE1 (pin 37):	A/D converter Sampling Rate Select
RFMODE1=H	fs=4096 kHz (low IF at fc = 3072 kHz)
RFMODE1=L	fs=8192 kHz (low IF at fc = 2048 kHz)
ADC (0)...ADC (7) (pins 39,41,43-48):	Parallel data input (ADC0 = LSB , ADC7 = MSB)
ADC_CLK (pin 38):	Output clock from the SH7490 to the A/D converter

Data at this input is expected to be valid at the positive edge of ADC_CLK. The A/D converter data must be in unsigned offset binary format. The sampling clock (ADC_CLK) is derived from the 49.152 MHz input clock (CLK_X) which is derived from the system VCXO frequency.

Tuner Control Interface

The SH7490 provides the controls for a DAB RF tuner, supporting VHF band 3 and L-Band reception. It performs

- AGC — Automatic Gain Control
- Band selection — L-Band, Upper VHF, Lower VHF
- Synthesiser setting — L-Band down-conversion, Low IF down conversion, tuning frequency inVHF band
- VCXO control — Adjustment of system clocks
- Spectrum Inversion

An example tuner block diagram is given in Figure 5.

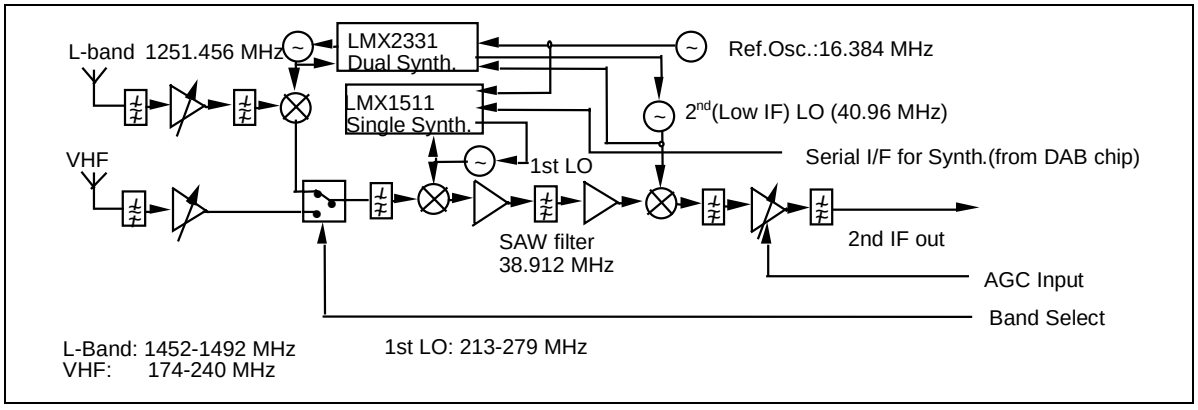


Figure 5 Example RF Tuner Block Diagram

The synthesiser programming data assumes that a 16.384MHz reference clock is being used for both synthesisers. This can be derived directly from the 16.384MHz VCXO (connected to EXTAL pin) or from an additional fixed crystal source of 16.384 MHz.

Automatic Gain Control

An automatic gain control (AGC) level output is provided by the SH7490 to control the level of input signal to the A/D converter.

This signal is generated by an over-sampled 1-bit D/A converter. The D/A converter operates at a clock speed of 16 MHz and has a resolution of 10 bit. A first order passive low pass filter is required at the output pin, see Figure 6. The time constant should be in the range of 0.5 to 1 ms.

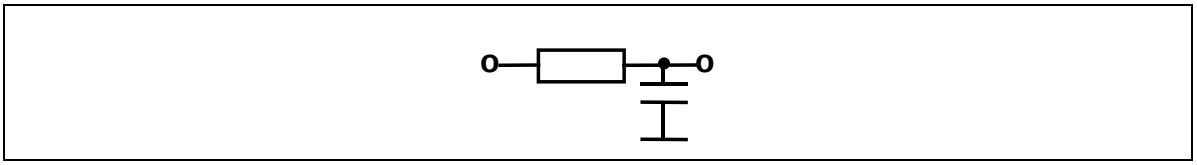


Figure 6 External Low Pass Filter for AGC Output

Recommended values: R= 27 kΩ and C = 20 nF

Directly after reset, the output is set to its highest possible value, which must correspond to the highest possible AGC gain setting. The SH7490 then starts to decrease the output value until a suitable setting is reached.

An increase in output voltage produced after low-pass filtering the signal from this pin must correspond to an increase in the tuner's overall gain. The approximate transfer characteristics of an external AGC is expected to be around 25dB/volt. Variations by a factor of 2 to 3 in AGC transfer characteristics can be tolerated without performance loss.

In case the external AGC circuit is not required to be controlled by the SH7490, the user should design the circuit in a manner which avoids the SH7490 to go into saturation at its AGC output.

PIN:

AGC (pin 59): AGC control pin.

Band Select

The SH7490 provides two output pins that can be used for selecting the tuning frequency range of the RF tuner. These pins reflect the tuning frequency requested by the CIP command, set centre frequency.

PINS:

BAND2 (pin 61): L-band selection Output
BAND2 = "H" L-band selected
BAND2 = "L" VHF band selected

BAND1 (pin 62): VHF -band selection Output;
BAND1 ="H" Upper VHF band selected, frequency range 212 to 240 MHz
BAND1="L" Lower VHF Band selected, frequency range 174 to 212 MHz

If these signals are not used by the application circuit, they should be left open.

Synthesiser Control

The SH7490 automatically provides serial data for the setting of RF tuner synthesiser ICs.

One possible system application shown in Figure 7 uses a dual mixer IC for generation of the L-Band down-conversion Mixer frequency (1251.456 MHz) and the 2nd Mixer Local Oscillator frequency (40.96 MHz). These frequencies are generated from an external reference oscillator (16.384 MHz).

A single synthesiser is used to provide the 1st Local Oscillator frequency, which together with the first IF mixer performs the receiver tuning. The SH7490 controls the setting of this synthesiser in conjunction with the on-chip digital rotator block to perform AFC.

Remark: The direct control of the RF tuner circuit by SH7490 can only operate under the following conditions:

1. Down converter for L-band and Low IF uses a dual synthesiser such as National Semiconductor LMX 2331 or a functionally compatible IC.
2. Down-conversion from VHF to IF of 38.912 MHz uses a synthesiser such as National Semiconductor LMX 1511 or a functionally compatible IC.
3. The local oscillator frequencies are set to 1251.456 MHz (L-Band), 40.96 MHz (Low IF). For band III the local oscillator has to be : ((VHF input) + 38.912) MHz .

The control interface for synthesisers uses the pins:

SY_CLK	(pin 52):	Synthesiser clock for serial data
SY_DATA	(pin 50):	Data to set external synthesiser, MSB first
SY_EN2	(pin 53):	Latch command for down conversion synthesiser
SY_EN1	(pin 54):	Latch command for tuning synthesiser

All data output is transmitted MSB first with data changing on negative edge of SY_CLK.

Basic timing chart for tuning synthesiser (LMX 1511 or compatible) is shown in Figure 7 and Figure 8.

Figure 7 shows the setting prescaler and reference divider when Control Bit is set “H”. Figure 8 shows the setting the swallow counter (A) and programmable counter (B) when Control bit is set “L”. See Appendix A for further details of the synthesiser programming.

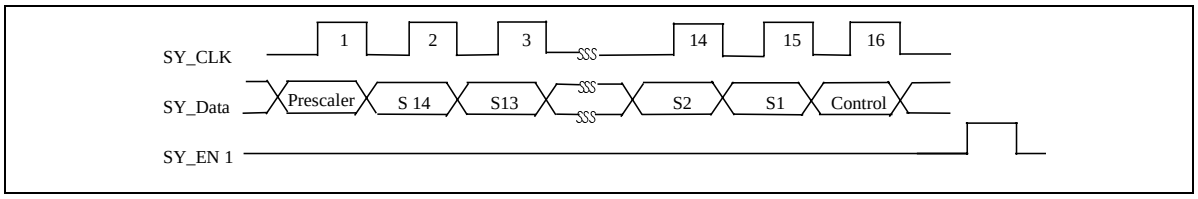


Figure 7 Setting Prescaler and Reference Divider of the Tuning Synthesiser

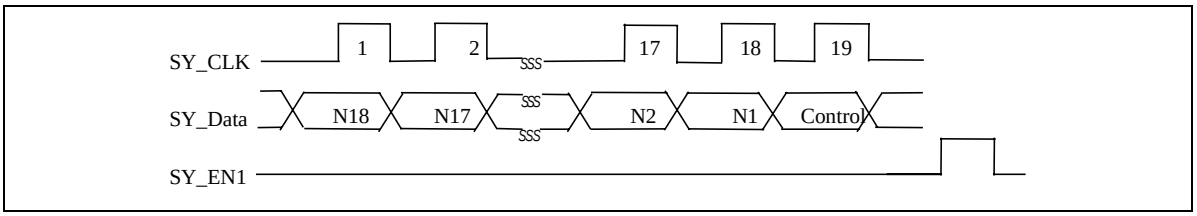


Figure 8 Setting the Swallow Counter (A) and Programmable Counter (B) of the Tuning Synthesiser

Basic timing chart for setting the registers in the down-conversion synthesiser (LMX2331 or compatible) is shown Figure 9. See Appendix A for further details of the synthesisers programming.

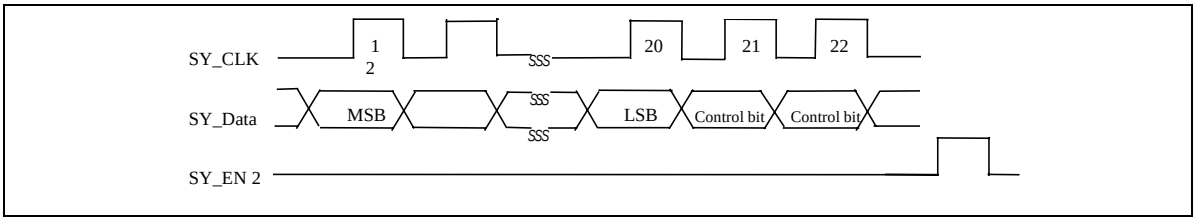


Figure 9 Timing Chart Down Conversion Synthesiser; Setting Registers

The SH7490 outputs pre-programmed values to the external synthesiser registers automatically. Data is output in the following sequence upon reset and after 1st *Set Centre Frequency* command:

0x020400	IF-Reference counter	(DAB System: Low IF)
0x020402	RF-Reference counter	(DAB System: L-band down converter)
0x105001	IF-Swallow/ Program counter	(DAB System: Low IF)
0x11318B	RF-Swallow/ Program counter	(DAB System: L-band down converter)
0x008801	Single PLL Reference counter	(DAB System: Tuning synthesiser)
0x010058	Single PLL Swallow/Program counter	(DAB System: Tuning synthesiser)

The first 5 values are fixed. They are determined by local oscillator definitions for down conversion and by the defined reference frequency (VCXO). See “Tuner Control Interface” for details.

The last (6th) value is an example for tuning to an ensemble centred at 223.936 MHz. This value can change within the acquisition phase and after *Set Centre Frequency* command.

For functional block diagram and register structure of the external synthesiser circuit see Appendix A.

For applications using a different RF tuner configuration, the RF tuner can be configured by the host microcontroller. The course frequency jump interrupt, provided by the CIP, still allows the wide acquisition range feature of the SH7490 to be used in such applications.

The spectrum of the A/D Data must be centred about or aliased to 2.048 MHz or 3.072 MHz at the selected sampling rate of 8.192 MHz or 4.096 MHz respectively.

Spectrum Inversion

The SH7490 provides the facility of inverting the complex spectrum of DAB ensemble about its centre frequency.

This function is provided by the RFMODE2 pin.

PIN:

RFMODE2 (pin 35): Spectrum inversion control

RFMODE2 = L spectrum inversion off

RFMODE2 = H spectrum inversion on

System clocks and Reset

All system clocks can be derived from a single voltage controlled crystal oscillator (VCXO). This configuration enables the use of a low cost VCXO and overtone detect filter. Figure 10 shows the clocking topology of the SH7490.

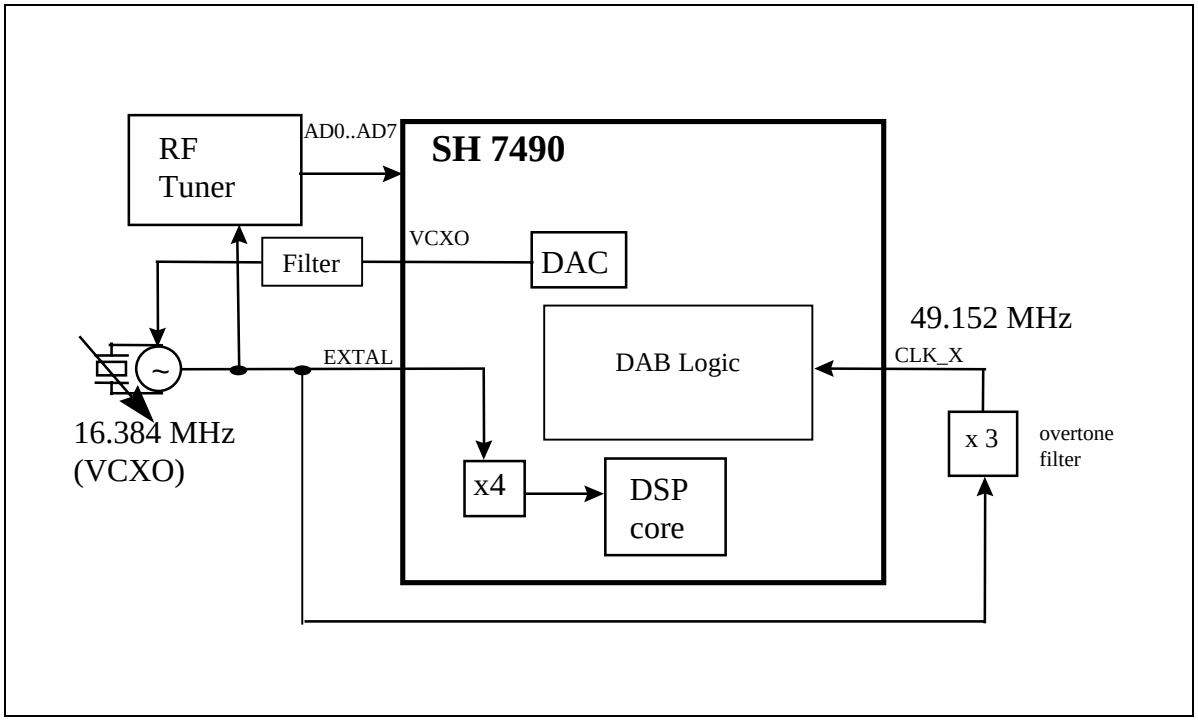


Figure 10 Clock Generation on SH7490

The SH7490 controls the VCXO by an analogue output voltage, provided by a one bit over-sampled D/A converter. The D/A converter works at a clock speed of 16 MHz and a resolution of 15 bit. The recommended time constant of the single pole reconstruction filter is 10 ms. It may be desirable to use higher order filters and/or longer time constants.

After reset, the output value is set to an average value around $0.5 \times Vcc$. This value is automatically increased by the internal tracking algorithm in case a higher frequency is required, and is decreased when a lower frequency is desired.

The approximate transfer characteristics should give a frequency change of around +20 ppm to +50 ppm for a voltage change of +1V. Other values can be tolerated, it is essential, that the VCXO can operate at the desired frequency over all temperature ranges.

PINS:

EXTAL	(pin 77):	VCXO (16.384 MHz) clock input pin
VCXO	(pin 60):	VCXO control output pin
CLK_X	(pin 81):	Clock (49.152 MHz) input pin for the DAB logic part
PLLGND	(pin 69):	GND for the PLL circuit
PLLVCC	(pin 71):	Power supply for the PLL circuit
PLLCAP	(pin 70):	External capacitor for the PLL circuit
RSTN	(pin 32):	SH7490 reset pin, reset by logic 'L' on this pin

The SH7490 requires a clock of 49.152 MHz at the pin denoted CLK_X (pin 81). It is recommended to derive this frequency from an overtone detect circuit applied to the external VCXO frequency of 16.384 MHz driving the EXTAL pin. The mark-to-space ration of CLK_X must be 1:1 with a variation of no more than +/-10%.

The SH7490 can be reset by applying a logic low signal to RSTN (pin 32).

The SH7490 incorporates the PLL circuit, which multiplies the externally supplied clock on the EXTAL pin by four, for use in the internal DSP. The internal PLL requires an external capacitor (C1) between the PLLCAP and PLLGND pins. Inductive elements should be reduced by placing the capacitor as close as possible to these pins allowing tracks to be kept short. It is recommended to make these traces extra wide and keep other signal tracking away from the PLLCAP pin and it's trace. The recommended value for C1 is 470pF. It is also recommended the PLLVCC pin be connected to 3.3V supply via a 100Ω resistor. The resistor should be de-coupled using a 0.1µF capacitor. See Figure 11: PLL Pin Connection Diagram.

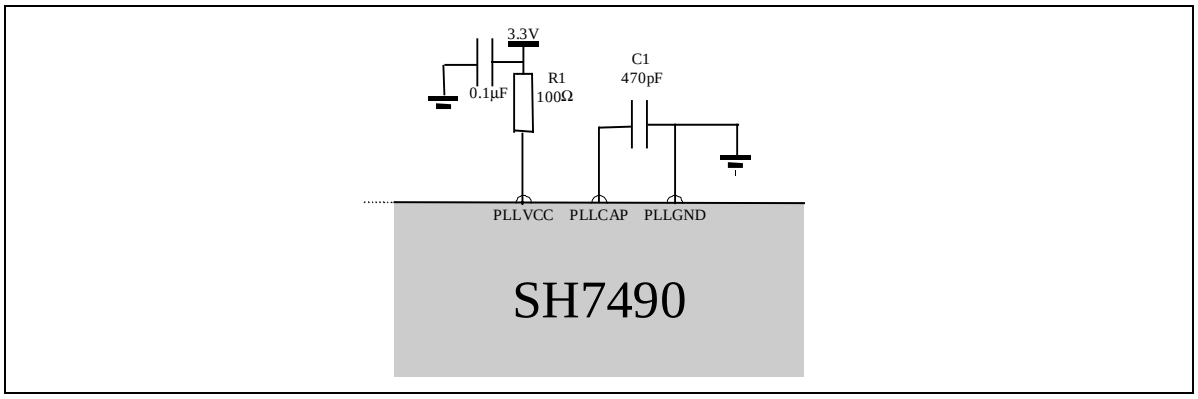


Figure 11 PLL Pin Connection Diagram

External SRAM Interface

The SH7490 requires two-byte wide external SRAMs, of 1 Mbit each. Figure 12 shows the connections between the SH7490 and the external SRAMs.

PINS:
DR(0) …DR(15) (pins 128,130,132-136,138,140-142,144,146,147,149,151) : Bi-directional data bus for external SRAM
AR(0) …AR (16) (pins 176,174,172,170,168-165,163,161-156,154,152) : Address bus outputs for external SRAM
SRAMWE0 (pin 127): SRAM write enable 0 (lower byte)
SRAMWE1 (pin 126): SRAM write enable 1 (upper byte)
SRAMOE (pin 125): SRAM output enable

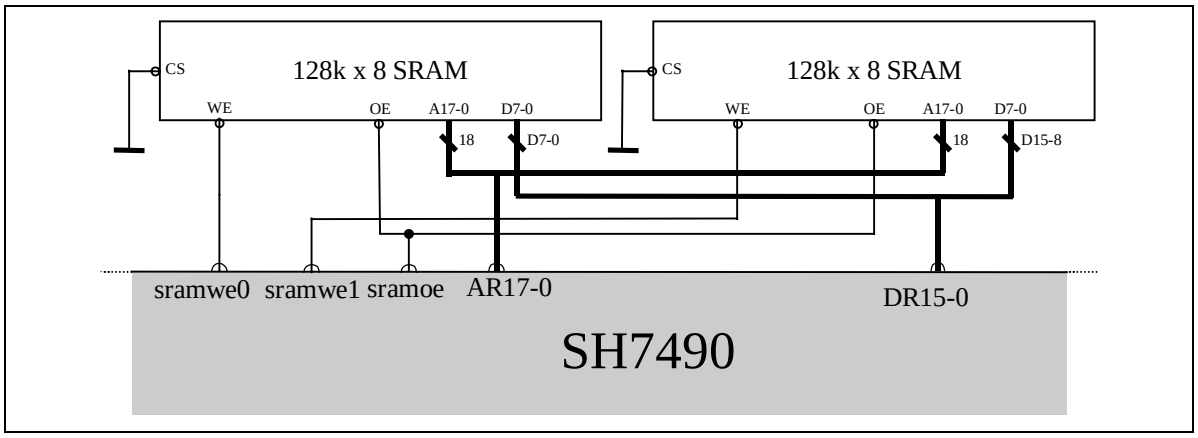


Figure 12 External SRAM Connection Diagram

External MPEG/Data Interface

This output provides an interface to access the bit stream after COFDM decoding. The selected sub-channel of MSC is available via this interface. The selected sub-channel could be either an audio or a data service.

When an audio service is selected, the output data represents a bit stream according to MPEG 2 standard. The bit stream can be processed by an external MPEG Audio decoder to a maximum bit rate of 384 kbit/s (r=0.5). The SH7490 can be instructed using a CIP command to perform scale factor CRC on the bit stream, allowing the use of a standard MPEG 1 audio decoder. In this case, internal concealment is switched on.

If the selected service is a data service, the bit stream can be output without further processing, independent from the service carrying data in stream mode or packet mode.

PINS:

M_DATA (pin 90): MPEG encoded audio bit stream or a data service bit stream, after COFDM decoding

R_CLK (pin 85): Clock output of 384 kHz, gated to correspond to the bit rate of the selected subchannel.

M_RSTN (pin 92): A output which is asserted ('L') whilst the SH7490 RSTN pin is asserted ('L') the output is then de-asserted synchronously with the negative edge of R_CLK shortly after RSTN input is de-asserted.

R_CLK is a gated clock of 384 kHz. Based on a 24 ms frame, R_CLK is active for the period of valid bits per frame and stopped for the remaining period, until next frame starts. One frame of 24 ms corresponds to 9216 clock cycles of 384 kHz.

The output data M_DATA changes on the negative edge of R_CLK.

Example: Output data rate: 256 kbit/s
Clock active: 6144 cycles, Clock stopped: 3072 cycles

The basic timing for this interface is shown in Figure 13 below.

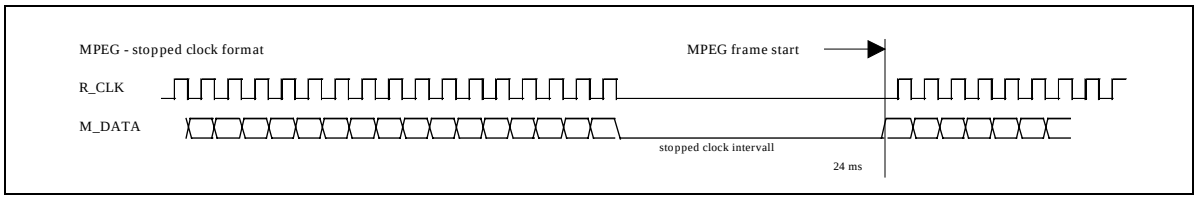


Figure 13 External MPEG/data Interface Basic Timing (MPEG – stopped clock format)

Digital Audio Input Interface

For applications requiring an external MPEG decoder, the audio data stream output of the external MPEG decoder can be connected to the Digital Audio Input interface. This allows the SH7490 to apply DRC and volume control processing to the audio data using CIP commands. The audio data is then available on the Digital Audio Output Interface (A_BICK, A_LRCLK and A_BICK).

When the internal MPEG decoder is selected the M_BICK and M_LRCK pins must be left open or driven to constant logic levels.

PINS:

M_BICK (pin 88): serial clock (f = 32 × 48 kHz)
M_SDATAI (pin 89): serial audio data, e.g. from external MPEG decoder
(data is latched on positive edge of M_BICK)
M_LRCK (pin 91): framing signal from external MPEG decoder (H = Left and L = Right)

The basic timing for this interface is shown in Figure 14 below.

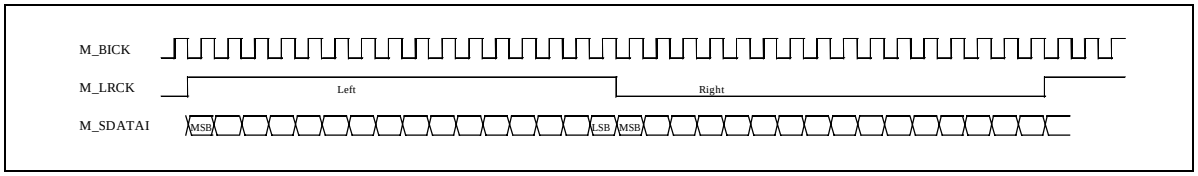


Figure 14 Digital Audio Input Timing

Digital Audio Output Interface

The Digital Audio Output Interface is a three-line interface that allows direct connection to a wide range of stereo Digital-to-analogue converters. The MPEG decoded audio data, available from this interface is always at a sampling frequency of 48 kHz. In cases when the decoded sub-channel is carrying a low sampling rate (24 kHz) service, this output provides an over-sampled signal of 48 kHz (internal MPEG decoding only). The serial data (A_SDATAI) changes on the negative edge of A_BICK.

PINS:

A_BICK (pin 101): Digital audio serial clock 1.536 MHz (f = 32 × 48 kHz)
A_SDATAI (pin 100): Digital audio output data
A_LRCK (pin 99): Digital audio framing signal 48 kHz (H = left and L = right channel)

The basic timing for this interface is shown in Figure 15.

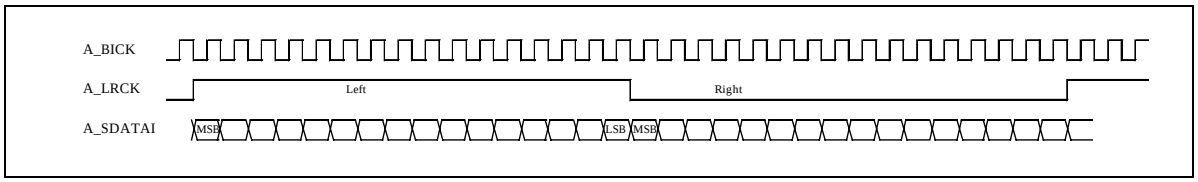


Figure 15 Digital Audio Output Timing

Parallel Port

An IEEE-1284 compliant parallel port supporting compatibility mode only (output only). This port gives access to FIC data, decoded MSC data, FFT window offset, null and phase reference symbols samples and the channel impulse response. The output data available from this port is controlled via CIP commands. This standard parallel interface allows direct connection to either the host microcontroller or an ECP compatible PC port.

Table below summarises the characteristics of the parallel port.

Table 1 Parallel Port Characteristics

Word width	8 bits
Direction	Output
Handshaking	Using P_CLK and H_ACK
Transfer Rate	Up to 210 k transfers per second

PINS:

PDATA(0) ..PDATA(7) (pins 113-111,109,107-104): Parallel data output pin
(P_DATA 0 = LSB,P_DATA 7 = MSB)

P_CLK (pin 103): Data transfer clock output pin to the host computer

H_ACK (pin 102): Acknowledge signal input pin driven by the host

Handshaking between the host computer and the SH7490 is taken care of by signals P_CLK and H_ACK. The output P_CLK is set to low level when the data PDATA(0..7) is valid. The input H_ACK is then driven high by the host computer as a response. The basic timing for this interface is given in Figure 16 below.

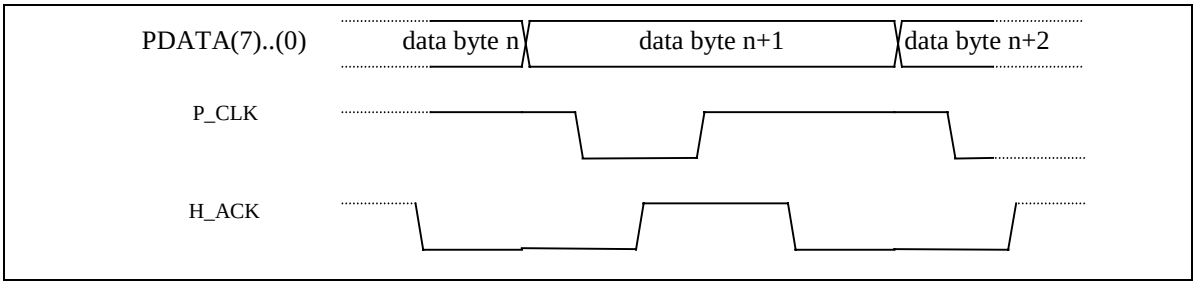


Figure 16 Basic Timing for Parallel Port

Receiver Data Interface

The SH7490 offers an RDI port conforming to the High Capacity Mode defined in Specification of the Receiver Data Interface (RDI) Issue 1.4, November 1996 [2]. Only the actually decoded data is included in the RDI output bit stream, this includes:

- FIC
- TII
- Decoded sub-channel(s), maximum 2 including related PAD

Since the SH7490 does not decode the full MSC, only the decoded data is provided.

PIN:
RDI_OUT (pin 33): RDI Output
Provides decoded data according to [2]

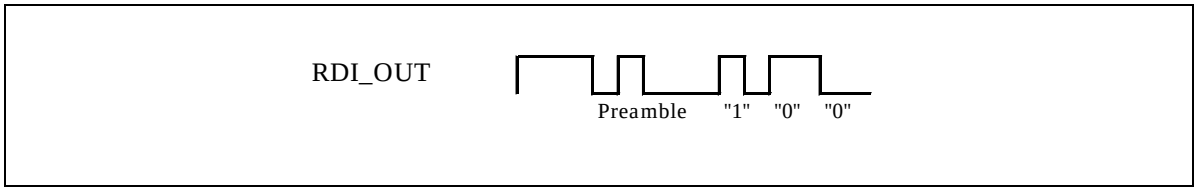


Figure 17

Clock for External Peripheral Devices

The SH7490 provides a number of clocks to simplify the interfacing to external peripheral devices, these include:

PINS:

M_CLK	(pin):	Outputs a clock of 512 × 48 kHz = 24.576 MHz. This clock can be used as a system clock for an external MPEG or a D/A converter.
CLK_6M	(in 93):	Outputs a clock of 128 × 48 kHz = 6.144 MHz. This clock can be used as a master clock for digital audio interface formatter ICs such as IEC958.
CLK_12M	(Pin 95):	Outputs a clock of 256 × 48 kHz = 12.288 MHz. This clock can be used as a clock source for each output signal of an external MPEG.

Host Microcontroller Interface

The SH7490 is controlled using a serial command interface protocol (CIP). This protocol treats the SH7490 as a slave, when it receives a command from the host processor it always responds by identifying the command it received, returning the status of the SH7490 and, where applicable data. All commands and data exchanges use a serial, asynchronous data format. Commands and data transfers are always byte unit multiples in length; the format of this data is as given below:

1 Start Bit
1 message or command byte
1 Stop Bit
No Parity Bit

PINS:

SCK0	(pin 29):	Serial bit rate clock input
TxD0	(pin 28):	Serial data transmit output
RxD0	(pin 26):	Serial data receive input
CIPCLK1	(pin 30):	Serial clock option 1 output (0.6144 MHz) enables a communication speed of 38.4 kbits/s
CIPCLK2	(pin31):	Serial clock option 2 output (1.8204 MHz) enables a communication speed 115.2 kbits/s

SCK0 is a 16 times bit rate clock input for the SH7490 internal asynchronous serial interface. Two clocks are provided by the SH7490 to drive SCK0. These are CIPCLK1 and CIPCLK2 which enable the CIP to communicate with host processors at bit rates of 38.4 kbits/s and 115.2 kbits/s respectively. The maximum frequency for SCK0 is 4 MHz; its frequency must be a 16 times multiple of the desired bit rate. The application design must select a bit rate high enough to allow access to the PAD, FIC data and onboard data storage area over the CIP. In applications were this is not possible the FIC and PAD data are also accessible to the host processor over the parallel port. The host microcontroller interface can service a maximum of 380 CIP commands per second.

Pin List

Pin-No.	I/O	Name	Function
1	I/O	RFU1	Internal pull-up provided ; do not connect
2	I/O	RFU2	Internal pull-up provided ; do not connect
3	I/O	RFU3	Internal pull-up provided ; do not connect
4	I	GND	Ground
5	I/O	RFU5	Internal pull-up provided ; do not connect
6	I	VCC	Vcc
7	I/O	RFU7	Internal pull-up provided ; do not connect
8	I/O	RFU8	Internal pull-up provided ; do not connect
9	I/O	RFU9	Internal pull-up provided ; do not connect
10	I/O	RFU10	Internal pull-up provided ; do not connect
11	I	GND	Ground
12	I/O	RFU12	Internal pull-up provided ; do not connect
13	I	VCC	Vcc
14	I	RFU14	Internal pull-up provided; do not connect
15	I	RFU15	Set to “L”
16	I	RFU16	Set to “L”
17	I	RFU17	Set to “L”
18	I	RFU18	Set to “L”
19	I	RFU19	Set to “L”
20	I	RFU20	Set to “L”
21	O	RFU21	do not connect
22	I	RFU22	do not connect
23	I	RFU23	do not connect
24	I	RFU24	do not connect
25	I	GND	Ground
26	I	RXD0	Serial data input for host microcontroller
27	I	VCC	Vcc
28	O	TXD0	Serial data output to host microcontroller
29	I	SCK0	Serial port clock input for host microcontroller
30	O	CIPCLK1	CIP clock 1 – 16 × bit rate clock for 38.4 kbps (0.6144 MHz)
31	O	CIPCLK2	CIP clock 2 - 16 × bit rate clock for 115.2 kbps (1.8204 MHz)
32	I	RSTN	Master reset for SH7490 (active low)
33	O	RDI_OUT	RDI output in IEC 958 format
34	I	GND	Ground
35	I	RFMODE2	Spectrum inversion control
36	I	VCC	Vcc
37	I	RFMODE1	A/D sample rate select

Pin-No.	I/O	Name	Function
38	O	ADC_CLK	Clock output to A/D converter
39	I	ADC(0)	Parallel data input bit 0 from A/D converter (LSB)
40	I	GND	Ground
41	I	ADC(1)	Parallel data input bit 1 from A/D converter
42	I	VCC	Vcc
43	I	ADC(2)	Parallel data input bit 2 from A/D converter
44	I	ADC(3)	Parallel data input bit 3 from A/D converter
45	I	ADC(4)	Parallel data input bit 4 from A/D converter
46	I	ADC(5)	Parallel data input bit 5 from A/D converter
47	I	ADC(6)	Parallel data input bit 6 from A/D converter
48	I	ADC(7)	Parallel data input bit 7 from A/D converter (MSB)
49	I	GND	Ground
50	O	SY_DATA	Synthesiser setting serial data
51	I	VCC	Vcc
52	O	SY_CLK	Synthesiser serial clock
53	O	SY_EN2	Down-conversion synthesiser latch command
54	O	SY_EN1	Tuning synthesiser latch command
55	I	GND	Ground
56	O	RFU56	Do not connect
57	I	VCC	Vcc
58	O	RFU58	Do not connect
59	O	AGC	AGC control signal (pulse output)
60	O	VCXO	VCXO control signal (pulse output)
61	O	Band2	L-band/VHF selection
62	O	Band1	Upper/lower VHF selection
63	O	N.C.	Do not connect
64	I	RFU64	Internal pull-up; do not connect
65	I	GND	Ground
66	O	RFU66	Do not connect
67	I	VCC	Vcc
68	I	RFU68	Internal pull-up - do not connect
69	Ana	PLLGND	GND of internal PLL circuit
70	Ana	PLLCAP	External capacitor for PLL
71	Ana	PLLVCC	Power supply for internal PLL
72	I	TEST72	Test pin - set to “H”
73	I	GND	Ground
74	I	TEST74	Test pin - set to “H”
75	I	VCC	Vcc
76	I	RFU76	Connect to Ground

Pin-No.	I/O	Name	Function
77	I	EXTAL	Input from external VCXO (16.384 MHz)
78	I	GND	Ground
79	O	N.C	Do not connect
80	I	VCC	Vcc
81	I	CLK_X	Input clock of 49.152 MHz ;derive fr. VCXO
82	I	TEST82	Test pin - do not connect
83	I	TEST83	Test pin - do not connect
84	I	GND	Ground
85	O	R_CLK	Serial clock for decoded MPEG /stream data output (384 kHz)
86	I	VCC	Vcc
87	O	M_CLK	512 × 48 kHz clock for external peripheral
88	I	M_BICK	Serial input clock from external MPEG decoder
89	I	M_SDATAI	Serial input data from external MPEG decoder
90	O	M_DATA	Serial output of MPEG/stream data
91	I	M_LRCK	Input frame signal from external MPEG decoder (48 kHz)
92	O	M_RSTN	MPEG reset (low active)
93	O	CLK_6M	128 × 48 kHz output for external peripheral support
94	I	TEST94	Connect to “L”
95	O	CLK_12M	256 × 48 kHz system clock for external peripheral devices
96	I	GND	Ground
97	O	RFU97	Do not connect
98	I	VCC	Vcc
99	O	A_LRCK	Decoded Audio Output frame signal (48 kHz)
100	O	A_SDATAI	Decoded Serial Audio Data Output (MSB first)
101	O	A_BICK	Serial Clock Output (32 × 48 kHz)
102	I	H_ACK	Parallel port acknowledge from the host computer
103	O	P_CLK	Parallel port clock to the host computer
104	O	PDATA(7)	Parallel port output data bit 7 (MSB) to the host computer
105	O	PDATA(6)	Parallel port output data bit 6 to the host computer
106	O	PDATA(5)	Parallel port output data bit 5 to the host computer
107	O	PDATA(4)	Parallel port output data bit 4 to the host computer
108	I	GND	Ground
109	O	PDATA(3)	Parallel port output data bit 3 to the host computer
110	I	VCC	Vcc
111	O	PDATA(2)	Parallel port output data bit 2 to the host computer
112	O	PDATA(1)	Parallel port output data bit 1 to the host computer
113	O	PDATA(0)	Parallel port ouput data bit 0 (LSB) to the host computer
114	I	TEST114	Test pin - do not connect
115	I	TEST115	Test pin - do not connect

Pin-No.	I/O	Name	Function
116	I	TEST116	Test pin - do not connect
117	I	TEST117	Test pin - do not connect
118	I	TEST118	Test pin - do not connect
119	I	TEST119	Test pin - do not connect
120	I	TEST120	Test pin - do not connect
121	I	TEST121	Test pin - do not connect
122	I	GND	Ground
123	I	TEST123	Test pin - do not connect
124	I	VCC	Vcc
125	O	SRAMOE	Output Enable signal for external SRAM
126	O	SRAMWE1	SRAM write enable 1
127	O	SRAMWE0	SRAM write enable 0
128	I/O	DR(0)	Data bus bit 0 for external SRAM (LSB)
129	I	GND	Ground
130	I/O	DR(1)	Data bus bit 1 for external SRAM
131	I	VCC	Vcc
132	I/O	DR(2)	Data bus bit 2 for external SRAM
133	I/O	DR(3)	Data bus bit 3 for external SRAM
134	I/O	DR(4)	Data bus bit 4 for external SRAM
135	I/O	DR(5)	Data bus bit 5 for external SRAM
136	I/O	DR(6)	Data bus bit 6 for external SRAM
137	I	GND	Ground
138	I/O	DR(7)	Data bus bit 7 for external SRAM
139	I	VCC	Vcc
140	I/O	DR(8)	Data bus bit 8 for external SRAM
141	I/O	DR(9)	Data bus bit 9 for external SRAM
142	I/O	DR(10)	Data bus bit 10 for external SRAM
143	I	GND	Ground
144	I/O	DR(11)	Data bus bit 11 for external SRAM
145	I	VCC	Vcc
146	I/O	DR(12)	Data bus bit 12 for external SRAM
147	I/O	DR(13)	Data bus bit 13 for external SRAM
148	I	GND	Ground
149	I/O	DR(14)	Data bus bit 14 for external SRAM
150	I	VCC	Vcc
151	I/O	DR(15)	Data bus bit 15 for external SRAM (MSB)
152	O	AR(16)	Address bus bit 16 for external SRAM (MSB)
153	I	GND	Ground
154	O	AR(15)	Address bus bit 15 for external SRAM

Pin-No.	I/O	Name	Function
155	I	VCC	Vcc
156	O	AR(14)	Address bus bit 14 for external SRAM
157	O	AR(13)	Address bus bit 13 for external SRAM
158	O	AR(12)	Address bus bit 12 for external SRAM
159	O	AR(11)	Address bus bit 11 for external SRAM
160	O	AR(10)	Address bus bit 10 for external SRAM
161	O	AR(9)	Address bus bit 9 for external SRAM
162	I	GND	Ground
163	O	AR(8)	Address bus bit 8 for external SRAM
164	I	VCC	
165	O	AR(7)	Address bus bit 7 for external SRAM
166	O	AR(6)	Address bus bit 6 for external SRAM
167	O	AR(5)	Address bus bit 5 for external SRAM
168	O	AR(4)	Address bus bit 4 for external SRAM
169	I	GND	Ground
170	O	AR(3)	Address bus bit 3 for external SRAM
171	I	VCC	Vcc
172	O	AR(2)	Address bus bit 2 for external SRAM
173	I	GND	Ground
174	O	AR(1)	Address bus bit 1 for external SRAM
175	I	VCC	Vcc
176	O	AR(0)	Address bus bit 0 for external SRAM (LSB)

Note: RFU = Reserved for future use
TEST = Test

Pin Arrangement

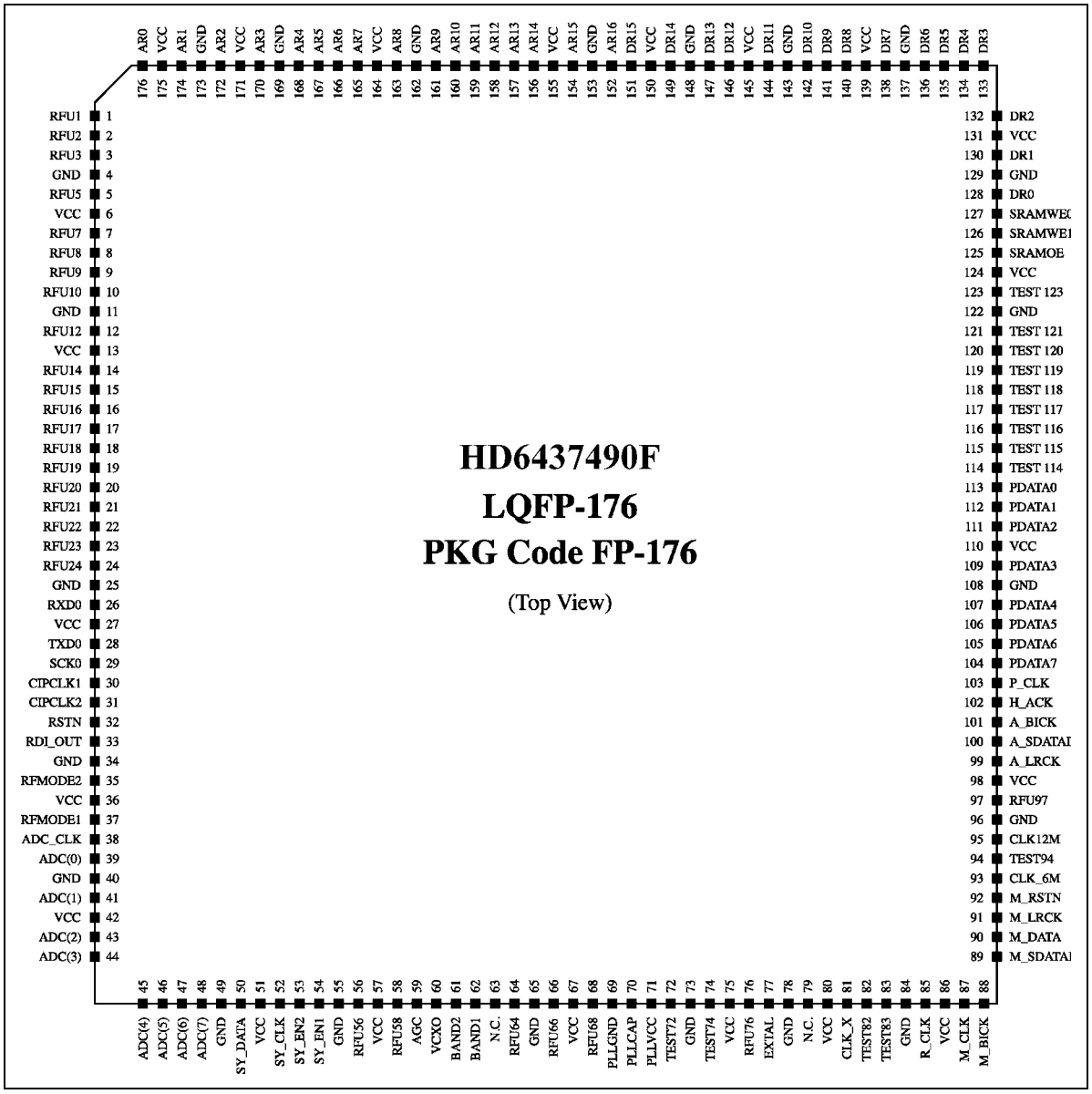


Figure 18 SH7490 Pin Arrangement

Programming Interface

Message Protocol

Protocol Description

The normal flow of information is initiated by a command from the host controller, which results in a response from the SH7490. The response may contain information requested in the command, or may trigger an action by the SH7490 that takes some time to complete. In the latter case, the response frame will be an acknowledgement that the command has been received and is being acted on and subsequently the completion of the action will be signalled by sending an interrupt. Interrupts are messages that signal either a change in the processor status or the asynchronous completion of a command.

Command Frame Format

Each command is transferred in a frame format, as shown in Figure 19. A command frame consists of the **command**, the **index** corresponding to the response, the **size** specifying number of data bytes, and command data. Each frame contains a whole number of bytes, allocated as follows:-

Command	Index	Size	Data...

Figure 19 CIP Command Frame Structure

- Command (1 byte).
- Index (1 byte).
- Size of data N (1 byte).
- Data (N bytes).

If size (N) is zero, no data bytes are present in the frame.

Response Frame Format

The SH7490 generates a response to every command frame received. A response frame consists of the **status** of the system, the **index** corresponding to the command, the number of data bytes (**size**) within the response frame, and response **data**. Thus, the response frame format is similar to the command frame, but with a **status** byte replacing the **command**, as shown Figure 20. Each frame contains a whole number of bytes allocated as follows:-

Status	Index	Size	Data...

Figure 20 CIP Response Frame Structure

- Status (1 byte).
- Index (1 byte).
- Size of data N (1 byte).
- Data (N bytes).

If size is zero, no data bytes are present in the frame.

Status contains an overall indication of the system's status. The **status** byte is illustrated in Figure 21.

7	6	5	4	3	2	1	0
MC	FDP	FPDP	XPDP	Rfu	Rfu	Rfu	OK

Figure 21 Status Byte

- **MC:** Forthcoming multiplex status change. This reflects the status of the change flag received within FIG0/0.
- **FDP:** FIC data present. The FIC buffer has data available.
- **FPDP:** F-PAD data present. The F-PAD buffer has data available.
- **XPDP:** X-PAD data present. The X-PAD buffer has data available.
- **Rfu:** Reserved for future use.
- **OK:** The command and parameters corresponding to index were valid. When an erroneous command is received, the SH7490 produces a minimal response frame with this bit clear, signalling an error.

Indexing

An **index** mechanism is used to keep track of all commands and their responses. Each command frame should contain an **index** within the range 0 to 127. The response returned from the SH7490 corresponds to the command with the same **index** number (Index 128 to 255 are used for interrupts described in "Interrupts".)

It is recommended that the index is increment each command frame in order to track all commands and their responses.

Interrupts

An interrupt is a response that is returned from the SH7490, which is asynchronous to the command. Interrupts use the index values 128 to 255. Interrupts are generated due to the two mechanisms described below.

Asynchronous Events

Interrupts that signal asynchronous events are generated in the following cases:

1. The status register goes into a status specified by **Interrupt Mask**
2. One of the currently selected services is no longer available
3. The DAB signal has been lost
4. The tracking algorithm requires a coarse frequency jump
5. Multiplex reconfiguration has occurred
6. MPEG CRC failure is detected (when MPEG errors interrupt is enabled)
7. Internal reset has taken place

Condition 1 is defined by the **Set Interrupt Mask** command. A full list of asynchronous event interrupts is given in "Interrupt Indixes".

Exclusive Command Completion

The command interpreter in the SH7490 generates a response to each command received. If the command is invalid or the command simply requests an item of available data such as status, the response completes the action of that command. However, commands requiring more complex processing continue after the response is transmitted. Completion of these exclusive commands is reported to the controller by interrupts. These interrupts contain information on execution results as well as command completion.

An example of an exclusive command is the **Set Centre Frequency** command. When this command is received, a response is returned. When the acquisition is completed, the SH7490 generates an interrupt to inform the controller of the outcome of the acquisition. A full list of exclusive commands is given in Table 2, and the associated interrupts are given in "Interrupt Indixes".

The controller should avoid issuing an exclusive command while another exclusive command is pending or currently being processed with the exception of the Set Centre Frequency command which can be re-issued whilst another Set Centre Frequency command is being processed.

The CIP defines a set of commands. This command set is split into six logical groups:

- Basic Control/Status
- System Commands
- Acquisition and Tracking
- FIC/PAD Access
- Channel Control/Status
- Audio Control/Status

The SH7490 allows up to two sub-channels to be decoded. The CIP uses a channel number to identify which of the two channels a specific command refers to. The channel number is defined by a 6 bit number (thus 64 possibilities, of which only 0 and 1 are valid). This channel number is not related to the multiplex configuration; it is a reference by which the controller and the SH7490 can identify a channel that is being decoded. When a sub-channel is selected using the **Set Channel Selection** command a channel number is given. That channel number is always used in other commands to refer to this specific sub-channel (until that channel is cancelled).

Note that the bits defined as Rfu are not currently in use. Clear these bits to 0 when issuing a command. These bit values in the interrupt/response are undefined. When a field has multiple bits, e.g. X5-0, X0 is the Lsb of that field.

The CIP includes a command set shown in Table 2.

Table 2 Commands

Command Name	Command Number
Basic Control/Status	
Get Status	00_{16}
Enable Exception	01_{16}
Disable Exception	02_{16}
Set Interrupt Mask	03_{16}
Get Interrupt Mask	04_{16}
System Commands	
Set Power Saving	22_{16}
Get Power Saving	23_{16}
Clear Commands	24_{16}
Reset*	25_{16}
Write Buffer Block	28_{16}
Read Buffer Block	29_{16}
Acquisition and Tracking	
Set Centre Frequency*	42_{16}
Get Centre Frequency	43_{16}
Get Mode	47_{16}
Get Acquisition and Tracking Status	48_{16}
Get RSSI	49_{16}
Read Tracking Data	$4A_{16}$
Write Tracking Parameters	$4B_{16}$
FIC/PAD Access	
Set Interesting FIGs	60_{16}
Get FIG Data	61_{16}
Get F-PAD	62_{16}
Set Interesting X-PAD Apps	63_{16}
Get X-PAD	64_{16}
Get Music/Speech Flags	65_{16}
Get ISRC_UPC Code	66_{16}
Get TII	67_{16}
Clear FIG Data	$6a_{16}$
Clear PAD Data	$6b_{16}$

Table 2 Commands (cont)

Command Name	Command Number
Channel Control/Status	
Move To Next Audio Service*	80_{16}
Set Channel Selection*	81_{16}
Get Channel Selection	82_{16}
Get BER Estimate	83_{16}
Get Channel Decode Status	84_{16}
Set Parallel Output	85_{16}
Audio Control/Status	
Select External Digital Audio	$A0_{16}$
Set DRC	$A1_{16}$
Get DRC Setting	$A2_{16}$
Set Volume Control	$A3_{16}$
Get Volume Control	$A4_{16}$
Set MPEG Control	$A5_{16}$
Get MPEG Status	$A6_{16}$

Note: * Exclusive Command

Command Group 0: Basic Control/Status

Get Status
Command Number: 00_{16}
Returns the status of the receiver. This command provides a simple mechanism to interrogate the receiver status.
Command Data: None.
Response Data: None.

Enable Exception
Command Number: 01_{16}
Enables the generation of CIP interrupts.
Command Data: None.
Response Data: None.
Interrupt Data: See “Interrupt Indixes”.

Disable Exception
Command Number: 02_{16}
Disables the generation of CIP interrupts.
Command Data: None.
Response Data: None.

Set Interrupt Mask
Command Number: 03_{16}
Specifies the condition where the **Status Mask Interrupt** (See "Interrupt Indixes") is issued to report the status byte change. This mask is AND'ed with the status byte, the **Status Mask Interrupt** is generated if this value changes and is not zero. Note that the bit corresponding to *Command OK* is ignored.
Command Data: 1 byte:

7	6	5	4	3	2	1	0
MC	FDP	FPDP	XPDP	Rfu	Rfu	Rfu	-

- MC: Mask bit for the MC bit in the Status byte
- FDP: Mask bit for the FDP bit in the Status byte
- FPDP: Mask bit for the FPDP bit in the Status byte
- XPDP: Mask bit for the XPDP bit in the Status byte

Response Data: None.
Interrupt Data: None.

Get Interrupt Mask
Command Number: 04_{16}
Returns the current interrupt mask
Command Data: None.
Response Data: 1 byte, data specified by the last **Set Interrupt Mask** command in the same format.

Command Group 1: System Commands

Set Power Saving
Command Number: 22_{16}
Sets the SH7490 into the given power saving mode. The lowest power setting is *Complete shutdown*. The *Track only* setting uses more power, but not as much as *Normal operation*. When the SH7490 is in *Track only* mode, FIC demodulation can start immediately on selection of *Normal operation*, as there is no delay in acquiring the DAB ensemble. When a **Set Centre Frequency** command is issued the SH7490 enters the *Normal operation* mode.
Command Data: 1 byte.

7	6	5	4	3	2	1	0
Rfu	Rfu	Rfu	Rfu	Rfu	Rfu	PS1	PS0

- PS1-0: Power saving modes.
  - 0 0 Normal operation.
  - 0 1 Track only (Disable all demodulation, including FIC).
  - 1 0 Complete shutdown (Processor sleeps except for CIP functions).
  - 1 1 Rfu.

Response Data: None.

Get Power Saving
Command Number: 23_{16}
Returns the current power saving mode.
Command Data: None.
Response Data: The same 1-byte format as the **Set Power Saving** command data.

Clear Commands
Command Number: 24_{16}

This command clears the CIP protocol and all pending command but not exclusive commands that are currently being processed. It will reset the CIP protocol and allow new commands to be performed. This command should only be issued under extreme circumstances such as the SH7490 not responding to a previous command or an error in data transmissions has occurred.

Command Data: None.
Response Data: None.

Reset
Command Number: 25_{16}
This command immediately performs a software reset of the receiver. This will cancel all command including exclusive command. **A Receiver has Reset** interrupt is generated when the reset takes place. This is an exclusive command.
Command Data: None.
Response Data: None.
Interrupt Data: A **Receiver Reset** Interrupt is generated when the reset completes.

Write Buffer Block
Command Number: 28_{16}
This command writes the block of data given in the command data to the specified buffer, starting at the given address in that buffer. Buffers 1 and 2 are shared memory with the Read Tracking Data command, so these commands should not be used together.
Command Data: 2 +2n bytes: 2 bytes of buffer number and address, followed by n 16 bit values (in 2n bytes, where n is in the range 0 to 126).

Byte 1:

7	6	5	4	3	2	1	0
BN1	BN0	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8

Byte 2:

7	6	5	4	3	2	1	0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

- BN1-0: Buffer number
  - 0 0 buffer number 0 (3.5 k words).
  - 0 1 buffer number 1 (5 k words).
  - 1 0 buffer number 2 (5 k words).
  - 1 1 Rfu.
- ADD13-0: Address, unsigned binary number indexing into the buffer. The valid ranges of addresses are from 0 to 3583 words in buffer 0 and up to 5119 words in buffers 1 and 2.

Response Data: None.

Read Buffer Block
Command Number: 29_{16}
This command reads a block of data from the given buffer/address and responds with the specified number of words of data. Buffers 1 and 2 are shared memory with the Read Tracking Data command, so these commands should not be used together.
Command Data: 3 bytes, Buffer number and address.

Byte 1:

7	6	5	4	3	2	1	0
BN1	BN0	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8

Byte 2:

7	6	5	4	3	2	1	0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

Byte 3:

7	6	5	4	3	2	1	0
Rfu	LEN6	LEN5	LEN4	LEN3	LEN2	LEN1	LEN0

- BN1-0: Buffer number
  - 0 0 buffer number 0 (3.5 kwords).
  - 0 1 buffer number 1 (5 kwords).
  - 1 0 buffer number 2 (5 kwords).
  - 1 1 Rfu.
- ADD13-0: Address, unsigned binary number indexing into the buffer. The valid ranges of addresses are from 0 to 3583 words in buffer 0 and up to 5119 words in buffers 1 and 2.
- LEN6-0: Length of the block of data to read in 16 bit words. The length can take any 7-bit value (0 to 127).

Response Data: 2 LEN bytes of data.

Notes on Write and Read Data Block Commands

Up to 126 words of data can be written or up to 127 words read at a time. The commands transfer multiples of 16 bit words and the addresses refer to 16 bit locations. Any attempt to write an odd number of bytes will result in the last byte not being written, but the rest of the data being written correctly.

When using these commands the following must be considered:

- Buffers 1 and 2 share memory with the **Read Tracking Data** command and therefore should not be used if this command is operating. It is the user's responsibility to ensure no conflict of use occurs.
- At reset the buffers are cleared and all previously written contents are lost.
- The buffers are each of a fixed size and if any access to a location outside of the buffer is attempted the command will fail and the data will not be read or written.

Command Group 2: Acquisition and Tracking

Set Centre Frequency
Command Number: 42_{16}
This is an exclusive command that defines the frequency of the ensemble to be received. Interrupts can be generated when an ensemble is acquired or when the SH7490 cannot receive a DAB signal at the specified frequency. If this command is re-issued before the current acquisition has complete the acquisition will restart with the parameters defined in the last command.
Command Data: 5 bytes.

Byte 1:

7	6	5	4	3	2	1	0
MD2	MD1	MD0	CF12	CF11	CF10	CF9	CF8

Byte 2:

7	6	5	4	3	2	1	0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Byte 3:

7	6	5	4	3	2	1	0
BND3	BND2	BND1	BND0	FF11	FF10	FF9	FF8

Byte 4:

7	6	5	4	3	2	1	0
FF7	FF6	FF5	FF4	FF3	FF2	FF1	FF0

Byte 5:

7	6	5	4	3	2	1	0
EI1	EI2	Rfu	Rfu	Rfu	Rfu	Rfu	Rfu

- MD2-0: 3 bit number, transmission mode.
  - 0 0 0: Auto-detect
  - 0 0 1: DAB transmission mode 1
  - 0 1 0: DAB transmission mode 2
  - 0 1 1: DAB transmission mode 3
  - 1 0 0: DAB transmission mode 4
  - Other combinations are not used.
- CF 12-0: 13-bit unsigned integer. Represents the frequency offset in 16 kHz units from the lowest frequency of each band specified by BND3 to 0.
- BND 3-0: Band
  - 0 0 1 1 Band III (174-240 MHz)
  - 1 0 0 0 L-Band (1452-1492 MHz)
  - All others Rfu.
- FF11-0: 12-bit unsigned integer. Fine frequency offset in 4 Hz steps from the coarse frequency defined above.
- EI1: Enable **Acquisition Successful** interrupt when ensemble has been acquired.
- EI2: Enable **Acquisition Failed** interrupt when acquisition fails.

Response Data: None.
Interrupt Data: The **Acquisition Successful** and/or **Acquisition Failed** interrupt can be generated by setting El1 and El2. Even after **Acquisition Failed** interrupt has been generated the acquisition is still trying to be attained should the acquisition then be successfully attained the **Acquisition Successful** interrupt will then be generated. See “Interrupt Indixes”.

Get Centre Frequency
Command Number: 43_{16}
Returns the frequency of the current ensemble. After acquisition, this command returns the centre frequency of the acquired ensemble, taking account of fine frequency modification made in the acquisition process.
Command Data: None.
Response Data: 4 bytes. Same format as the first four bytes of command data of the **Set Centre Frequency** command.

Get Mode
Command Number: 47_{16}
Returns the transmission mode of the DAB signal currently being received.
Command Data: None.
Response Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	Rfu	Rfu	Rfu	MD2	MD1	MD0

- MD2-0: 3-bit number representing the DAB transmission mode in use. If an ensemble has not been acquired this command will return '0'.
  - 0 0 1: DAB transmission mode 1
  - 0 1 0: DAB transmission mode 2
  - 0 1 1: DAB transmission mode 3
  - 1 1 0: DAB transmission mode 4
  - Other combinations are not used.

Get Acquisition and Tracking Status
Command Number: 48_{16}
Requests the status of the ensemble acquisition and tracking.
Command Data: None.
Response Data: 1 byte:

7	6	5	4	3	2	1	0
ACQ	SNP	CFL	FFL	SMTL	FDS	Rfu	Rfu

- ACQ: This is set when the Sh7490 is trying to acquire.
- SNP: This is set when the SH7490 fails to find a DAB signal when acquiring. (1 when not present).
- CFL: Coarse frequency locked is set during acquisition when the carrier frequency known to within one sub-carrier spacing. This bit is always set whilst in tracking mode.
- FFL: Fine frequency locked is set when the SH7490 believes it has locked the frequency to within 5% of the sub-carrier spacing.
- SMTL: This is set when the SH7490 believes that the sample rate is locked within 3ppm of the transmitter sample clock.
- FDS: The bit is set when the SH7490 has decoded any FIC successfully. This is used to indicate that that the acquisition and tracking have achieved sufficiently good demodulation to obtain FIC.

  Only the FFL and SMTL bits are continuous updated during tracking. These bits however do not guarantee to accurately reflect the status of the incoming DAB signal. The SH7490 may believe that it is tracking correctly to a signal even if it has disappeared as it tries to continue to track even when a signal disappears.

Get RSSI

Command Number: 49_{16}

Returns an indication of the received signal strength.

Command Data: None.

Response Data: 1 byte, 8 bit unsigned integer, representing an arbitrary scale where 255 is maximum signal strength and 0 is the minimum. The RSSI figure reflects the value of the AGC signal used by the SH7490 to control the gain of the RF front end. The interpretation of this value is dependent upon the form of the RF front-end design.

Read Tracking Data

Command Number: $4A_{16}$

This command instructs the SH7490 to write tracking parameters to the parallel port. The output information is specified by command data. When the ATH bit is set, the output data type and the data length is prefixed at the start of data. The first byte of the header is 4A16 and the second is the command data from the last instance of this command. The third and fourth bytes of the header form a 16 bit unsigned number that represents the number of bytes to be written, excluding the header. The header should always be prefixed if data set-up using the 85_{16} is being sent to the parallel port when data set-up with the 85_{16} is being sent .

Command Data: 1 byte.

7	6	5	4	3	2	1	0
ENDP	ATH	NULL	PRS	CIR	Rfu	Rfu	SO

- ENDP: Enables tracking information to be continuously written to the parallel port. When set to 0, only the tracking data for the current frame is sent. When set to 1, tracking data is sent for the current and subsequent frames.
- ATH: Add tracking Header.
- NULL: Null symbol. The Null Symbol is a sequence of complex samples that are captured during a Null in the DAB frame. These complex samples are each two 8-bit signed numbers (first the real sample then the imaginary sample). The size of the NULL symbol is mode dependent, see Table 3.
- PRS: Phase referenced symbol. The Phase reference symbol is a sequence of complex samples that are captured in the phase reference symbol of a DAB frame. These complex samples are in the same format as the Null symbol. The size of the phase reference symbol is mode dependent, see Table 3.
- CIR: Channel impulse response. The channel impulse response is written as a sequence of 16 bit unsigned numbers (MS byte first) representing the impulse response calculated by the SH7490. The sample number representing the start of the guard period is mode dependent; see Table 3. The size of the channel impulse response is mode dependent; see Table 3.
- SO: Symbol offset. This is a 16 bit signed number that represents the number of samples by which the SH7490 intends to move the symbol timing window. It is the same format as the command data for the Symbol timing offset in the Write Tracking Parameters command.

Only the selected item(s) is (are) output via the parallel port in the order defined above.

Table 3 Read Tracking Data Field Sizes

Mode	1	2	3	4
Size of NULL (Bytes)	4096	1024	512	2048
Size of PRS (Bytes)	4096	1024	512	2048
Size of CIR (Bytes)	2048	512	256	1024
Start of guard period in CIR (samples)	256	64	32	128

Response Data: None.

Write Tracking Parameters
Command Number: $4B_{16}$
Allows an external controller to select the symbol timing window position by making the essential control parameters accessible.
Command Data: 3 bytes, Control byte and a 16-bit value.

Byte 1:

7	6	5	4	3	2	1	0
Rfu	Rfu	Rfu	Rfu	Rfu	Rfu	Rfu	STO

Byte 2:

7	6	5	4	3	2	1	0
SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8

Byte 3:

7	6	5	4	3	2	1	0
SC7	SC6	SC5	SC4	SC3	Sc2	SC1	SC0

- STO: Symbol timing offset valid bit.
- SC15-0: A 16 bit signed integer that controls the symbol timing offset, only valid when the STO bit is set. This command instructs the SH7490 to shift its symbol timing window by SC samples. A positive value of SC delays the symbol timing window and a negative value advances it. Once STO has been set to 1 by the external controller, the SH7490 will ignore its own calculated value of SC until STO is cleared (either by reset or by a **Write Tracking Parameters** command).

Response Data: None

Command Group 3: FIC/PAD Access

These commands allow the controller to identify types of FIG and PAD data as interesting and read the stored data. The interesting FIG and PAD data is stored in cyclic buffers. Data is stored in the order it is received. When the buffer becomes full, the oldest data is overwritten. The length of time it takes to wrap around the buffer is dependent upon the size of the buffer and rate at which interesting data is received.

To efficiently use a buffer to the maximum extent, the controller should select the data it requires (using the **Set Set Interesting FIGs** or **Interesting X-PAD Apps** commands). The FIC and X-PAD buffers are each 2 Kbytes long and the F-PAD buffer is 40 F-PADs long. All three buffers are circular. If they overflow, the oldest data in the buffer is removed to make way for new data.

Set Interesting FIGs
Command Number: 60_{16}
This command defines the FIGs to be buffered in the FIC buffer. The extension is specified by the mask byte and the match byte for each FIG type indicated by FT0 to FT2. Each FIG type has an independent list of mask and match bytes that can contain up to 127 pairs.

Received FIG data is processed using the list of mask and match bytes corresponding to its FIG type. The mask/match bytes are compared with the first byte in the FIG data field which carries the extension field and other bits. This byte is referred to as EXT. For each mask/match pair in the list, the SH7490 compares (EXT & mask) with match, and the FIG is stored in the FIC buffer if (EXT & mask) == match. To buffer all FIGs of a given type, set a mask/match pair to 0/0, to disable all FIGs of a given type, set a mask/match pair to $0/ff_{16}$.

The list of mask and match bytes (for a given FIG type) is overwritten by a new **Set Interesting FIGs** command for that FIG type. Upon reset the SH7490 considers all type 0 FIGs to be of interest.
Command Data: 1 + 2n byte: Byte 1:

7	6	5	4	3	2	1	0
Rfu	Rfu	Rfu	Rfu	Rfu	FT2	FT1	FT0

- FT2-0: FIG type (0-7)
- Followed by pairs of mask and match bytes defining the interesting FIGs.

Response Data: None.

Get FIG Data
Command Number: 61_{16}
Reads next FIG from the FIC buffer. This command accesses the next interesting FIGs, the interesting FIGs are specified by the Set Interesting FIG command.
Command Data: None.
Response Data: Up to 30 bytes of FIG data are returned. If no interesting FIGs are stored within the FIC buffer, no data is present in the response.

Get F-PAD

Command Number: 62_{16}

Reads the F-PAD data from the defined channel. A circular buffer is holding up to one second of F-PAD data, the next available F-PAD from this buffer is returned by this command. Note that PAD data can only be extracted from the audio channel that is configured to MPEG decoded. A command error will result if any PAD data is requested from a channel that is not configured to be MPEG decoded.

Command Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Response Data: 2 bytes of F-PAD (Byte L, followed by Byte L-1), or no data if the buffer is empty.

Set Interesting X-PAD Apps

Command Number: 63_{16}

This command defines the X-PAD Application Types to be stored in the X-PAD buffer for the controller to later read. Any number and type of X-PAD applications can be selected. At reset no X-PAD Application Types are defined as interesting. Note that PAD data can only be extracted from the audio channel that is configured to be MPEG decoded. A command error will result if any PAD data is requested from a channel that is not configured to be MPEG decoded.

Command Data: 2 bytes:

Byte 1:

7	6	5	4	3	2	1	0
EXT	AR	CH5	CH4	CH3	CH2	CH1	CH0

- EXT: Extension flag, defines interpretation of the second byte
- AR: Add or Remove the application type (this bit should be 1 for adding an Application Type)
- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Byte 2: Application type, AT7-0.
Extension flag clear: 8 bit number, application types 0-255, i.e. application type = AT7-0.
Extension flag set: 8 bit number, application types 31-286, i.e. application type = 31 + AT7-0

Response Data: None.

Get X-PAD

Command Number: 64_{16}

This command reads X-PAD data from the X-PAD buffer. For the specified channel, the oldest X-PAD data from the buffered interesting application is extracted. The **Set Interesting X-PAD Apps command** defines the interesting application on a channel to be buffered. Note that PAD data can only be extracted from the audio channel that is configured to be MPEG decoded. A command error will result if any PAD data is requested from a channel that is not configured to be MPEG decoded.

Command Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Response Data:

The first two bytes define the content indicator from the X-PAD to be returned and a 9-bit Application Type. Remaining bytes are X-PAD data of one MPEG frame.

Byte 1:

7	6	5	4	3	2	1	0
CI	XI1	XI0	OV	Rfu	Rfu	Rfu	AP8

Byte 2:

7	6	5	4	3	2	1	0
AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0

- CI: Contents indicator, also used to signal start of an X-PAD data group.
- XI1-0: X-PAD Indicator
  - 0 0 Rfu
  - 0 1 Short X-PAD
  - 1 0 Variable size X-PAD
  - 1 1 Rfu
- OV: Overflow, used to signal that the X-PAD data buffer has overflowed
- AP8-0: Application Type of X-PAD data to be returned

Get Music / Speech Flags

Command Number: 65_{16}

Returns the status of the music/speech flags for the specified channel. Note that the music/speech flags can only be extracted from the audio channel that is configured to be MPEG decoded. A command error will result if these flags are requested from a channel that is not configured to be MPEG decoded.

Command Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Response Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	Rfu	Rfu	Rfu	Rfu	MS1	MS0

- MS1-0: Music / Speech flags as defined in Section 7.4.1 of ETS 300 401 standard [1]
  - 0 0 Music / Speech flags is not signalled
  - 0 1 Music
  - 1 0 Speech
  - 1 1 Undefined

Get ISRC_UPC Code

Command Number: 66_{16}

Returns the ISRC or UPC code from the specified channel. Note that the ISRC/UPC code can only be extracted from the audio channel that is configured to be MPEG decoded. A command error will result if these codes are requested from a channel that is not configured to be MPEG decoded.

Command Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Response Data: 16 bytes:

Byte 1:

7	6	5	4	3	2	1	0
Rfu	Rfu	Rfu	Rfu	Rfu	Rfu	ISRC	UPC

- ISRC: If this bit is set an ISRC code has been received since the last action of this command the code present in the following bytes is valid.
- UPC: If this bit is set an UPC code has been received since the last action of this command and the code present in the final bytes of this response is valid.

Note: These bits are reset upon the selection of a service.

Byte 2 - 9: 58 bits of ISRC code, right justified, unused bits are set to zero.
Byte 10 - 16: 52 bits of UPC code, right justified, unused bits are set to zero.

Get TII
Command Number: 67_{16}
Returns the TII main, and sub-identifiers and field strengths found in the last processed Null Symbol, which contained TII.
Command Data: None.
Response Data: 1 + 2n bytes: One byte for the number of transmitters (n: integer in the range between 1 and 24) and each two bytes for TII information on each found transmitter

Byte 1:

7	6	5	4	3	2	1	0
NSI	Rfu	NRT4	NRT4	NRT3	NRT2	NRT1	NRT0

Byte 2:

7	6	5	4	3	2	1	0
MI6	MI5	MI4	MI3	MI2	MI1	MI0	SI4

Byte 3:

7	6	5	4	3	2	1	0
SI3	SI2	SI1	SI0	FS2	FS1	FS0	Rfu

If two or more transmitters are found, the format of the 4th and the following bytes is the same as that of the second and the third bytes.

- NSI: Null Symbol Indicator, this flag will be set when this command returns the data processed from an individual null symbol for the first time.
- NRT4-0: Number of TIIs in response data
- MI6-0: Main-Identifier, pattern (0-69)
- SI4-0: Sub-Identifier, comb (0-23)
- FS2-0: Field strength, an indicator of the relative strength of the transmitter (Format defined in section 4.6.1 of ETS 300 401 standard [2])

Clear FIG Data

Command Number: $6a_{16}$
Clears the FIC buffer of all stored FIGs.
Command Data: None.
Response Data: None.

Clear PAD Data

Command Number: $6b_{16}$
Clears the X-PAD and F-PAD buffers. All X-PAD data and F-PAD data are discarded. Note that PAD data can only be extracted from the audio channel that is configured to be MPEG decoded. A command error will result if any PAD data is requested from a channel that is not configured to be MPEG decoded.
Command Data: 1 byte.

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid.

Response Data: None.

Command Group 4: Channel Control / Status

Move to Next Audio Service
Command Number: 80_{16}
This is an exclusive command that de-selects the current audio service and selects the next primary audio service in the same ensemble. Control for audio output and MPEG decoding will not be changed even if this command is executed. This command just selects an audio service. This commands operates on channel number 0 and should only be used if the Channel 0 has been select using Service Identifier and Service Component Description.
Command Data: None.
Response Data: None.
Interrupt Data: Two Channel Selection Complete Interrupts are generated. First one is generated when completing the channel de-selection and latter one is generated when completing the channel selection of the next audio service.

Set Channel Selection

Command Number: 81_{16}

This is an exclusive command that selects a sub-channel to be decoded by the SH7490. The sub-channel may be selected by either the service identifier and service component description or by the sub-channel identifier. Channel selection with service identifier and service component description is only valid for stream audio and stream data sub-channels. If a sub-channel is currently selected for a given channel it must first be deselected (FM=11) before selecting a new sub-channel. Selection of a packet data sub-channel can only be made with a sub-channel identifier. At any time a given sub-channel should not be assigned to both channel 0 and 1. A Channel Selection Complete Interrupt is generated when the command has completed processing. If the decodable capacity exceeds its limitation, priority is given to lower numbered channels, i.e. channel 0 has priority over channel 1. This channel will be deselected if the requested sub-channels exceed the maximum decodable capacity. All decoded channels are transmitted from the RDI.

Command Data:

7	6	5	4	3	2	1	0
FM1	FM0	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number used by other CIP commands to identify the decoded sub-channel (the capacity of the SH7490 is limited to two sub-channels, only channels 0 and 1 are valid.)
- FM1-0: Format of selection.
  - — 0 0

    A sub-channel to be decoded is specified by Service Identifier and Service Component Description.

    Second and third bytes: Service Component description

    Fourth and the following bytes: Service Identifier (16 or 32 bits)

    This specification is defined in section 6.3.1 of [1]
  - — 0 1

    A sub-channel to be decoded is specified by Sub Channel Identifier.

Byte 2:

7	6	5	4	3	2	1	0
Rfu	Rfu	SC5	SC4	SC3	SC2	SC1	SC0

- SC5-0: 6-bit sub-channel identifier as defined in Section 6.2 of [1].
  - — 1 0 Rfu. Not supported.
  - — 1 1 Cancels the selection of the subchannel that is identified by CH5 to CH0.

    There is no additional byte.

Response Data: None:

Interrupt Data: A Channel Selection Complete Interrupt is generated when completing the channel selection.

Get Channel Selection

Command Number: 82_{16}

Returns selection information on the channel being decoded.

Command Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Response Data: Returns the command data for the **Set Channel Selection** command on the specified channel.

Get BER Estimate

Command Number: 83_{16}

Returns an estimate of the bit error rate (BER) of the specified channel.

Command Data: 1 byte

7	6	5	4	3	2	1	0
FIC	MIE	CH5	CH4	CH3	CH2	CH1	CH0

- FIC: When bit set to 1. CH5-0 are ignored the number of CRC failures in the FIC and the corrected errors in the FIC from the Viterbi are returned. The returned values relate to the FIC data for the previous CIF and not the whole FIC.

  When bit set to 0. The number of CRC failures in the MSC and the corrected errors from the Viterbi for channels selected by CH5-0 are returned. The returned values relate to the MSC data for the previous CIF.

  When BER is being used to evaluate signal quality assessment it is recommended that the BER estimate for the FIC is used. The BER estimate in the MSC may vary with protection profile, bit rate and start CU.
- MIE: MPEG interrupt enable. When this bit is set, the MPEG Errors Interrupt is enabled. This bit is completely independent of the value of the channel number or state of the FIC bit
- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Response Data: 11 bytes:
Bytes 1 and 2: Error estimate from Viterbi decoder. The number of errors corrected in the previous CIF is indicated by 16-bit number, and errors are counted that are corrected by Viterbi output re-coding and compared with Viterbi input This specification conforms to the definition in Section 4.4 in RDI Specifications [2].

Byte 3: Count of CRC failures in the last CIF processed on the given channel. CRC checks are performed upon each FIB in the FIC and upon the header and scale factors of the MPEG decoded channel in the MSC. When the FIC bit is set only the number CRC failures in the FIBs in the previous CIF are returned. When the bit is 0 only the CRC failures in the MSC are returned.

Bytes 4 and 5: A 16 bit number(n) defining the number of CIFs used to produce the accumulated error estimate from the Viterbi decoder (bytes 6-9) and the accumulated CRC failures (bytes 10-11).

Bytes 6 - 9: Accumulated error estimate from Viterbi decoder. A 32-bit number representing the number of corrected errors in the last n CIFs.

Bytes 10 - 11: Accumulated CRC failures. A 16-bit number representing the total number of failed CRC checks in the last n CIFs.

The accumulated CRC and BER counts for each channel are independently reset. The reset for a given channel occurs either when a Get BER command is issued for the given channel or when the number of CIFs since the last BER command for a given channel has reached 12500.

Get Channel Decode Status
Command Number: 84_{16}
Returns the decode status of the specified channel. The channel is specified with a 6-bit channel number that is assigned by the **Set Channel Selection** command.
Command Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid

Response Data: 1 byte:

7	6	5	4	3	2	1	0
SCE	CS1	CS0	Rfu	Rfu	TDF	MDP	Rfu

- SCE: Service Component Exists. This will return 0 if the selected service component is not present in the multiplex or if no service has been selected.
- CS1-0: Channel size-
  - 0 0 OK
  - 0 1 Too large for time de-interleave buffer
  - 1 0 Too large for Viterbi decoder
  - 1 1 Too large for symbol decoding
- TDF: Time de-interleave buffer full. Viterbi decoding of MSC data is executed when the time de-interleave buffer becomes full of valid data of the selected sub-channel. When the channel is first selected, the time de-interleave buffer is empty; 16 CIFs of data are required to fill the buffer.
- MDP: MPEG decoding being performed successfully.

Set Parallel Output

Command Number: 85_{16}

This command directs the defined channels to the parallel port for external processing. The data sent to the parallel port is grouped into segments, each of which contains the data received in one CIF. Each segment may be prefixed with a 4-byte header when the AHD bit is 1. The first byte of the header is 85_{16} and the second byte is the channel being transferred (the second byte has the same format as the first byte of the command data). The third and fourth bytes of the header form a 16 bit unsigned number that represents the number of bytes in this transfer excluding the header.

Command Number: 2 bytes

Byte 1:

7	6	5	4	3	2	1	0
FIC	Rfu	CH5	CH4	CH3	CH2	CH1	CH0

Byte 2:

7	6	5	4	3	2	1	0
ADH	EN	Rfu	Rfu	Rfu	Rfu	Rfu	Rfu

- FIC: If this bit is set, CH5-0 are ignored and FIC is written to the parallel port.
- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid.
- ADH: Add Data Header. This bit adds a header to the data written to the parallel port.
- EN: If this bit is set, the defined channel is written to the parallel port. If this bit is cleared, the defined channel is no longer written parallel port. All output channels are disabled after acquisition of an ensemble.

Response Data: None.

Command Group 5: Audio Control / Status

Select External Digital Audio
Command Number: $A0_{16}$
Allows the Digital Audio Output Interface to output the data driving the Digital Audio Input Interface. Digital volume control is applied to this data, but DRC is disabled. This function allows the Digital Audio Output Interface that can drive a DAC directly to source its data from outside the SH7490. This command overrides any MPEG output defined as active and is itself overridden if, later, a channel is defined to be MPEG decoded.

Command Data: 1 byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	Rfu	Rfu	Rfu	Rfu	Rfu	DAS

- DAS: Digital Audio Select. When this bit is set to 1, the digital audio is sourced from the external digital audio input. Otherwise, the digital audio is sourced from the MPEG decoder defined as active.

Response Data: None:

Set DRC
Command Number: $A1_{16}$
Specifies the amount of the DRC from F-PAD is to be applied to the audio data available on the Digital Audio Output Interface. The 6-bit DRC value (DF) obtained from F-PAD is converted into the 6-bit control value (DA) by the expressions below (1) and (2), and is then applied to the audio signal. Units of DF and DA are 0.25 dB.
Command Data: 1 byte:

7	6	5	4	3	2	1	0
ED	Rfu	DRC5	DRC4	DRC3	DRC2	DRC1	DRC0

- ED: Enables DRC.
- DRC5-0: Unsigned integer (DRC) representing the level of DRC to be applied.
  If (ED == 1) DA = DF * (DRC+1) / 64 (1)
  If (ED == 0) DA = 0 (2)

Response Data: None

Get DRC Setting
Command Number: $A2_{16}$
Returns the DRC value that was set with the **Set DRC** command.
Command Data: None.
Response Data: 1 byte, in the same format as for the command data of the Set DRC command.

Set Volume Control
Command Number: $A3_{16}$
Defines the digital volume control setting.
Command Data: 1 byte, an 8 bit unsigned integer (V) representing the attenuation to be applied in half dB steps. The actual attenuation applied is the combination of this value and the gain defined by the DRC setting.
Gain of Volume Control = 0.25 * DA – 0.5 * V dB. Where DA is the value as defined by Set DRC command.
Response Data: None

Get Volume Control
Command Number: $A4_{16}$
Returns the current digital volume control setting.
Command Data: None.
Response Data: 1 byte, in the same format as for the command data of the Set Volume Control command.

Set MPEG Control
Command Number: $A5_{16}$
Sets the MPEG decoding of the specified channel. Note that only one channel can be MPEG decoded at a time. A command to select another channel for MPEG decoding will override the previously selected channel. To avoid any interruptions in the audio output stream MPEG selection should be made before the Set Channel Selection command is issued to select the audio channel.
Command Data: 1 byte:

7	6	5	4	3	2	1	0
MC1	MC0	CH5	CH4	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid.
- MC1-0 MPEG Control bits
  - 0 0 No MPEG decoding (no data output from External MPEG Output port)
  - 0 1 Stream sent to MPEG Output Port after pre-processing
  - 1 1 Internal MPEG used (audio data sent to Audio Interface Port)
  - 1 0 Stream sent to external MPEG port without any pre-processing

  The pre-processing option performs the following on the output bit stream.
  Re-framing for LSF
  Check header and CRCs
  Pad extraction
  Error concealment

Response Data: None

Get MPEG Status
Command Number: $A6_{16}$
Requests the status of the MPEG decoder for the specified channel.
Command Data: 1 byte:

First byte:

7	6	5	4	3	2	1	0
Rfu	Rfu	CH5	CH	CH3	CH2	CH1	CH0

- CH5-0: 6-bit channel number. Only channel numbers 0 and 1 are valid.

Response Data: 1 byte:

7	6	5	4	3	2	1	0
MC1	MC0	LSF	Rfu	Rfu	Rfu	MD1	MD0

- MC1-0 MPEG Control bits
  - 0 0 No MPEG decoding (no data output from External MPEG Output port)
  - 0 1 Stream sent to MPEG Output Port after pre-processing
  - 1 1 Internal MPEG used (audio data sent to Audio Interface Port)
  - 1 0 Stream sent to external MPEG port without any pre-processing
- LSF: Low Sampling Frequency. This bit is set if the channel being decoded is LSF.
- MD1-0: MPEG Mode of the decoded audio channel.
  - 0 0 Stereo.
  - 0 1 Joint Stereo.
  - 1 0 Dual Channel.
  - 1 1 Single Channel.

Interrupt Indixes

Channel Selection Complete 80_{16}
This interrupt is generated on completion of the **Set Channel Selection** command when channel selection processing is complete. The possible outcomes of the channel selection are: sub-channel found, decoding; sub-channel found, but cannot decode or sub-channel not found. These states are signalled in the channel decode status in the interrupt data.
Interrupt Data: 2 bytes consisting of 1 byte for a channel number and 1 byte for the channel decode status. The format of the channel decode status is the same as that of response data of the **Get Channel Decode Status** command.

Acquisition Successful 82_{16}
This interrupt is generated on the completion of the command **Set Centre Frequency** when the SH7490 has successfully acquired a DAB signal. This interrupt signals that carrier frequency lock as been made to within one sub-carrier and sample rate is either acceptable or locked previously. Only if the EI1 bit was set in the command data of the **Set Centre Frequency** will this interrupt be generated.
Interrupt Data: 1 byte, in the same format as response data of the **Get Acquisition and Tracking Status** command.

Receiver has Reset 84_{16}
This interrupt is generated when execution of the **Reset** command completes or when the SH7490 enters an invalid state where it can only recover by resetting.
Interrupt Data: None

Tracking Lost 85_{16}
This interrupt is generated when the channel impulse response of the DAB signal being received degrades to the point where reliable tracking is no longer possible.
Interrupt Data: None

Service Lost 86$_{16}$
This interrupt is generated when as a result of a multiplex reconfiguration one of the services being decoded is deselected. The can either be due to the service being removed from the multiplex or the services bit-rate or protection profile has changed so it is no longer within the decoding capacity of the SH7490 (see “Decoding Capacity”).
Interrupt Data: 1 byte, channel number of the lost service.

Multiplex Reconfiguration has occurred 87$_{16}$
This interrupt signals that a multiplex reconfiguration has just been performed.
Interrupt Data: None

Coarse Frequency Jump 88$_{16}$
This interrupt is generated when the SH7490 needs to change the carrier frequency by an amount greater than the digital AFC alone. This is common during acquisition, but very rare during tracking. The digital AFC is adjusted by a maximum of +/-8kHz during acquisition and +/-16kHz during tracking before this interrupt is issued.
Interrupt Data: 1 byte, 8 bit signed integer, representing the frequency change in a 16kHz units

Acquisition Failed 89$_{16}$
This interrupt is generated on the completion of the exclusive command **Set Centre Frequency** when the SH7490 does not believe that a DAB signal is present at the requested frequency. Only if the EI2 bit was set in the commands data, will this interrupt be generated.
Interrupt Data: 1 byte, the same format as the response of **Get Acquisition / Tracking Status** command.

MPEG Errors 8A$_{16}$
This interrupt is generated when errors are detected by either the header CRC or scale factor CRCs in the channel being MPEG decoded. When the MIE bit in **Get BER** command is set, will this interrupt be generated.
Interrupt Data: 11 bytes, in the same format the same as the response data for the **Get BER Estimate** command.

Status Mask Interrupt FF$_{16}$
This interrupt is generated when one of the bits in the status byte, specified by the **Set Interrupt Mask** command, goes high.
Interrupt Data: None, status byte carries all required data.

Electrical and Mechanical Data

Electrical Data

Absolute Maximum Ratings

This data is currently unavailable.

Recommended DC Operating Condition

This data is currently unavailable.

DC Characteristics

This data is currently unavailable.

AC Characteristics

This data is currently unavailable.

Mechanical Data

This data is currently unavailable.

References and Abbreviations

List of Abbreviations

The following abbreviations are used throughout this document -

A/D	Analogue-to-Digital
CIF	Common Interleaved Frame
CIP	Controller Interface Protocol
CRC	Cyclic Redundancy Check
CU	Capacity Unit
D/A	Digital-to-Analogue
DAB	Digital Audio Broadcasting
DRC	Dynamic Range Control
ECP	Extended Capability Port
ETS	European Telecommunication Standard
ETSI	European Telecommunications Standards Institute
F-PAD	Fixed Programme Associated Data
FIB	Fast Information Block
FIC	Fast Information Channel
FIDC	Fast Information Data Channel
FIG	Fast Information Group
FIGm/n	Fast Information Group type m, extension n
ISRC	International Standard Recording Code
Lsb	Least significant bit
LSB	Least Significant Byte
MCI	Multiplex Configuration Information
MPEG	Moving Pictures Expert Group
Msb	Most significant bit
MSB	Most Significant Byte
MSC	Main Service Channel
MSPS	Million Samples Per Second
PAD	Programme Associated Data
RDI	Receiver Data Interface
Rfu	Reserved for future use
RSSI	Received Signal Strength Indicator
TII	Transmitter Identification Information
UEP	Unequal Error Protection
UPC	Universal Product Code
X-PAD	Extended Programme Associated Data.

References

[1] ETS 300 401 *Radio broadcast systems; Digital Audio Broadcasting (DAB) to mobile, portable and fixed receivers, revised version, June 96.*

[2] Eureka Project 147 – *Specification of the Receiver Data Interface (RDI) Issue 1.4, November 1996.*

Appendix A External Synthesisers

This section descries an external synthesiser circuit suitable for direct programming by the SH7490.

The block diagrams show the expected registers to be programmed. This section does not intend to describe existing components in detail.

Two suitable devices which can be directly programmed by the SH7490 are LMX1511 and LMX2331, both by National Semiconductor.

Block diagram illustrating expected outline function of the tuning synthesiser
(LMX1511 or compatible)

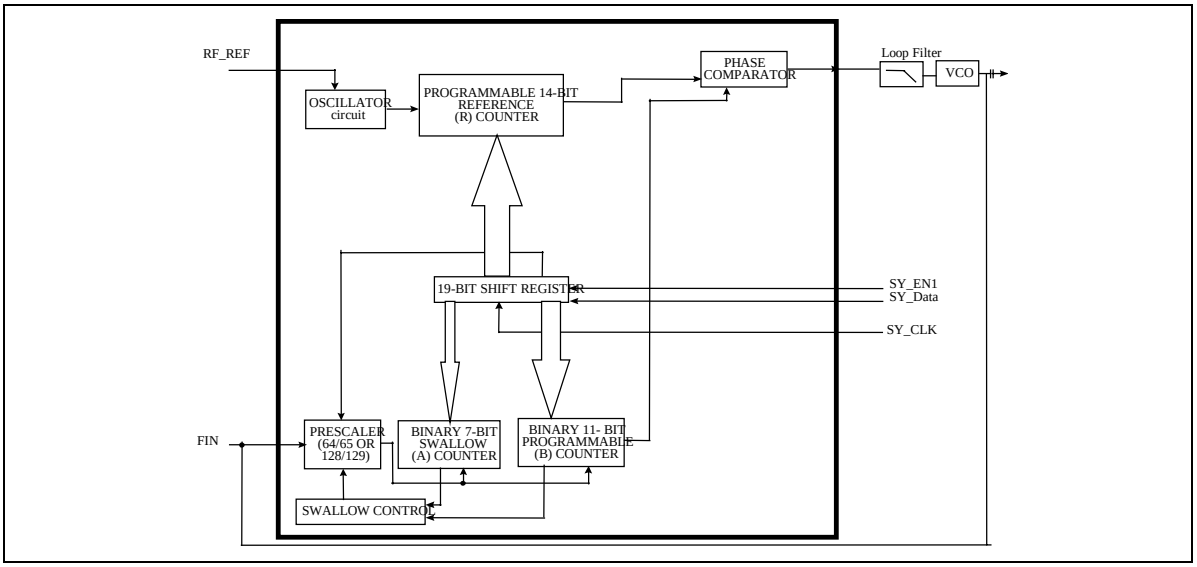


Figure 22

SY_EN1, SY_DATA and SY_CLK signals are provided from SH7490 (see “Synthesiser Control”).

RF_REF frequency is 16.384MHz (see “System Clocks and Reset”) FIN : feedback input for VCO output.

Programmable reference divider (R counter) and prescaler select

If the Control Bit (LSB) is HIGH, data is transferred from the 19-bit shift register to the 14-bit R Counter and prescaler (S15, which sets the prescaler: 64/65 or 128/129). The serial data format is shown in Figure 23 below.

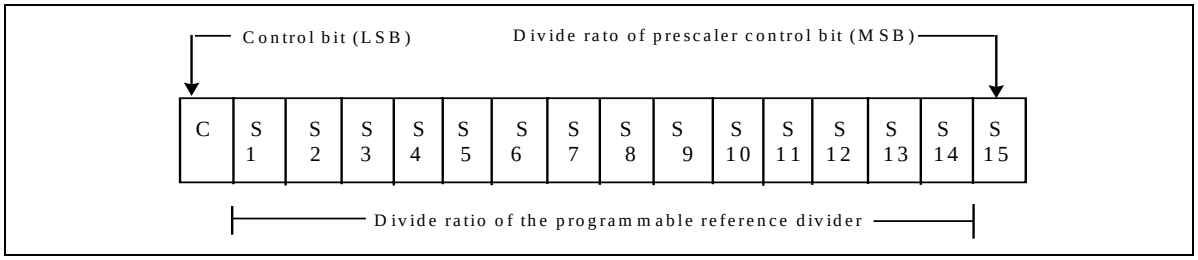


Figure 23 Serial Data Format

Programmable divider

The N counter consists of a 7-bit swallow counter (A counter) and an 11-bit programmable counter (B counter). If the Control Bit (last bit shifted into the Data Register) is LOW, data is transferred from the 19-bit shift register to set the swallow (A) and programmable (B) counter. The serial data format is shown in Figure 24 below.

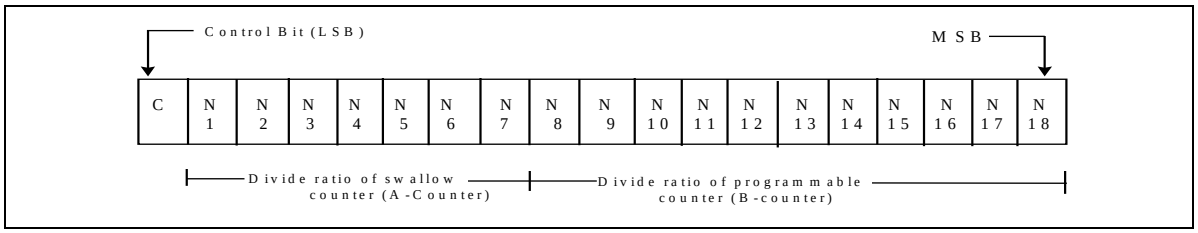


Figure 24 Serial Data Format for Setting A/B Counters

Block diagram of the dual synthesiser (LMX2331 or compatible):

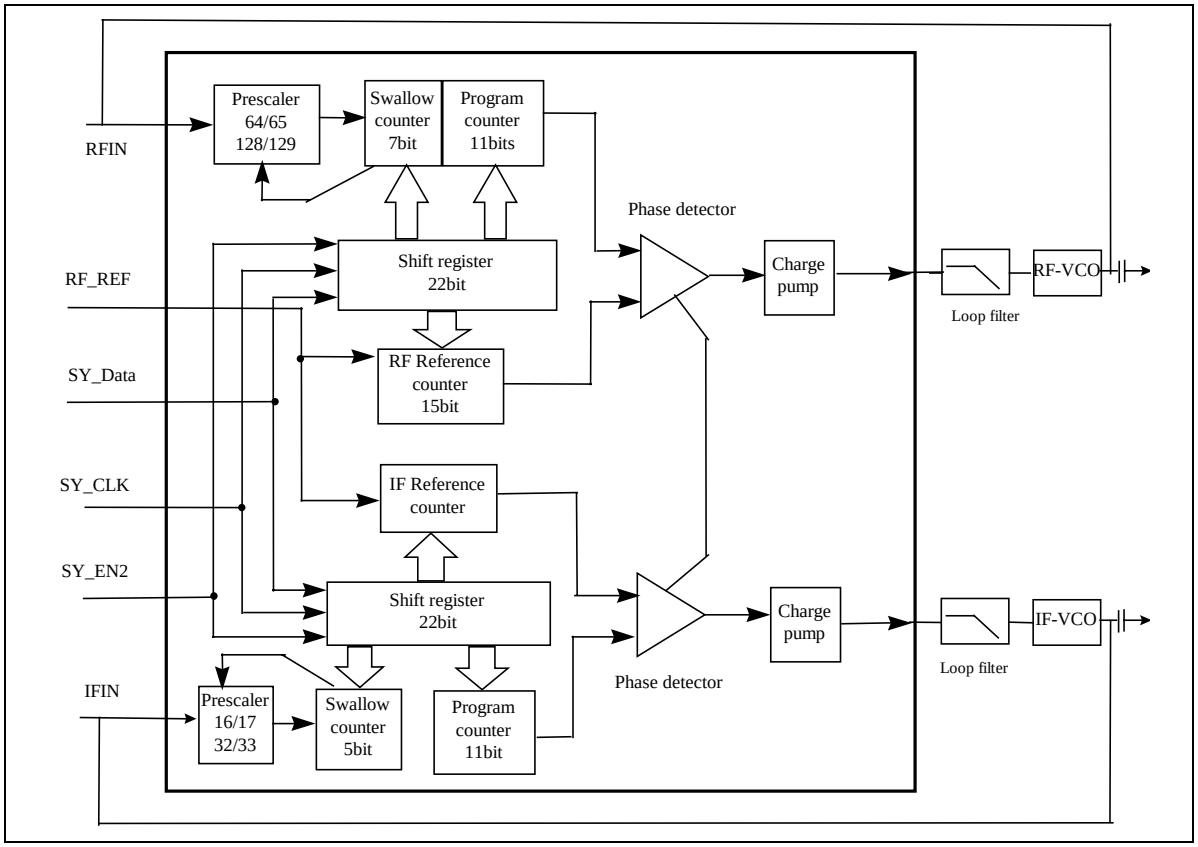


Figure 25

SY_EN2, SY_DATA and SY_CLK signals are provided from SH7490 (see “Synthesiser Control”).

RF_REF frequency is 16.384MHz (see “System Clocks and Reset”) .RFIN : VCO output connection for the RF VCO. IFIN : VCO output connection for the IF VCO.

Register setting and operation modes:

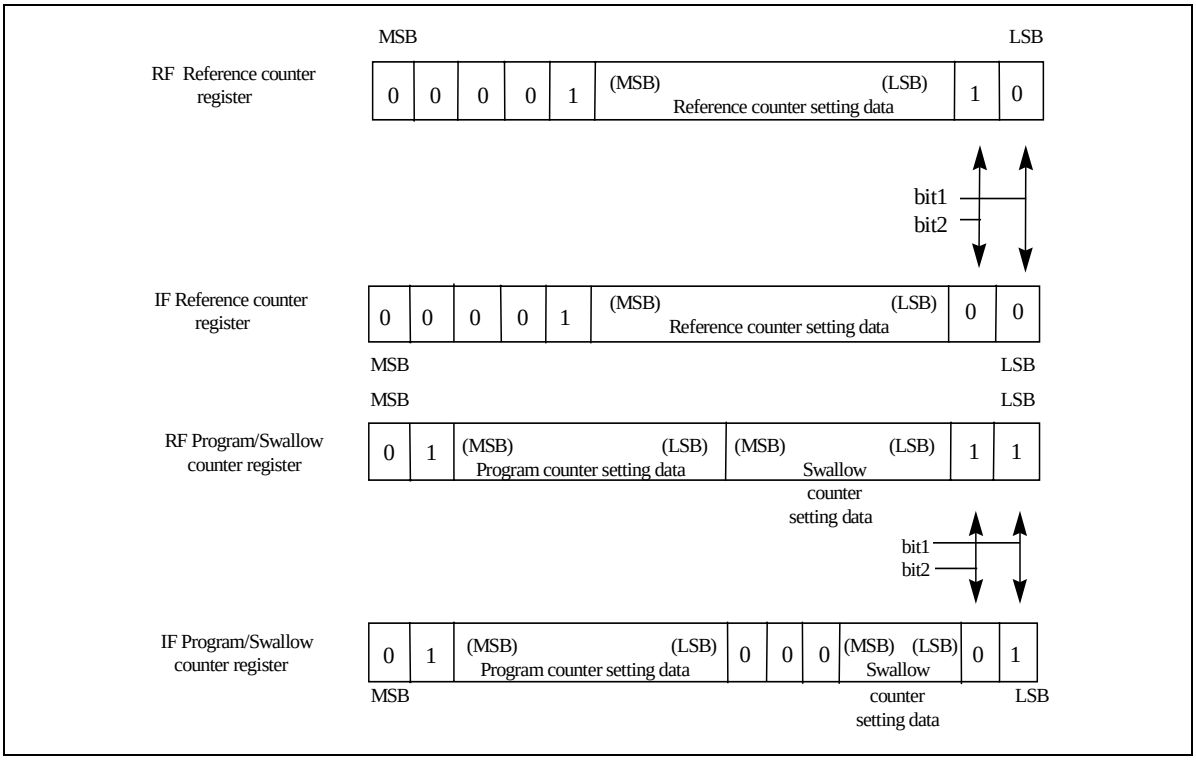


Figure 26 Register Settings

Control bit function:

bit1 (LSB)	bit2	Register
H	L	IF Program/Swallow counter
L	L	IF Reference counter
H	H	RF Program/Swallow counter
L	H	RF Reference counter

VCO frequency calculation formula (Program/swallow function):

Fvco=((PxB)+A)x Fosc/R

Fvco: Output frequency of external VCO
B: Divide ratio of Program counter
A: Divide ratio of Swallow counter
Fosc: Output frequency of external reference frequency oscillator
R: Divide ratio of reference counter
P: Divide ratio of prescaler

Appendix B Decoding Capability

This table defines the decoding capacity of the SH7490 using external and internal MPEG decoding for a given bit rate and protection profile.

	Internal MPEG					External MPEG				
	PL1	PL2	PL3	PL4	PL5	PL1	PL2	PL3	PL4	PL5
32Kbps										
48Kbps										
56Kbps										
64Kbps										
80Kbps										
96Kbps										
112Kbps										
128Kbps										
160Kbps										
192Kbps										
224Kbps										
256Kbps										
320Kbps										
384Kbps										

Key

	Decodable
	Not decodable
	Not valid combination in ETS specification

Appendix C External Dimensions

Figure 27 shows the external dimensions of the SH7490 (FP-176).

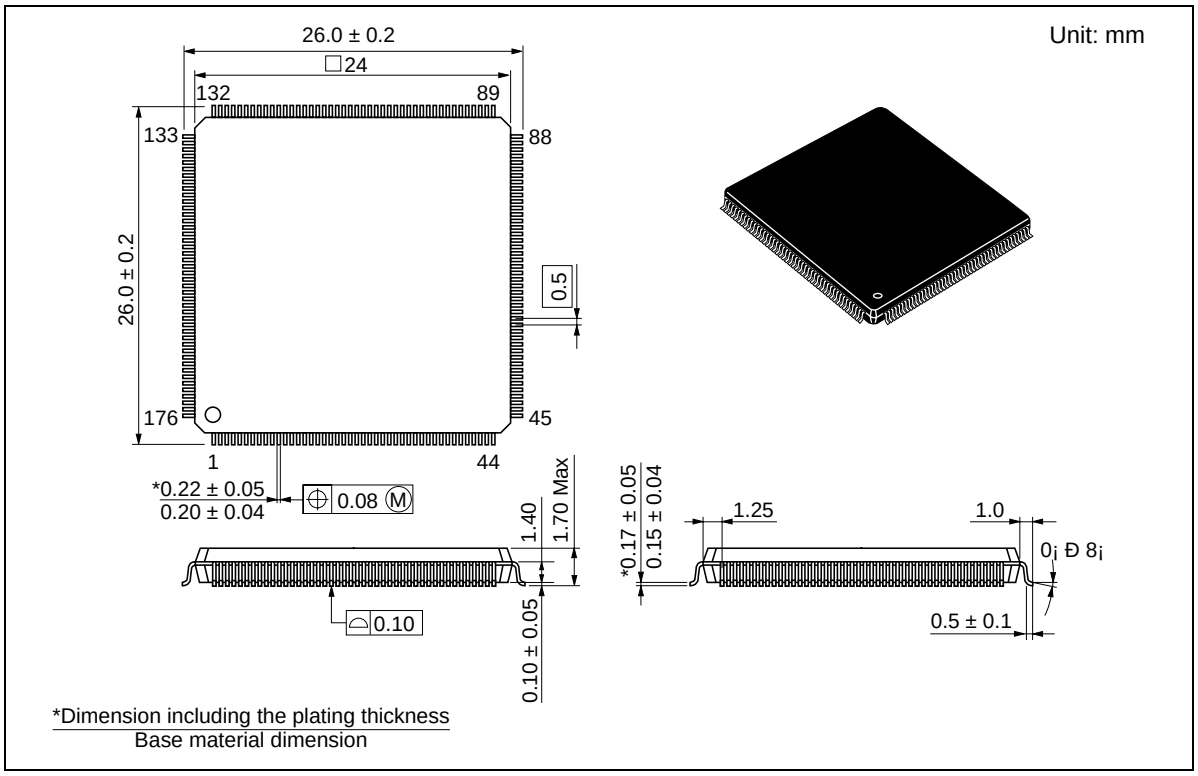
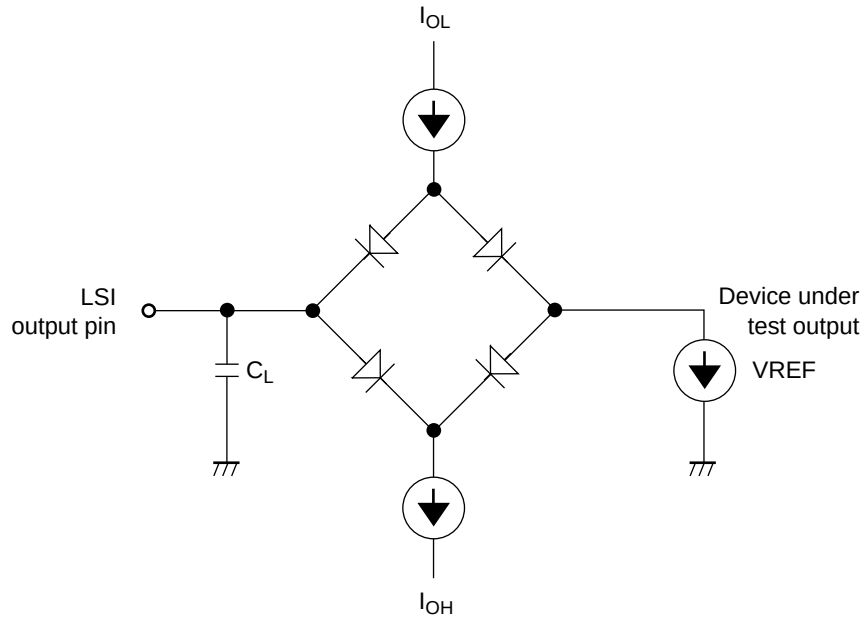


Figure 27 Extenal Dimensions

Appendix D Output Load Circuit



Note: 1. C_L is the total capacitance including the measurement equipment, etc., and is established as follows for each pin:
30 pF: CLK, A23–A0 BS, RD, WE3–WE0, CAS3–CAS0, DACK1, DACK0
50 pF: All pins other than the above.

Figure 28 Output Load Circuit

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