HD66410

(RAM-Provided 128-Channel Driver for Dot-Matrix Graphic LCD)

HITACHI

ADE-207-298(Z)
'99.9
Rev. 0.0

Description

The HD66410 drives and controls a dot-matrix graphic LCD using a bit-mapped display method. It provides a highly flexible display through its on-chip display RAM, in which each bit of data can be used to turn on or off one dot on the LCD panel.

A single HD66410 can display a maximum of 128 × 33 dots using its powerful display control functions. It features 24-channel annunciator output operating with 1/3 duty cycle that is available even during standby modes, which makes it suitable for time and other mark indications.

An MPU can access the HD66410 at any time because the MPU operations are asynchronous with the HD66410's system clock and display operations.

Its low-voltage operation at minimum 2.2V and the standby function provides low power-dissipation, making the HD66410 suitable for small portable device applications.

Features

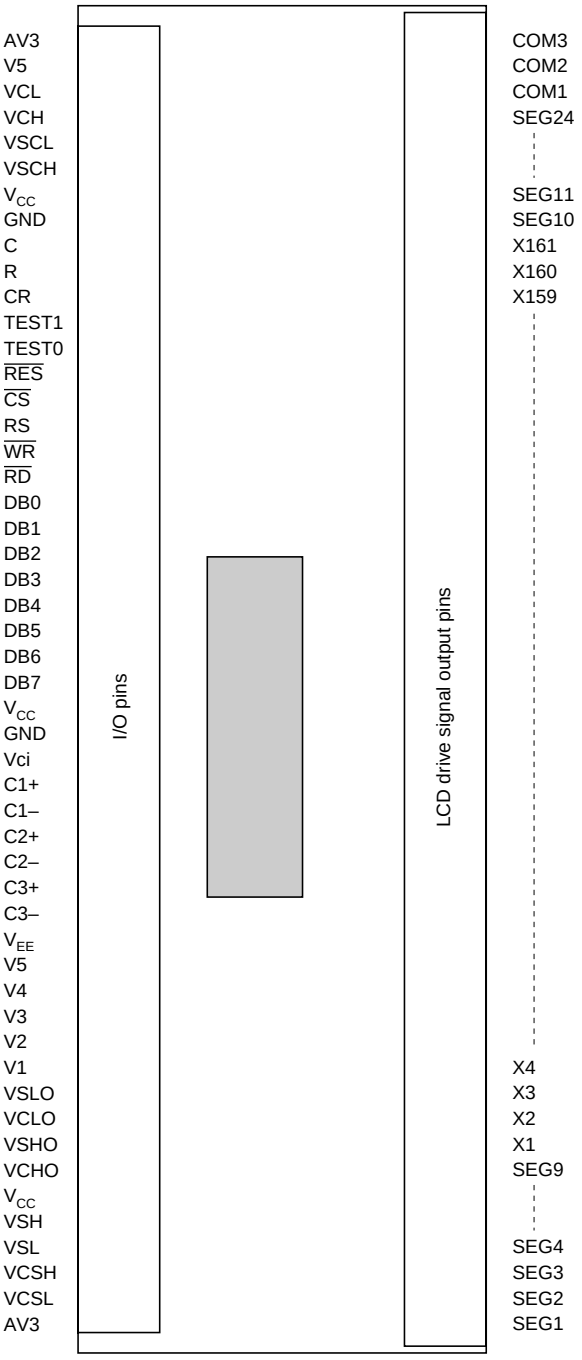
- 4.2-kbits (128 × 33-bit) bit-mapped display RAM
- 128 × 33 dots displayed using a single HD66410
  - — 8 characters × 2 lines (16 × 16-dot character)
  - — 21 characters × 4 lines (6 × 8-dot character)
- Annunciator display using dedicated output channels
  - — Maximum of 72 segments displayed with 1/3 duty cycle
  - — Available even during standby modes

- Flexible LCD driver configuration
  - — Row output from both sides of an LCD panel
  - — Row output from one side of an LCD panel
- Low power-dissipation suitable for long battery-based operation
  - — Voltage operation: 2.2 to 5.5V
  - — Two standby modes: modes with and without annunciator display
- On-chip double to quadruple booster
- Versatile display control functions
  - — Display data read/write
  - — Display on/off
  - — Column address inversion according to column driver layout
  - — Vertical display scroll
  - — Blink area select
  - — Read-modify-write
- 80-system MPU interface through 8-bit asynchronous data bus
- On-chip oscillator combined with external resistor and capacitor
- Tape carrier package (TCP)

Ordering Information

Type No.	Package
HD66410TA0	Outer Lead Pitch 300 μm (TCP-239)
HCD66410BP	Die with gold bump

Pin Arrangement

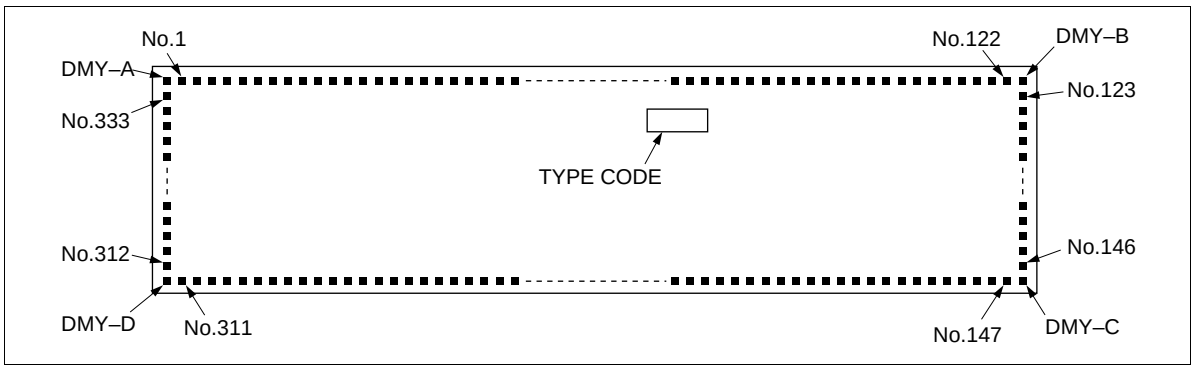


Note: This figure is not drawn to a scale.

HD66410 Pad Arrangement

Chip size : 14.28 × 2.72mm
Coordinate : Pad Center
Orgin : Chip Center
Bump size : 50 × 70 × 20 µm
Dummy pad 1: Bump size 70 × 70 × 20 µm (Typ.)
(DMY–A, DMY–B, DMY–C, DMY–D)
Dummy pad 2: Bump size 50 × 70 × 20 µm (Typ.)
(DMY–1 to DMY–40)

Note 1. The same voltage must be supplied to AV3-1 and AV3-2, V5-1 and V5-2, Vcc-1, Vcc-2, Vcc-3, and Vcc-4, GND-1, GND-2 and GND-3.
ALL (GND) pads are connected to GND internally, must be connected to GND or left open.
All (Vcc) pads, pad No. 41 to 89, are connected to Vcc internally, must be connected to Vcc or left open.
2. All dummy pads, DMY1 to DMY40, are not connected to any signal internally. However, these pads are not tested. Do not use these pads as a terminal.



HD66410 Pad Location Coordinates

Pad No.	Pad Name	Coordinate X	Coordinate Y
1	AV3-1	–6788	1056
2	(DMY1)	–6708	1056
3	VCSL	–6628	1056
4	(DMY2)	–6548	1056
5	VCSH	–6468	1056
6	VSL	–6388	1056
7	(DMY3)	–6308	1056
8	VSH	–6228	1056
9	V_{CC}-1	–6106	1056
10	VCHO	–5961	1056
11	(DMY4)	–5881	1056
12	VSHO	–5801	1056
13	(DMY5)	–5721	1056
14	VCLO	–5641	1056
15	VSLO	–5561	1056
16	(DMY6)	–5481	1056
17	V1	–5401	1056
18	(DMY7)	–5321	1020
19	V2	–5241	1020
20	V3	–5161	1020
21	(DMY8)	–5081	1020
22	(DMY9)	–5001	1020
23	(DMY10)	–4894	1056
24	V4	–4814	1056
25	V5-1	–4729	1056
26	(DMY11)	–4524	1069
27	(DMY12)	–4444	1069
28	V_{EE}	–4268	1069
29	C3–	–4178	1069
30	(DMY13)	–3987	1069
31	C3+	–3701	1076
32	C2–	–3621	1076
33	C2+	–3456	1076
34	C1–	–3376	1076
35	C1+	–3088	1069
36	VCI	–3008	1069
37	GND-1	–2887	1069
38	(GND)	–2767	1069
39	(GND)	–2687	1069
40	(GND)	–2607	1069
41	(V_{CC})	–2527	1202
42	(V_{CC})	–2447	1202
43	(V_{CC})	–2367	1202
44	(V_{CC})	–2287	1202
45	(V_{CC})	–2207	1202
46	(V_{CC})	–2127	1202
47	(V_{CC})	–2047	1202
48	(V_{CC})	–1967	1202
49	(V_{CC})	–1887	1202
50	(V_{CC})	–1807	1202
51	(V_{CC})	–1727	1202
52	(V_{CC})	–1647	1202
53	(V_{CC})	–1567	1202
54	(V_{CC})	–1487	1202
55	(V_{CC})	–1407	1202
56	(V_{CC})	–1327	1202
57	(V_{CC})	–1247	1202
58	(V_{CC})	–1167	1202
59	(V_{CC})	–1087	1202
60	(V_{CC})	–1007	1202
61	(V_{CC})	–927	1202
62	(V_{CC})	–847	1202
63	(V_{CC})	–767	1202
64	(V_{CC})	–687	1202
65	(V_{CC})	–607	1202
66	(V_{CC})	–527	1202
67	(V_{CC})	–447	1202
68	(V_{CC})	–367	1202
69	(V_{CC})	–287	1202
70	(V_{CC})	–207	1202
71	(V_{CC})	–127	1202
72	(V_{CC})	–47	1202
73	(V_{CC})	33	1202
74	(V_{CC})	113	1202
75	(V_{CC})	193	1202
76	(V_{CC})	273	1202
77	(V_{CC})	353	1202
78	(V_{CC})	433	1202
79	(V_{CC})	513	1202
80	(V_{CC})	593	1202
81	(V_{CC})	673	1202
82	(V_{CC})	753	1202
83	(V_{CC})	833	1202
84	(V_{CC})	913	1202
85	(V_{CC})	993	1202
86	(V_{CC})	1073	1202
87	(V_{CC})	1153	1114
88	(V_{CC})	1233	1114
89	(V_{CC})	1313	1114
90	V_{CC}-2	1393	1114
91	DB7	1583	1114
92	DB6	1795	1114
93	DB5	2008	1114
94	DB4	2220	1114
95	DB3	2433	1114
96	DB2	2645	1114
97	DB1	2858	1114
98	DB0	3070	1114
99	RD	3278	1114
100	WR	3482	1114
101	RS	3686	1114
102	CS	3890	1114
103	RES	4094	1114
104	TEST0	4298	1114
105	TEST1	4477	1114
106	CR	4685	1114
107	R	4893	1114
108	C	5102	1114
109	GND-2	5360	1114
110	GND-3	5440	1114
111	V_{CC}-3	5711	1114
112	V_{CC}-4	5791	1114
113	(DMY14)	5975	1114
114	VSCH	6055	1114
115	VSCL	6135	1114
116	(DMY15)	6215	1114
117	VCH	6295	1114
118	(DMY16)	6375	1114
119	VCL	6455	1114
120	V5-2	6535	1114
121	(DMY17)	6663	1114
122	AV3-2	6744	1114
123	(DMY18)	6925	939
124	COM3	6925	769
125	COM2	6925	689
126	COM1	6925	609
127	SEG24	6925	529
128	SEG23	6925	449
129	SEG22	6925	369
130	SEG21	6925	289
131	SEG20	6925	209
132	SEG19	6925	129
133	SEG18	6925	49
134	SEG17	6925	–31
135	SEG16	6925	–111
136	SEG15	6925	–191
137	SEG14	6925	–271
138	SEG13	6925	–351
139	SEG12	6925	–431
140	SEG11	6925	–511
141	SEG10	6925	–591
142	(DMY19)	6925	–699
143	(DMY20)	6925	–779
144	(DMY21)	6925	–859
145	(DMY22)	6925	–939
146	(DMY23)	6925	–1019
147	(DMY24)	6754	–1139
148	(DMY25)	6674	–1139
149	(DMY26)	6594	–1139
150	(DMY27)	6514	–1139
151	X161	6123	–1139
152	X160	6043	–1139
153	X159	5963	–1139
154	X158	5883	–1139
155	X157	5803	–1139
156	X156	5723	–1139
157	X155	5643	–1139
158	X154	5563	–1139
159	X153	5483	–1139
160	X152	5403	–1139
161	X151	5323	–1139
162	X150	5243	–1139
163	X149	5163	–1139
164	X148	5083	–1139
165	X147	5003	–1139
166	X146	4923	–1139
167	X145	4843	–1139
168	X144	4763	–1139
169	X143	4683	–1139
170	X142	4603	–1139
171	X141	4523	–1139
172	X140	4443	–1139
173	X139	4363	–1139
174	X138	4283	–1139
175	X137	4203	–1139
176	X136	4123	–1139
177	X135	4043	–1139
178	X134	3963	–1139
179	X133	3883	–1139
180	X132	3803	–1139
181	X131	3723	–1139
182	X130	3643	–1139
183	X129	3563	–1139
184	X128	3483	–1139
185	X127	3403	–1139
186	X126	3323	–1139
187	X125	3243	–1139
188	X124	3163	–1139
189	X123	3083	–1139
190	X122	3003	–1139
191	X121	2923	–1139
192	X120	2843	–1139
193	X119	2763	–1139
194	X118	2683	–1139
195	X117	2603	–1139
196	X116	2523	–1139
197	X115	2443	–1139
198	X114	2363	–1139
199	X113	2283	–1139
200	X112	2203	–1139

Pad No.	Pad Name	Coordinate X	Coordinate Y
201	X111	2123	–1139
202	X110	2043	–1139
203	X109	1963	–1139
204	X108	1883	–1139
205	X107	1803	–1139
206	X106	1723	–1139
207	X105	1643	–1139
208	X104	1563	–1139
209	X103	1483	–1139
210	X102	1403	–1139
211	X101	1323	–1139
212	X100	1243	–1139
213	X99	1163	–1139
214	X98	1083	–1139
215	X97	1003	–1139
216	X96	923	–1139
217	X95	843	–1139
218	X94	763	–1139
219	X93	683	–1139
220	X92	603	–1139
221	X91	523	–1139
222	X90	443	–1139
223	X89	363	–1139
224	X88	283	–1139
225	X87	203	–1139
226	X86	123	–1139
227	X85	43	–1139
228	X84	–37	–1139
229	X83	–117	–1139
230	X82	–197	–1139
231	X81	–277	–1139
232	X80	–357	–1139
233	X79	–437	–1139
234	X78	–517	–1139
235	X77	–597	–1139
236	X76	–677	–1139
237	X75	–757	–1139
238	X74	–837	–1139
239	X73	–917	–1139
240	X72	–997	–1139
241	X71	–1077	–1139
242	X70	–1157	–1139
243	X69	–1237	–1139
244	X68	–1317	–1139
245	X67	–1397	–1139
246	X66	–1477	–1139
247	X65	–1557	–1139
248	X64	–1637	–1139
249	X63	–1717	–1139
250	X62	–1797	–1139
251	X61	–1877	–1139
252	X60	–1957	–1139
253	X59	–2037	–1139
254	X58	–2117	–1139
255	X57	–2197	–1139
256	X56	–2277	–1139
257	X55	–2357	–1139
258	X54	–2437	–1139
259	X53	–2517	–1139
260	X52	–2597	–1139
261	X51	–2677	–1139
262	X50	–2757	–1139
263	X49	–2837	–1139
264	X48	–2917	–1139
265	X47	–2997	–1139
266	X46	–3077	–1139
267	X45	–3157	–1139
268	X44	–3237	–1139
269	X43	–3317	–1139
270	X42	–3397	–1139
271	X41	–3477	–1139
272	X40	–3557	–1139
273	X39	–3637	–1139
274	X38	–3717	–1139
275	X37	–3797	–1139
276	X36	–3877	–1139
277	X35	–3957	–1139
278	X34	–4037	–1139
279	X33	–4117	–1139
280	X32	–4197	–1139
281	X31	–4277	–1139
282	X30	–4357	–1139
283	X29	–4437	–1139
284	X28	–4517	–1139
285	X27	–4597	–1139
286	X26	–4677	–1139
287	X25	–4757	–1139
288	X24	–4837	–1139
289	X23	–4917	–1139
290	X22	–4997	–1139
291	X21	–5077	–1139
292	X20	–5157	–1139
293	X19	–5237	–1139
294	X18	–5317	–1139
295	X17	–5397	–1139
296	X16	–5477	–1139
297	X15	–5557	–1139
298	X14	–5637	–1139
299	X13	–5717	–1139
300	X12	–5797	–1139
301	X11	–5877	–1139
302	X10	–5957	–1139
303	X9	–6037	–1139
304	X8	–6117	–1139
305	X7	–6197	–1139
306	X6	–6277	–1139
307	X5	–6357	–1139
308	X4	–6437	–1139
309	X3	–6517	–1139
310	X2	–6597	–1139
311	X1	–6677	–1139
312	(DMY28)	–6935	–1018
313	(DMY29)	–6935	–938
314	(DMY30)	–6935	–858
315	(DMY31)	–6935	–778
316	(DMY32)	–6935	–698
317	(DMY33)	–6935	–618
318	(DMY34)	–6935	–538
319	(DMY35)	–6935	–458
320	(DMY36)	–6935	–378
321	(DMY37)	–6935	–298
322	(DMY38)	–6935	–218
323	(DMY39)	–6935	–138
324	(DMY40)	–6935	–58
325	SEG9	–6927	99
326	SEG8	–6927	179
327	SEG7	–6927	259
328	SEG6	–6927	339
329	SEG5	–6927	419
330	SEG4	–6927	499
331	SEG3	–6927	579
332	SEG2	–6927	659
333	SEG1	–6927	739
334	(DMY-A)	–6927	927
335	(DMY-B)	6925	1114
336	(DMY-C)	6925	–1139
337	(DMY-D)	–6935	–1139

Pin Description

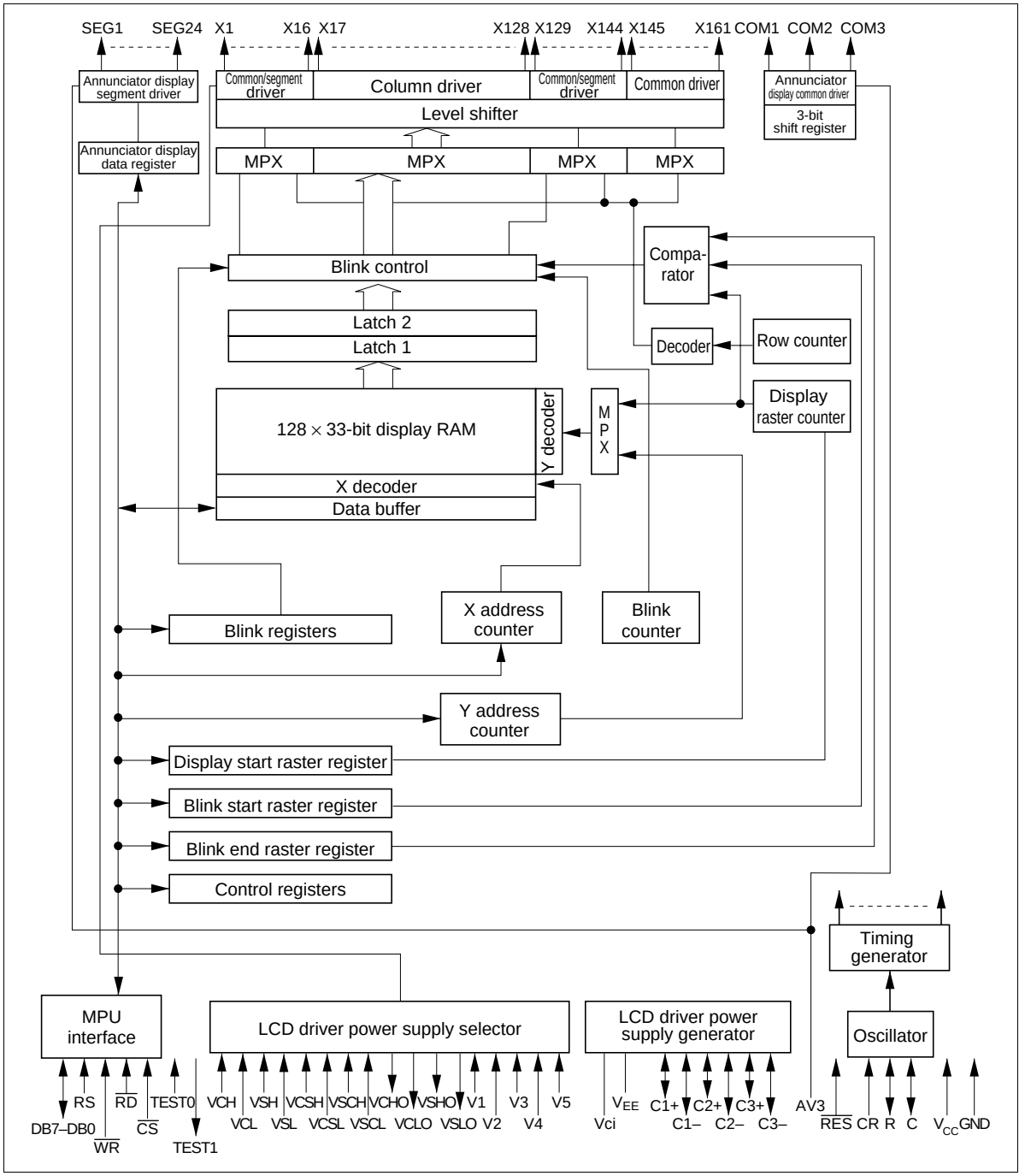
Pin Name	Number of Pins	I/O	Connected to	Description
V_{CC}, GND	5	—	Power supply	V_{CC}: +2.2 to +5.5V, GND: 0V
Vci	1	—	Power supply	Inputs voltage to the booster to generate the base of the LCD drive voltages (V_{EE}); must be below V_{CC}. Vci: 0 to +3.6V.
AV3	2	—	Power supply	Supplies power to the internal annunciator drivers to generate the annunciator drive voltages using AV3 and V_{CC}. V_{CC}–AV3: 0 to 3.6V; must be above GND.
V_{EE}	1	—	Booster capacitors and V5	Boosts and outputs the voltage input to the Vci pin; must be connected to the booster capacitors and V5 pin.
V5	2	—	V_{EE}, Resistive divider	Power supply for LCD driving circuit. Supplies several levels of power to the internal LCD drivers for dot-matrix display; must be connected to the V_{EE} pin.
V1, V2, V3, V4	4	—	Resistive divider	Supplies several levels of power to the internal LCD drivers for dot-matrix display; must be applied with the appropriate level of bias for the LCD panel used.
C1+ to C3+, C1– to C3–	6	—	Booster capacitor	Must be connected to external capacitors according to the boosting ratio.
VSHO, VSLO	2	O	VSH, VSL, VCSH, VCSL, (VSCH, VSCL)	Output voltage to be supplied to the internal column drivers.
VCHO, VCLO	2	O	VCH, VCL, VCSH, VCSL, (VSCH, VSCL)	Output voltage to be supplied to the internal row drivers.
VSH, VSL	2	I	VSHO, VSLO	Input voltage to be supplied to internal drivers X17 to X128.
VCH, VCL	2	I	VCHO, VCLO	Input voltage to be supplied to internal drivers X145 to X160.
VCSH, VCSL	2	I	VCHO, VCLO, VSHO, VSLO	Input voltage to be supplied to internal drivers X1 to X16.
VSCH, VSCL	2	I	VCHO, VCLO, VSHO, VSLO	Input voltage to be supplied to internal drivers X129 to X144.
C, R, CR	3	I, I/O	Oscillator resistor and capacitor	Must be connected to external capacitors and resistors when using R-C oscillation. When using an external clock, it must be input to the CR pin.
$\overline{RES}$	1	I	—	Resets the LSI internally when driven low.
$\overline{CS}$	1	I	MPU	Selects the LSI, specifically internal registers (index and data registers) when driven low.
RS	1	I	MPU	Selects one of the internal registers; selects the index register when driven low and data registers when driven high.
$\overline{WR}$	1	I	MPU	Inputs write strobe; allows a write access when driven low.

Pin Name	Number of Pins	I/O	Connected to	Description
$\overline{RD}$	1	I	MPU	Inputs read strobe; allows a read access when driven low.
DB7 to DB0	8	I/O	MPU	8-bit three-state bidirectional data bus; transfers data between the HD66410 and MPU through this bus.
X1 to X16, X129 to X144	32	O	Liquid crystal display	Output column or row drive signals; either column or row can be selected by programming.
X17 to X128	112	O	Liquid crystal display	Output column drive signals.
X145 to X161	17	O	Liquid crystal display	Output row drive signals.
COM1 to COM3	3	O	Liquid crystal display	Output row drive signals for annunciator display; available even during standby modes. Can operate statically or with 1/3 duty cycle.
SEG1 to SEG24	24	O	Liquid crystal display	Output column drive signals for annunciator display; available even during standby modes.
TEST0	1	I	GND	Tests the LSI; must be grounded.
TEST1	1	O	—	Tests the LSI; must be left unconnected.

Register List

CS	RS	Index Register Bits					Register Symbol	Register Name	R/W	Data Bits							
		4	3	2	1	0				7	6	5	4	3	2	1	0
1	—	—	—	—	—	—											
0	0	—	—	—	—	—	IR	Index register	W				IR4	IR3	IR2	IR1	IR0
0	1	0	0	0	0	0	R0	Control register 1	W		DISP	STBY	PWR	OSC	IDTY	CNF	ADC
0	1	0	0	0	0	1	R1	Control register 2	W					RMW	DDTY	INC	BLK
0	1	0	0	0	1	0	R2	X address register	W					XA3	XA2	XA1	XA0
0	1	0	0	0	1	1	R3	Y address register	W			YA5	YA4	YA3	YA2	YA1	YA0
0	1	0	0	1	0	0	R4	Display memory access register	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	R5	Display start raster register	W			ST5	ST4	ST3	ST2	ST1	ST0
0	1	0	0	1	1	0	R6	Blink register 1	W	BK0	BK1	BK2	BK3	BK4	BK5	BK6	BK7
0	1	0	0	1	1	1	R7	Blink register 2	W	BK8	BK9	BK10	BK11	BK12	BK13	BK14	BK15
0	1	0	1	0	0	0	R8	Blink start raster register	W			BSL5	BSL4	BSL3	BSL2	BSL1	BSL0
0	1	0	1	0	0	1	R9	Blink end raster register	W			BEL5	BEL4	BEL3	BEL2	BEL1	BEL0
0	1	0	1	0	1	0		Reserved									
0	1	0	1	0	1	1		Reserved									
0	1	0	1	1	0	0		Reserved									
0	1	0	1	1	0	1		Reserved									
0	1	0	1	1	1	0		Reserved									
0	1	0	1	1	1	1		Reserved									
0	1	1	0	0	0	0	A0	Annunciator display data register 1	W	IC1A	IC1B	IC1C	IC1D	IC1E	IC1F	IC1G	IC1H
0	1	1	0	0	0	1	A1	Annunciator display data register 2	W	IC2A	IC2B	IC2C	IC2D	IC2E	IC2F	IC2G	IC2H
0	1	1	0	0	1	0	A2	Annunciator display data register 3	W	IC3A	IC3B	IC3C	IC3D	IC3E	IC3F	IC3G	IC3H
0	1	1	0	0	1	1	A3	Annunciator display data register 4	W	IC1I	IC1J	IC1K	IC1L	IC1M	IC1N	IC1O	IC1P
0	1	1	0	1	0	0	A4	Annunciator display data register 5	W	IC2I	IC2J	IC2K	IC2L	IC2M	IC2N	IC2O	IC2P
0	1	1	0	1	0	1	A5	Annunciator display data register 6	W	IC3I	IC3J	IC3K	IC3L	IC3M	IC3N	IC3O	IC3P
0	1	1	0	1	1	0	A6	Annunciator display data register 7	W	IC1Q	IC1R	IC1S	IC1T	IC1U	IC1V	IC1W	IC1X
0	1	1	0	1	1	1	A7	Annunciator display data register 8	W	IC2Q	IC2R	IC2S	IC2T	IC2U	IC2V	IC2W	IC2X
0	1	1	1	0	0	0	A8	Annunciator display data register 9	W	IC3Q	IC3R	IC3S	IC3T	IC3U	IC3V	IC3W	IC3X
0	1	1	1	0	0	1	A9	Annunciator blink register 1	W	IP11	IP10	IB15	IB14	IB13	IB12	IB11	IB10
0	1	1	1	0	1	0	A10	Annunciator blink register 2	W	IP21	IP20	IB25	IB24	IB23	IB22	IB21	IB20
0	1	1	1	0	1	1	A11	Annunciator blink register 3	W	IP31	IP30	IB35	IB34	IB33	IB32	IB31	IB30
0	1	1	1	1	0	0		Reserved									
0	1	1	1	1	0	1		Reserved									
0	1	1	1	1	1	0		Reserved									
0	1	1	1	1	1	1		Reserved									

Block Diagram



System Description

The HD66410 comprises two kinds of independent LCD drivers: one operating with 1/33 or 1/17 duty cycle for dot-matrix displays and the other operating statically or with 1/3 duty cycle for annunciator displays. These drivers can display a maximum of 128 × 33 dots (eight 16× 16-dot characters × 2 lines) on an LCD panel together with a 72-segment annunciator. Annunciator display is available even during standby modes, thus enabling constant display such as for a time function. The HD66410 can reduce power dissipation without affecting display because data is retained in the display RAM even during standby modes. An LCD system can be configured simply by attaching external capacitors and resistors (Figure 1) since the HD66410 incorporates booster circuits.

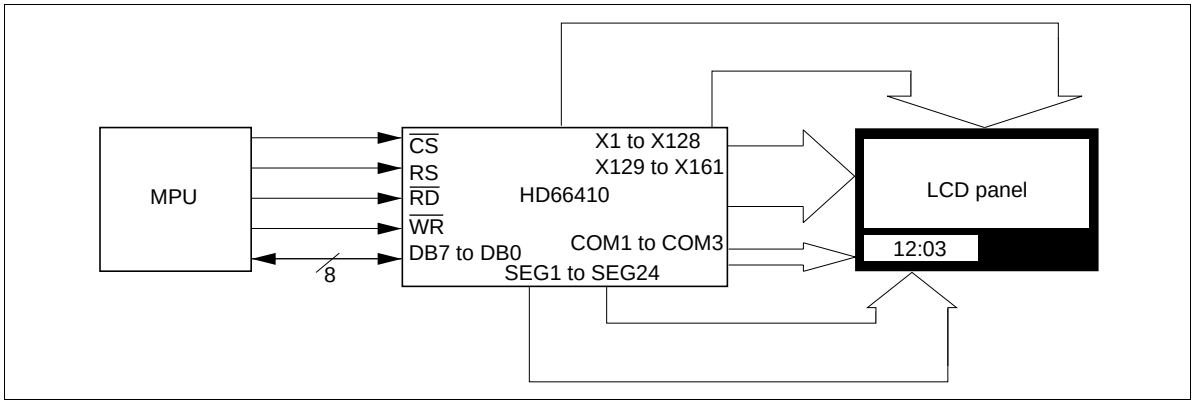


Figure 1 System Block Diagram

MPU Interface

The HD66410 can interface directly to an MPU through an 8-bit data bus or through an I/O port (Figure 2). The MPU can access the HD66410 internal registers independent of internal clock timing.

The index register can be directly accessed but the other registers (data registers) cannot. Before accessing a data register, its register number must be written to the index register. Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. An example of a register access sequence is shown in Figure 3.

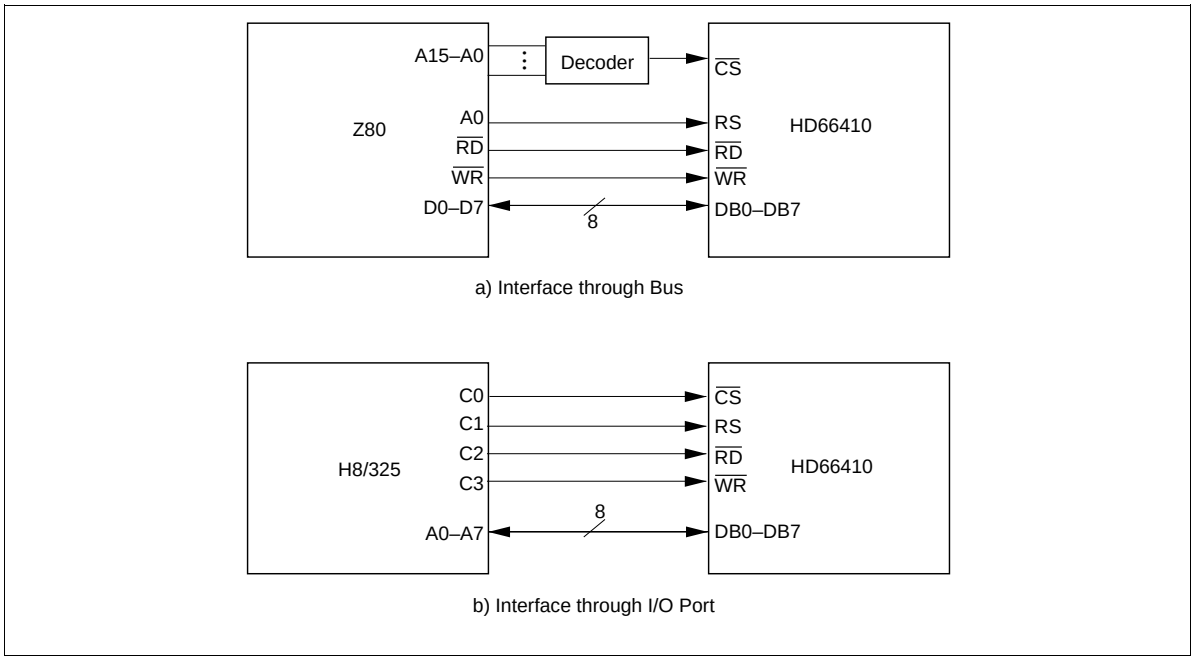


Figure 2 8-Bit MPU Interface Examples

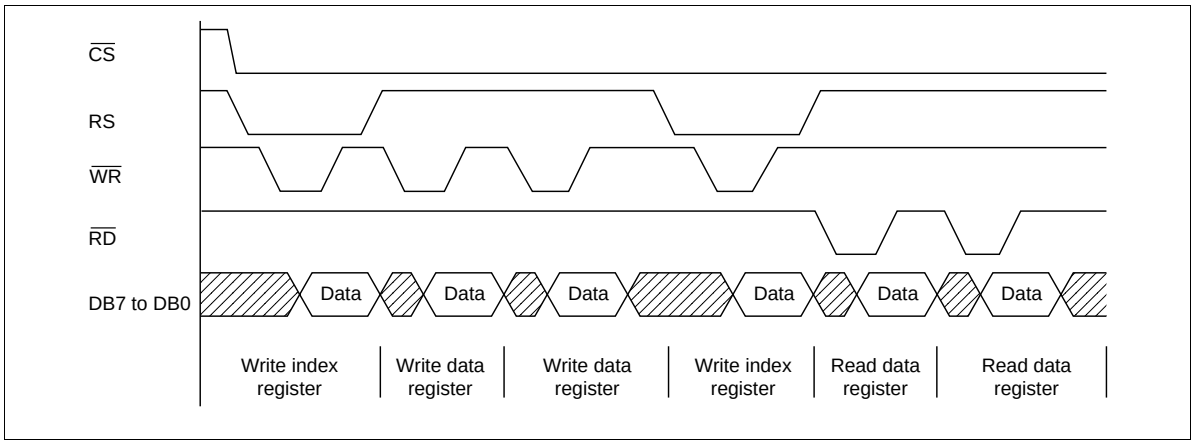


Figure 3 8-Bit Data Transfer Sequence

LCD Driver Configuration

Common/Segment Output Assignment: The HD66410 can assign LCD driver output pins X1 to X16 and X129 to X144 to either common or segment output depending on the CNF bit value in control register 1, while X17 to X128 and X145 to X161 are fixed to segment output and common output, respectively. With this function, common output can be positioned on either one side or two sides of an LCD panel. Figure 4 shows an example where 33-channel common output is positioned to the right of an LCD panel, with X129 to X144 assigned to row output and X1 to X16 assigned to column output. Figure 5 shows an example where 33-channel common output is divided into two and positioned to the right and left of the LCD panel, with X129 to X144 assigned to segment output and X1 to X16 assigned to common output. These assignment are valid in the case of 1/17 display duty. Only seventeen X terminals output common signal; unselected signal is output from the rest of terminals which are assigned to row output.

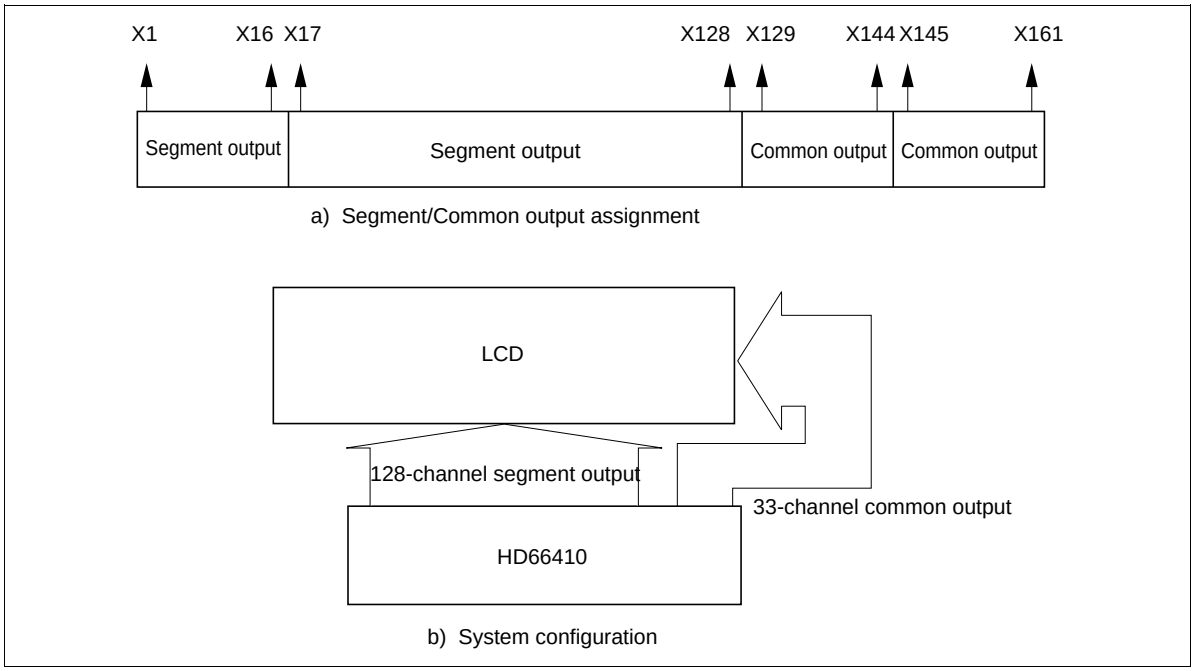
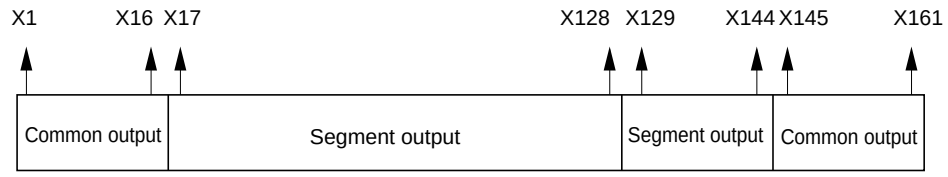
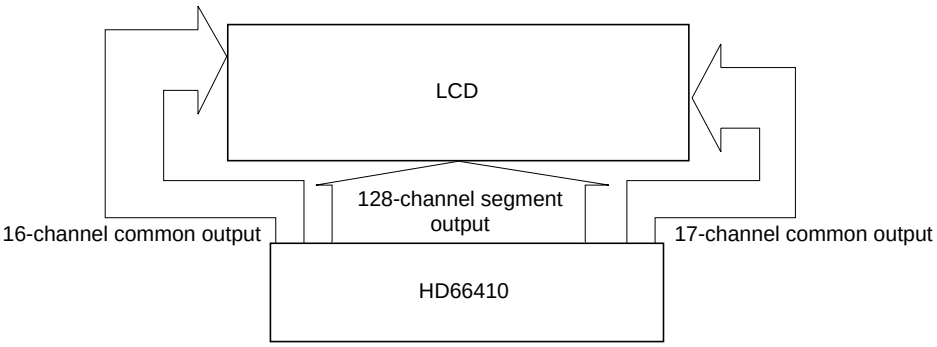


Figure 4 Common Output on Right Side



a) Segment/Common output assignment



b) System configuration

Figure 5 Common Output on Right and Left Sides

X-Address Inversion According to LCD Driver Layout: The HD66410 can always display data in address H'0 on the top left of an LCD panel regardless of where it is positioned with respect to the panel. This is because the HD66410 can invert the positional relationship between display RAM addresses and LCD driver output pins by inverting RAM addresses. Specifically, the HD66410 outputs data in address H'0 from X1 (X17) when the ADC bit in control register 1 is 0, and from X128 (X144) otherwise. Here, the scan direction of row output is also inverted according to the situation, as shown in Figure 6. Note that addresses and scan direction are inverted when data is written to the display RAM, and thus changing the ADC bit after data has been written has no effect. Therefore, hardware control bits such as CNF and ADC must be set immediately after reset is canceled, and must not be set while data is being displayed.

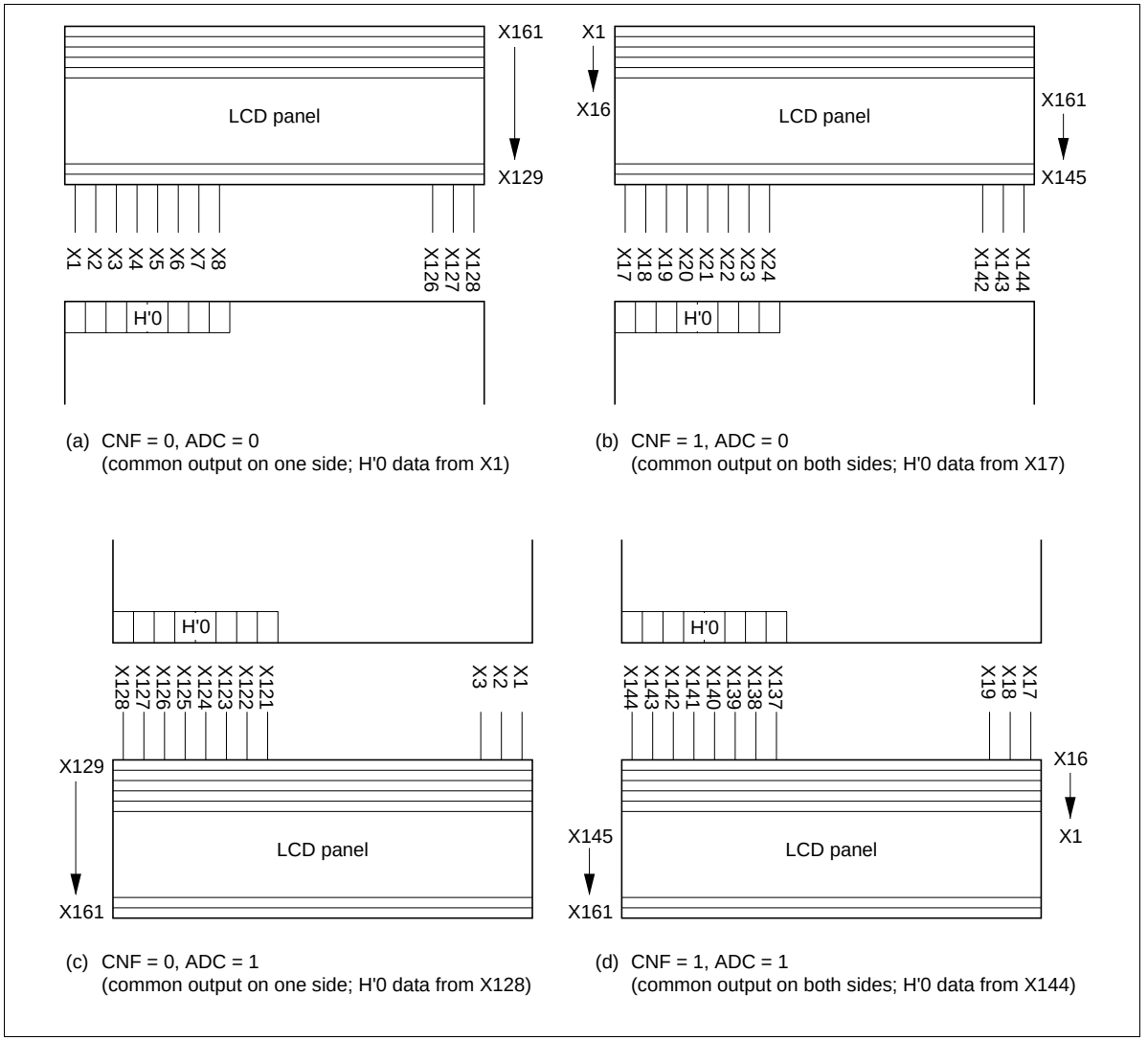


Figure 6 LCD Driver Layout and RAM Addresses (1/33 Duty)

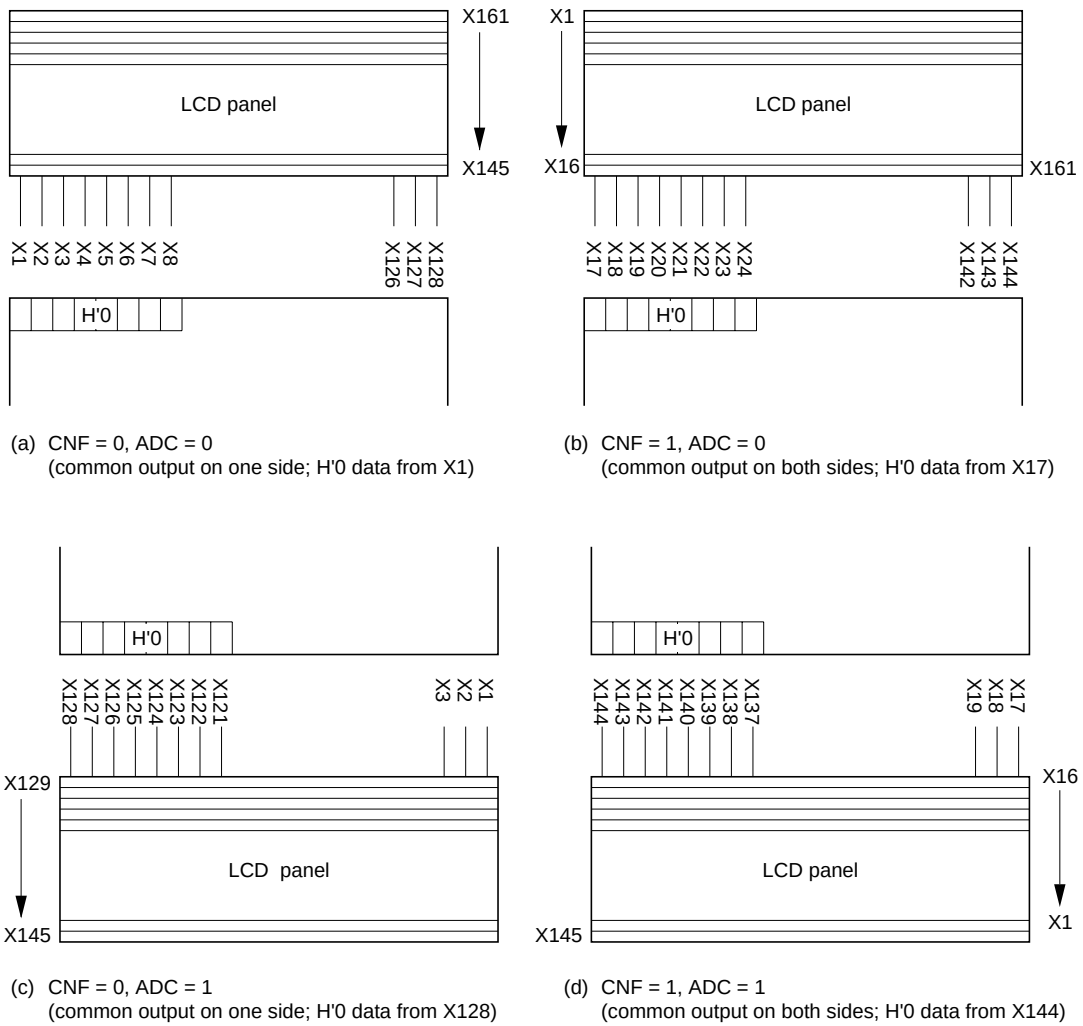


Figure 7 LCD Driver Layout and RAM Addresses (1/17 Duty)

Display RAM Configuration and Display

The HD66410 incorporates a bit-mapped display RAM. It has 128 bits in the X direction and 33 bits in the Y direction. The 128 bits are divided into sixteen 8-bit groups. As shown in Figure 8, data written by the MPU is stored horizontally with the MSB at the far left and the LSB at the far right. A display data of 1 turns on (black) the corresponding dot of an LCD panel and 0 turns it off (transparent).

The ADC bit of control register 1 can control the positional relationship between X addresses of the RAM and LCD driver output (Figure 9). Specifically, the data in address H'0 is output from X1 (X17) when the ADC bit in control register 1 is 0, and from X128 (X144) otherwise. Here, data in each 8-bit group is also inverted. Because of this function, the data in X address H'0 can be always displayed on the top left of an LCD panel with the MSB at the far left regardless of the LSI is positioned with respect to the panel.

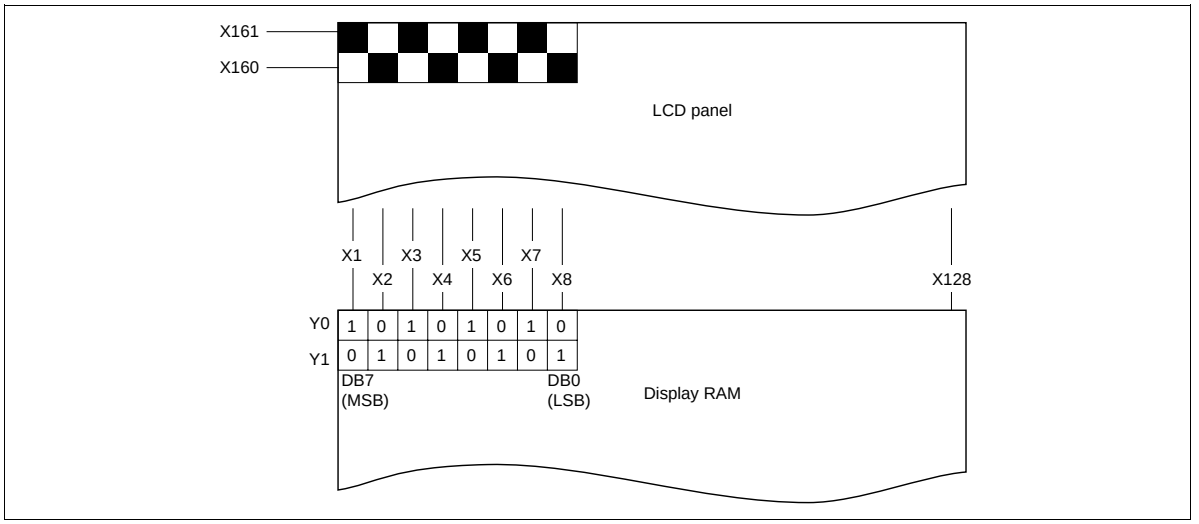


Figure 8 Display RAM Data and Display

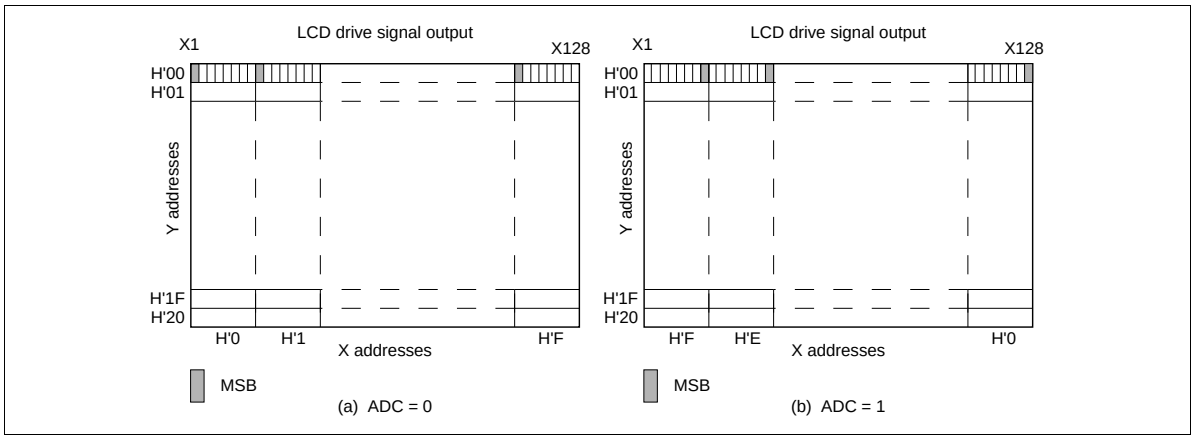


Figure 9 Display RAM Configuration

Access to Internal Registers and Display RAM

Access to Internal Registers by the MPU: The internal registers include the index register and data registers. The index register can be accessed by driving both the $\overline{CS}$ and RS signals low. To access a data register, first write its register number to the index register with RS set to 0, and then access the data register with RS set to 1. Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. Some data registers contain unused bits; they should be set to 0. Note that all data registers except the display memory access register can only be written to.

Access to Display RAM by the MPU: To access the display RAM, first write the RAM address desired to the X address register (R2) and the Y address register (R3). Then read/write the display memory access register (R4). Memory access by the MPU is independent of memory read by the HD66410 and is also asynchronous with the system clock, thus enabling an interface independent of HD66410's internal operations. However, when reading, data is temporarily latched into a HD66410's buffer and then output next time a read is performed in a subsequent cycle. This means that a dummy read is necessary after setting X and Y addresses. The memory read sequence is shown in Figure 10.

X and Y addresses are automatically incremented after each memory access according to the INC bit value in control register 2; therefore, it is not necessary to update the addresses for each access. Figure 11 shows two cases of incrementing display RAM address. When the INC bit is 0, the Y address will be incremented up to H'3F with the X address unchanged. However, actual memory is valid only within H'00 to H'20; accessing an invalid address is ignored. When the INC bit is 1, the X address will be incremented up to H'F with the Y address unchanged. After address H'F, the X address will return to H'0; if more than 16 bytes of data are consecutively written, data will be overwritten at the same address.

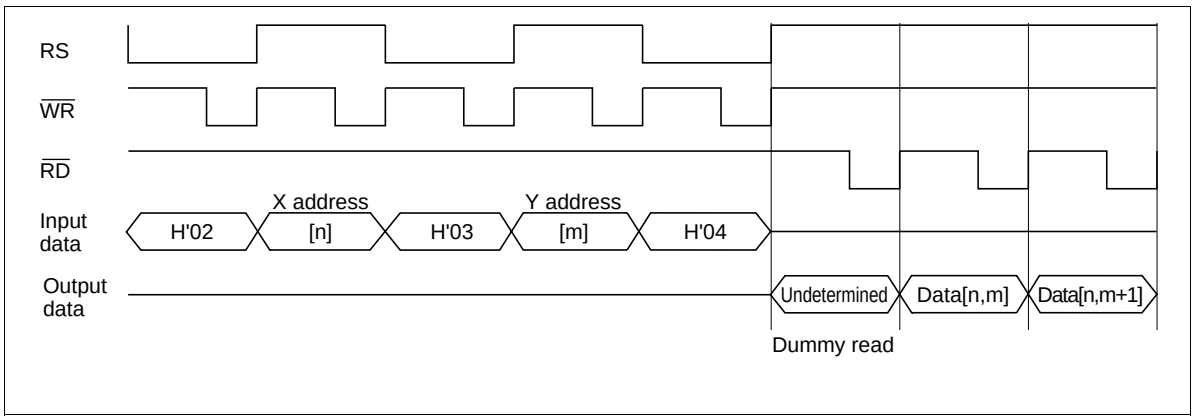


Figure 10 Display RAM Read Sequence

Display RAM Reading by LCD Controller: Data is read by the HD66410 to be displayed asynchronously with accesses by the MPU. However, because simultaneous access could damaging data in the display RAM, the HD66410 internally arbitrates access timing; access by the MPU usually has priority and so access by the HD66410 is placed between accesses by the MPU. Accordingly, an appropriate time must be secured (see the given electrical characteristics between two accesses by the MPU).

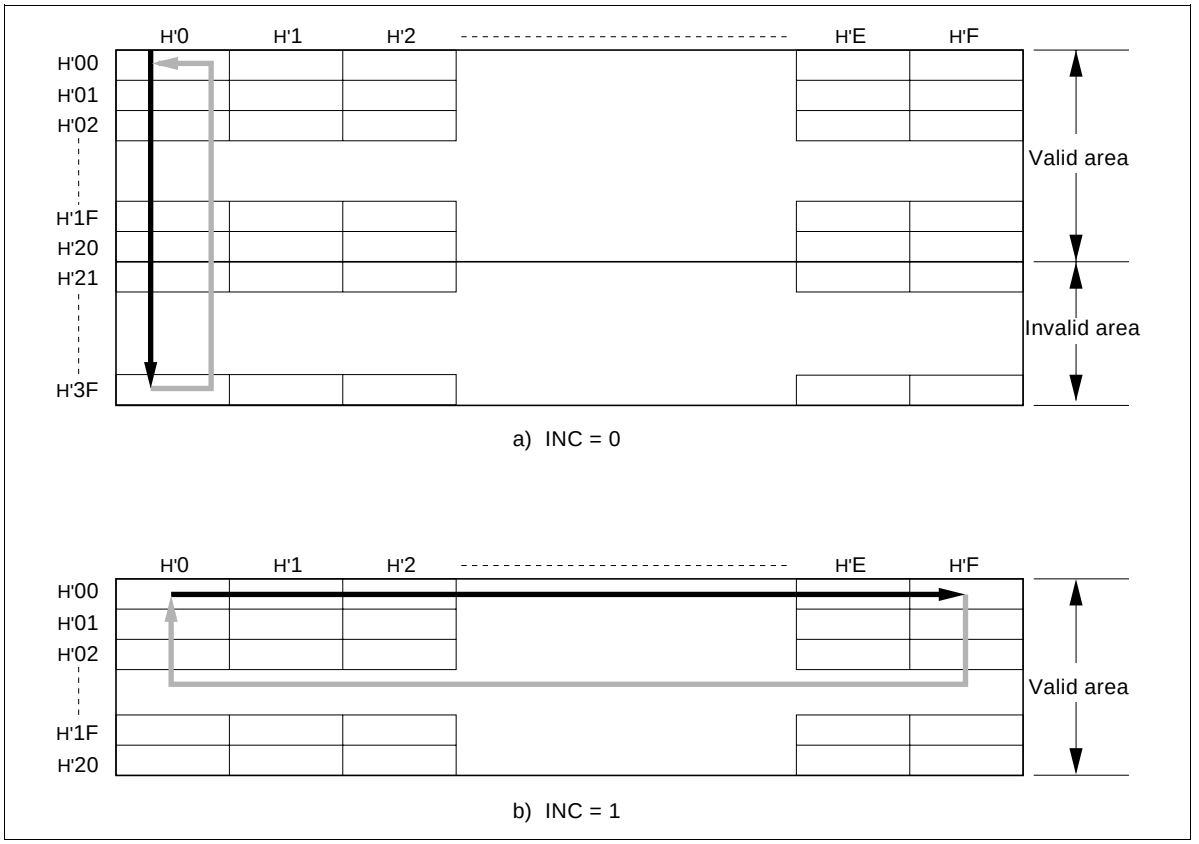


Figure 11 Display RAM Address Increment

Read-Modify-Write: X- or Y-address is incremented after reading from or writing data to the display RAM at normal mode. However, X- or Y-address is not incremented after reading data from the display RAM at read-modify-write mode. The data which is read from the display RAM may be modified and written to the same address without resetting the address. Data is temporarily latched into a HD66410's buffer and then output next time a read is performed in a subsequent cycle. This means that the dummy read is necessary after every cycle. This sequence is shown in Figure 12.

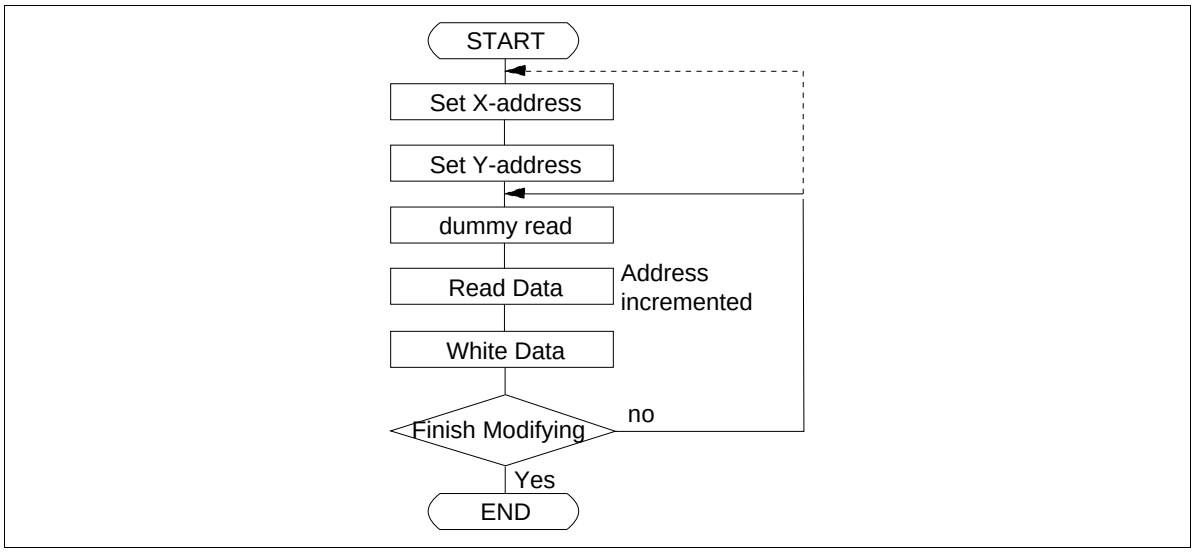


Figure 12 The Flow Chart for Read-Modify-Write

Vertical Scroll Function

The HD66410 can vertically scroll a display by varying the top raster to be displayed, which is specified by the display start raster register. Figure 13 and 14 show vertical scroll examples. As shown, when the top raster to be displayed is set to 1, data in Y address H'00 is displayed on the 33rd raster. To display another frame on the 33rd raster, therefore, data in Y address H'00 must be modified after setting the top raster.

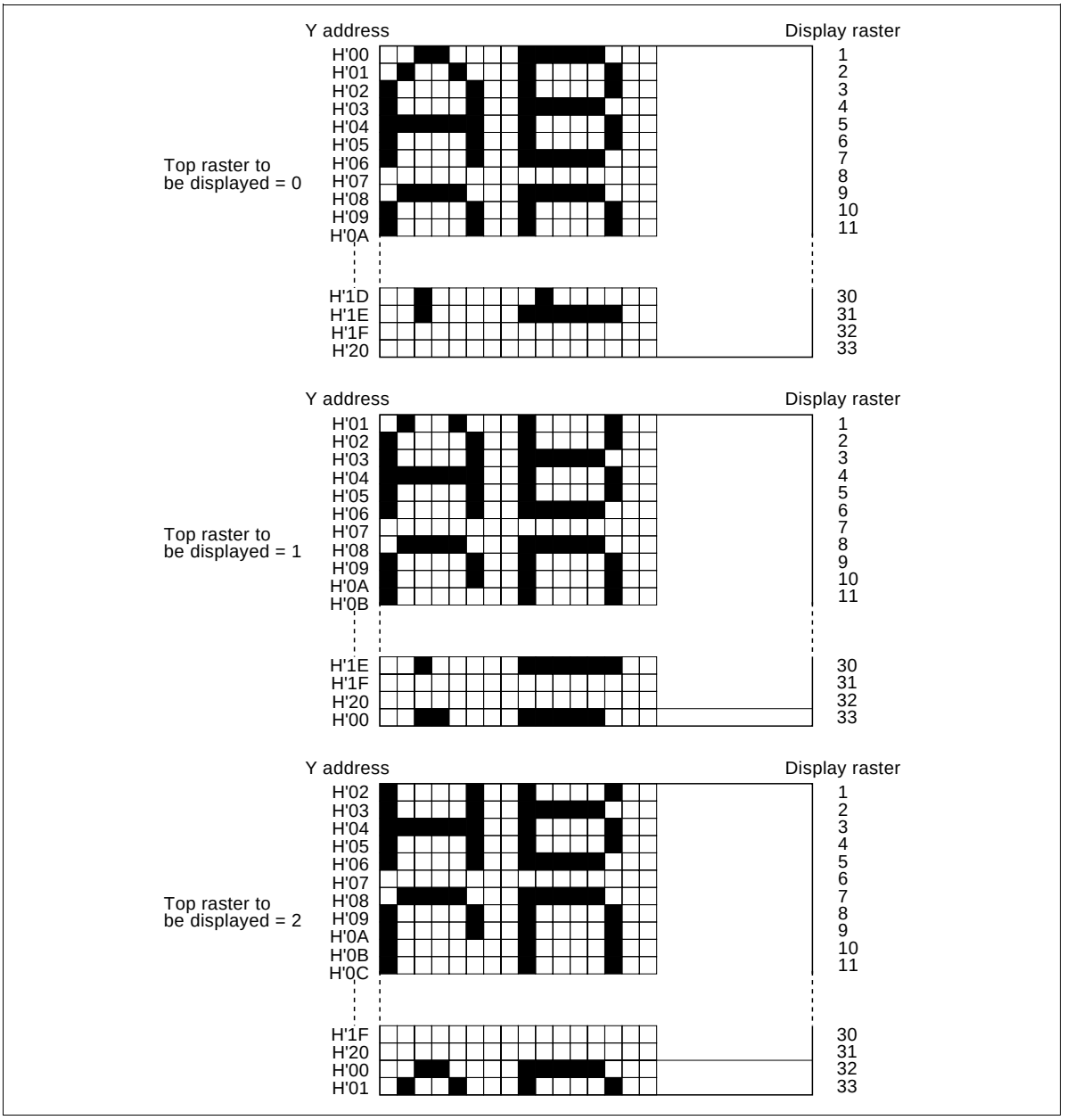


Figure 13 Vertical Scroll (1/33 Duty)

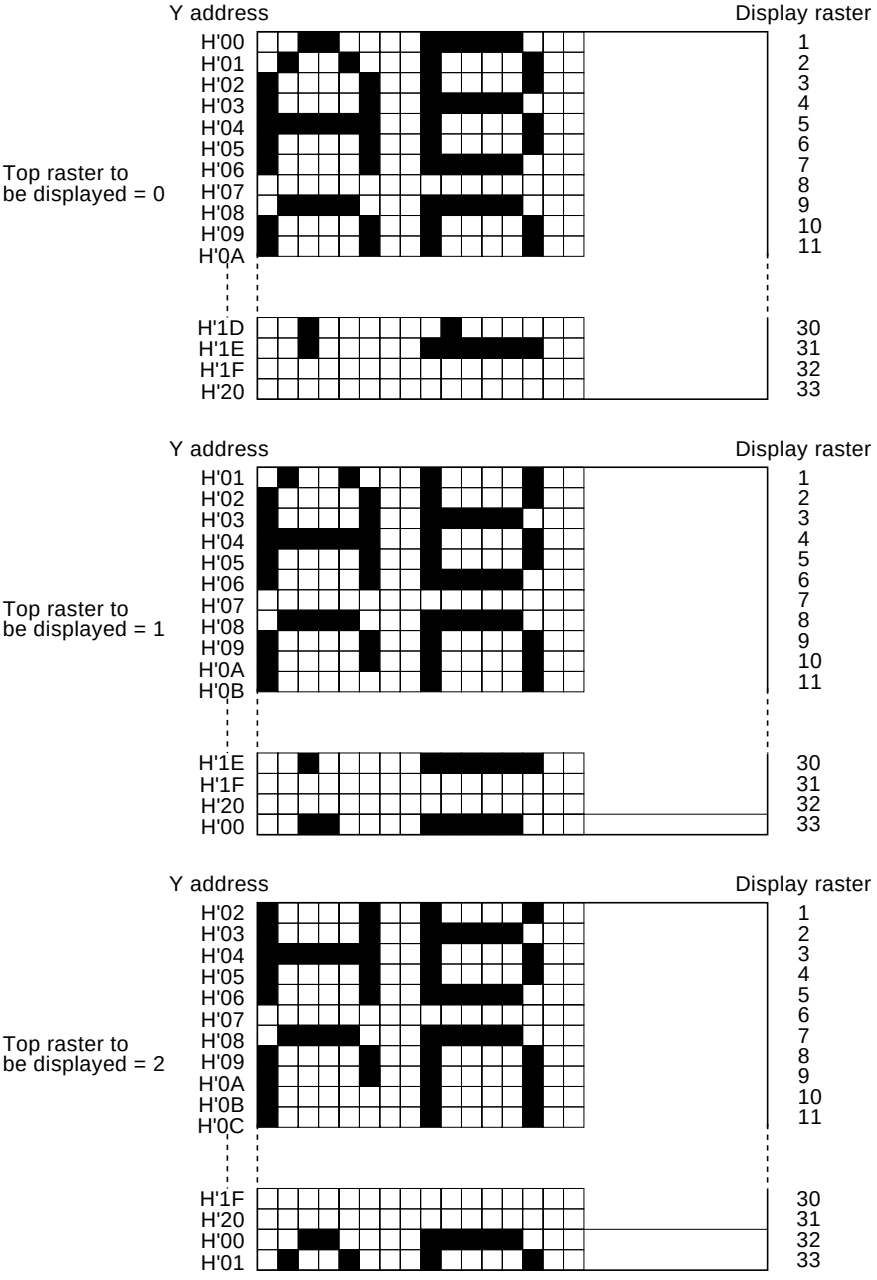


Figure 14 Vertical Scroll (1/17 Duty)

Blink Function

Blinking Dot-Matrix Display Area: The HD66410 can blink a specified area on the dot-matrix display. Blinking is achieved by repeatedly turning on and off the specified area at a frequency of one sixty-fourth the frame frequency. For example, when the frame frequency is 80 Hz, the area is turned on and off every 0.8 seconds.

The area to be blinked can be designated by specifying vertical and horizontal positions of the area. The vertical position, or the rasters to be blinked, are specified by the blink start raster register (R8) and blink end raster register (R9). The horizontal position, or the dots to be blinked in the specified rasters, are specified by the blink registers (R6 and R7) in an 8-dot group; each data bit in the blink registers controls its corresponding 8-dot group. The relationship between the registers and blink area is shown in Figure 15. Setting the BLK bit to 1 in control register 2 after setting the above registers starts blinking the designated area. Note that since the area to be blinked is designated absolutely with respect to the display RAM, it will move along with a scrolling display (Figure 16).

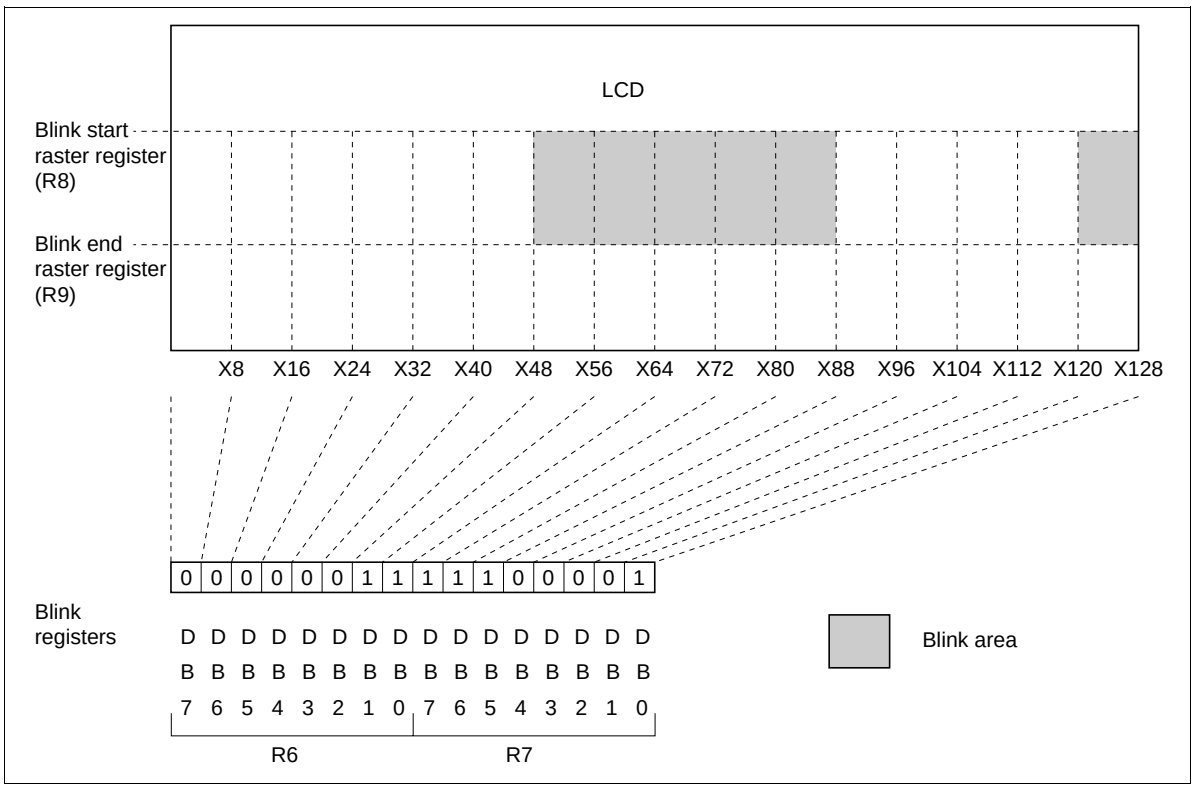
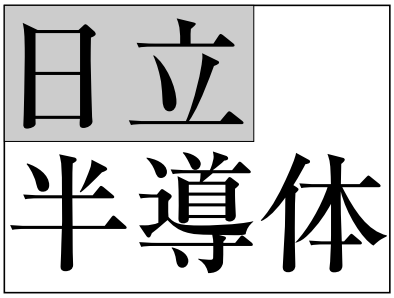
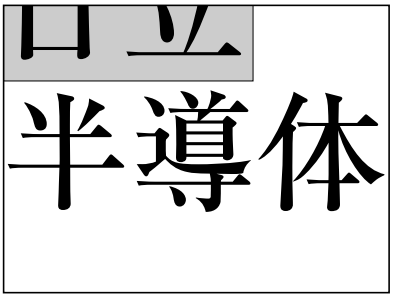


Figure 15 Blink Area Designation by Blink Control Registers



Display start raster = 0
Blink start raster = 0
Blink end raster = H'F



Display start raster = H'5
Blink start raster = H'5
Blink end raster = H'F

Figure 16 Scrolling Blink Area

Blinking Annunciator Display Area: The HD66410 can blink up to 18 dots among a maximum of 72 dots on the annunciator display. This function is controlled by a blink controller independent of that for the main dot-matrix display part. The dots to be blinked can be designated by annunciator blink registers 1, 2, and 3, each of which contains two bits to specify a block and six bits to specify dots to be blinked in the specified block (Figures 17 and 18).

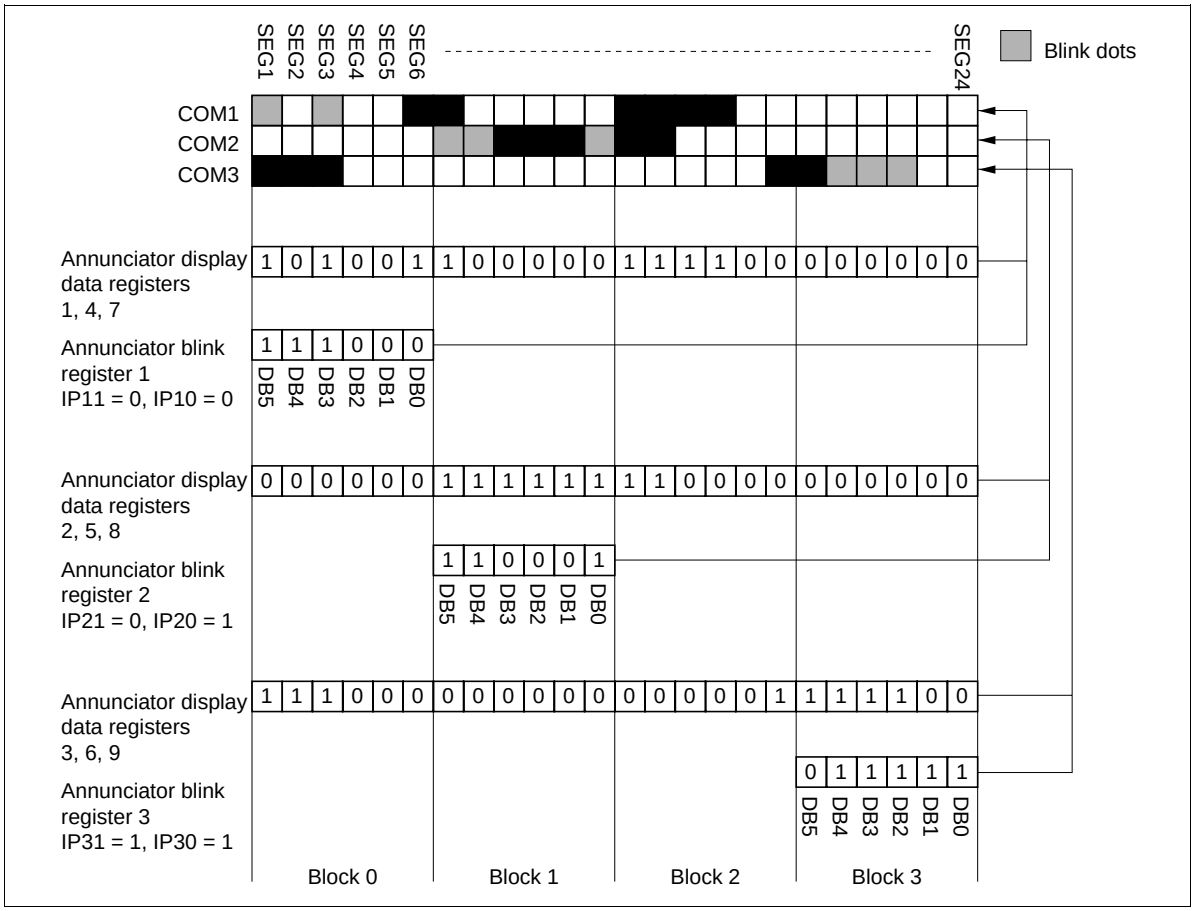


Figure 17 Blink Area Designation by Annunciator Blink Control Registers

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Annunciator blink register 1	IP11	IP10	IB15	IB14	IB13	IB12	IB11	IB10
Annunciator blink register 2	IP21	IP20	IB25	IB24	IB23	IB22	IB21	IB20
Annunciator blink register 3	IP31	IP30	IB35	IB34	IB33	IB32	IB31	IB30

IPn1	IPn0	Blink Block
0	0	Block 0 (SEG1–SEG6)
0	1	Block 1 (SEG7–SEG12)
1	0	Block 2 (SEG13–SEG18)
1	1	Block 3 (SEG19–SEG24)

IPn1, IPn0: Block select bits (n = 1, 2, 3)

Figure 18 Annunciator Blink Registers

Power Down Modes

The HD66410 has a standby function providing low power-dissipation, which is initiated by internal register settings. There are two standby modes: in one, all the HD66410 functions are inactive, and in the other, only the annunciator display function is active. In both modes, the internal booster halts but data in the display RAM and internal registers except the DISP bit is retained. However, only control registers can be accessed during standby modes. In the standby mode with annunciator display, the oscillator does not halt, thus dissipating more power than in the other standby mode. Table 1 lists the LCD driver output pin status during standby modes. Figure 19 shows the procedure for initiating and canceling a standby mode. Note that the cancelation procedure must be strictly followed to protect data in the display RAM.

Table 1 Output Pin Status during Standby Modes

X1 to X161	Output V_{CC} (display off)	
COM1 to COM3	OSC = 0	Output V_{CC} (display off)
	OSC = 1	Output common signals (display on)
SEG1 to SEG24	OSC = 0	Output V_{CC} (display off)
	OSC = 1	Output segment signals (display on)

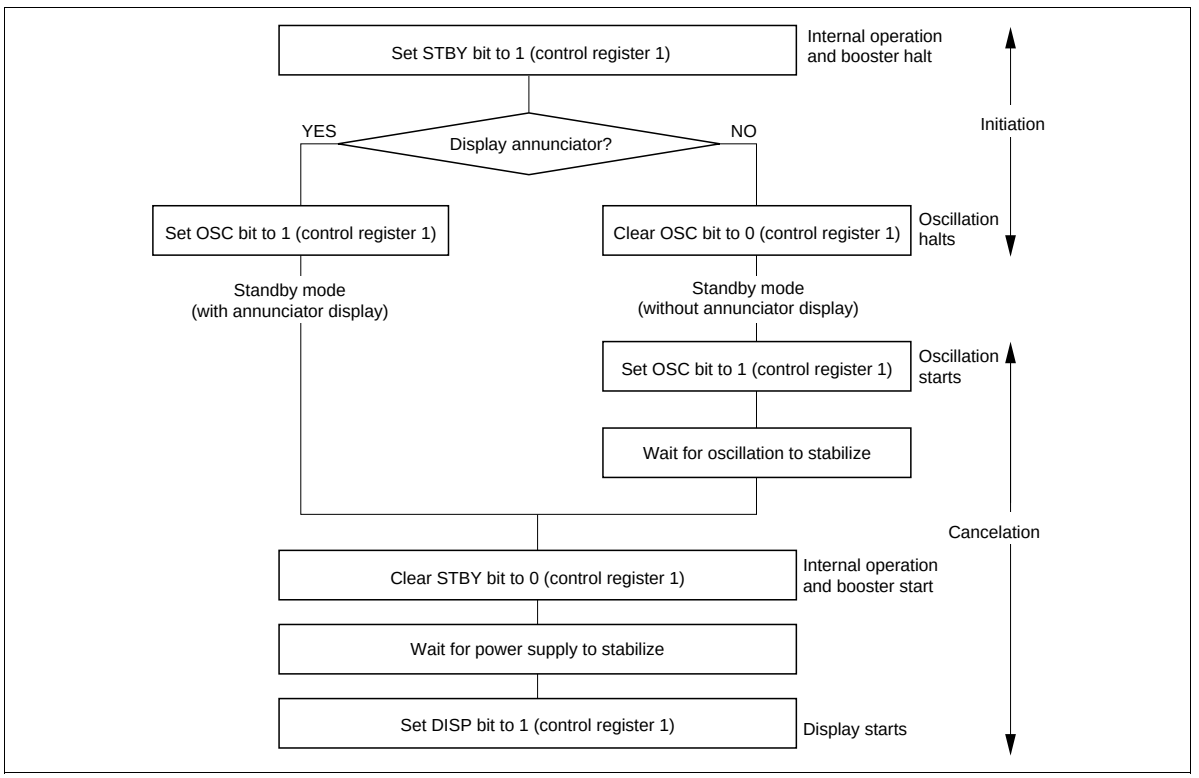


Figure 19 Procedure for Initiating and Canceling a Standby Mode

Power On/Off Procedure

Figure 20 shows the procedure for turning the power supply on and off. This procedure must be strictly followed to prevent incorrect display because the HD66410 incorporates all power supply circuits .

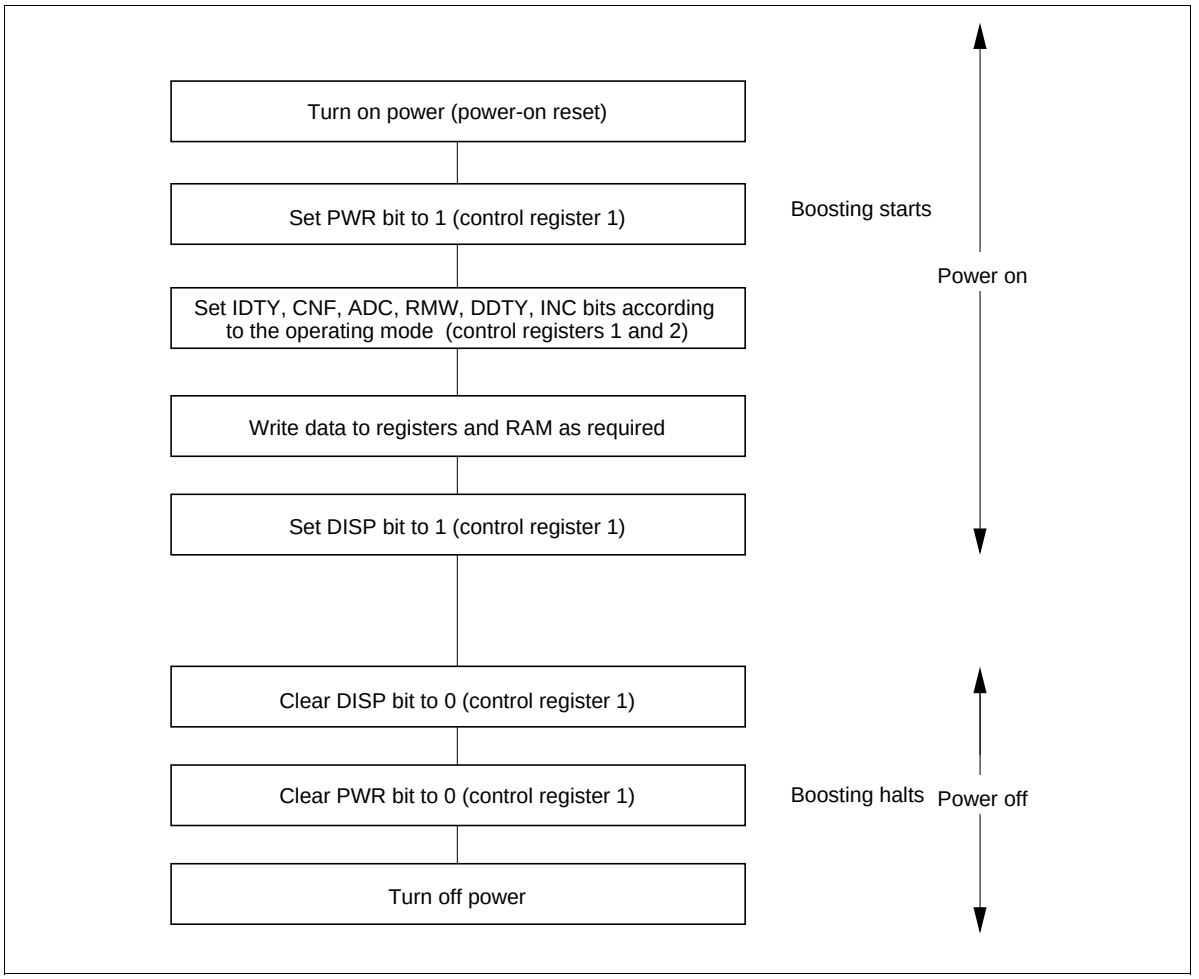


Figure 20 Procedure for Turning Power Supply On/Off

Annunciator Display Function

The HD66410 can display up to 72 dots of annunciator using 24 segment (column) drivers (SEG1 to SEG24) and three common (row) drivers (COM1 to COM3). These drivers, independent of the display RAM, operate statically or with a 1/3 duty cycle. They are available even during standby modes, where dot-matrix display and the internal booster is turned off, making them suitable for time and other mark indications with reduced power dissipation.

The dots to be displayed are designated by annunciator display data registers 1 to 9. For static drive, only display data registers 1, 3, and 7 and row driver COM1 are used. A maximum of 18 turned-on dots can be blinked. For details on blinking, see the Blink Function section. Figure 21 shows the relationship between annunciator display data register bits and display positions. In the figure, alphanumerics in the ovals indicate the bit names of annunciator display data registers. Data value 1 turns on the corresponding dot on the panel, and data value 0 turns off the corresponding dot. Table 2 lists the annunciator display data registers.

Table 2 Annunciator Display Data Register Bits

Register		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Annunciator display data register 1	A0	IC1A	IC1B	IC1C	IC1D	IC1E	IC1F	IC1G	IC1H
Annunciator display data register 2	A1	IC2A	IC2B	IC2C	IC2D	IC2E	IC2F	IC2G	IC2H
Annunciator display data register 3	A2	IC3A	IC3B	IC3C	IC3D	IC3E	IC3F	IC3G	IC3H
Annunciator display data register 4	A3	IC1I	IC1J	IC1K	IC1L	IC1M	IC1N	IC1O	IC1P
Annunciator display data register 5	A4	IC2I	IC2J	IC2K	IC2L	IC2M	IC2N	IC2O	IC2P
Annunciator display data register 6	A5	IC3I	IC3J	IC3K	IC3L	IC3M	IC3N	IC3O	IC3P
Annunciator display data register 7	A6	IC1Q	IC1R	IC1S	IC1T	IC1U	IC1V	IC1W	IC1X
Annunciator display data register 8	A7	IC2Q	IC2R	IC2S	IC2T	IC2U	IC2V	IC2W	IC2X
Annunciator display data register 9	A8	IC3Q	IC3R	IC3S	IC3T	IC3U	IC3V	IC3W	IC3X

Note: Only annunciator display data registers 1, 3, and 7 are used for static display.

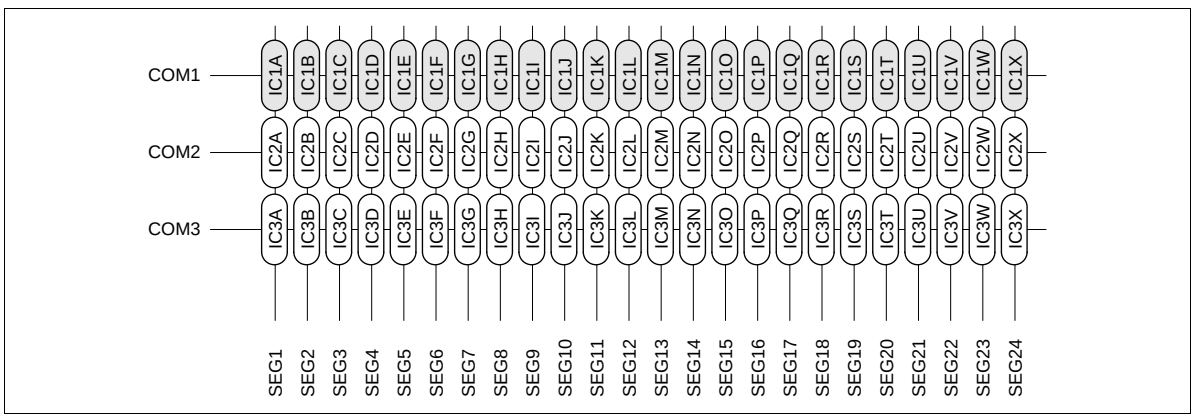


Figure 21 Annunciator Display Data and Display Positions

Oscillator

The HD66410 incorporates an R-C oscillator with low power-dissipation, in which the oscillation frequency can be adjusted by appropriate selection of oscillator resistor R_f and capacitor C_f. The adjusted clock signal is used for system internal circuits; thus, if this oscillator is not used, an appropriate clock signal must be externally input through the CR pin. In this case, the C and R pins must be left unconnected. Figure 22 shows oscillator connections.

Clock and Frame Frequency

The HD66410 generates the frame frequency (LCD drive frequency) by dividing the input clock frequency by 132. The division ratio is the same for all LCD duty cycles.

The frame frequency is usually 70 to 90 Hz; when the frame frequency is 80 Hz, for example, the input clock frequency must be 10.56 kHz.

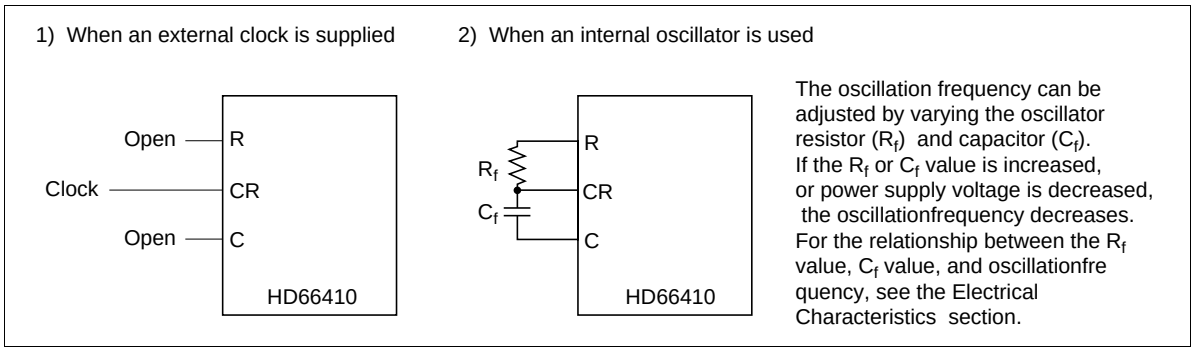
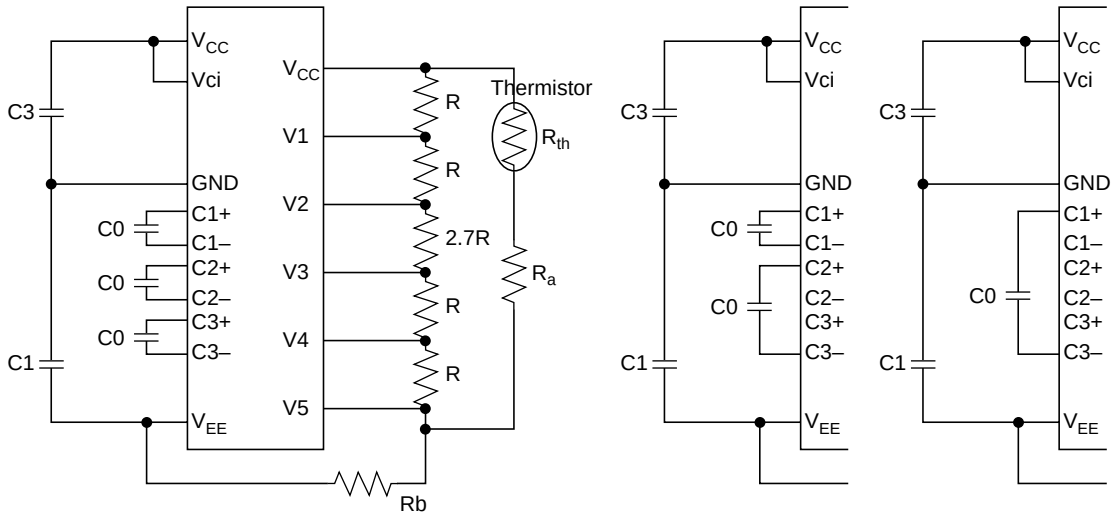


Figure 22 Oscillator Connections

Power Supply Circuits

The HD66410 incorporates a double to quadruple booster to supply power to LCD drivers. The booster is automatically turned off during standby mode, dissipating no power. If the current capacity provided is insufficient for the user system, external power supply circuits are necessary. In this case, the internal power supply can be turned off by register settings. Figure 23 shows examples of power supply circuits for different boosting ratios.

Booster: The internal booster raises the input voltage between V_{CC} and GND two to four times every raster by turning on the internal power supply with capacitors attached between C1+ and C1–, C2+ and C2–, C3+ and C3–, and to V_{EE}. The booster uses the system clock, and thus the internal oscillator must be operating to activate the booster (if the internal oscillator has been selected to generate the system clock). V_{EE} outputs V_{CC} level when the booster is inactive.



C0 ≥ 1.0 µF
C1 ≥ 2.2 µF

a) Quadruple boosting

C2–, C3+: open

b) Triple boosting

C1–, C2+, C2–, C3+: open

c) Double boosting

Notes: 1. Adjust the power supply voltage and capacitance of external capacitors according to the characteristics of the LCD used because the output voltage (V_{EE}) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors, and manufacturing tolerance. Refer to the Electrical Characteristics section for details.

2. Adjust the power supply voltage so that the output voltage (V_{EE}) after boosting will not exceed the absolute maximum rating of the LCD power supply voltage (13V).

3. Vci is both a reference voltage and power supply for the booster; it needs to be supplied with at least three times the current consumed by the LCD drivers including the current flowing in the resistive divider. Make sure that Vci is below V_{CC}.

4. V_{EE} terminal will be in high impedance state when DC/DC converter stops working. In this case V_{EE} level is pulled up to V_{CC} level with external resistors and the voltage supplied to the capacitor C1 is reserved. Do not use polarized capacitor to C1.

Figure 23 Power Supply Circuit Examples

LCD Drive Voltage Power Supply Levels: To drive the LCD, a 6-level power supply is necessary. These levels can be usually generated by dividing the V_{CC}–V5 power supply using resistive dividers. If the total resistance is small, current consumption increases, and if the total resistance is large, display quality degrades. Appropriate resistance should be selected for the user system.

Brightness Adjust: The booster drives liquid crystals with a voltage after raising the voltage supplied to the Vci pin two to four times. Accordingly, brightness can be adjusted by varying the Vci level. Attaching a thermister is recommended to vary the voltage according to the thermal characteristics of liquid crystals.

Annunciator: Annunciator has it's own power circuit apart from the main power circuit. Four power supply levels are used: these are V_{CC}, AV3 and two levels generated by dividing the V_{CC}–AV3 power supply using internal resistive dividers. The level of AV3 must be inside of V_{CC}–GND power supply or connected to GND unless bright adjust is used. Brightness of annunciator can be adjusted by inseriting a resistor into between AV3 and GND. The value of this resistor might be several hundred kilo-ohm because the value of internal resistor is around one mega-ohm. Figure 24 shows the power circuit for annunciator.

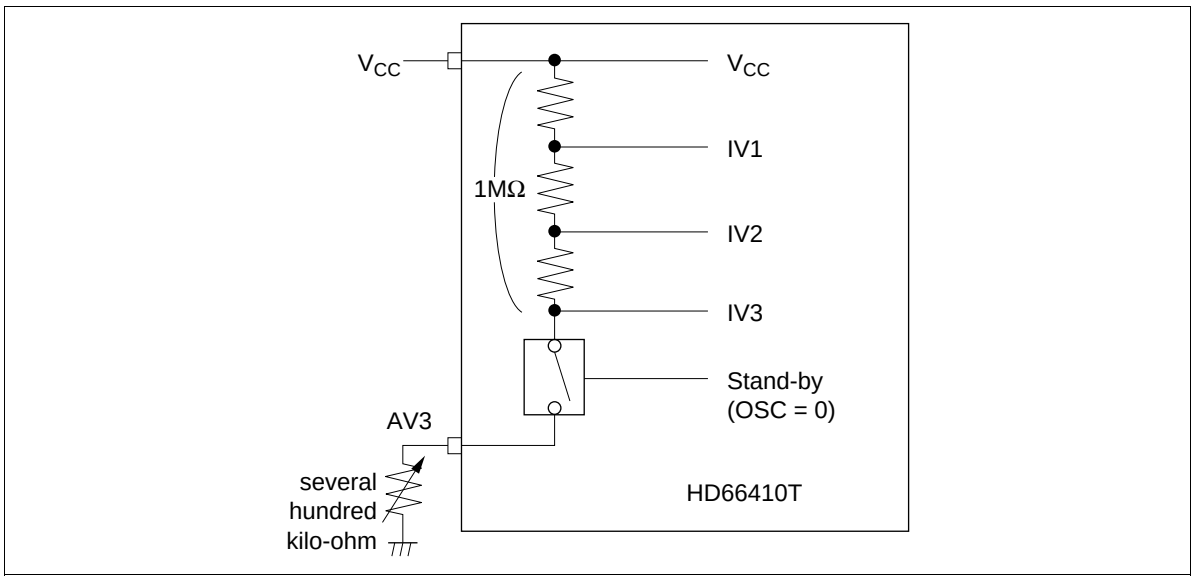


Figure 24 Power Circuit for Annunciator

Row/Column Output Switchover: LCD column drivers use V_{CC}, V2, V3, and V5, while row drivers use V_{CC}, V1, V4, and V5. These voltage levels are switched to AC and are output to an LCD panel. Since the HD66410 can assign X1 to X16 and X129 to X144 to either row or column output, the power supply connection must be externally changed according to the assignment, which is determined by the CNF bit value in control register 1. The select and deselect levels for row output are temporarily output from the VCHO and VCLO pins, and the two levels for column output are output from the VSHO and VSLO pins; these outputs must be connected according to row and column output assignment as shown in Figure 25.

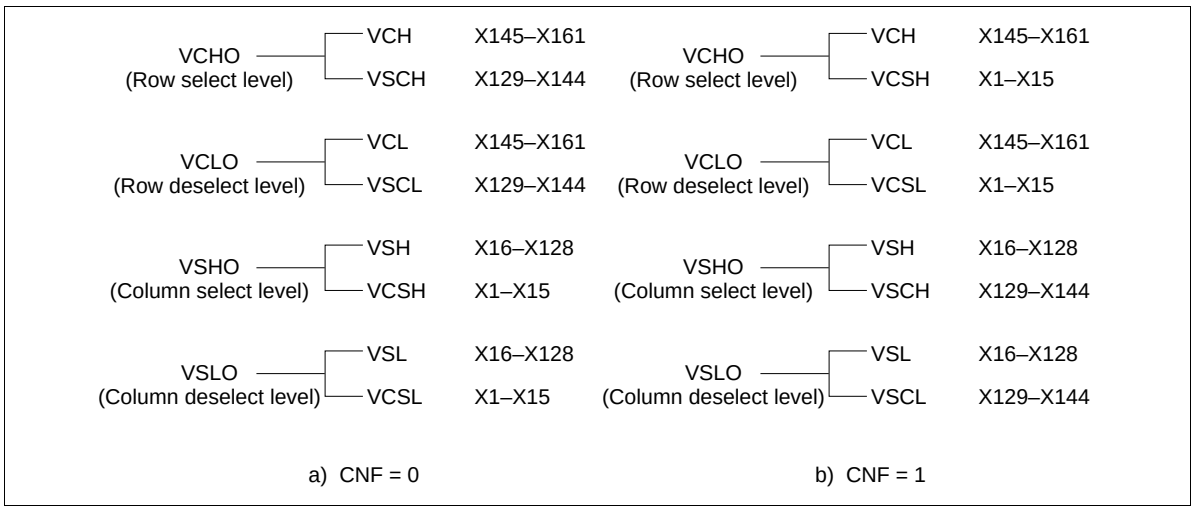


Figure 25 Connection of LCD Drive Voltage Level Pins

Reset

The low $\overline{RES}$ signal initializes the HD66410, clearing all the bits in the internal registers. During reset, the internal registers cannot be accessed.

Note that if the reset conditions specified in the Electric Characteristics section are not satisfied, the HD66410 will not be correctly initialized. In this case, the internal registers of the HD66410 must be initialized by software.

Initial Setting of Internal Registers: All the internal register bits are cleared to 0. Details are listed below.

- The data in index register is not affected
- The data in the internal RAM are not affected
- All counters are cleared to zero
- Modes after reset
  - — Normal operation
  - — Oscillator is active
  - — Display is off (including annunciator display)
  - — Booster is not used
  - — Y address of display RAM is incremented
  - — 1/33 duty cycle
  - — X and Y addresses are 0
  - — Data in address H'0 is output from the X1 pin
  - — Blink function is inactive

Initial Setting of Pins:

- Bus interface pins

  During reset, the bus interface pins do not accept signals to access internal registers; data is undefined when read.
- LCD driver output pins

  During reset, all the LCD driver output pins (X1 to X161, SEG1 to SEG33, COM1 to COM3) output V_{CC}-level voltage, regardless of data value in the display RAM, turning off the LCD. Here, the output voltage is not alternated. Note that the same voltage (V_{CC}) is applied to both column and row output pins to prevent liquid crystals from degrading.
- Booster output pins

  Since the PWR bit in control register 1 is 0 during reset, the booster halts. Accordingly, the output state of the V_{EE} pin depends on the value of the booster's external capacitor.

Internal Registers

The HD66410 has one index register and 22 data registers, all of which can be accessed asynchronously with the internal clock. All the registers except the display memory access register are write-only. Accessing unused bits or addresses affects nothing; unused bits should be set to 0 when written to.

Index Register (IR): The index register (Figure 26) selects one of 22 data registers. The index register itself is selected when both the $\overline{CS}$ and RS signals are low. Data bits 7 to 5 are unused; they should be set to 0 when written to.

Control Register 1 (R0): Control register 1 (Figure 27) controls general operations of the HD66410. Each bit has its own function as described below. Data bit 7 bit is unused; it should be set to 0 when written to.

- DSP bit
  DSP = 1: Display on
  DSP = 0: Display off (all LCD driver output pins output V_{CC} level)
- STBY bit
  STBY = 1: Internal operation and booster halt; display off
  STBY = 0: Normal operation
  The STBY bit does not affect the state of PWR and DISP bit.
- PWR bit
  PWR = 1: Booster active
  PWR = 0: Booster inactive
- OSC bit
  OSC = 1: Internal operation and booster halt; oscillator does not halt to provide annunciator display
  OSC = 0: Internal operation, booster, and oscillator halt
  The OSC bit is valid only when the STBY bit is 1.
- IDTY bit
  IDTY = 1: Annunciator display signals are operating statically
  IDTY = 0: Annunciator display signals are operating with 1/3 duty cycle
- CNF bit
  CNF = 1: Row output on both sides of the LCD panel
  CNF = 0: Row output on one side of the LCD panel
- ADC bit
  ADC = 1: Data in X address H'0 is output from X128 or X144; row signals are scanned from X129 to X161.
  ADC = 0: Data in X address H'0 is output from X1 or X17; row signals are scanned from X161 to X129.

	Data bit	7	6	5	4	3	2	1	0
IR	Set value				Register number				

Figure 26 Index Register (IR)

	Data bit	7	6	5	4	3	2	1	0
R0	Set value		DISP	STBY	PWR	OSC	IDTY	CNF	ADC

Figure 27 Control Register 1 (R0)

Control Register 2 (R1): Control register 2 (Figure 28) controls general operations of the HD66410. Each bit has its own function as described below. Data bits 7 to 4 are unused; they should be set to 0 when written to.

- RMW bit

  RMW = 1: Read-modify-write mode

  Address is incremented only after write access

  RMW = 0: Address is incremented after both write and read accesses
- DDTY bit

  DDTY = 1: 1/17 display duty cycle

  DDTY = 0: 1/33 display duty cycle
- INC bit

  INC = 1: X address is incremented for each access

  INC = 0: Y address is incremented for each access
- BLK bit

  BLK = 1: Blink function is used

  BLK = 0: Blink function is not used

  The blink counter is reset when the BLK bit is set to 0. It starts counting and at the same time initiates blinking when the BLK bit is set to 1.

X Address Register (R2): The X address register (Figure 29) designates the X address of the display RAM to be accessed by the MPU. The set value must range from H'0 to H'F; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bits 7 to 4 are unused; they should be set to 0 when written to.

Y Address Register (R3): The Y address register (Figure 30) designates the Y address of the display RAM to be accessed by the MPU. The set value must range from H'00 to H'20; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bit 7 is unused; it should be set to 0 when written to.

	Data bit	7	6	5	4	3	2	1	0
R1	Set value					RMW	DDTY	INC	BLK

Figure 28 Control Register 2 (R1)

	Data bit	7	6	5	4	3	2	1	0
R2	Set value					XA3	XA2	XA1	XA0

Figure 29 X Address Register (R2)

	Data bit	7	6	5	4	3	2	1	0
R3	Set value			YA5	YA4	YA3	YA2	YA1	YA0

Figure 30 Y Address Register (R3)

Display Memory Access Register (R4): The display memory access register (Figure 31) is used to access the display RAM. If this register is write-accessed, data is directly written to the display RAM. If this register is read-accessed, data is first latched to this register from the display RAM and sent out to the data bus on the next read; therefore, a dummy read access is necessary after setting the display RAM address.

Display Start Raster Register (R5): The display start raster register (Figure 32) designates the raster to be displayed at the top of the LCD panel. Varying the set value scrolls the display vertically. The set value must be one less than the actual top raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. If the value is set outside these ranges, data may not be displayed correctly. Data bits 7 and 6 are unused; they should be set to 0 when written to.

Blink Registers (R6, R7): The blink bit registers (Figure 33) designate the 8-bit groups to be blinked. Setting a bit to 1 blinks the corresponding 8-bit group. Any number of groups can be blinked; setting all the bits to 1 will blink the entire LCD panel. These bits are valid only when the BLK bit of control register 2 is 1.

	Data bit	7	6	5	4	3	2	1	0
R4	Set value	D7	D6	D5	D4	D3	D2	D1	D0

Figure 31 Display Memory Access Register (R4)

	Data bit	7	6	5	4	3	2	1	0
R5	Set value			ST5	ST4	ST3	ST2	ST1	ST0

Figure 32 Display Start Raster Register (R5)

	Data bit	7	6	5	4	3	2	1	0
R6	Set value	BK0	BK1	BK2	BK3	BK4	BK5	BK6	BK7
R7	Set value	BK8	BK9	BK10	BK11	BK12	BK13	BK14	BK15

Figure 33 Blink Registers (R6, R7)

Blink Start Raster Register (R8): The blink start raster register (Figure 34) designates the top raster in the area to be blinked. The set value must be one less than the actual top raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. If the value is set outside these ranges, operations may not be correct. Data bits 7 and 6 are unused; they should be set to 0 when written to.

Blink End Raster Register (R9): The blink end raster register (Figure 35) designates the bottom raster in the area to be blinked. The area to be blinked is designated by the blink registers, blink start raster register, and blink end raster register. The set value must be one less than the actual bottom raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. It must also be greater than the value set in the blink start raster register. If an inappropriate value is set, operations may not be correct. Data bits 7 and 6 are unused; they should be set to 0 when written to.

	Data bit	7	6	5	4	3	2	1	0
R8	Set value			BSL5	BSL4	BSL3	BSL2	BSL1	BSL0

Figure 34 Blink Start Raster Register (R8)

	Data bit	7	6	5	4	3	2	1	0
R9	Set value			BEL5	BEL4	BEL3	BEL2	BEL1	BEL0

Figure 35 Blink End Raster Register (R9)

Annunciator Display Data Registers (A0 to A8): The annunciator display data registers (Figure 36) store data for annunciator (icon) display. Setting a data bit to 1 turns on the corresponding dot on the LCD panel.

Annunciator Blink Registers (A9 to A11): The annunciator blink registers (Figure 37) designate bits to be blinked on the annunciator display. For details, see the Blink Function section.

- IPn1, IPn0 bits (n = 1, 2, 3)
  These bits select annunciator blocks to be blinked.
  IPn1, IPn0 = 0, 0: Block 0 is selected (SEG1 to SEG6)
  IPn1, IPn0 = 0, 1: Block 1 is selected (SEG7 to SEG12)
  IPn1, IPn0 = 1, 0: Block 2 is selected (SEG13 to SEG18)
  IPn1, IPn0 = 1, 1: Block 3 is selected (SEG19 to SEG24)
- IBn5, IBn0 bits (n = 1, 2, 3)
  These bits select bits to be blinked in the selected blocks.

	Data bit	7	6	5	4	3	2	1	0
A0	Set value	IC1A	IC1B	IC1C	IC1D	IC1E	IC1F	IC1G	IC1H
A1	Set value	IC2A	IC2B	IC2C	IC2D	IC2E	IC2F	IC2G	IC2H
A2	Set value	IC3A	IC3B	IC3C	IC3D	IC3E	IC3F	IC3G	IC3H
A3	Set value	IC1I	IC1J	IC1K	IC1L	IC1M	IC1N	IC1O	IC1P
A4	Set value	IC2I	IC2J	IC2K	IC2L	IC2M	C2N	IC2O	IC2P
A5	Set value	IC3I	IC3J	IC3K	IC3L	IC3M	C3N	IC3O	IC3P
A6	Set value	IC1Q	IC1R	IIC1S	IC1T	IC1U	IIC1V	IIC1W	IC1X
A7	Set value	IC2Q	IC2R	IC2S	IC2T	IC2U	IC2V	IC2W	IC2X
A8	Set value	IC3Q	IC3R	IC3S	IC3T	IC3U	IC3V	IC3W	IC3X

Figure 36 Annunciator Display Data Registers (A0 to A8)

	Data bit	7	6	5	4	3	2	1	0
A9	Set value	IP11	IP10	IB15	IB14	IB13	IB12	IB11	IB10
A10	Set value	IP21	IP20	IB25	IB24	IB23	IB22	IB21	IB20
A11	Set value	IP31	IP30	IB35	IB34	IB33	IB32	IB31	IB30

Figure 37 Annunciator Blink Registers (A9 to A11)

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuits	V_{EE}	V_{CC} – 18.0 to V_{CC} + 0.3	V	
Input voltage 1		VT1	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2		VT2	V5 – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature		T_{opr}	–30 to +75	°C	
Storage temperature		T_{stg}	–55 to +110	°C	

Notes: 1. Measured relative to GND.
2. Applies to pins CR, DB7 to DB0, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, RS, $\overline{RES}$, TEST0.
3. Applies to pins V1, V2, V3, V4, V5, VSH, VSL, VCH, VCL, VSCH, VSCL, VCSH, VCSL.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics to prevent malfunction or unreliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.2 to 5.5V, GND = 0V, V_{CC}–V5 = 6 to 15V, Ta = –30 to +75°C)[*8]

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input leakage current (1)	I_{IL1}		–1	—	1	µA	Vin = V_{CC} to GND	1
Input leakage current (2)	I_{IL2}		–10	—	10	µA	Vin = V_{CC} to V5	2
Driver "on" resistance	R_{ON}	X1 to X161			20	kΩ	I_{ON} = 100 µA V_{CC}–V5 = 8V	3
Input high voltage	V_{IH1}		0.8 × V_{CC}	—	V_{CC}	V		1
Input low voltage	V_{IL1}		0	—	0.2 × V_{CC}	V		1
Output high voltage	V_{OH}	DB7 to DB0	0.8 × V_{CC}	—	V_{CC}	V	I_{OH} = –50 µA	
Output low voltage	V_{OL}	DB7 to DB0	0	—	0.2 × V_{CC}	V	I_{OL} = 50 µA	
Current consumption during display	I_{disp}		—	55	80	µA		4, 5
Current consumption during annunciator display	I_{ann}		—	17	30	µA		4, 6
Current consumption during standby	I_{stb}		—	0.1	5	µA		4, 7

Notes:
1. Applies to pins: $\overline{CS}$, RS, $\overline{WR}$, $\overline{RD}$, $\overline{RES}$, CR, TEST0, DB7 to DB0
2. Applies to pins: V1, V2, V3, V4, VCH, VCL, VSH, VSL, VCSH, VCSL, VSCH, VSCL
3. Indicates the resistance between one pin from X1 to X161 and another pin from V1, V2, V3 and V4. VCHO, VCLO, VSHO, VSLO and VCH, VCL, VSH, VSL, VCSH, VCSL, VSCH, VSCL are connected according to the configuration. V1 and V2 should be near V_{CC} level, and V3 and V4 should be near V5 level. All voltage must be within ΔV. ΔV is the range within which R_{ON} is stable. V1 to V4 levels should keep following condition: $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$
4. Input and output current are excluded. When a CMOS input is floating, excess current flows from power supply to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively. The current which flows at resistive divider and LCD are excluded. When the unmolded side of LSI is exposed to light, exess current flows. Use under sealded condition.
5. Specified under following conditions:
   Internal oscillator is used; Rf = 470 kΩ, Cf = 100 pF
   Triple boosting is used; C0 = 1.0 µF, C1 = 2.2 µF
   V_{CC} = Vci = 3.0V, V5 = V_{EE}, AV3 = GND, Ta = 25°C
   Checker board is displayed
   No access from MPU
6. Measured when STB bit is 1 and OSC bit is 1.
   Internal oscillator is used; Rf = 470 kΩ, Cf = 100 pF
   V_{CC} = 3.0V, AV3 = GND
7. Measured when STB bit is 1 and OSC bit is 0. V_{CC} = 3.0V, All LCD driving outputs, X1 to X161, output V_{CC} level, so no current is consumed at the resistive divider.
8. Specified at +75°C for die products.

Booster Characteristics (V_{CC} = 2.2 to 5.5V, GND = 0V, V_{CC}–V5 = 6 to 15V, Ta = –30 to +75°C)[*3]

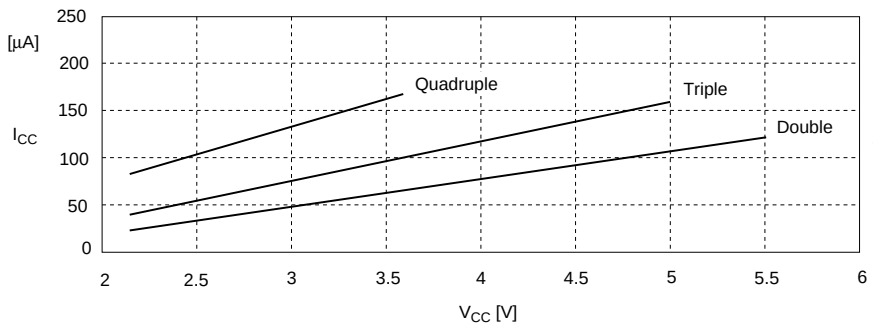
Item	Symbol	Min.	Typ	Max	Unit	Measurement Condition	Notes
Output voltage	V_{EE}	V_{CC}–10	V_{CC}–11	V_{CC}–12	V		1
Input voltage	V_{ci}	—	—	5.5	V		2

Notes: 1. Measured when V_{CC} = Vci = 3.0V, Io (load current) = 0.25 mA, C0 = 1 µF, C1 = 2.2 µF
f_{OSC} (oscillation frequency) = 10 kHz, and the input voltage is boosted four times.
2. Input voltage must be below V_{CC}. Keep the voltage which is generated with DC/DC counter below the maximum voltage of V_{CC}–V5. If this restriction is not kept, LSI may be destroyed.
3. Specified at +75°C for die products.

Current Consumption

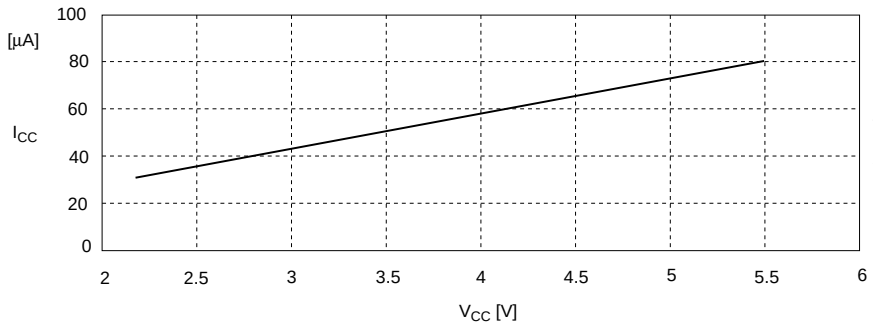
Current consumption are shown below under various conditions. These values are shown as a reference, and are not guaranteed.

Current Consumption during Display 1



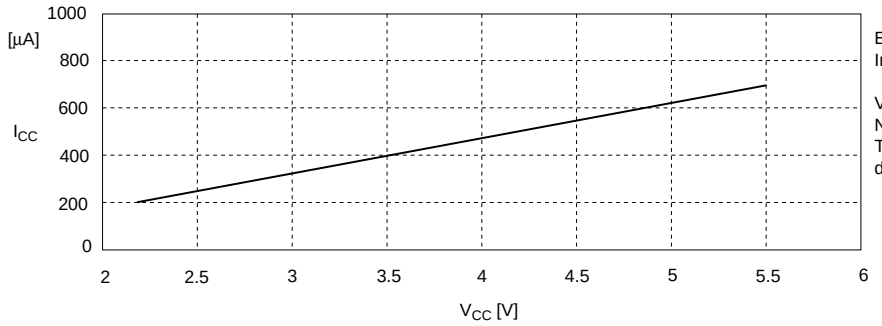
Internal booster is used;
V_{CC} = Vci
C0 = 1.0 µF, C1 = 2.2 µF
Internal oscillator is used:
Cf = 100 pF, Rf = 470 kΩ
$V5 = V_{EE}$
No access from MPU
The current whih flows at resistive divider and LCD are excluded.

Current Consumption during Display 2



Internal triple booster is used;
V_{CC} = Vci
C0 = 1.0 µF, C1 = 2.2 µF
External clock: 10 kHz
$V5 = V_{EE}$
No access from MPU
The current whih flows at resistive divider and LCD are excluded.

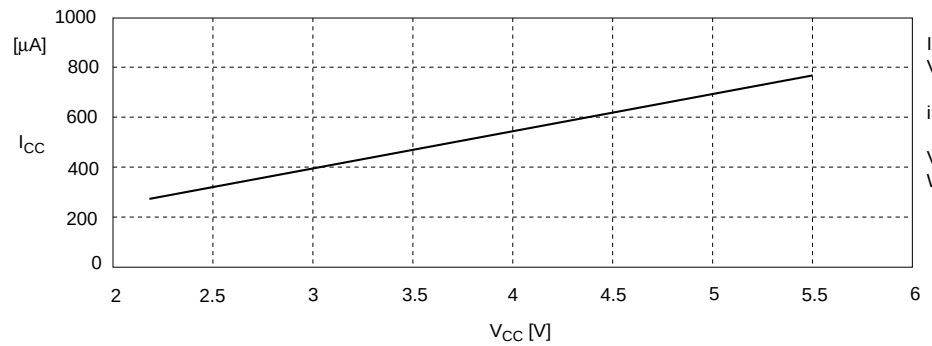
Current Consumption during Display 3



External power is supplied to V5
Internal oscillator is used:
Cf = 100 pF, Rf = 470 kΩ
V5 = 10V
No access from MPU
The current which flows at resistive divider and LCD are excluded.

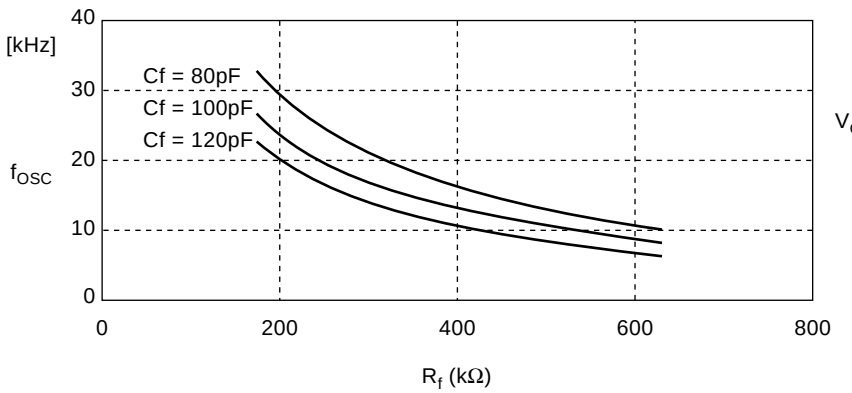
Note : When the external power supply is supplied to V5, this voltage must be less than five times V_{CC}

Current Consumption during being accessed form MPU



Internal booster is used:
V_{CC} = Vci
C0 = 1.0 µF, C1 = 2.2 µF
internal oscillator is used:
Cf = 100 pF, Rf = 470 kΩ
V5 = V_{EE}
Writing checker board data

Oscillation Frequency



V_{CC} = 3.0V

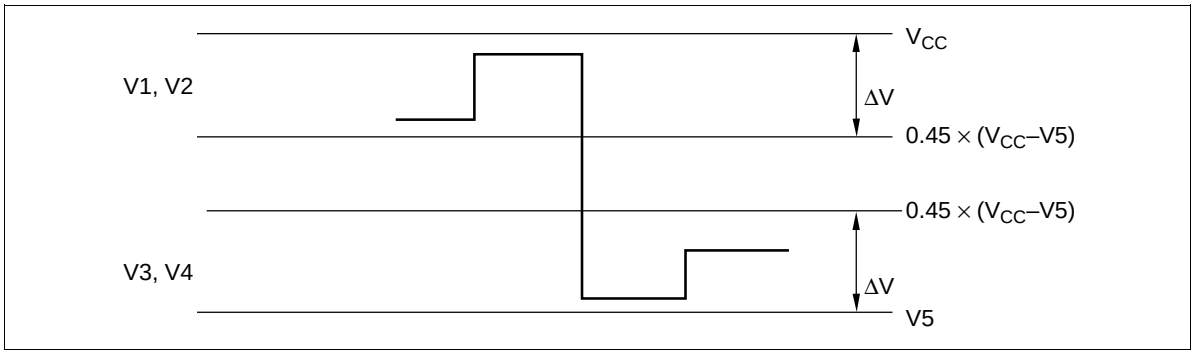


Figure 38 Limitation of V1 to V4 Levels

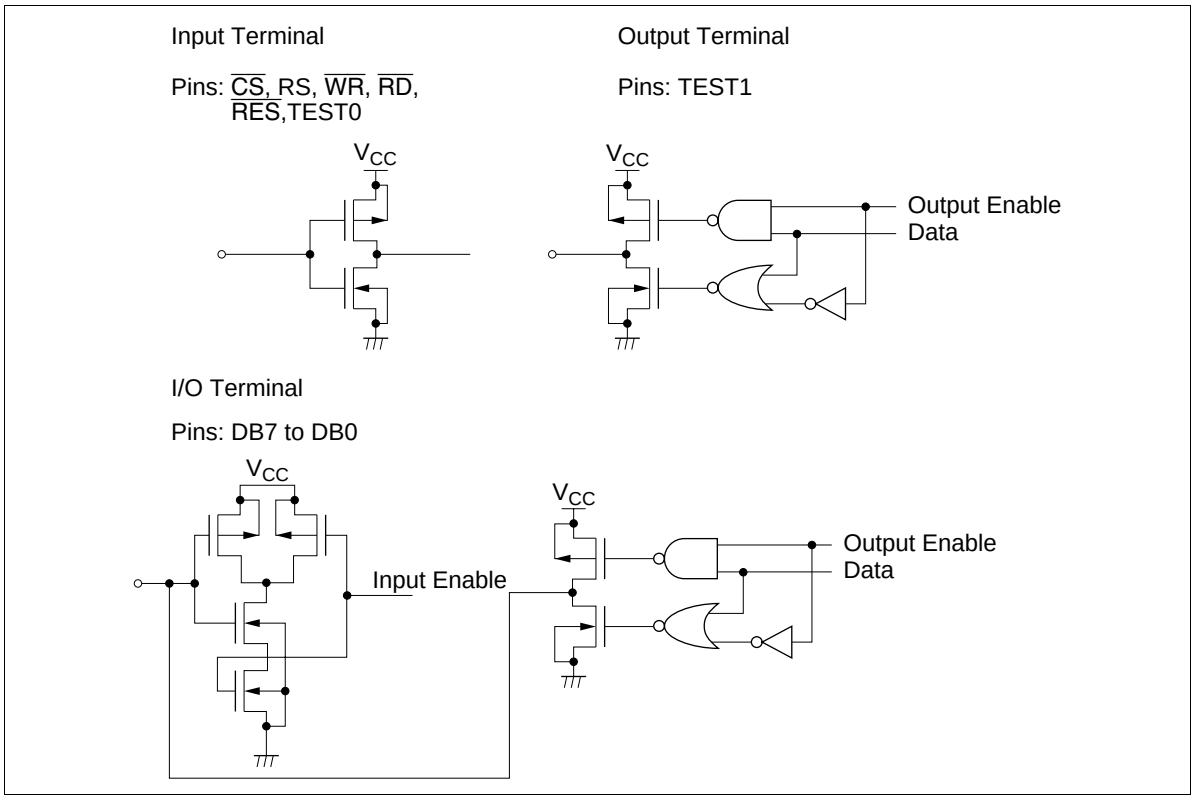


Figure 39 Terminal Configuration

AC Characteristics 1 (V_{CC} = 2.2 to 4.5V, GND = 0V, Ta = –30 to +75°C)[*3]

Clock Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
Oscillation frequency	f_{OSC}	7	10	13	kHz	Cf = 100 pF, Rf = 470 kΩ
External clock frequency	f_{CP}	7	10	20	kHz	
External clock duty cycle	Duty	45	50	55	%	
External clock fall time	t_r	—	—	0.2	µS	
External clock rise time	t_f	—	—	0.2	µS	

MPU Interface

Item	Symbol	Min	Typ	Max	Unit	Notes
$\overline{RD}$ low-level width	t_{WRDL}	450	—	tcyc/2–450	ns	1, 2
$\overline{RD}$ high-level width	t_{WRDH}	450	—	—	ns	1
$\overline{WR}$ low-level width	t_{WWRL}	450	—	tcyc/2–450	ns	1, 2
$\overline{WR}$ high-level width	t_{WWRH}	450	—	—	ns	1
Address setup time	t_{AS}	10	—	—	ns	
Address hold time	t_{AH}	10	—	—	ns	
Data delay time	t_{DDR}	—	—	360	ns	
Data output hold time	t_{DHR}	10	—	—	ns	
Data setup time	t_{DSW}	150	—	—	ns	
Data hold time	t_{DHW}	10	—	—	ns	

MPU Interface

Item	Symbol	Min	Typ	Max	Unit	Notes
$\overline{RES}$ low-level width	t_{RES}	1	—	—	ms	

Notes 1. tcyc is a period of the clock.

2. Keep these specifications even if $\overline{CS}$ is high. If these conditions are not kept, display flickering may happen.

3. Specified at +75°C for die products.

AC Characteristics 2 (V_{CC} = 4.5V to 5.5V, GND = 0V, Ta = –30 to +75°C)[*3]

Clock Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
Oscillation frequency	f_{OSC}	8	11.5	14	kHz	Cf = 100 pF, Rf = 470 kΩ
External clock frequency	f_{CP}	7	—	20	kHz	
External clock duty cycle	Duty	45	50	55	%	
External clock fall time	t_r	—	—	0.2	µS	
External clock rise time	t_f	—	—	0.2	µS	

MPU Interface

Item	Symbol	Min	Typ	Max	Unit	Notes
$\overline{RD}$ low-level width	t_{WRDL}	450	—	tcyc/2–450	ns	1, 2
$\overline{RD}$ high-level width	t_{WRDH}	450	—	—	ns	1
$\overline{WR}$ low-level width	t_{WWRL}	450	—	tcyc/2–450	ns	1, 2
$\overline{WR}$ high-level width	t_{WWRH}	450	—	—	ns	1
Address setup time	t_{AS}	10	—	—	ns	
Address hold time	t_{AH}	10	—	—	ns	
Data delay time	t_{DDR}	—	—	360	ns	
Data output hold time	t_{DHR}	10	—	—	ns	
Data setup time	t_{DSW}	150	—	—	ns	
Data hold time	t_{DHW}	20	—	—	ns	

MPU Interface

Item	Symbol	Min	Typ	Max	Unit	Notes
$\overline{RES}$ low-level width	t_{RES}	1	—	—	ms	

Notes 1. tcyc is a period of the clock.

2. Keep these specifications even if $\overline{CS}$ is high. If these conditions are not kept, display flickering may happen.

3. Specified at +75°C for die products.

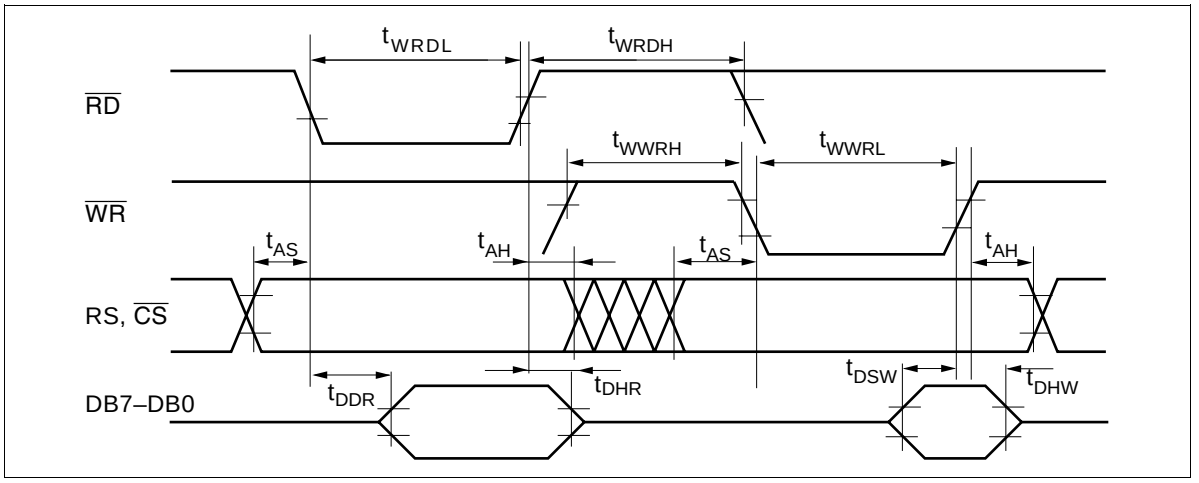


Figure 40 MPU Interface

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