HM5212325FBPC-B60

128M LVTTL interface SDRAM
100 MHz
1-Mword × 32-bit × 4-bank
PC/100 SDRAM

HITACHI

ADE-203-1122B (Z)
Preliminary
Rev. 0.2
Feb. 29, 2000

Description

The Hitachi HM5212325FBPC is a 128-Mbit SDRAM organized as 1048576-word × 32-bit × 4-bank. All inputs and outputs are referred to the rising edge of the clock input. It is packaged in standard 90-bump fine pitch BGA.

Features

- Single chip wide bit solution (× 32)
- 3.3 V power supply
- Clock frequency: 100 MHz (max)
- LVTTL interface
- Extremely small foot print: 0.8 mm pitch
  - Package: FBGA (BP-90)
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 4/8/full page
- 2 variations of burst sequence
  - Sequential (BL = 4/8/full page)
  - Interleave (BL = 4/8)
- Programmable $\overline{\text{CAS}}$ latency: 2/3
- Byte control by DQMB
- Refresh cycles: 4096 refresh cycles/64 ms

Preliminary: The Specifications of this device are subject to change without notice. Please contact to your nearest Hitachi's sales Dept. regarding specifications.

Hitachi semiconductor

- 2 variations of refresh
  - — Auto refresh
  - — Self refresh
- Full page burst length capability
  - — Sequential burst
  - — Burst stop capability

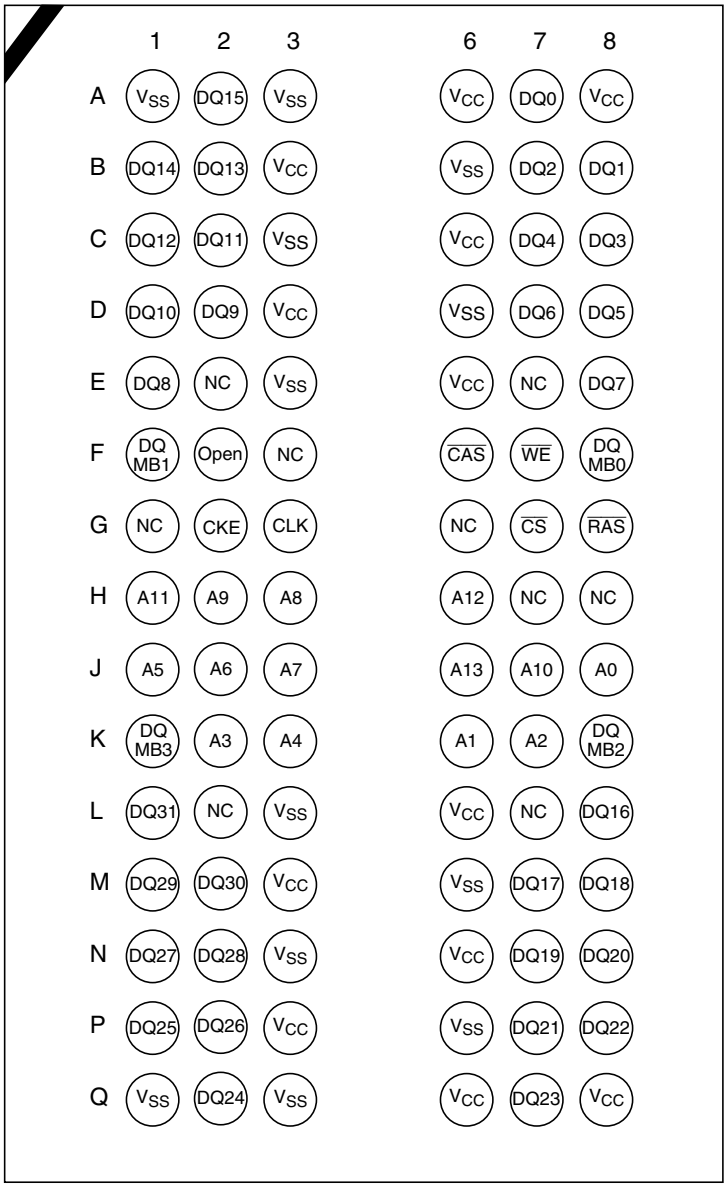
Ordering Information

Type No.	Frequency	$\overline{\text{CAS}}$ latency	Package
HM5212325FBPC-B60*	100 MHz	3	10 mm × 13 mm 90 bump FBGA (BP-90)

Note: 66 MHz operation at $\overline{\text{CAS}}$ latency = 2.

Pin Arrangement

90-bump FBGA



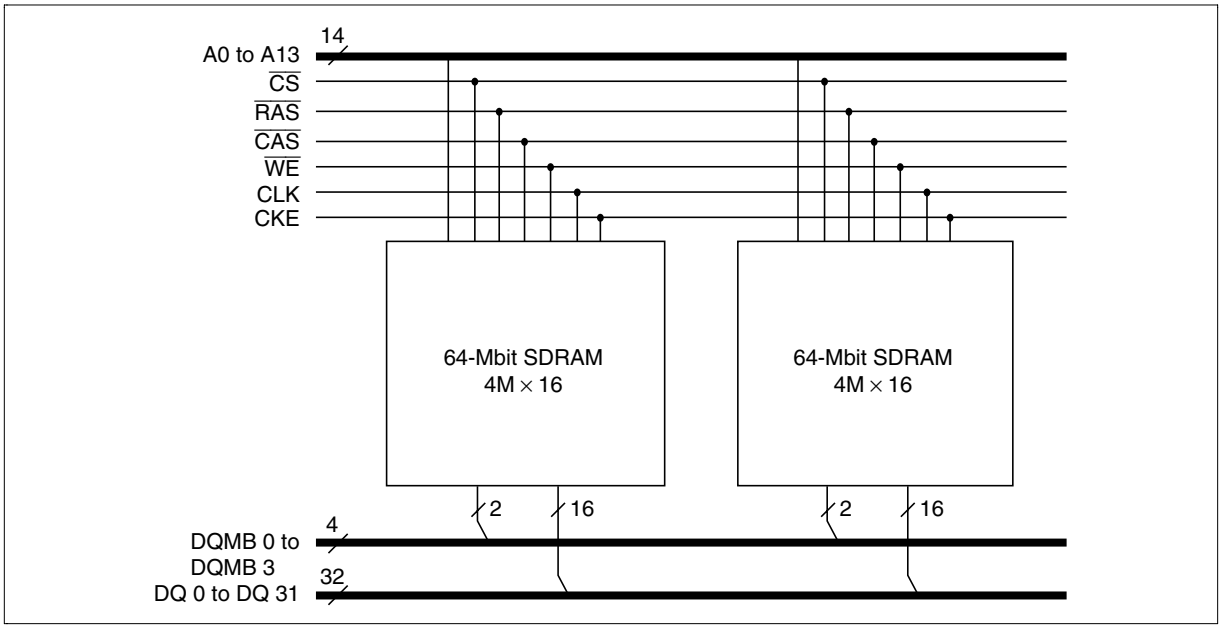
(Top view)

Pin Description

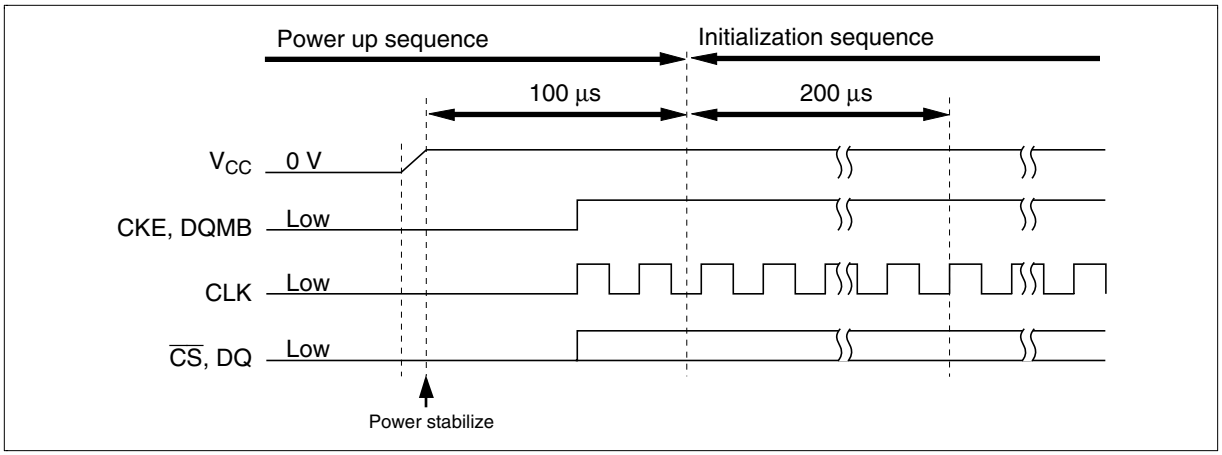
Pin name	Function
A0 to A13	Address input Row address A0 to A11 Column address A0 to A7 Bank select address A12/A13 (BS)
DQ0 to DQ31	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
DQMB0 to DQMB3	Byte data mask*1
CLK	Clock input
CKE	Clock enable
V_{CC}	Power supply
V_{SS}	Ground
Open	Open*2

Note: 1. DQMB0: DQ0 to DQ7
DQMB1: DQ8 to DQ15
DQMB2: DQ16 to DQ23
DQMB3: DQ24 to DQ31
2. Don't connect. Internally connected with die.

Block Diagram



Power-up Sequence and Initialization Sequence



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Operating temperature	Topr	0 to +70 (Tj max = 110)	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Respect to V_{SS}.

DC Operating Conditions (Tcase = 0 to +70°C [Tj max = 110°C])

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.6	V	1, 2
	V_{SS}	0	0	V	3
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	1, 4
Input low voltage	V_{IL}	–0.3	0.8	V	1, 5

Notes: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.
4. V_{IH} (max) = V_{CC} + 2.0 V for pulse width ≤ 3 ns at V_{CC}.
5. V_{IL} (min) = V_{SS} – 2.0 V for pulse width ≤ 3 ns at V_{SS}.

DC Characteristics

(Tcase = 0 to +70°C [Tj max = 110°C]), V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HM5212325F				
		-B60				
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current ($\overline{CAS}$ latency = 2)	I_{CC1}	—	100	mA	Burst length = 1 t_{RC} = min	1, 2, 3
($\overline{CAS}$ latency = 3)	I_{CC1}	—	110	mA		
Standby current in power down	I_{CC2P}	—	6	mA	CKE = V_{IL}, t_{CK} = 12 ns	6
Standby current in power down (input signal stable)	I_{CC2PS}	—	4	mA	CKE = V_{IL}, t_{CK} = ∞	7
Standby current in non power down	I_{CC2N}	—	32	mA	CKE, $\overline{CS}$ = V_{IH}, t_{CK} = 12 ns	4
Standby current in non power down (input signal stable)	I_{CC2NS}	—	18	mA	CKE = V_{IH}, t_{CK} = ∞	9
Active standby current in power down	I_{CC3P}	—	8	mA	CKE = V_{IL}, t_{CK} = 12 ns	1, 2, 6
Active standby current in power down (input signal stable)	I_{CC3PS}	—	6	mA	CKE = V_{IL}, t_{CK} = ∞	2, 7
Active standby current in non power down	I_{CC3N}	—	40	mA	CKE, $\overline{CS}$ = V_{IH}, t_{CK} = 12 ns	1, 2, 4
Active standby current in non power down (input signal stable)	I_{CC3NS}	—	30	mA	CKE = V_{IH}, t_{CK} = ∞	2, 9
Burst operating current ($\overline{CAS}$ latency = 2)	I_{CC4}	—	110	mA	t_{CK} = min, BL = 4	1, 2, 5
($\overline{CAS}$ latency = 3)	I_{CC4}	—	135	mA		
Refresh current	I_{CC5}	—	190	mA	t_{RC} = min	3
Self refresh current	I_{CC6}	—	2	mA	$V_{IH} \geq V_{CC}$ – 0.2 V $V_{IL} \leq$ 0.2 V	8
Self refresh current (L-version)	I_{CC6}	—	0.8	mA		
Input leakage current	I_{LI}	–2	2	µA	0 ≤ Vin ≤ V_{CC}	
Output leakage current	I_{LO}	–3	3	µA	0 ≤ Vout ≤ V_{CC} DQ = disable	
Output high voltage	V_{OH}	2.4	—	V	I_{OH} = –4 mA	
Output low voltage	V_{OL}	—	0.4	V	I_{OL} = 4 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CLK operating current.
7. After power down mode, no CLK operating current.
8. After self refresh mode set, self refresh current.
9. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (CLK)	C_{I1}	4	8	pF	1, 2, 4
Input capacitance (Input except DQM)	C_{I2}	4	8	pF	1, 2, 4
Input capacitance (DQM)	C_{I3}	2	5	pF	1, 2, 4
Output capacitance (DQ)	C_O	2	5	pF	1, 2, 3, 4

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1 MHz, 1.4 V bias, 200 mV swing.
3. DQMB = V_{IH} to disable Dout.
4. This parameter is sampled and not 100% tested.

AC Characteristics

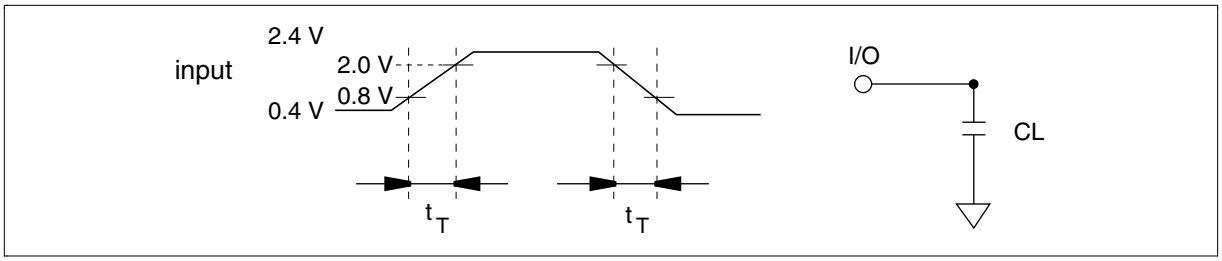
(Tcase = 0 to +70°C [Tj max = 110°C]), V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

			HM5212325F-B60			
Parameter	**HITACHI Symbol**	**PC/100 Symbol**	**Min**	**Max**	**Unit**	**Notes**
System clock cycle time ($\overline{CAS}$ latency = 2)	t_{CK}	Tclk	15	—	ns	1
($\overline{CAS}$ latency = 3)	t_{CK}	Tclk	10	—	ns	
CLK high pulse width	t_{CKH}	Tch	3	—	ns	1
CLK low pulse width	t_{CKL}	Tcl	3	—	ns	1
Access time from CLK ($\overline{CAS}$ latency = 2)	t_{AC}	Tac	—	8	ns	1, 2
($\overline{CAS}$ latency = 3)	t_{AC}	Tac	—	6	ns	
Data-out hold time	t_{OH}	Toh	3	—	ns	1, 2
CLK to Data-out low impedance	t_{LZ}		2	—	ns	1, 2, 3
CLK to Data-out high impedance	t_{HZ}		—	6	ns	1, 4
Input setup time	t_{AS}, t_{CS}, t_{DS}, t_{CES}	Tsi	2	—	ns	1, 5, 6
CKE setup time for power down exit	t_{CESP}	Tpde	2	—	ns	1
Input hold time	t_{AH}, t_{CH}, t_{DH}, t_{CEH}	Thi	1	—	ns	1, 5
Ref/Active to Ref/Active command period	t_{RC}	Trc	70	—	ns	1
Active to Precharge command period	t_{RAS}	Tras	50	120000	ns	1
Active command to column command (same bank)	t_{RCD}	Trcd	20	—	ns	1
Precharge to active command period	t_{RP}	Trp	20	—	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	Tdpl	10	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	Trrd	20	—	ns	1
Transition time (rise and fall)	t_{T}		1	5	ns	
Refresh period	t_{REF}		—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.5 V.
2. Access time is measured at 1.5 V. Load condition is CL = 50 pF.
3. t_{LZ} (min) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} define CKE setup time to CLK rising edge except power down exit command.
6. t_{AS}/t_{AH}: Address, t_{CS}/t_{CH}: $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM.
t_{DS}/t_{DH}: Data-in, t_{CES}/t_{CEH}: CKE

Test Conditions

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures

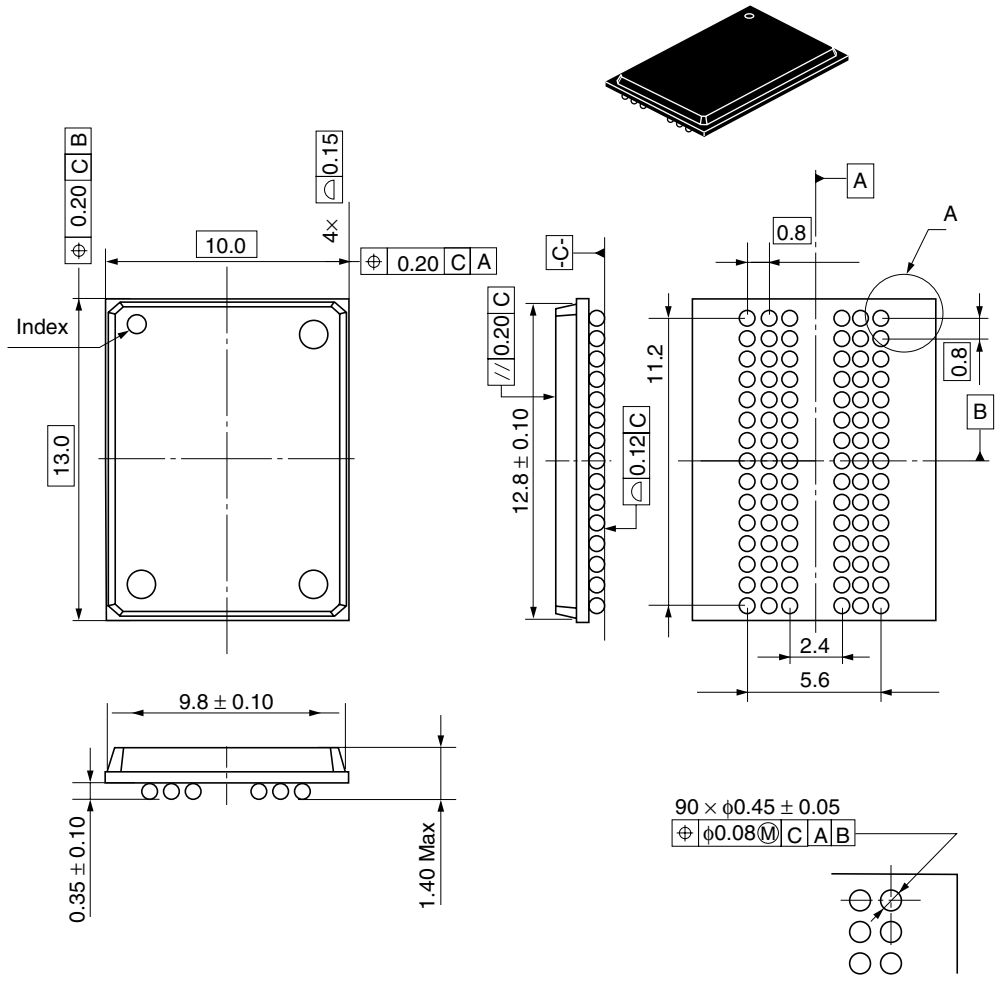


Package Dimensions

HM5212325FBPC (BP-90)

Preliminary

Unit: mm



Details of the part A

Hitachi Code	BP-90
JEDEC	—
EIAJ	—
Mass (reference value)	0.28 g

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