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# 2SJ408(L), 2SJ408(S)

Silicon P-Channel MOS FET

## HITACHI

November 1996

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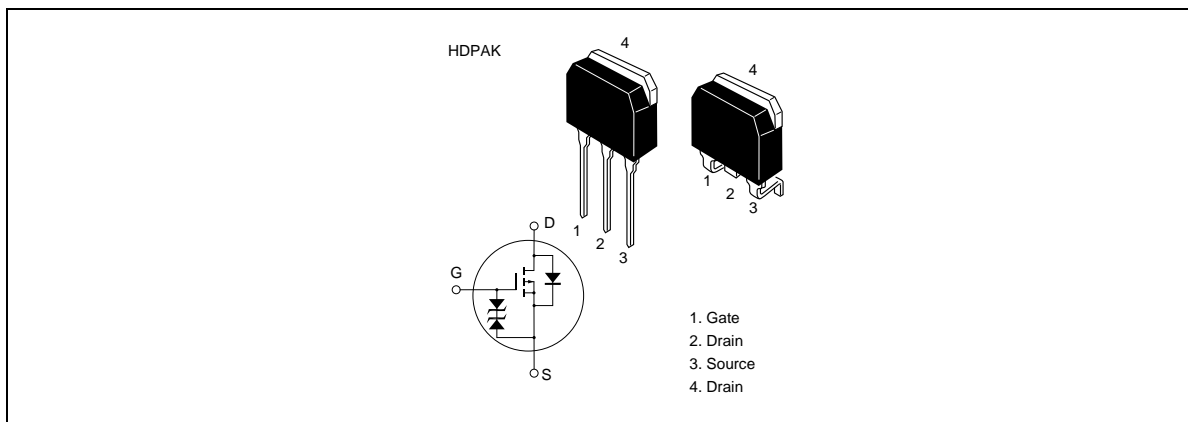
### Application

High speed power switching

### Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC - DC converter
- Avalanche Ratings

### Outline



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### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	-50	A
Drain peak current	$I_{D(pulse)}^{*1}$	-200	A
Body to drain diode reverse drain current	$I_{DR}$	-50	A
Avalanche current	$I_{AP}^{*3}$	-50	A
Avalanche energy	$E_{AR}^{*3}$	214	mJ
Channel dissipation	$P_{ch}^{*2}$	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
2. Value at Tc = 25°C  
3. Value at Tch = 25°C, Rg  $\geq 50 \Omega$

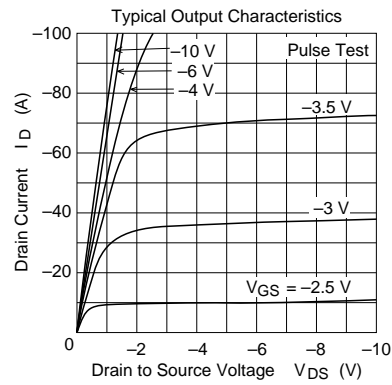
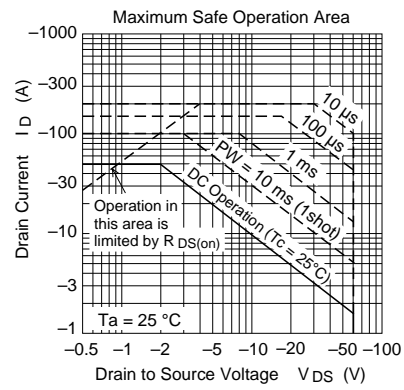
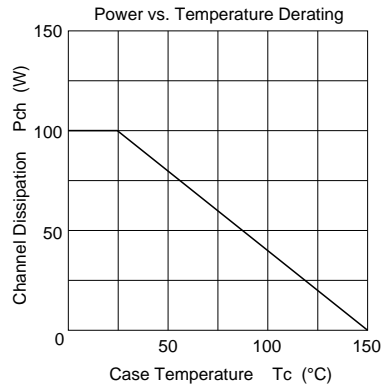
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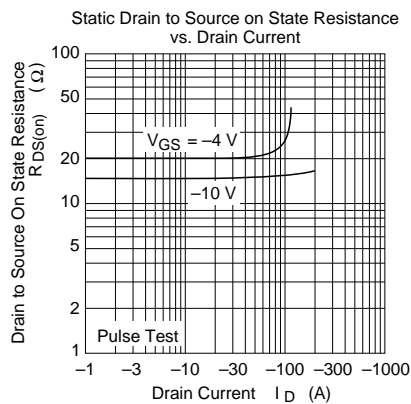
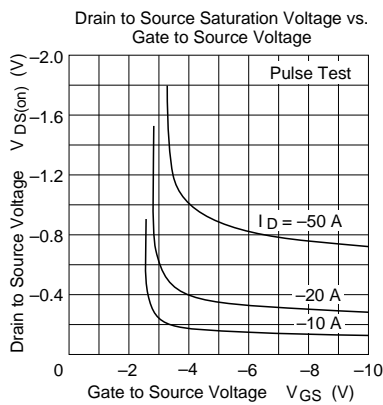
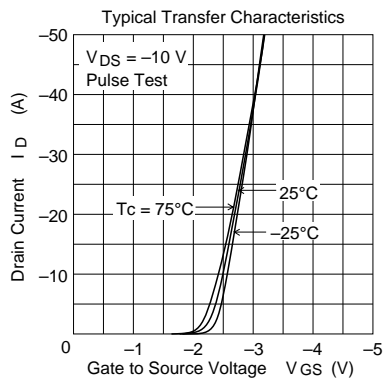
### Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \text{ } \mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-250	μA	$V_{DS} = -50 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.25	V	$I_D = -1 \text{ mA}$ , $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.015	0.02	Ω	$I_D = -25 \text{ A}$ $V_{GS} = -10 \text{ V}^{*1}$
		—	0.02	0.028	Ω	$I_D = -25 \text{ A}$ $V_{GS} = -4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	30	50	—	S	$I_D = -25 \text{ A}$ $V_{DS} = -10 \text{ V}^{*1}$
Input capacitance	Ciss	—	8200	—	pF	$V_{DS} = -10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	Coss	—	3650	—	pF	
Reverse transfer capacitance	Crss	—	750	—	pF	
Turn-on delay time	$t_{d(on)}$	—	55	—	ns	$I_D = -25 \text{ A}$ $V_{GS} = -10 \text{ V}$ $R_L = 1.2 \text{ } \Omega$
Rise time	$t_r$	—	340	—	ns	
Turn-off delay time	$t_{d(off)}$	—	1150	—	ns	
Fall time	$t_f$	—	620	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	-1.0	—	V	$I_F = -50 \text{ A}$ , $V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	250	—	ns	$I_F = -50 \text{ A}$ , $V_{GS} = 0$ , $diF/dt = 50 \text{ A}/\mu\text{s}$

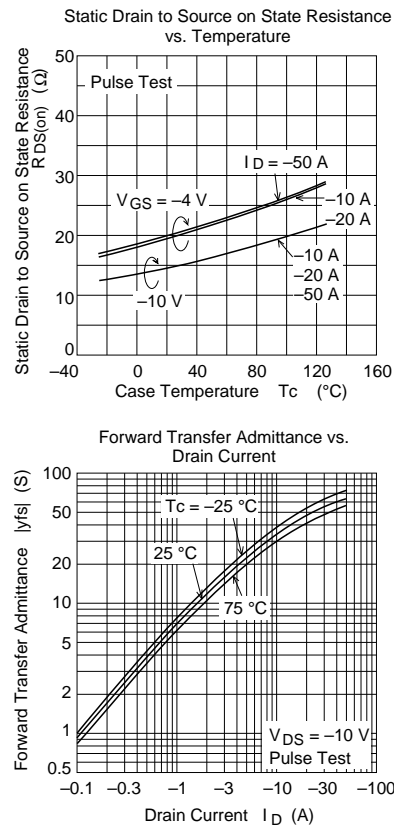
Note 1. Pulse Test

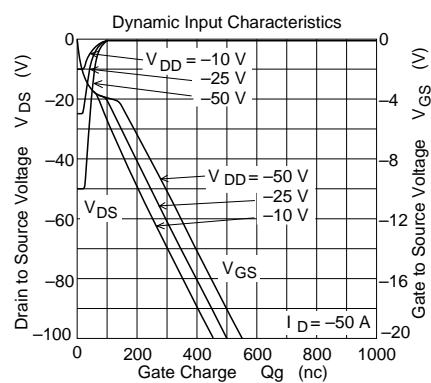
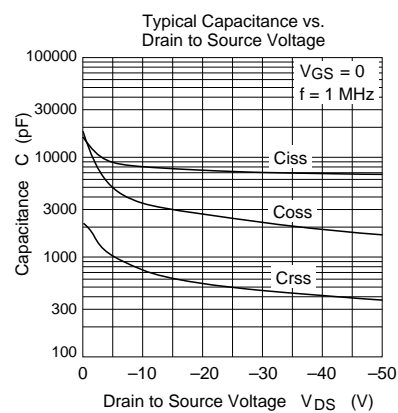
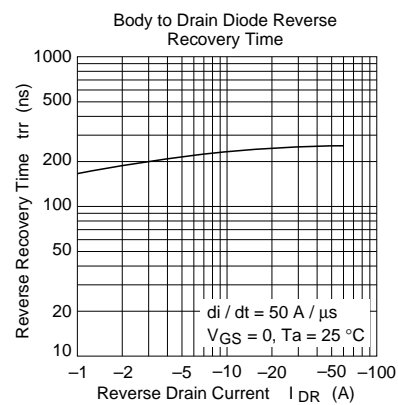
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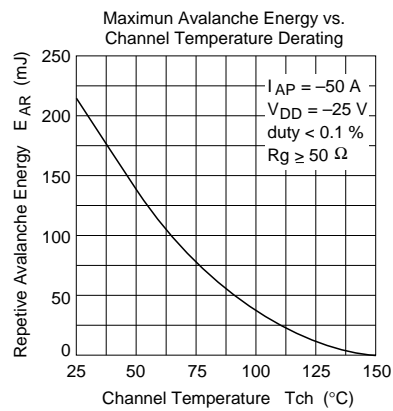
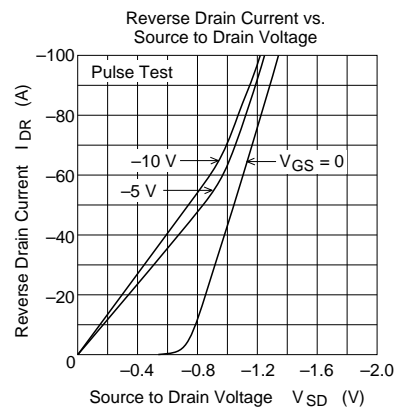
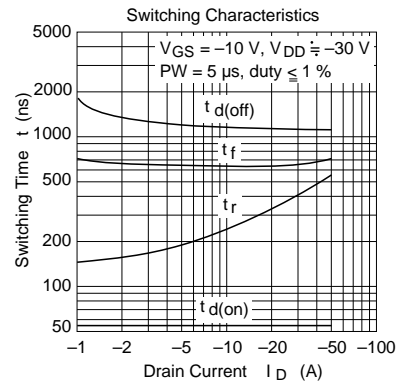


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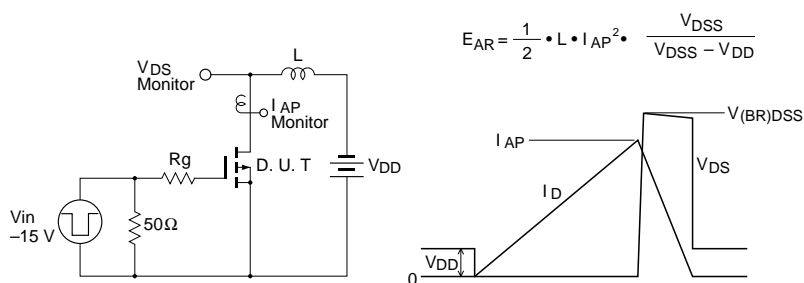
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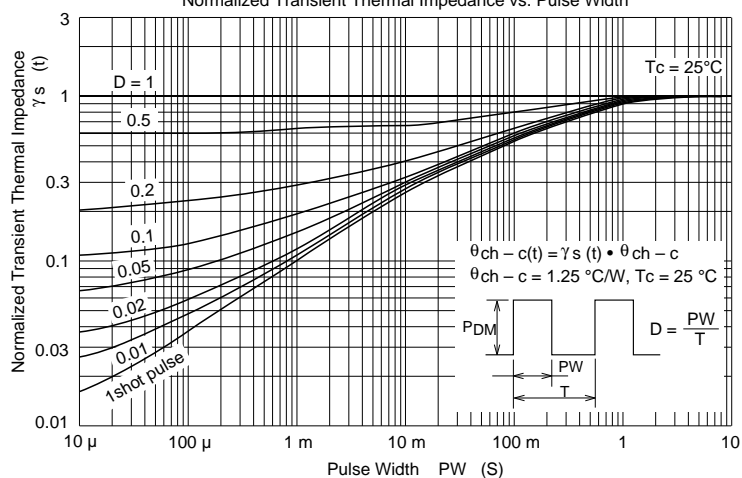


## 2SJ408(L), 2SJ408(S)

Avalanche Test Circuit and Waveform



Normalized Transient Thermal Impedance vs. Pulse Width



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