MC14049B
MC14050B

Hex Buffer

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage, V_{DD}.

The input–signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS–to–TTL/DTL converter (V_{DD} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

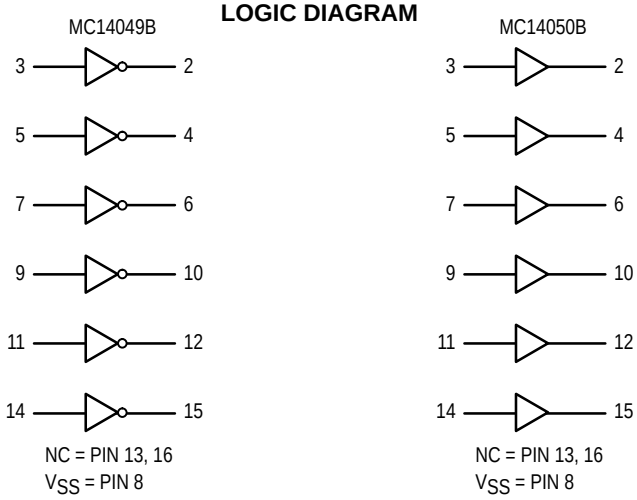
- High Source and Sink Currents
- High–to–Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- V_{IN} can exceed V_{DD}
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs

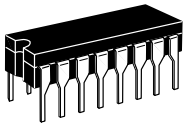
MAXIMUM RATINGS[1] (Voltages Referenced to V_{SS})

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18.0	Vdc
Input Voltage (DC or Transient)	V_{IN}	– 0.5 to + 18.0	Vdc
Output Voltage (DC or Transient)	V_{out}	– 0.5 to V_{DD} + 0.5	Vdc
Input Current (DC or Transient), per Pin	I_{in}	± 10	mA
Output Current (DC or Transient), per Pin	I_{out}	+ 45	mA
Power Dissipation, per Package[2] (Plastic/Ceramic) (SOIC)	P_D	 825 740	mW
Storage Temperature	T_{stg}	– 65 to + 150	°C
Lead Temperature (8 – Second Soldering)	T_L	260	°C

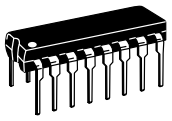
[1]Maximum Ratings are those values beyond which damage to the device may occur.
[2]Temperature Derating: See Figure 3.

LOGIC DIAGRAM

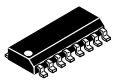




L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



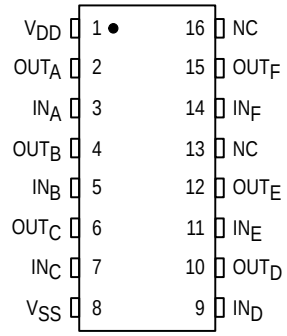
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

PIN ASSIGNMENT



REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	+ 25°C Min	+ 25°C Typ[1]	+ 25°C Max	+ 125°C Min	+ 125°C Max	Unit
Output Voltage “0” Level $V_{in} = V_{DD}$	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level $V_{in} = 0$	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 1.6	—	– 1.25	– 2.5	—	– 1.0	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.30	– 2.6	—	– 1.0	—	
(V_{OH} = 13.5 Vdc)		15	– 4.7	—	– 3.75	– 10	—	– 3.0	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.75	—	3.2	6.0	—	2.6	—	mAdc
(V_{OL} = 0.5 Vdc)		10	10	—	8.0	16	—	6.6	—	
(V_{OL} = 1.5 Vdc)		15	30	—	24	40		19	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	10	20	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	1.0	—	0.002	1.0	—	30	µAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current [2,3] (Dynamic plus Quiescent, per package) (C_L = 50 pF on all outputs, all buffers switching	I_T	5.0	$I_T = (1.8\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (3.5\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.3\ \mu A/kHz)\ f + I_{DD}$							

1 Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

2 The formulas given are for the typical characteristics only at + 25°C

3 To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

Where: I_T is in µA (per Package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency and k = 0.002.

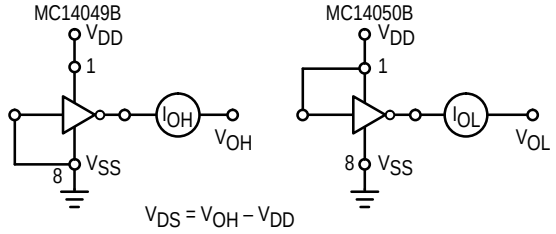
This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \le V_{in} \le 18$ V and $V_{SS} \le V_{out} \le V_{DD}$ are recommended.

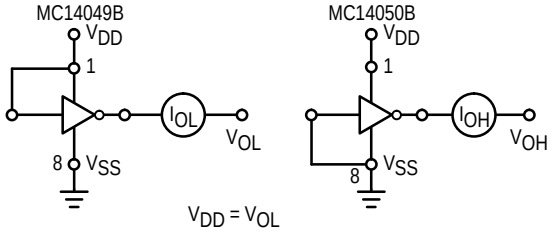
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC SWITCHING CHARACTERISTICS[1] (C_L = 50 pF, T_A = + 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ[2]	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.7 ns/pF) C_L + 65 ns		5.0	—	100	160	
t_{TLH} = (0.25 ns/pF) C_L + 37.5 ns		10	—	50	80	
t_{TLH} = (0.2 ns/pF) C_L + 30 ns		15	—	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.2 ns/pF) C_L + 30 ns		5.0	—	40	60	
t_{THL} = (0.06 ns/pF) C_L + 17 ns		10	—	20	40	
t_{THL} = (0.04 ns/pF) C_L + 13 ns		15	—	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.33 ns/pF) C_L + 63.5 ns		5.0	—	80	140	
t_{PLH} = (0.19 ns/pF) C_L + 30.5 ns		10	—	40	80	
t_{PLH} = (0.06 ns/pF) C_L + 27 ns		15	—	30	60	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.2 ns/pF) C_L + 30 ns		5.0	—	40	80	
t_{PHL} = (0.1 ns/pF) C_L + 15 ns		10	—	20	40	
t_{PHL} = (0.05 ns/pF) C_L + 12.5 ns		15	—	15	30	

1 The formulas given are for the typical characteristics only at 25°C.
2 Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.





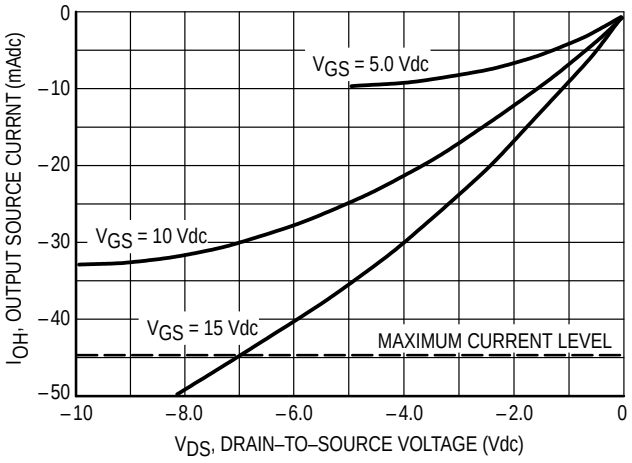


Figure 1. Typical Output Source Characteristics

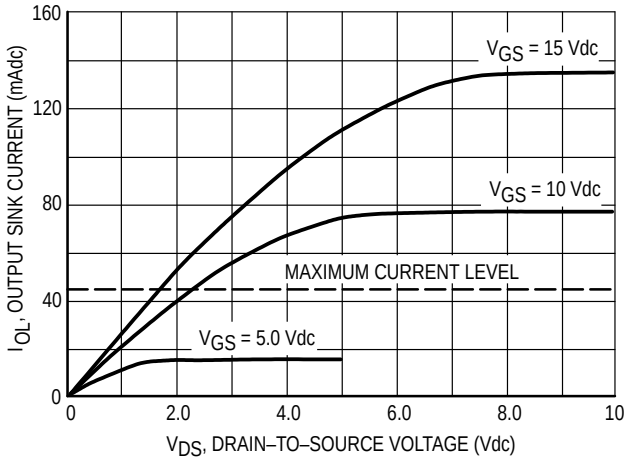


Figure 2. Typical Output Sink Characteristics

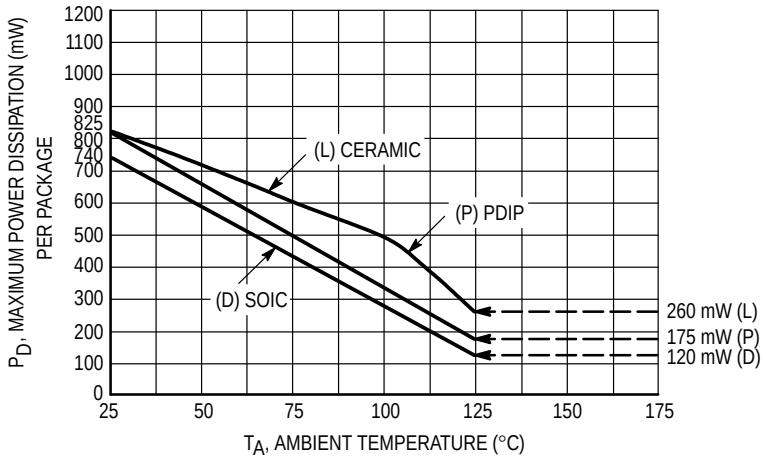


Figure 3. Ambient Temperature Power Derating

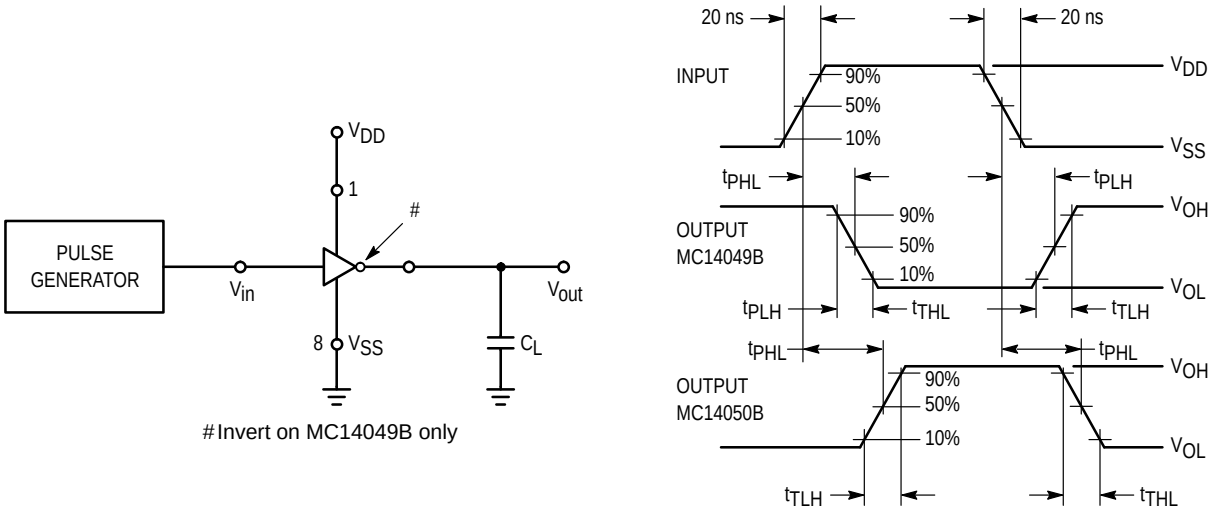
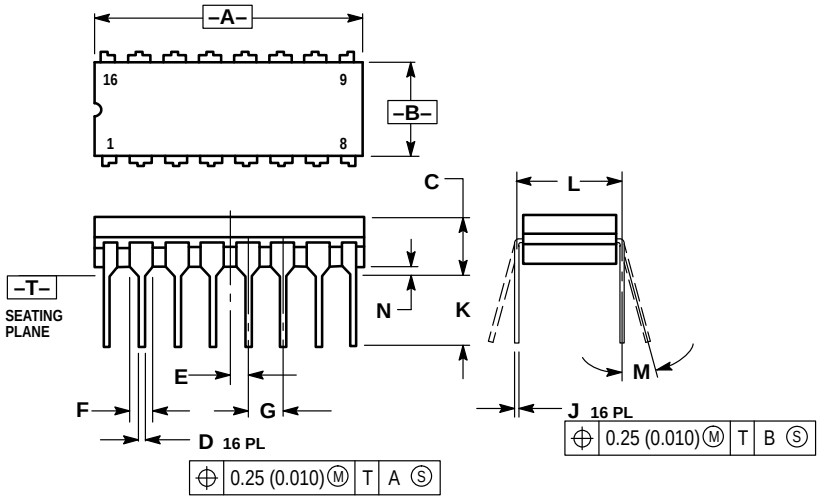


Figure 4. Switching Time Test Circuit and Waveforms

OUTLINE DIMENSIONS

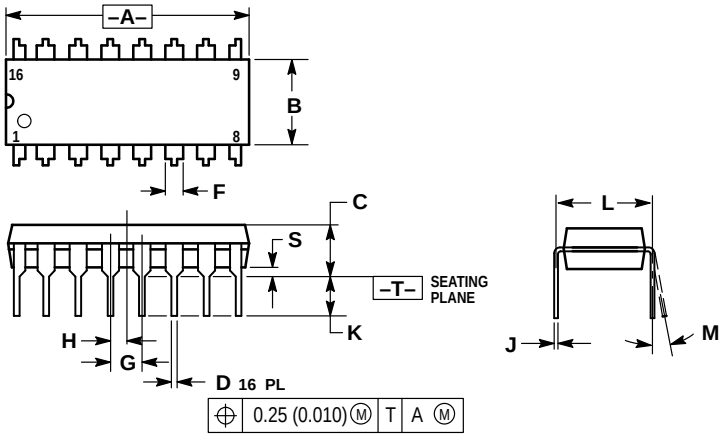
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

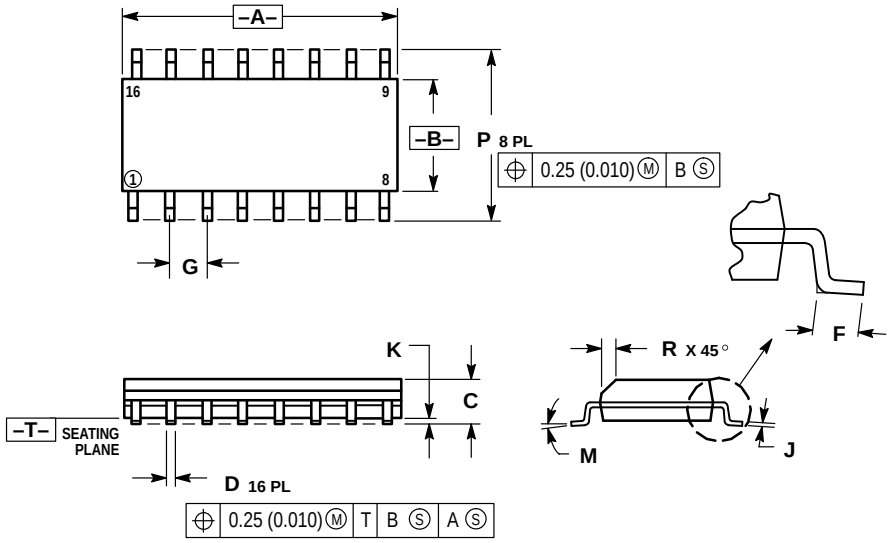


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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