AN1465
APPLICATION NOTE

A LNA OPTIMIZED FOR HIGH IP3out AT 1.9GHz USING THE NPN Si START540 TRANSISTOR

F. Caramagno - N. Micalizzi - G. Privitera

Data at 1.9GHz (3V, 5mA)

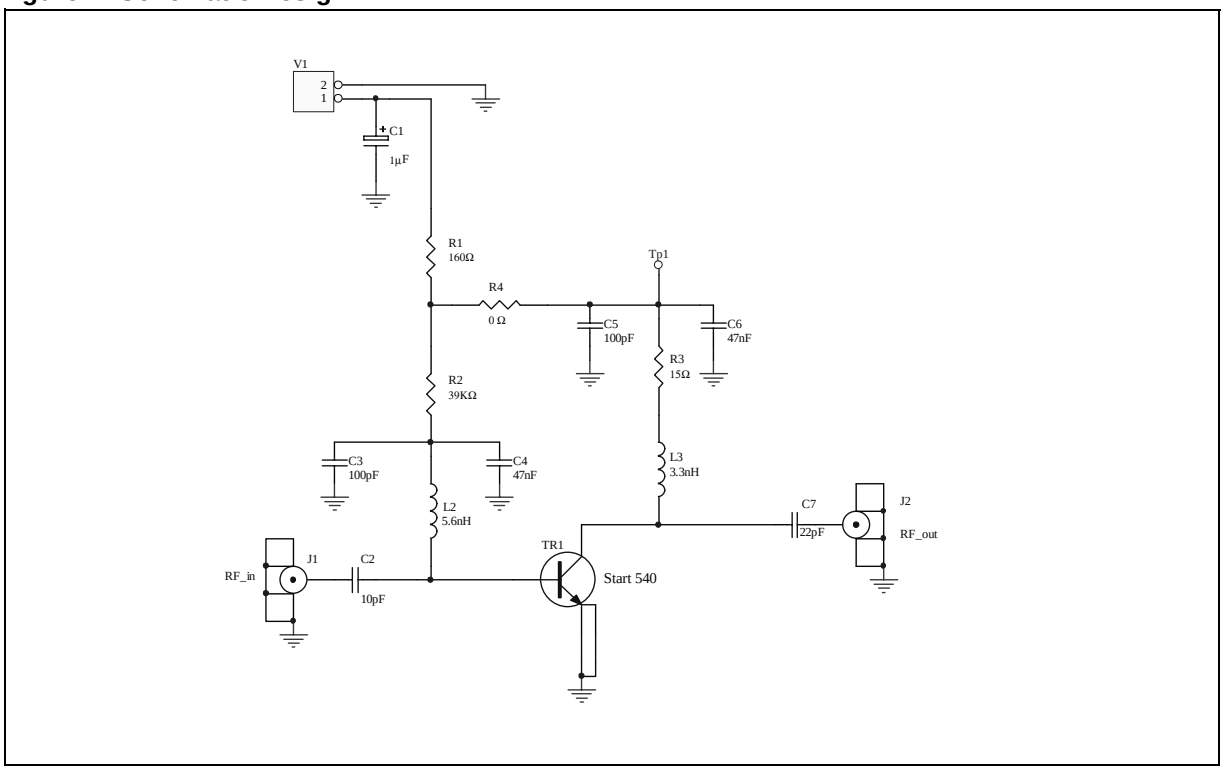
Gain = 15dB, $IP3_{out}$ = 24dBm, NF = 1.25dB, RL_{in} > 7dB, RL_{out} >20dB

1. INTRODUCTION.

START540 is a product of the START Family (ST Advanced Radio frequency Transistor). It is a high performance silicon bipolar transistor housed in the ultra miniature 4-lead SOT-343 (SC-70) surface mount plastic package. The amplifier is designed for use with 30mils thickness FR-4 printed circuit board material. The amplifier application circuit has been optimized to achieve high IP3out and a good compromise among Noise Figure, Gain and return loss at 1.9GHz, with V_{ce}=2V and I_c=5mA. The amplifier has 1.25dB of Noise Figure, 15dB of Gain, an Input Return Loss>7dB, an output Return Loss>20dB, -0.5dBm $P1dB_{out}$ and an IP3 of +24dBm (1.9GHz, 3V, 5mA).

2. LNA DESIGN.

Figure 1: Schematic Design



A single pin (V_{cc}=3V) for voltage supply is used. A 1µF bypass capacitor to filter the supply at the common V_{cc} node is also used. The transistor's base is connected to the power supply through a choke inductor (L2) and the transistor's collector is connected to the power supply through a choke inductor (L3). The collector's voltage is 2V. The input matching is realized with a 50ohm series transmission line.The L2 inductor is used to reduce the Noise Figure value The output matching is realized with a 50ohm series transmission line and inductor (L3). Resistor (R3) is used to improve RF circuit stability.Low frequency decoupling capacitors C4 (47nF) for the base and C6 (47nF) for the collector improve the IP3 considerably. It's possible, removing R4, to supply separately the collector and the base using a different voltage supply. In this way, it's possible to set a different value of current in the collector (Icc).

3. DEMOBOARD Specification.

Figure 2 is the PC board cross section. The board material is standard FR4. Note that spacing from the top layer RF traces to the internal ground plane is 0.010 inch (0.254 mm). The width of 50ohm microstrip is 0.45 mm.

Figure 2: Cross-section of pcb board

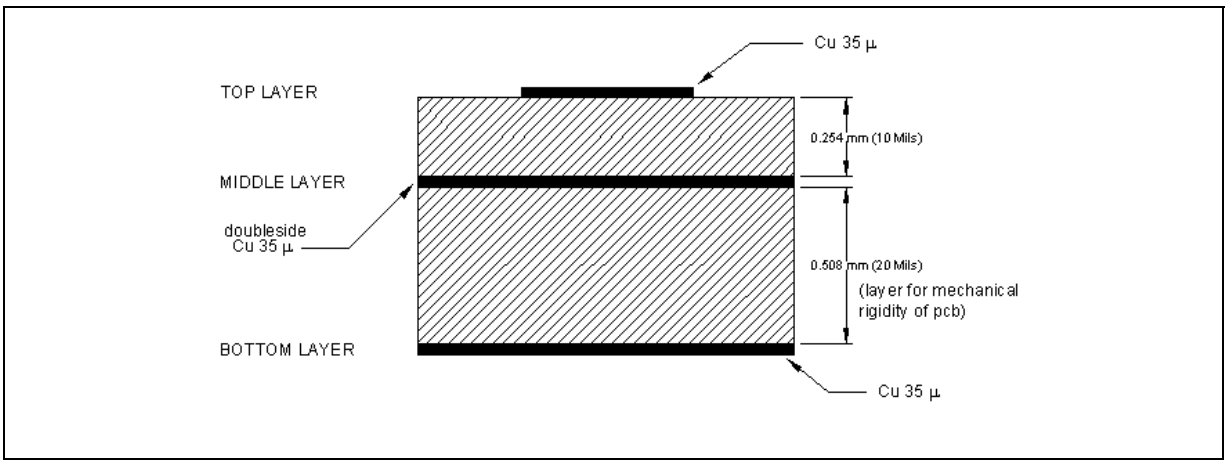


Figure 3: Image of the START540 DEMOBOARD (Size 22x30 mm)

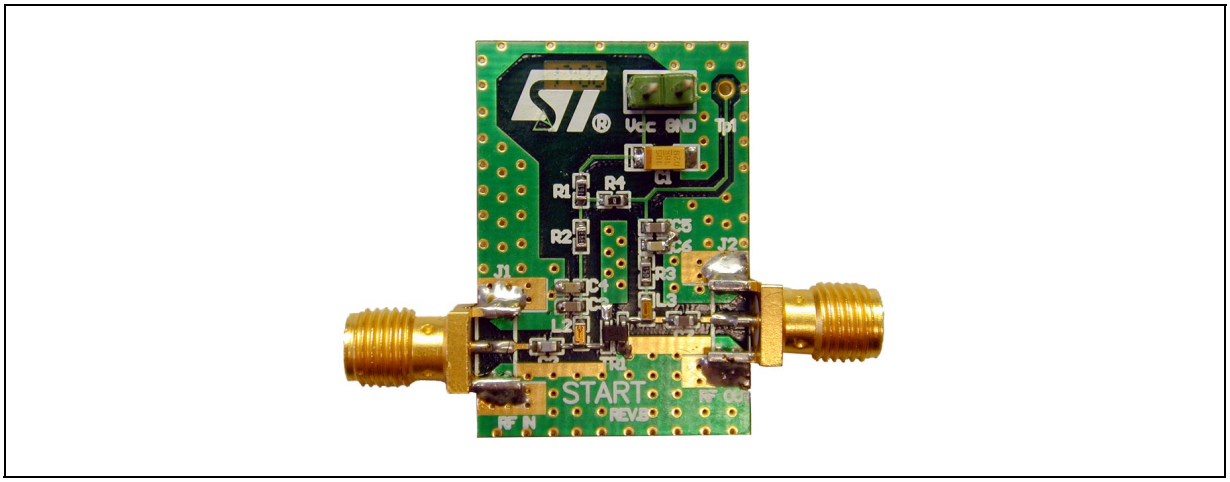
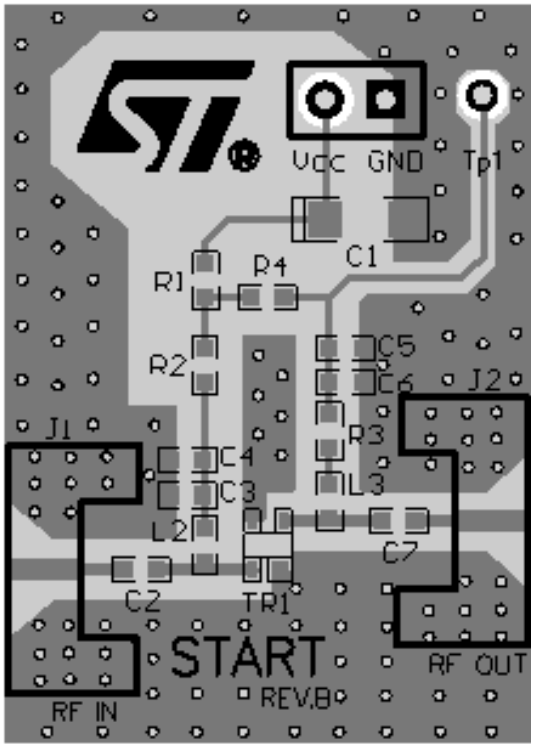
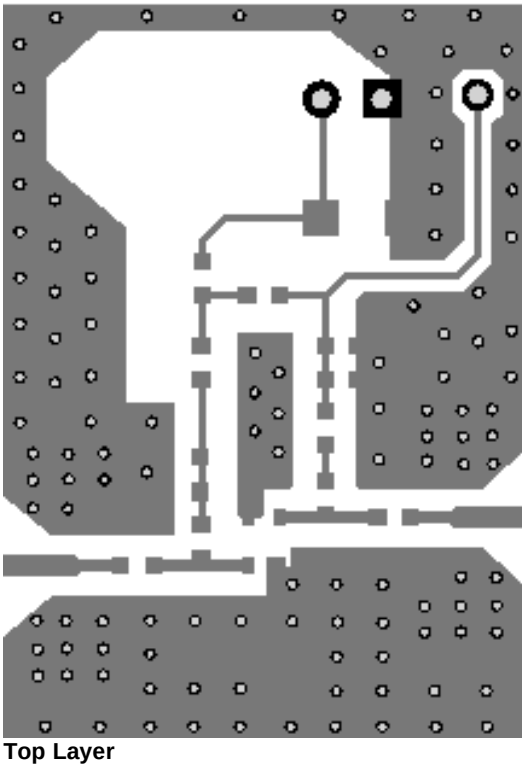


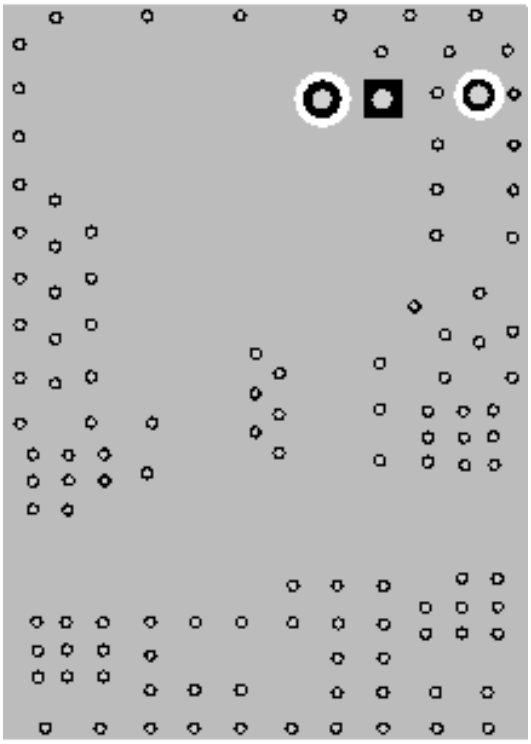
Figure 4: DEMOBOARD Layout



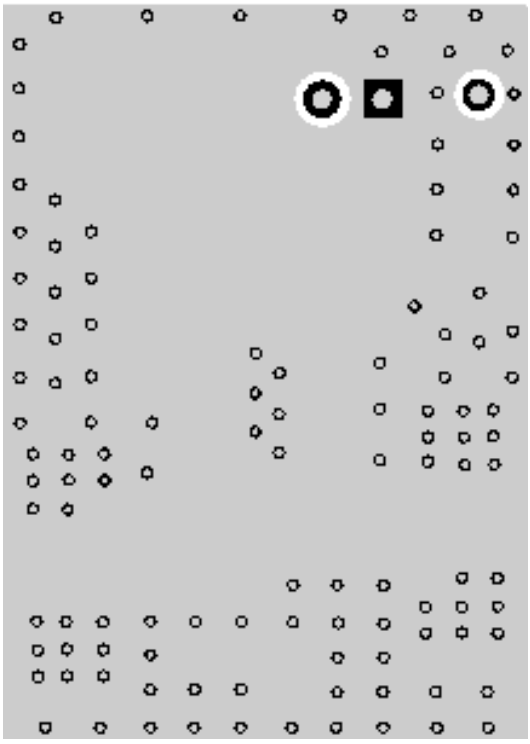
View Of Components Position



Top Layer



Mid Layer



Bottom Layer

Table 1: Bill of Materials

Component	Value	Size	Manufacturer	Comment
C1	1µF	Case_A	Various (electrolytic)	Supply filter
C2	10pF	0603	Murata (GRM39)	Input dc block
C3	100pF	0603	Murata (GRM39)	RF Bypass, Block
C4	47nF	0603	Murata (GRM39)	IP3 Improvement
C5	100pF	0603	Murata (GRM39)	RF Bypass, Block
C6	47nF	0603	Murata (GRM39)	IP3 Improvement
C7	22pF	0603	Murata (GRM39)	Output dc block
L2	5.6nH	0603	Murata (LQP11)	RF Choke, Input Matching
L3	3.3nH	0603	Murata (LQP11)	RF Choke, Stability Improvement
R1	160 ohm	0603	Various	Dc bias
R2	160 ohm	0603	Various	Dc bias
R3	15 ohm	0603	Various	Stability Improvement
R4	0 ohm	0603	Various	Jumper
TR1	-	SOT-343	ST Microelectronics	Start540
J1	-	-	Johnson 142-0701-881	RF input connector
J2	-	-	Johnson 142-0701-881	RF output connector
J3	-	-	Various	DC connector
Substrate	FR4	-	Various	Layer = 3;h=0.03inch; Er=4.5

4. LNA PERFORMANCE.

The high intercept point START540 amplifier is biased at Vce=2V and Ic=5ma.
Table 2 shows the measured parameter values at 1900MHz, 25ºC,Icc=5mA,Vcc=3V

Table 2: Measured data

Parameter	Typical	Unit	Reference
Power Gain	15	dB	Figure 5
Noise Figure	1.25	dB	Figure 6
Input Return Loss	7.5	dB	Figure 7
Output Return Loss	20	dB	Figure 8
Isolation	22	dB	Figure 9
Output Power at 1dBcp	-0.5	dBm	Figure 10
Third-Order Intercept Point	24	dBm	Figure 13

The measured gain and noise figure is shown in figures 5 and 6. Optimum amplifier noise figure is 1.25 dB and occurs at 1900 MHz. This value included the losses of the input SMA connector and microstrip lines of the FR4 board. If the input transmission line and connector losses were subtracted, the noise figure result would improve by 0.2 dB.
Measured input/output return loss and isolation are shown in figures 7, 8 and 9.
In figure 10 is shown the power gain vs. power output at 1.9 GHz (the output P1dB is -0.5 dBm).

Figure 5: Power Gain vs. Frequency

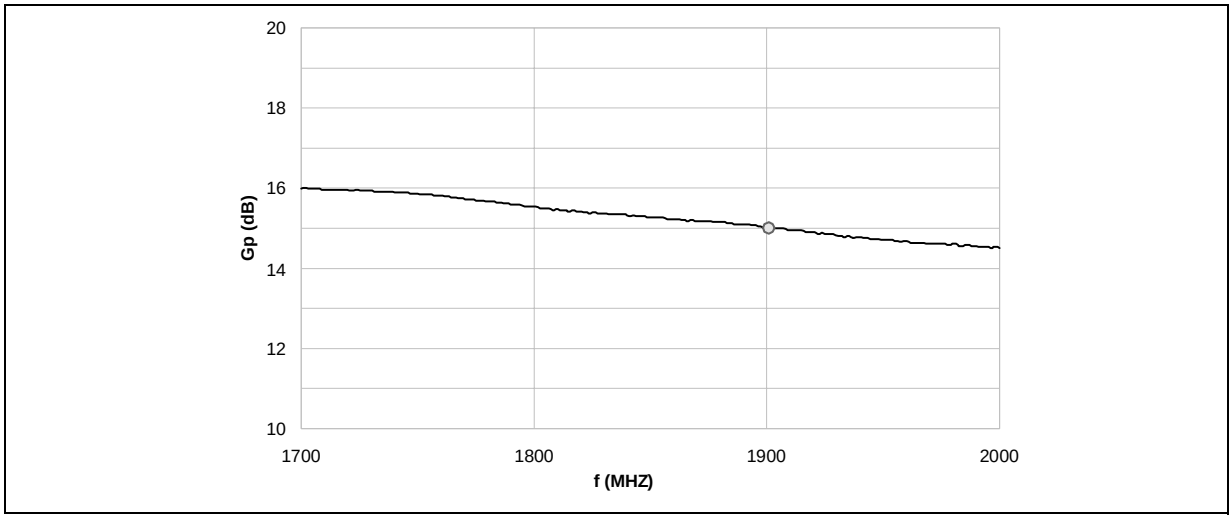


Figure 6: Noise Figure vs. Frequency

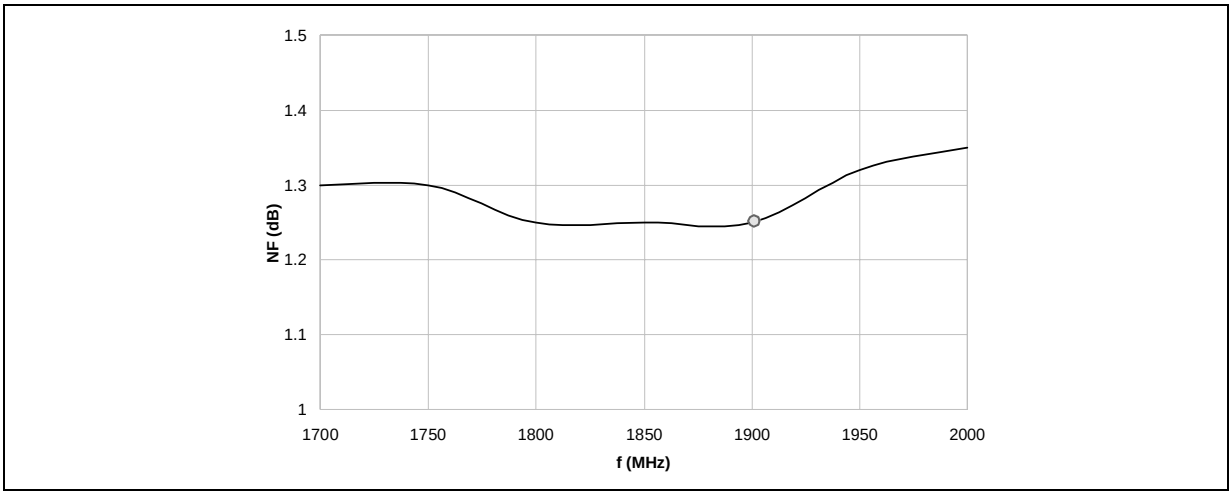


Figure 7: Input Return Loss vs. Frequency

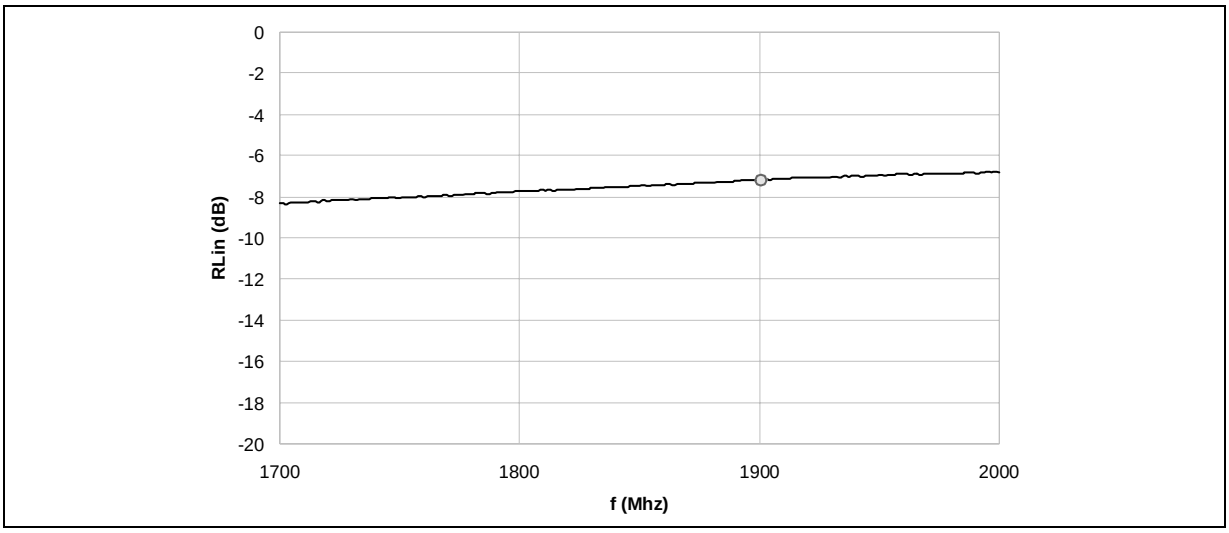


Figure 8: Output Return Loss vs. Frequency

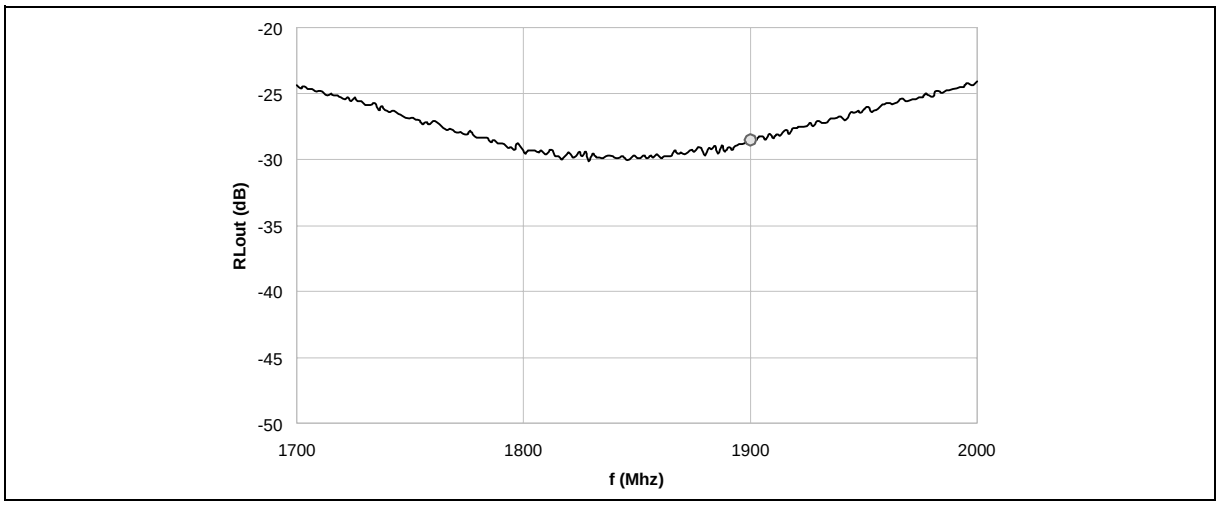


Figure 9: Isolation vs. Frequency

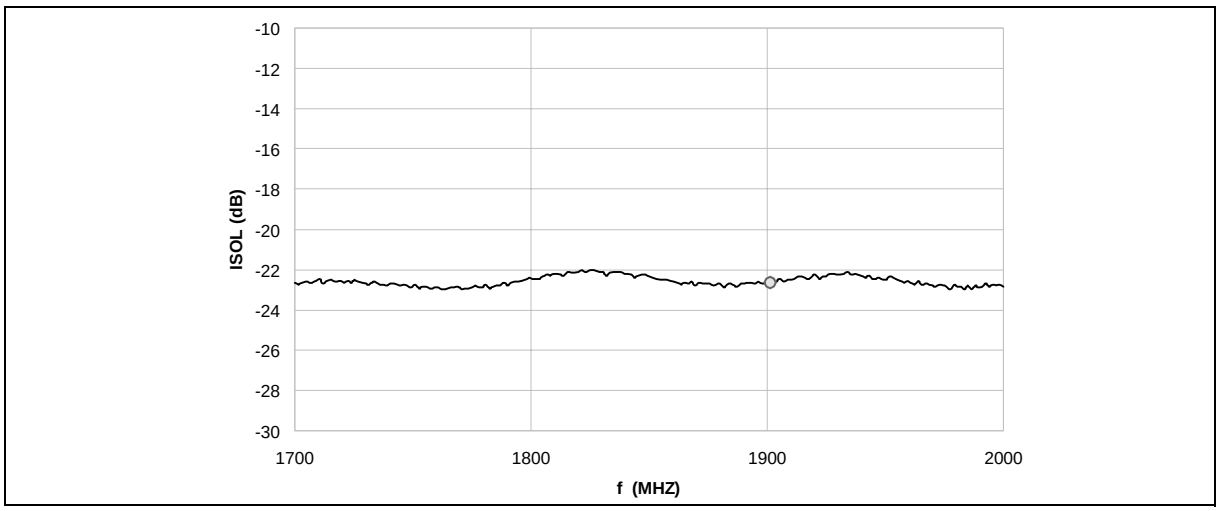
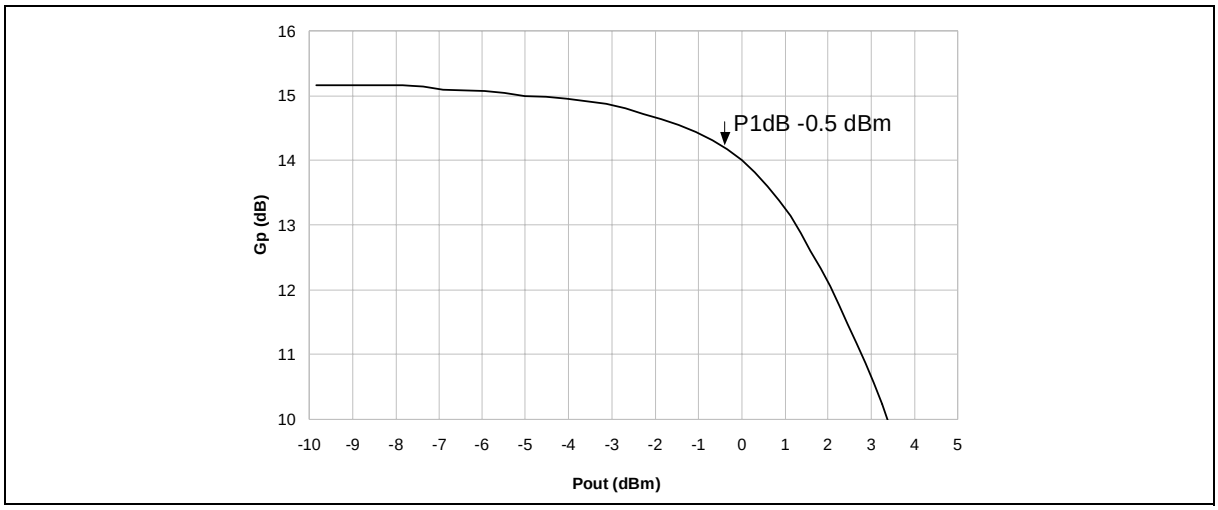


Figure 10: Power Gain vs. Power Output (at 1.9GHz)



The stability analysis of the amplifier is show in figure 11
A linear two port device is unconditionally stable if the real parts of its input and output impedances remain positive for all passive load and source impedances. The circuit is unconditionally stable if μ >1, or if D < 1 and simultaneously K > 1 at all frequency.

$$\left|\Delta\right| = \left|S_{11}S_{22} - S_{12}S_{21}\right| < 1$$

$$K = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|} > 1$$

$$\mu = \frac{1 - \left|S_{11}\right|^2}{\left|S_{22} - S_{11}\Delta\right| + \left|S_{12}S_{21}\right|}$$

K, Δ and μ parameters were calculated for 100 MHz ≤ f ≤ 6 GHz. Those conditions are always verified in this band frequency.

Figure 11: Stability Factor M ,k, The Magnitude Of The S-matrix

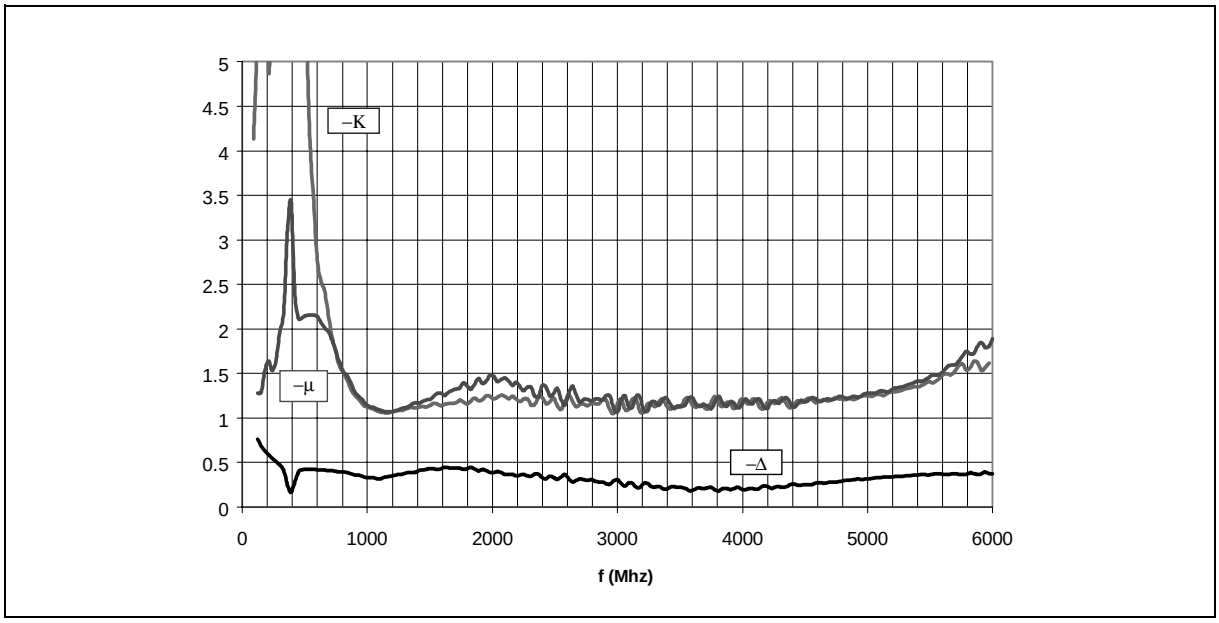
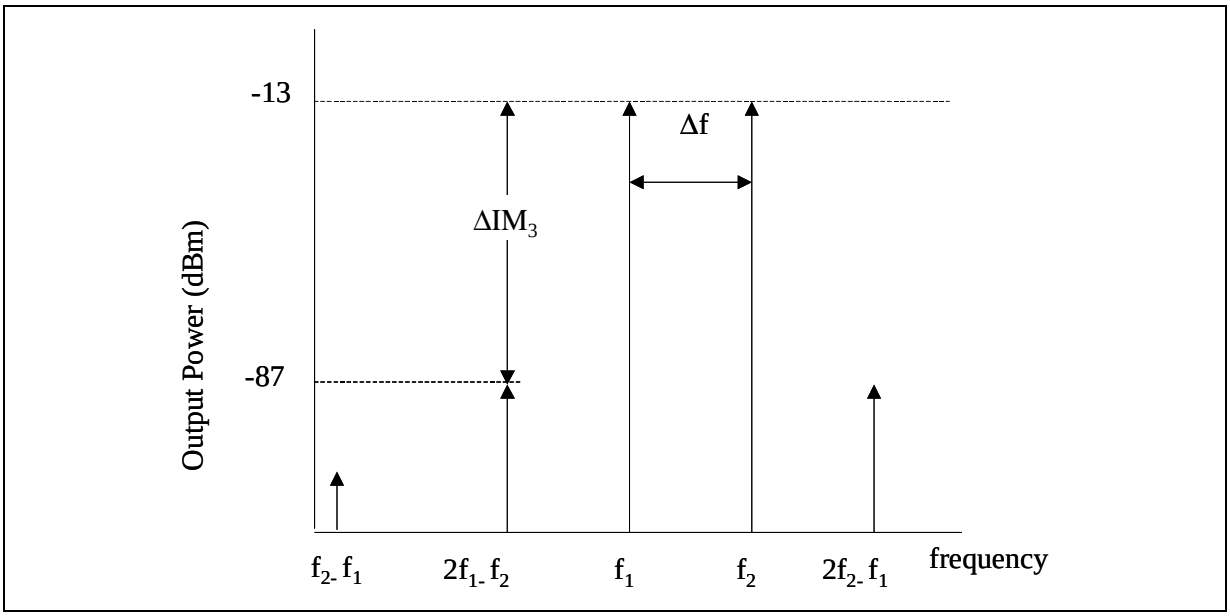


Figure 12 is a partial representation of the LNA output spectrum. f_1=1900MHz and f_2 =1900,4MHz are equal amplitude input test tones. For this LNA we use -28dBm input power in order to reach -13dBm of output power for each test tones. Other signals besides f_1 and f_2 are generated as a result of non-linear device behavior.

Figure 12: In-band Third Order Intermodulation Product Distorsion



The generated low frequency product (f2-f1) modulates the base-emitter and colle ctor-emitter voltages of the transistor. This modulation causes a base and collector voltages fluctuation that lowers the linearity of the amplifier.
The base voltage, in fact, determines the quiescent current for the device and the collector voltage determines the saturation point. In order to reduce this effect a proper bypassing has been implemented at both c ollector and base. For that reason with the introduction of low frequency decoupling capacitors C6 (47nF) on the collector and C4 (47nF) on the base improves the IP3 significantly.

The Output IP3 is calculated as follows:

$$IP3out = \frac{\Delta IM3}{2} + Pout$$

where ΔIM3 (please refer figure 13) is the difference between one of two equal amplitude test tones present at the amplifier output, and the level of the highest 3rd -order distortion product. The ΔIM3 measured is 74dB.

So we have:

$$IP3out = \frac{\Delta IM3}{2} + Pout = \frac{74}{2} + (-13) = 24dBm$$

Figure 13: Output IP3 Measurement