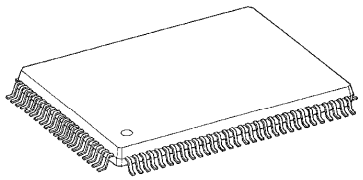
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A30AF

MOTION-ADAPTIVE 3-DIMENSIONAL YC SEPARATION / NOISE REDUCTION (NR) LSI

TC90A30AF is a motion-adaptive 3-dimensional YC separation / NR LSI.
A 3-dimensional YC separation / 3-dimensional NR system can be easily created by combining this LSI with a 2MEG-bit FIFO memory.



QFP100-P-1420-0.65A

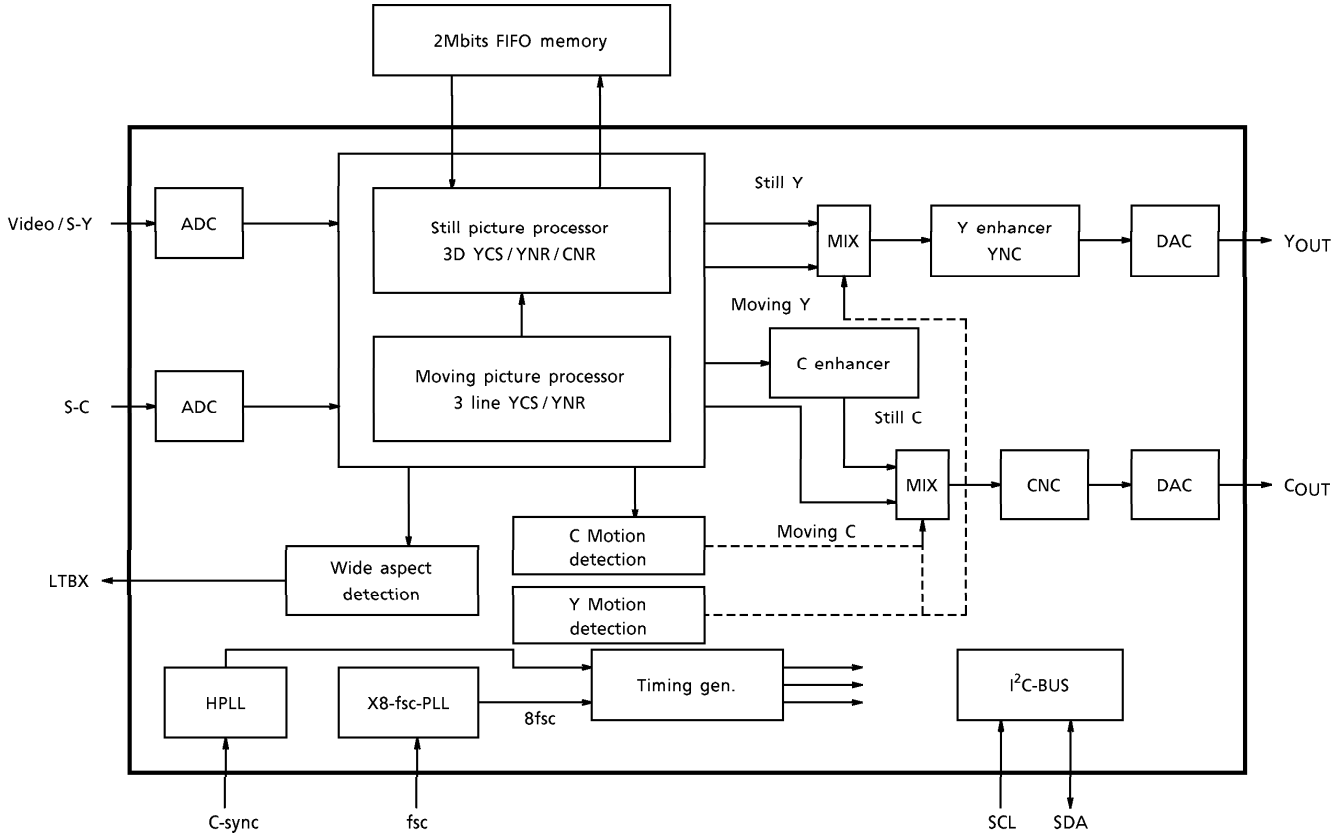
Weight : 1.6 g (Typ.)

FEATURES

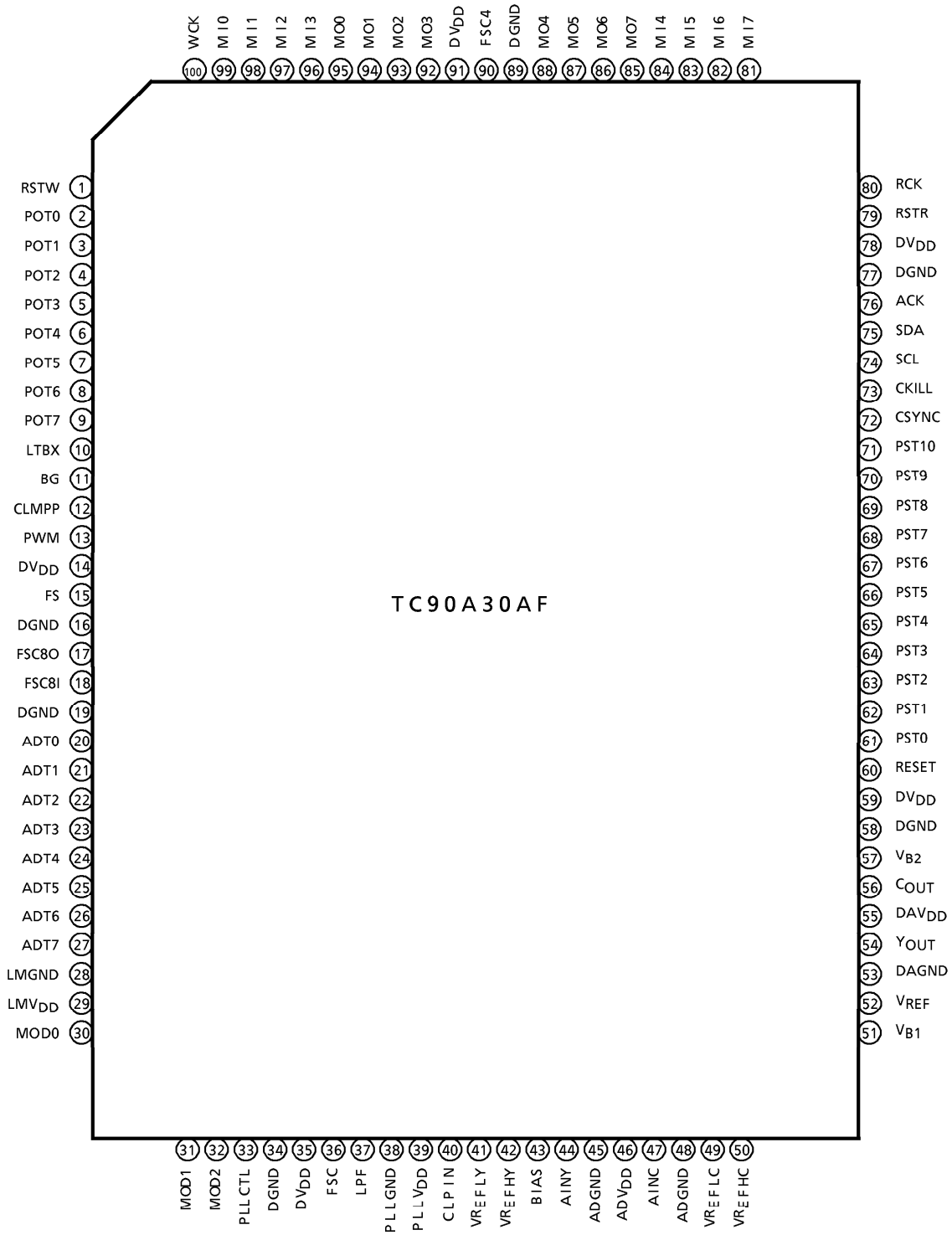
- 3-D YC separation
  - Still picture area : Frame comb filter
  - Motion picture area : 3-line comb filter
- 3-D noise reduction
  - Still picture area : Frame recursive Y, C noise reduction
  - Motion picture area : 3-line comb filter
- Y and demodulated color signal edge enhancer
- High-precision motion detection
  - Motion detection independent of Y or C
    Switch automatically motion detection sensitivity based on motion data for each frame
- Built-in fsc 8 × PLL
- Built-in digital HPLL
- Built-in two 8-bit ADCs (for Y, C input)
- Built-in two 10-bit DACs (for Y, C output)
- Supports 2MEG-bit external FIFO memory (Recommended memory MSM51V8221)
- Supports I^2C bus (slave address : B2H)
- 3.3 V single power supply
- 100-pin QFP

980910EBA1

BLOCK DIAGRAM



TERMINAL CONNECTION DIAGRAM



TERMINAL FUNCTION

PIN No.	PIN NAME	I / O	FUNCTION	REMARKS
1	RSTW	O	Memory write reset output	—
2	POT0	O	Test output	—
3	POT1	O	Test output	—
4	POT2	O	Test output	—
5	POT3	O	Test output	—
6	POT4	O	Test output	—
7	POT5	O	Test output	—
8	POT6	O	Test output	—
9	POT7	O	Test output	—
10	LTBX	O	Letterbox detection output	—
11	BG	O	Burst gate pulse output for TA1221AF	—
12	CLMPP	O	Clamp pulse external monitor output	—
13	PWM	O	Clamp PWM voltage output	—
14	DV_{DD}	—	Digital power supply	+ 3.3 V
15	FS	I	External 4 fsc input	Normally connect to V_{SS}
16	DGND	—	Digital GND	—
17	FSC8O	O	8 × PLL clock output	8fsc
18	FSC8I	I	8 fsc input	—
19	DGND	—	Digital GND	—
20	ADT0	I	Test input	Normally connect to V_{SS}
21	ADT1	I	Test input	Normally connect to V_{SS}
22	ADT2	I	Test input	Normally connect to V_{SS}
23	ADT3	I	Test input	Normally connect to V_{SS}
24	ADT4	I	Test input	Normally connect to V_{SS}
25	ADT5	I	Test input	Normally connect to V_{SS}
26	ADT6	I	Test input	Normally connect to V_{SS}
27	ADT7	I	Test input	Normally connect to V_{SS}
28	LMGND	—	Digital GND	—
29	LMV_{DD}	—	Digital power supply	+ 3.3 V
30	MOD0	I	Test input	Normally connect to V_{SS}
31	MOD1	I	Test input	Normally connect to V_{DD}
32	MOD2	I	Test input	Normally connect to V_{DD}
33	PLLCTL	I	8 × PLL control	Normally connect to V_{DD}
34	DGND	—	Digital GND	—
35	DV_{DD}	—	Digital power supply	+ 3.3 V
36	FSC	I	fsc input for 8 × PLL	Self biased
37	LPF	—	Loop filter for 8 × PLL	For filter connection
38	PLLGND	—	Analog GND	—
39	$PLLV_{DD}$	—	Analog power supply	+ 3.3 V
40	CLPIN	I	Y clamp voltage input	—

PIN No.	PIN NAME	I/O	FUNCTION	REMARKS
41	VR_{EFLY}	—	ADC reference voltage (L side for Y)	64LSB
42	VR_{EFHY}	—	ADC reference voltage (H side for Y)	208LSB
43	BIAS	—	ADC bias voltage (Y/C common)	—
44	ADGND	—	Analog GND	—
45	AINY	I	Composite video/Y signal input	Pedestal clamp
46	ADV_{DD}	—	Analog power supply	+3.3V
47	AINC	I	C signal input	No clamp
48	ADGND	—	Analog GND	—
49	VR_{EFLC}	—	ADC reference voltage (L side for C)	64LSB
50	VR_{EFHC}	—	ADC reference voltage (H side for C)	208LSB
51	V_{B1}	—	DAC bias voltage 1 (Y/C common)	—
52	V_{REF}	I	DAC reference voltage (Y/C common)	V_{DD} – 1.5V
53	DAGND	—	Analog GND	—
54	Y_{OUT}	O	Y signal output	D range : V_{DD} to V_{REF}
55	DAV_{DD}	—	Analog power supply	+3.3V
56	C_{OUT}	O	C signal output	D range : V_{DD} to V_{REF}
57	V_{B2}	—	DAC bias voltage 2 (Y/C common)	—
58	DGND	—	Digital GND	—
59	DV_{DD}	—	Digital power supply	+3.3V
60	RESET	I	Reset input	—
61	PST0	I	Test input	Normally connect to V_{SS}
62	PST1	I	Test input	Normally connect to V_{SS}
63	PST2	I	Test input	Normally connect to V_{SS}
64	PST3	I	Test input	Normally connect to V_{SS}
65	PST4	I	Test input	Normally connect to V_{SS}
66	PST5	I	Test input	Normally connect to V_{SS}
67	PST6	I	Test input	Normally connect to V_{SS}
68	PST7	I	Test input	Normally connect to V_{SS}
69	PST8	I	Test input	Normally connect to V_{SS}
70	PST9	I	Test input	Normally connect to V_{SS}
71	PST10	I	Test input	Normally connect to V_{SS}
72	CSYNC	I	Composite sync input (positive polarity)	—
73	CKILL	I	Color killer input	—
74	SCL	I	Clock input for I^2C bus	—
75	SDA	I/O	Data I/O for I^2C bus	—
76	ACK	O	I^2C bus acknowledge timing output	—
77	DGND	—	Digital GND	—
78	DV_{DD}	—	Digital power supply	+3.3V
79	RSTR	O	Reset output for reading frame memory	—
80	RCK	O	Clock output for reading frame memory	—
81	MI7	I	Data input from frame memory	—
82	MI6	I	Data input from frame memory	—

PIN No.	PIN NAME	I / O	FUNCTION	REMARKS
83	MI5	I	Data input from frame memory	—
84	MI4	I	Data input from frame memory	—
85	MO7	O	Data output to frame memory	—
86	MO6	O	Data output to frame memory	—
87	MO5	O	Data output to frame memory	—
88	MO4	O	Data output to frame memory	—
89	DGND	—	Digital GND	—
90	FSC4	O	4fsc clock monitor output	—
91	DV_{DD}	—	Digital power supply	+3.3V
92	MO3	O	Data output to frame memory	—
93	MO2	O	Data output to frame memory	—
94	MO1	O	Data output to frame memory	—
95	MO0	O	Data output to frame memory	—
96	MI3	I	Data input from frame memory	—
97	MI2	I	Data input from frame memory	—
98	MI1	I	Data input from frame memory	—
99	MI0	I	Data input from frame memory	—
100	WCK	O	Clock output for writing to frame memory	—

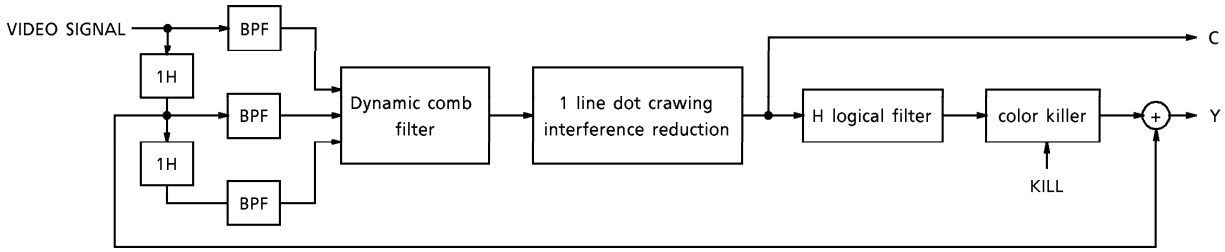
FUNCTION DESCRIPTION

1. Y / C separation

TC90A30AF is a three dimension Y / C separation IC which is motion adaptive and specialized in NTSC composite video signals. TC90A30AF has two motion detectors for Y and C signals individually which discriminates between 'motion' area and 'still' area of the picture, gets Y and C signals by applying a 3-line comb filter to the motion area and a 3D comb filter to the still area, and mixes Y and C signals output from each the 3-line comb and the 3D comb filters to get final Y / C separated signals.

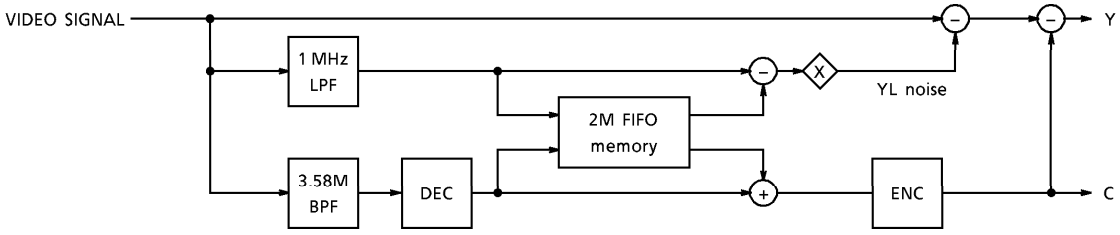
(A) 3-line comb filter for motion area

In motion area of the input picture, there is seldom correlation between two continuous frames, so that 3-line comb filter is applied to the motion area. The 3-line comb filter consists of two 1H line memories, digital band pass filters to discriminate frequency component near to the chroma signal frequency, a dynamic comb filter, a one line dot crawling interference reduction circuit and a horizontal logical filter to discriminate Y signal.



(B) 3D comb filter for still area

In still area of the input picture, Y and C signals are separated by a 3D comb filter, i.e. a frame comb filter. To get the best performance of the 3D comb filter with only 2-meg external FIFO memory, the frame comb filter processes base band color signals demodulated from discriminated chroma signals by the band pass filters with 3.58 MHz + / − 1.5 MHz band width. A frame noise reduction circuit, which uses 0 to 1MHz of low frequency component of the input video signal discriminated by a low pass filter, reduces low frequency noise of the separated Y signal.

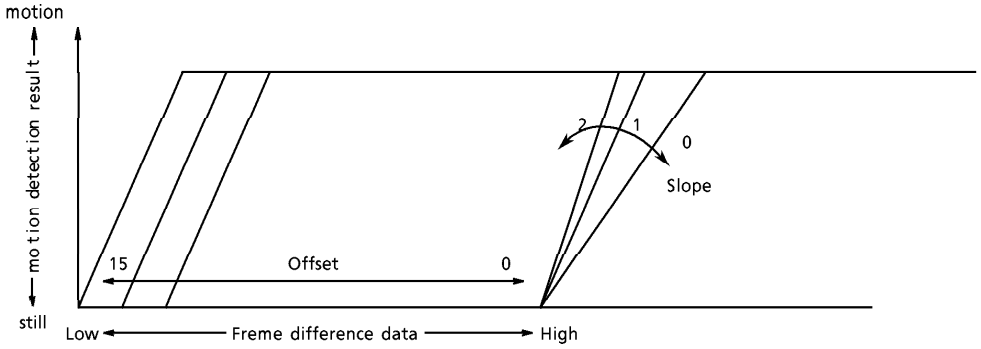


(C) Motion detectors

Motion detection of TC90A30AF consists of 1-frame motion detectors for both Y and C signals, so that each detection sensitivity can be set up individually. Y and C motion detectors process low frequency component of Y signal and demodulated color signal of two continuous frames with non-linear sensitivities described in the next (D), respectively. If amount of differences between two frames of Y signal and demodulated color signal are small, output from the C motion detector is ignored.

(D) Non-linear sensitivity of the motion detectors

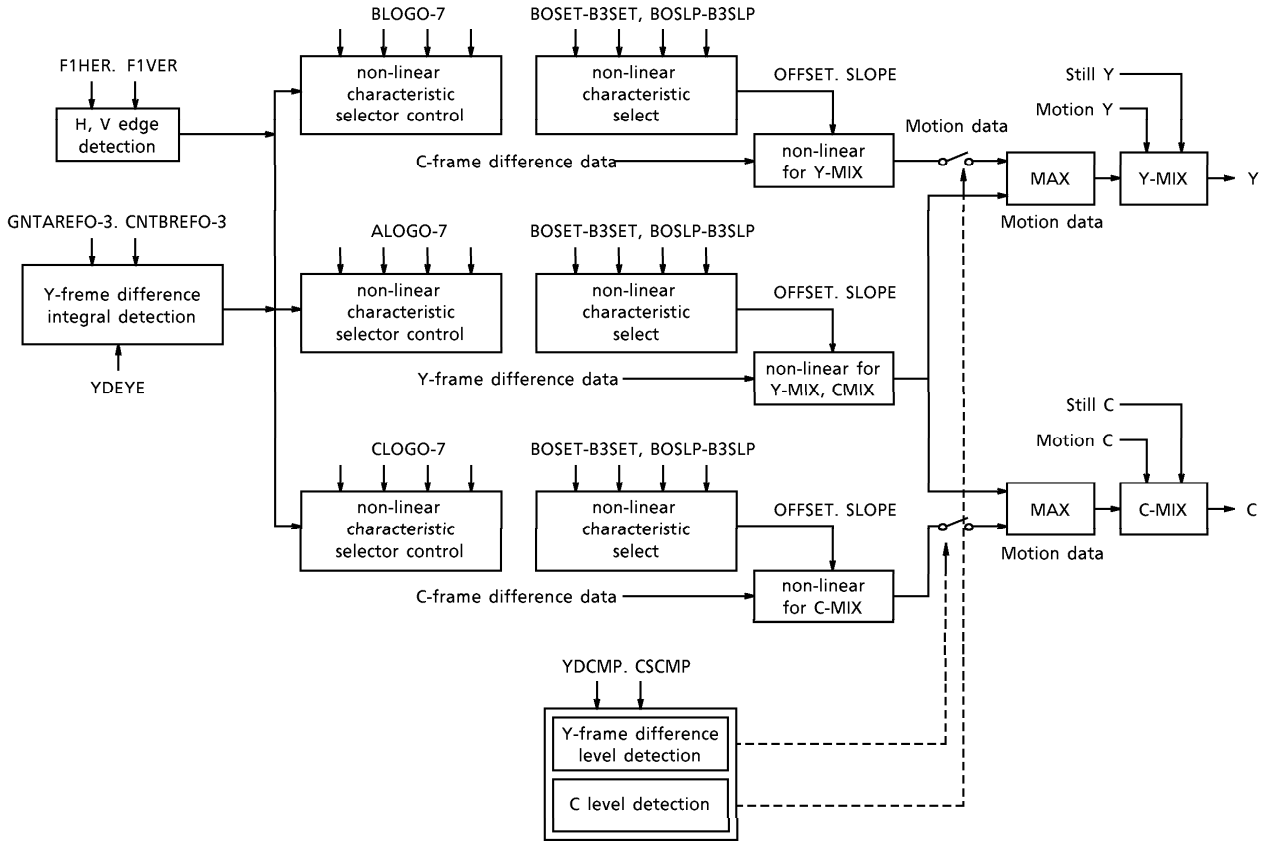
The motion detectors for Y and C signals have non-linear sensitivities to amount of differences between two frames in an area. Four sets of OFFSET and SLOPE of the non-linear characteristic can be set up through I^2C bus for both Y and C motion detectors individually.



The motion detector includes horizontal and vertical edges detectors to judge an objective pixel if it is on an edge of the picture, and calculates amount of differences between two frames in an area which includes the objective pixel to judge if the area is motion or still. There are four combination cases of the result for each pixel of the picture as below,

- on an edge in a motion area
- not on an edge in a motion area
- on an edge in a still area
- not on an edge in a still area

Four parameter sets of OFFSET and SLOPE, set up in 5CH to 5FH for Y signal (A0SET-A3SET and A0SLP-A3SLP) and 60H to 63H (B0SET-B3SET and B0SLP-B3SLP) for C signal, are applicable to each combination. Which parameter set is applied to a result combination is set up in 59H, 5AH and 5BH.

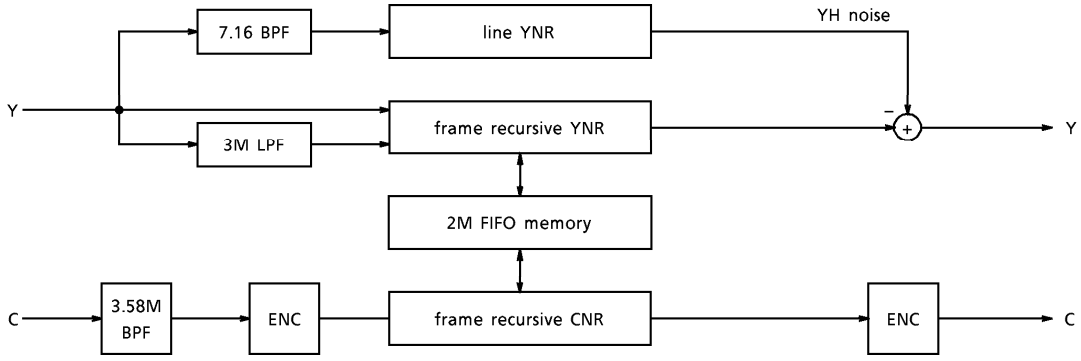


(E) Letter box detector (with simple method)

TC90A30AF can identify an input signal as a letter box picture with three results. One is to check if there are no-picture areas on upper and lower sides. The second is to check if there is the NRZ flags of the EDTV-2 on the line of 22H and 285H. The last is to check if there is the HH signal of the EDTV-2. Each result can be fixed ON / OFF through IIC bus. If all results are ON and if the input signal is identified as standard NTSC signal. The input signal is identified as a letter box picture. LTBX (pin 10) outputs the final result.

2. Noise reduction for VCR play back

TC90A30AF provides motion adaptive YNR and CNR functions. Noise signal in an still area of continuous two frames has seldom correlation, so that noise component is reduced after adding frames and dividing recursively. Frame recursive YNR applied to low frequency component of Y signal and demodulated color signal. High frequency component of Y signal discriminated with a 7.16MHz band pass filter applied coring to get high frequency noise, and added to the Y signal passing out of the recursive YNR.



3. Standard / non-standard detection

The standard / non-standard detection circuit identifies an input signal as a standard NTSC signal with checking synchronization between horizontal sync. and vertical sync. and between horizontal sync. and fsc. If the relation described as the equation below is formed, the input signal is identified as standard.

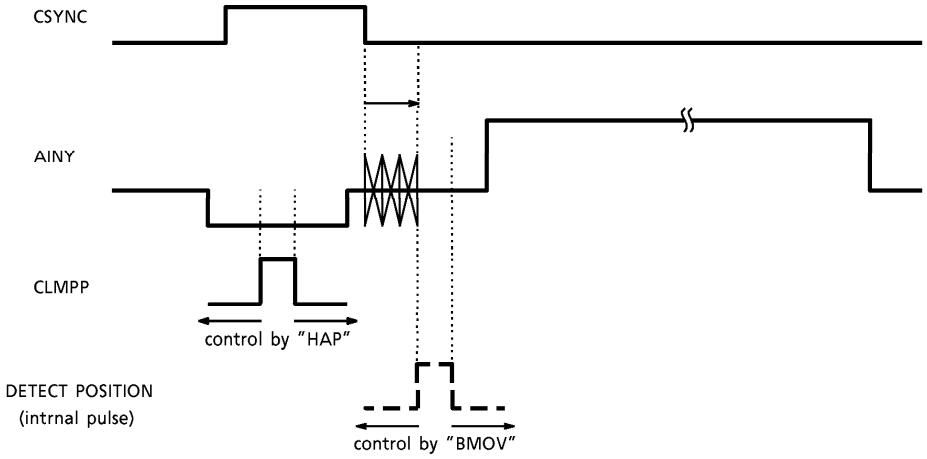
$$4\,fsc = 910 \times 525 / 2fv$$

4. On-chip AD converter

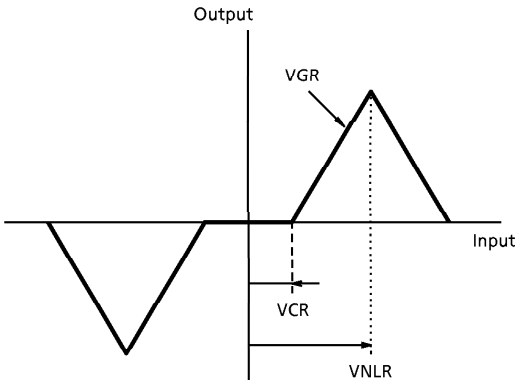
Two high speed 8-bit A / D converter are included in TC90A30AF. One is for Y and composite video signals' common use (YADC), The other is for chroma signal (CADC). Input level of both A / D converter should be smaller than 1.1 Vp-p.

YADC has a clamping circuit, so that the pedestal level is getting to be a level, between 63 to 78 LSB of YADC, set up by IIC bus. Actual clamping timing is at horizontal sync. period. Position of clamping pulse and width are set up by IIC bus in 3EH. CLMPP (pin 12) outputs the clamping pulse to be monitored. Timing to check the pedestal level for clamping operation is set up in 6CH (BMOV). There is no output to monitor the key pulse for pedestal level checking. Instated, CSYNC (pin 72) is available for a reference pulse for the key pulse. When BMOV = 0, the key pulse start from the position 0.7 usec delayed from the end of CSYNC. Width of the key pulse is fixed as 1.12 usec.

CADC does not have a clamping circuit, so that an external bias circuit is required.



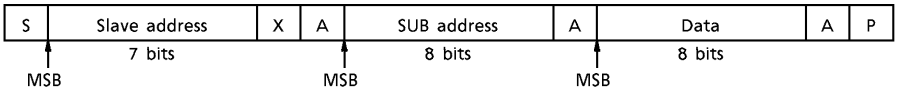
5. On-chip D / A converter
   Two 8-bit D / A converter are included in TC90A30AF. One is for Y signal output, and the other is for C signal output. The maximum output dynamic range is 1.5 Vp-p. VREF (52 pin) should be applied voltage more than (Vdd – 1.5 V).
6. Vertical edge enhancer
   Parameters for built-in vertical edge enhancer are set up in 46H. Gain, coring amplitude and coring limit are available to be controlled.



OUTLINE OF I²C BUS CONTROL FORMAT

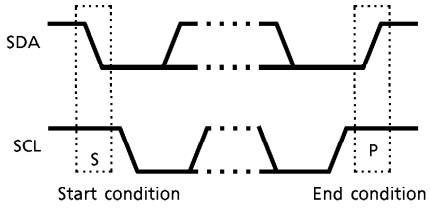
The bus control format of TC90A30AF conforms to the Philips I²C bus control format.

Data transfer format

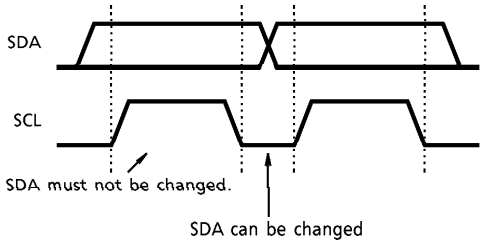


S : Start condition
P : Stop condition
A : Acknowledgement

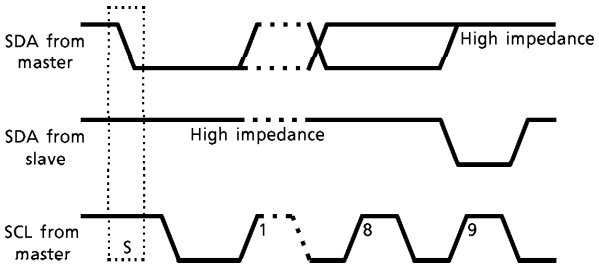
(1) Start and end conditions



(2) Bit transfer



(3) Acknowledgement



(4) Slave address

A6	A5	A4	A3	A2	A1	A0	R / $\overline{W}$
1	0	1	1	0	0	1	×

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

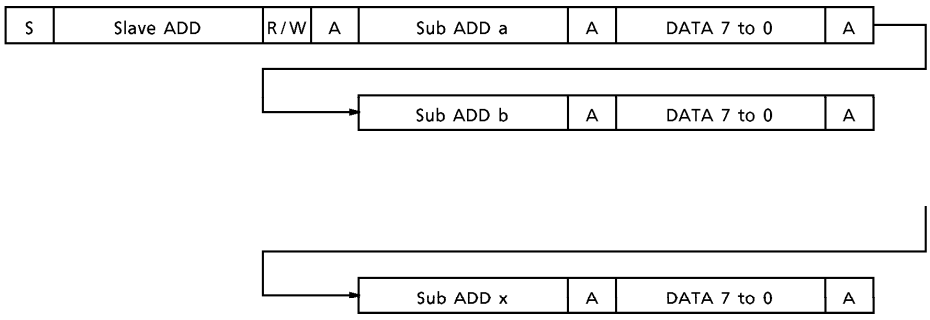
TC90A30AF I^2C COMMUNICATIONS FORMATS

(1) Write mode

The device supports continuous communications and auto increment as well as ordinary communications.

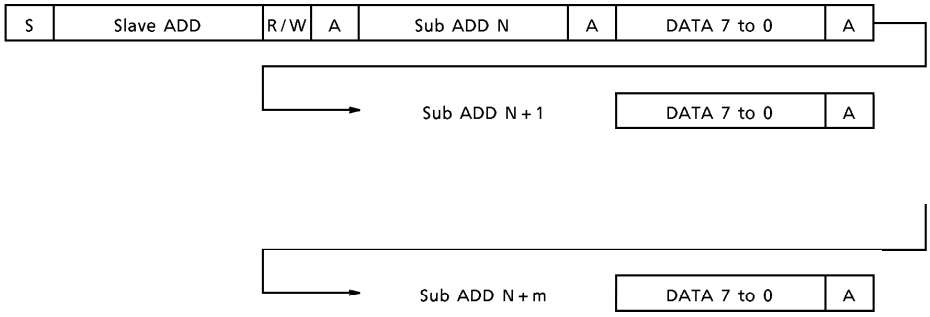
① Continuous communications

(Sub addresses can be set as desired. However, set sub address MSB = 0.)



② Auto increment

(Sub addresses are sequentially incremented from N. However, set sun address MSB = 1)



IIC Bus Map (slave address : B2H)

- Before applying power, set the RESET pin (pin 60) to low level and clear the register contents. All the register contents are then set to 0. With the TC90A30AF, default values are not set. Thus, note that unless settings are made, the device does not operate normally.
- Where register names are not given in the bus map below, set to the recommended values (0 or 1). Recommended values separated by slashes (eg, 1 / 0 and 0 / 1) are recommended values for YC separation mode / NR mode.

SUB ADDRESS	7	6	5	4	3	2	1	0
31-34	0	0	0	0	0	0	0	0
35	EDBLREF3-0				0	0	0	0
36	0	0	0	0	NRZOFF	LBOXOFF	0	M2MOFF
37-3F	Blank							
3D	ITKILL	0	0	0	0	0	0	0
3E	HAP7-0							
3F	0	0	0	0 / 1	0	0	0	0
40	KFY3-0				LIMLVLY3-0			
41	KFC3-0				LIMLVLC3-0			
42	DOTOFF	KLS	0	0	0	0	F1HER1-0	
43	0	F1VER1-0		L1DOT4-0				
44	Y2DNR1-0		0	0	0	0	0	0
45	0	0 / 1	0	0	0 / 1	VGR2-0		
46	VCR2-0			VNLR4-0				
47	0	0	0	0	0	0	0	0
48	0	0	0	INV	CSCMPY3-0			
49	0	0	FRPH5-0					
4A	0	FMPH6-0						
4B	0	0	0	0	0	0	1	0
4C	0	0	0	0	0	0	NE	0
4D	0	0	0	0	0	0	0	0
4E	MOINH	0	0	0	0	0	1 / 0	0
4F	0	0	0	0	0	0	1 / 0	1 / 0
50	0	1	HVSTD2	HVSTD1	HBSTD2	HBSTD1	0	0
51	0	0	0	VMPBL3-1			0	1
52	0	BGMODE	BGPH2-0			1	1 / 0	1
53	0	0	0	0	0	0	VENHACT / 0	0
54	1 / 0	1 / 0	1 / 0	1 / 0	1 / 0	1 / 0	0	YNONRCSV
55	SETUP2-0			0	0 / 1	0	MOMOVE	0
56	YSEIGAH	CYSEIGA	CCSEIGA	YHABAH	0	DOUGAH	0	0
57	YDCMP3-0				CSCMP3-0			
58	YDEYE3-0				CNTAREF1-0		CNTBREF1-0	

SUB ADDRESS	7	6	5	4	3	2	1	0
59	ALOG7-0							
5A	BLOG7-0							
5B	CLOG7-0							
5C	A0SET3-0				A0SLP1-0		1 / 0	1 / 0
5D	A1SET3-0				A1SLP1-0		0	0
5E	A2SET3-0				A2SLP1-0		0	0
5F	A3SET3-0				A3SLP1-0		0	0
60	B0SET3-0				B0SLP1-0		1 / 0	DOTW
61	B1SET3-0				B1SLP1-0		0	0
62	B2SET3-0				B2SLP1-0		0	0
63	B3SET3-0				B3SLP1-0		0	0
64	YDC1-0		YENHMP21-20		YENHMP31-30		ENH2MON	YNCON
65	CORE3-0				LIMLVLIT3-0			
66	LIMLVL13-10				LIMLVL23-20			
67	CNCLIM3-0				CNCON	REFLVL2-0		
68	YDL1-0		CDL1-0		YORC	YEMHMP41-40		0
69	ENHCORE3-0				GTCORE3-0			
6A	RECPLAY	ENHGAIN1-0		ENHON	0	1	1	0
6B	MBLNKACT	0	0	0	0	0	PSLICES	PSLICEOF
6C	OFFSET3-0				0	0	BPLKILL	0
6D	BMOV7-0							
70-7E	0	0	0	0	0	0	0	0

Sub address : 35H

○ EDBLREF : Switches sensitivity for detecting top and bottom blank portion (black level).

0 : Easy to determine top and bottom blank portion.
↓
15 : Hard to determine top and bottom blank portion.

Sub address : 36H

○ NRZOFF : Detects EDTV2 identifier NRZ signal.

0 : Detection on
1 : Detection off (always assumes NRZ)

○ NRZOFF : Detects EDTV2 identifier NRZ signal.

0 : Detection on
1 : Detection off (always assumes NRZ)

○ LBOXOFF : Detects top and bottom blank portion (black level).

0 : Detection on
1 : Detection off (always assumes top and bottom blank portion)

○ M2MOFF : Detects negative level of 4/7 fsc.

0 : Detection on
1 : Detection off (always assumes negative level)

Sub address : 3DH

○ ITKILL : Controls YC separation during IT and multiplex signal (10H to 21H, 273H to 284H)

0 : Stops YC separation during IT and multiplex signal.
1 : Separates YC during IT and multiplex signal.

Sub address : 3EH

○ HAP7 to 6 : Adjusts clamp pulse width.

0 : Narrow (approx. 2μs)
1 : Wide (approx. 5μs)

○ HAP5 to 0 : Adjusts clamp pulse position.

0 : Near beginning
↓ (variable in units of approx. 280ns)
63 : Near end

Sub address : 40H

○ KFY : YNR frame rotation coefficient.

0 : Rotation off (NR off)
1 : Low rotation coefficient (low NR effect)
↓
13 : High rotation coefficient (high NR effect)
(No 14 or 15)

○ LIMLVLY : YNR limter level

0 : Low limiter level
↓
15 : High limiter level

Sub address : 41H

○ KFC : CNR frame rotation coefficient

0 : Rotation off (NR off)
1 : Low rotation coefficient (low NR effect)
↓
13 : High rotation coefficient (high NR effect)
(No 14 or 15)

○ LIMLVLC : CNR limiter level

0 : Low limiter level
↓
15 : High limiter level

Sub address : 42H

○ DOTOFF : 1-line dot detector circuit

0 : Detection on
1 : Detection off

○ KLS : Controls color killer.

0 : Control on
1 : Control off

○ F1HER : Horizontal edge detection sensitivity

0 : Detection off
1 : Low detection sensitivity (hard to determine edge)
↓
3 : Hige detection sensitivity (easy to determine egde)

Sub address : 43H

○ F1VER : Vertical edge detection sensitivity

0 : Detection off
1 : Low detection sensitivity (hard to determine edge)
↓
3 : High detection sensitivity (easy to determine edge)

○ L1DOT : 1-line dot detection sensitivity

0 : Low detection sensitivity (easy to determine 1-line dot)
↓
31 : High detection sensitivity (easy to determine 1-line dot)

Sub address : 44H

○ Y2DNR : Controls Y high-frequency line NR gain.

0 : NR off
1 : Low NR effect
↓
3 : High NR effect

Sub address : 45H

○ VGR : Controls vertical enhancer component gain.

0 : Vertical enhancer off
3 : Low gain
Others : High gain

Sub address : 46H

○ VCR : Controls core ring amplitude of vertical enhancer.

0 : Core ring off
1 : Minimum
↓
7 : Maximum

○ VNLR : Controls amplitude limit level of vertical enhancer components.

0 : Limit control off
1 : Minimum limit level
↓
15 : Maximum limit level

Sub address : 49H

○ FRPH : Adjusts phase difference for frame memory read or write (adjusts frame delay time).

0 to 63 : Adjusts in units of 70 ns.

- YC separation mode : 35 (23Hex), NR mode : 23 (17Hex)

Sub address : 4AH

○ FMPH : Adjusts memory blanking position (adjusts memory load position).

0 to 127 : Adjusts in units of 70 ns.

- NR mode : 73 to 127, Adjusts in units of 70 ns.

Sub address : 4CH

○ NE : Selects memory (read / write reset polarity, write data delay time).

0 : NEC 2M (negative polarity, 1ck delay)
1 : Oki 2M (positive polarity, 0ck delay)

Sub address : 4EH

○ MOINH : Controls external memory control output high impedance.

0 : Normal
1 : Outputs high impedance.

Sub address : 50H

○ HVSTD2 : Controls H / V standard discriminator circuit.

0 : Uses circuit (discrimination on)
1 : Forcibly controls standard / non-standard (discrimination off)

○ HVSTD1 : Switches forced H / V standard / non-standard.

0 : Non-standard
1 : Standard
• Valid when HVSTD2 = 1.

○ HBSTD2 : Controls H-fsc standard discriminator circuit.

0 : Uses circuit (discrimination on).
1 : Forcibly controls standard / non-standard (discrimination off).

○ HBSTD1 : Switches forced H-fsc standard / non-standard.

0 : Non-standard
1 : Standard
• Valid when HBSTD2 = 1.

Sub address : 51H

○ VMPBL : Adjusts mask pulse position during V.

Sub address : 52H

○ BGMODE : Adjusts burst gate (BG) output amplitude for TA1221AF.

0 : Wide
1 : Narrow

○ BGPH : Finely adjusts burst gate (BG) output position for TA1221AF.

0 to 7 : Adjusts in units of 70 ns.

Sub address : 53H

○ VENHACT : Turns on / off vertical enhancer.

0 : Off
1 : On
• Used in YC separation mode. Set to 0 in NR mode.

Sub address : 54H

○ YNONRCSV : Switches recursive / non-recursive YNR.

0 : Recursive
1 : No recursive

Sub address : 55H

○ SETUP : Controls slice level for pedestal slice.

• When PSLICES = 0 at sub address 6BH :

0 : Slices at 64LSB.
↓
7 : Slices at 78LSB.

• When PSLICES = 1 at sub address 6BH :

0 : Slices 48LSB.
↓
7 : Slices at 62LSB.

MOMOVE : Forces motion picture (dedicated to YC separation mode).

0 : Normal
1 : Forces motion picture.

Sub address : 56H

○ YSEIGAH : Forces Y still picture.

0 : Normal
1 : Forces still picture.

○ CYSEIGA : Forces Y still picture for detecting C motion picture.

0 : Normal
1 : Forces still picture.

○ CCSEIGA : Forces C still picture for detecting C motion picture.

0 : Normal
1 : Forces still picture.

○ YHABAH : Controls Y motion picture processing width.

0 : Narrow
1 : Wide

○ DOUGAH : Forces motion picture (dedicated to NR mode).

0 : Normal
1 : Forces motion picture.

Sub address : 57H

○ YDACMP : Controls Y-frame difference detection sensitivit
(for detecting Y-frame difference level).

0 : High detection sensitivity (easy to determine frame difference).
1 : Low detection sensitivity (hard to determine frame difference).

○ CSCMP : Controls C level detection sensitivity (for detecting C-frame level).

0 : High detection sensitivity (easy to determine color).
1 : Low detection sensitivity (hard to determine color).

Sub address : 58H

○ YDEYE : Controls Y-frame difference detection sensitivity
(for detecting Y-frame difference integral).

0 : High detection sensitivity (easy to determine frame difference).
1 : Low detection sensitivity (hard to determine frame difference).

○ CNTAREF : Detects number of motion picture pixels per field for detecting Y motion picture (for detecting Y-frame difference integral).

0 : High detection sensitivity (easy to determine motion picture).
1 : Low detection sensitivity (hard to determine motion picture).

○ CNTBREF : Detects number of motion picture pixels per field for detecting Y motion picture (for detecting Y-frame difference integral).

0 : High detection sensitivity (easy to determine motion picture).
1 : Low detection sensitivity (hard to determine motion picture).

Sub address : 59H

○ ALOG : Automatically switches Y motion picture detection non-linear characteristic for Y.

- Selects non-linear characteristic (A0SET, A0SLP to A3SET, A3SLP) for four combinations of results of detecting Y-frame difference integral (for detecting Y motion picture) and edge.

DETERMINING PARAMETER	NON-LINEAR CHARACTERISTIC SELECTE			
Y-frame Difference Integral Detection Result	Motion picture determined	Motion picture determined	Still picture determined	Still picture determined
Edge Detection Result	Edge determined	Plane determined	Edge determined	Plane determined
	Set by AL0G7, 6	Set by AL0G5, 4	Set by AL0G3, 2	Set by AL0G1, 0

0 : Selects A0SET and A0SLP.
1 : Selects A1SET and A1SLP.
2 : Selects A2SET and A2SLP.
3 : Selects A3SET and A3SLP.

Sub address : 5AH

○ BLOG

- In YC separation mode : Automatically switches C motion picture detection non-linear characteristic for Y.

  Selects non-linear characteristic (B0SET, B0SLP to B3SET, B3SLP) for four combinations of results of detecting Y-frame difference integral (for detecting Y motion picture) and edge.

DETERMINING PARAMETER	NON-LINEAR CHARACTERISTIC SELECTE			
Y-frame Difference Integral Detection Result	Motion picture determined	Motion picture determined	Still picture determined	Still picture determined
Edge Detection Result	Edge determined	Plane determined	Edge determined	Plane determined
	Set by BL0G7, 6	Set by BL0G5, 4	Set by BL0G3, 2	Set by BL0G1, 0

0 : Selects B0SET and B0SLP.
1 : Selects B1SET and B1SLP.
2 : Selects B2SET and B2SLP.
3 : Selects B3SET and B3SLP.

- In NR mode : Automatically switches Y motion picture detection non-linear characteristic for C.

  Selects non-linear characteristic (A0SET, A0SLP to A3SET, A3SLP) for four combinations of results of detecting Y-frame difference integral (for detecting C motion picture) and edge.

DETERMINING PARAMETER	NON-LINEAR CHARACTERISTIC SELECTE			
Y-frame Difference Integral Detection Result	Motion picture determined	Motion picture determined	Still picture determined	Still picture determined
Edge Detection Result	Edge determined	Plane determined	Edge determined	Plane determined
	Set by AL0G7, 6	Set by AL0G5, 4	Set by AL0G3, 2	Set by AL0G1, 0

0 : Selects A0SET and A0SLP.
1 : Selects A1SET and A1SLP.
2 : Selects A2SET and A2SLP.
3 : Selects A3SET and A3SLP.

Sub address : 5BH

○ CLOG

- In YC separation mode : Automatically switches C motion picture detection non-linear characteristic for C.

  Selects non-linear characteristic (B0SET, B0SLP to B3SET, B3SLP) for four combinations of results of detecting Y-frame difference integral (for detecting C motion picture) and edge.

DETERMINING PARAMETER	NON-LINEAR CHARACTERISTIC SELECTE			
Y-frame Difference Integral Detection Result	Motion picture determined	Motion picture determined	Still picture determined	Still picture determined
Edge Detection Result	Edge determined	Plane determined	Edge determined	Plane determined
	Set by CL0G7, 6	Set by CL0G5, 4	Set by CL0G3, 2	Set by CL0G1, 0

0 : Selects B0SET and B0SLP.
1 : Selects B1SET and B1SLP.
2 : Selects B2SET and B2SLP.
3 : Selects B3SET and B3SLP.

- In NR mode : Automatically switches C motion picture detection non-linear characteristic for C. Selects non-linear characteristic (B0SET, B0SLP to B3SET, B3SLP) for four combinations of results of detecting Y-frame difference level, C-frame level and edge.

DETERMINING PARAMETER	NON-LINEAR CHARACTERISTIC SELECTE			
Y-frame Difference Level, C-frame Level Detection Result	No color determined	No color determined	Color determined	Color determined
Edge Detection Result	Edge determined	Plane determined	Edge determined	Plane determined
	Set by CL0G7, 6	Set by CL0G5, 4	Set by CL0G3, 2	Set by CL0G1, 0

0 : Selects B0SET and B0SLP.
1 : Selects B1SET and B1SLP.
2 : Selects B2SET and B2SLP.
3 : Selects B3SET and B3SLP.

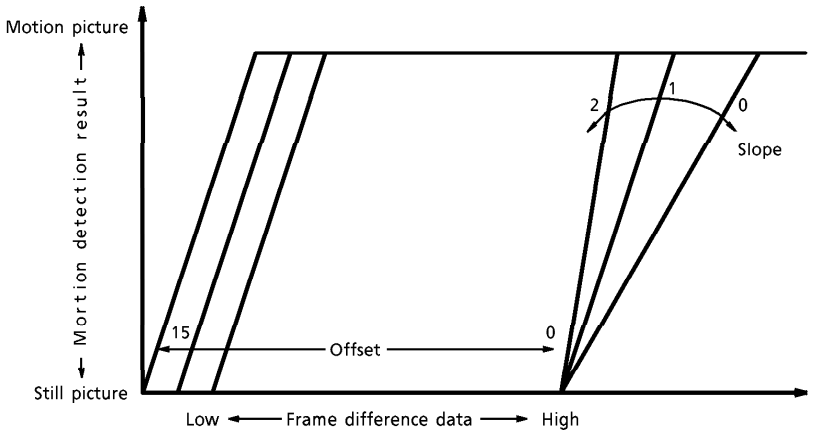
Sub address : 5CH

○ A1SET : Non-linear characteristic offset 0 for detecting Y motion picture

0 : High offset (still picture direction)
↓
15 : Low offset (moving picture direction)

○ A0SLP : Non-linear characteristic slope 0 for detecting Y motion picture

0 : Low slope (still picture direction)
↓
2 : High slope (moving picture direction)
3 : Not available



Sub address : 5DH

○ A1SET : Non-linear characteristic offset 1 for detecting Y motion picture

0 : High offset (still picture direction)
↓
15 : Low offset (nearer to motion picture)

○ A1SLP : Non-linear characteristic slope 1 for detecting Y motion picture

0 : Low slope (nearer to still picture)
↓
2 : High slope (nearer to motion picture)
3 : Not available

Sub address : 5EH

○ A2SET : Non-linear characteristic offset 2 for detecting Y motion picture

0 : High offset (nearer to still picture)
↓
15 : Low offset (nearer to motion picture)

○ A2SLP : Non-linear characteristic slope 2 for detecting Y motion picture

0 : Low slope (nearer to still picture)
↓
2 : High slope (nearer to motion picture)
3 : Not available

Sub address : 5FH

○ A3SET : Non-linear characteristic offset 3 for detecting Y motion picture

0 : High offset (nearer to still picture)
↓
15 : Low offset (nearer to motion picture)

○ A3SLP : Non-linear characteristic slope 3 for detecting Y motion picture

0 : Low slope (nearer to still picture)
↓
2 : High slope (nearer to motion picture)
3 : Not available

Sub address : 60H

○ B0SET : Non-linear characteristic offset for detecting C motion pictur.

0 : High offset (nearer to still picture)
↓
15 : Low offset (nearer to motion picture)

○ B0SLP : Non-linear characteristic slope for detecting C motion picture

0 : Low slope (nearer to still picture)
↓
2 : High slope (nearer to motion picture)
3 : Not available

○ DOTW : Motion picture processing range for detecting color motion picture

0 : 2 dots
1 : 4 dots

Sub address : 61H

○ B1SET : Non-linear characteristic offset for detecting C motion picture.

0 : High offset (nearer to still picture)
↓
15 : Low offset (nearer to motion picture)

○ B1SLP : Non-linear characteristic slope for detecting C motion picture

0 : Low slope (nearer to still picture)
↓
2 : High slope (nearer to motion picture)
3 : Not available

Sub address : 62H

○ B2SET : Non-linear characteristic offset for detecting C motion picture.

0 : High offset (nearer to still picture)
↓
15 : Low offset (nearer to motion picture)

○ B2SLP : Non-linear characteristic slope for detecting C motion picture

0 : Low slope (nearer to still picture)
↓
2 : High slope (nearer to motion picture)
3 : Not available

Sub address : 63H

○ B3SET : Non-linear characteristic offset for detecting C motion picture.

0 : High offset (nearer to still picture)
↓
15 : Low offset (nearer to motion picture)

○ B3SLP : Non-linear characteristic slope for detecting C motion picture

0 : Low slope (nearer to still picture)
↓
2 : High slope (nearer to motion picture)
3 : Not available

Sub address : 64H

○ YDC : Adds DC gain for Y enhancer.

0 : Addition off
1 : High gain
↓
3 : Low gain

○ YENHMP2 : Enhances 3.58MHz components for Y enhancer.

0 : Enhancement off
1 : Low enhancement
↓
3 : High enhancement

○ YENHMP3 : Enhances 2MHz components for Y enhancer.

0 : Enhancement off
1 : Low enhancement
↓
3 : High enhancement

○ ENH2MON : Turns on / off 2MHz components for Y enhancer.

0 : 2MHz components off
1 : 2MHz components on

○ YNC : Turns on / off YNC (noise canceller) for Y enhancer.

0 : YNC off
1 : YNC on

Sub address : 65H

○ CORE : Core ring level of 2MHz components for Y enhancer.

0 : Core ring off
1 : Minimum
↓
15 : Maximum

○ LIMLVL1 : IT duration limit level of YNC.

0 : Low limit level
↓
15 : High limit level

Sub address : 66H

○ LIMLVL1 : YNC still picture limit level

0 : Low limit level
↓
15 : High limit level

○ LIMLVL2 : YNC motion picture limit level

0 : Low limit level
↓
15 : High limit level

Sub address : 67H

○ CNCLIM : CNC (C noise canceller) limit level

0 : Low limit level
↓
15 : High limit level

○ CNC : Turns on / off CNC (C noise canceller).

0 : CNC off
1 : CNC on

○ REFLVL : Motion / still picture switching level for YNC limiter level

0 : Nearer to motion picture
1 : Nearer to still picture

Sub address : 68H

○ YDL : Adjusts Y signal delay time.

0 to 3 : Adjusts in units of 70ns.
- Valid only when YROC = 0. When YROC = 1, set to 0.

○ CDL : Adjusts C signal delay time.

0 to 3 : Adjusts in units of 70ns.
- Valid only when YROC = 1. When YROC = 0, set to 0.

○ YROC : Switches Y / C delay

0 : Delays Y.
1 : Delays C.

○ YENHMP4 : Enhances 3.58MHz components for Y enhancer (during IT)

0 : Enhancement off
1 : Low enhancement
↓
3 : High enhancement

Sub address : 69H

○ ENHCORE : C enhancer core ring level

0 : Core ring off
1 : Minimum
↓
15 : Maximum

○ GTCORE : C enhancer core ring level (during range specification gate)

0 : Core ring off
1 : Minimum
↓
15 : Maximum

Sub address : 6AH

○ RECPLAY : C enhancer high-frequency filter tap width

0 : Four steps (YC separation mode)
1 : Eight steps

○ ENHGAIN : C enhancer gain

0 : High gain
1 : Low gain

○ ENHON : Turns on / off C enhancer.

0 : Off
1 : On

Sub address : 6BH

○ MBLKACT : Turns on / off C enhancer during memory blank.

0 : Memory blank duration on
1 : Memory blank duration off

○ PSLICES : Pedestal slice level

0 : NR mode (48LSB)
1 : YC separation mode (64LSB)

○ PSLICEOFF : Turns on / off pedestal slice.

0 : On
1 : Off

Sub address : 6BH

○ OFFSET : Sets clamp level for Y composite.

0 : 63LSB
↓
15 : 78LSB

○ BPLKILL : Controls clamp during V.

0 : Does not stop.
1 : Stops.

Sub address : 6CH

○ BMOV : Adjusts clamp level detection position flag.

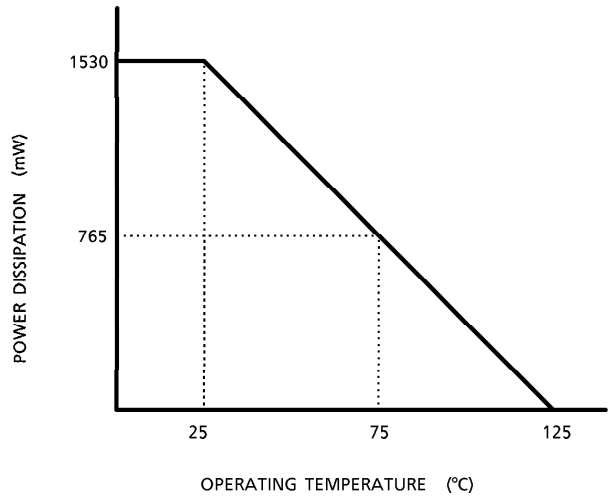
0 to 7 : Adjusts in units of 280 ns.

MAXIMUM RATINGS (Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}~V_{SS} + 4.5	V
Input Voltage 1	V_{IN1}	− 0.3~V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	− 0.3~5.5 (Note 1)	V
Power Dissipation	P_D	1530 (Note 2)	mW
Storage Temperature	T_{stg}	− 55~125	°C

(Note 1) : Applicable to the MI7 to MI0, SCL, and SDA pins.
(Note 2) : When using the device at Ta = 25°C or higher, reduce power dissipation by 15.3 mW per degree.

Power Dissipation versus Operating Temperature (when device mounted on board)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V_{DD}	—	3.0	3.3	3.6	V
Input Voltage	V_{IN}	—	0	—	V_{DD}	V
Operating Temperature	V_{opr}	—	– 20	—	75	°C

ELECTRICAL CHARACTERISTICS

DC characteristics

DC characteristics for digital portion (Ta = 25°C, V_{DD} = 3.3V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	APPLICABLE PIN
Current Dissipation	IDD	—			180	210	mA	
High-level Output Voltage	VOH1	—	When 10H = – 4mA	V_{DD} – 0.4			V	(Note 1)
Low-level Output Voltage	VOL1	—	When 10L = 4mA			0.4	V	(Note 1, 2)
High-level Input Voltage	VIH1	—		V_{DD} *0.8			V	(Note 3)
	VIH2	—		2.4				(Note 4)
	VIH3	—		2.4		5.5		(Note 5, 2)
Low-level Input Voltage	VIL1	—				V_{DD} *0.2	V	(Note 3)
	VIL2	—				0.8		(Note 4)
	VIL3	—				0.8		(Note 5, 2)
High-level Input Current	IIH	—	VIH = V_{DD}			10	μA	(Note 3, 4, 5)
Low-level Input Current	IIL	—	VIL = GND	– 10			μA	(Note 3, 4, 5)

(Note 1) RSTW, POTO-7, LTBX, BG, CLMPP, PWM, FSC80, ACK, RSTR, RCK, MO7-4, FSC4, MO3-0, WCK

(Note 2) SDA

(Note 3) ADT0-7, MOD0-2, PLLCTL, RESET, PST0-10, CKILL

(Note 4) CSYNC

(Note 5) MI7-0, SCL

Electrical characteristics for ADC and clamp portions (Ta = 25°C, V_{DD} = 3.3V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	APPLI-CABLE PIN
Resolution	Rs	—			8		bits	
Signal Input Level	ADIN	—	0~140IRE			1.1	V_{p-p}	(Note 6)
Input Dynamic Range		—		1 / 3 V_{DD}		2 / 3 V_{DD}	V	
Integral Non-linear Error	ILE	—	Operation @14.3MHz		± 1.0		LSB	
Differential Non-linear Error	DLE	—	Operation @14.3MHz		± 1.0		LSB	
AINY Clamp Level	YIN	—	Pedestal level		63		LSB	

(Note 6) AINY, AINC

Electrical characteristics for DAC portion (Ta = 25°C, V_{DD} = 3.3V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	APPLI-CABLE PIN
Resolution	Rs	—			8		bits	
Output Dynamic Range	DAOUT	—				1.5	V_{p-p}	(Note 7)
Reference Voltage Input Level	VREFDA	—		V_{DD} – 1.5			V	VREF
Output Resistance	Zout	—			200		Ω	(Note 7)
Integral Non-linear Error	ILE	—	Operation @14.3MHz		± 1.0		LSB	
Differential Non-linear Error	DLE	—	Operation @14.3MHz		± 1.0		LSB	

(Note 7) YOUT, COUT

AC characteristics (Ta = 25°C, V_{DD} = 3.3 V)

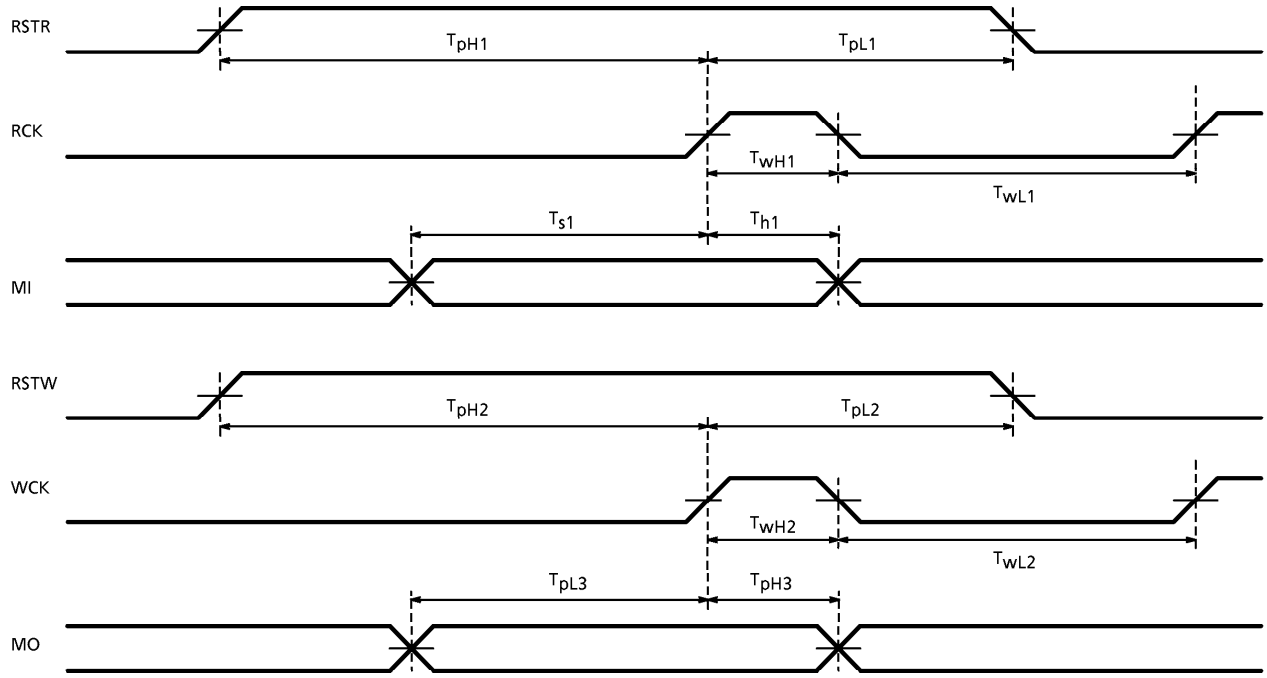
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	APPLICABLE PIN
Memory Read Data Setup Time	Ts1	—	Load capacitance of 20 pF	20			ns	RCK versus MI0 to MI7
Memory Read Data Hold Time	Th1	—		0			ns	
Memory Write Data Output Signal Phase Difference	TpL3	—		20			ns	WCK versus MO0 to MI7
	TpH3	—		20				
Memory Read Reset Output Signal Phase Difference	TpH1	—		20			ns	RCK versus RSTR
	TpL1	—		20				
Memory Write Reset Output Signal Phase Difference	TpH2	—		20			ns	WCK versus RSTW
	TpL2	—		20				
Memory Read Clock High-level Width	TwL1	—		20			ns	RCK
Memory Read Clock Low-level Width	TwH1	—		20			ns	
Memory Write Clock High-level Width	TwL2	—		20			ns	WCK
Memory Write Clock Low-level Width	TwH2	—		20			ns	
fsc (pin 36) Input Level	Lsc	—		0.3	1	2	V_{p-p}	
fsc Input Frequency Range	Fsc	—		3.57	3.58	3.59	MHz	

AC characteristics for IIC bus portion (Ta = 25°C, V_{DD} = 3.3 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	REMARK
SCL Clock Frequency	f_{SCL}	—	f_{SCL} = 1 / TSCL *B	0	—	100	kHz	
SCL High-level Duration	f_{SH}	—	C_L = 400 pF *B	4	—	—	μs	
SCL Low-level Duration	f_{SL}	—	C_L = 400 pF *B	4.7	—	—	μs	
Data Setup Time	f_{DS}	—	C_L = 400 pF *B	250	—	—	ns	
Data Hold Time	f_{DH}	—	C_L = 400 pF *B	5	—	—	μs	
Transfer Start Condition Hold Time	f_{SCH}	—	C_L = 400 pF *B	4	—	—	μs	
Transfer End Condition Hold Time	f_{ECS}	—	C_L = 400 pF *B	4.7	—	—	μs	
Data Transfer Interval	f_{BUF}	—	C_L = 400 pF *B	4.7	—	—	μs	
IIC Rise Time	f_{Ir}	—	C_L = 400 pF *B	—	—	1	μs	
IIC Fall Time	f_{If}	—	C_L = 400 pF *B	—	—	300	ns	

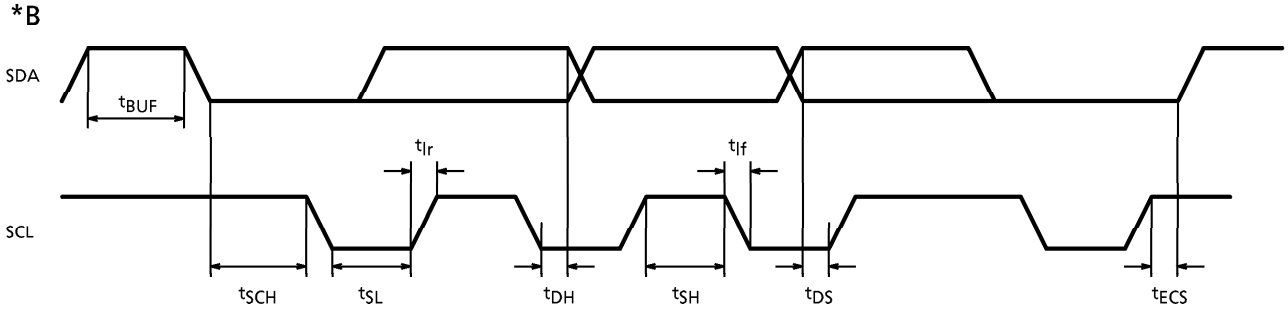
TIMING CHART

*A



IIC BUS TIMING

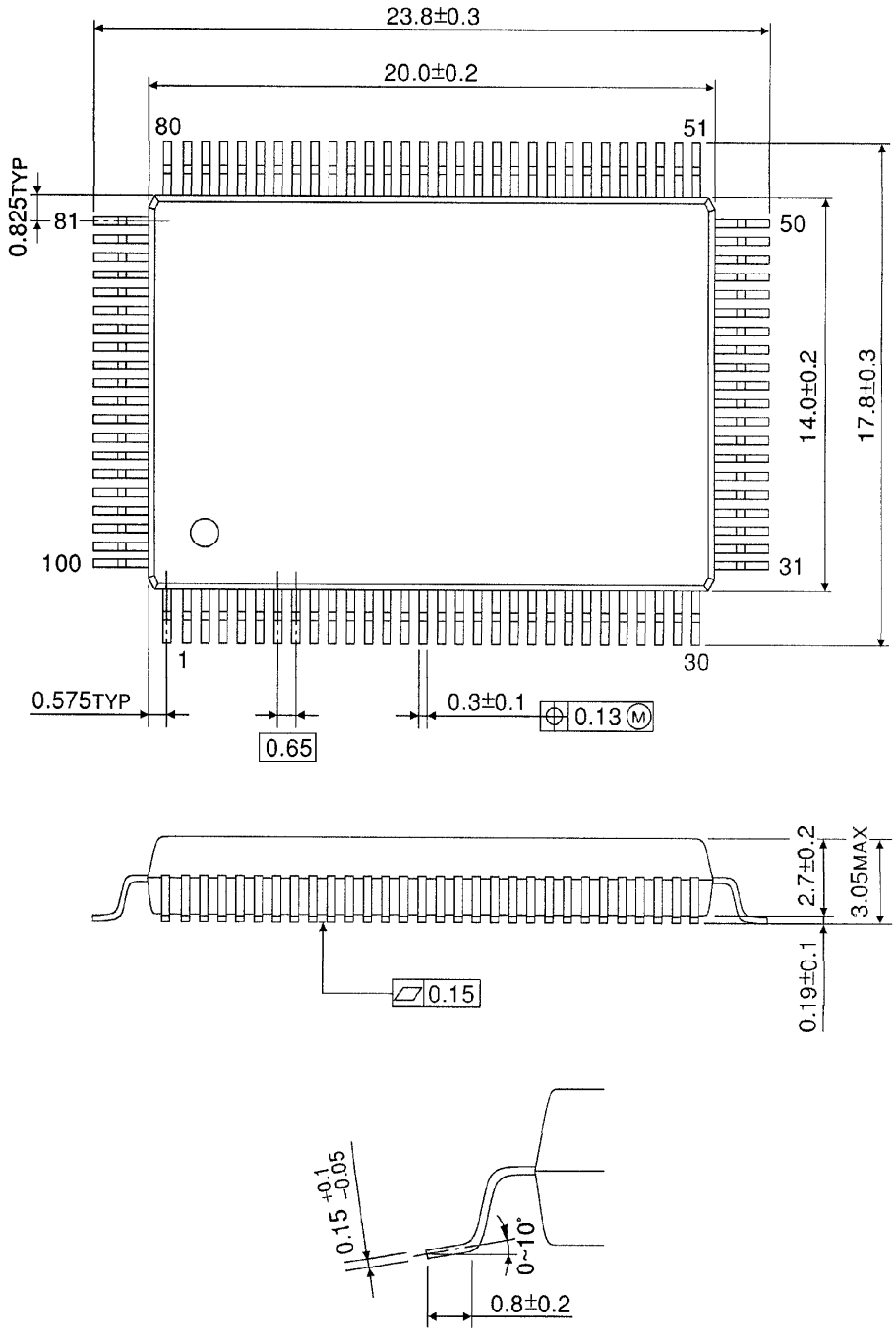
*B



Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

PACKAGE DIMENSIONS

QFP100-P-1420-0.65A Unit : mm



Weight : 1.6 g (Typ.)