Intel® 460GX Chipset Datasheet

Product Features

- High performance hardware based on IA-64 architecture
  - — 4.2 GB/s memory bandwidth can simultaneously support both the full system bus and the full I/O bus bandwidths
  - — Architectural support for 64 MB to 64 GB of SDRAM
  - — Support for up to four bridge chips that interface to the 82461GX (SAC) through four Expander channels, each 30 bits wide and providing 533 MB/s peak bandwidth
  - — AGP 4X compatible, via the 82465GX (GXB) and two Expander channels running at 266 MHz totaling 1 GB/s peak bandwidth
  - — Support for two 64-bit, 66-MHz PCI buses using one 82466GX (WXB) component per Expander channel
  - — Support for two independent 32-bit, 33-MHz PCI buses or one 64-bit, 33-MHz PCI bus via the 82467GX (PXB) per Expander channel
  - — Data streaming support between Expanders and DRAM, up to 533 MB/s per Expander channel
- Extensive RAS features for mission-critical needs
  - — ECC protection on the system bus data signals
  - — Memory ECC with single-bit error correction, double and nibble error detection
  - — Address and data flows protected by parity throughout chipset
  - — ECC bits in DRAM accessible by diagnostics
  - — Fault recording of multiple errors; sticky through reset
  - — JTAG TAP port for debug and boundary scan capability
  - — I2C slave interface for viewing and modifying specific error and configuration registers
  - — Bus, memory and I/O performance counters
  - — Support of ACPI/DMI functions (support is provided in the IFB)
- High bandwidth system bus for multiprocessor scalability
  - — Support of the Intel® Itanium™ processor 64-bit data bus
  - — Full support for 4-way multiprocessing
  - — 266 MHz data bus frequency
  - — Cache line size of 64 bytes
  - — Enhanced defer feature for out-of-order data delivery using IDS#
  - — AGTL+ bus driver technology
- Features to support flexible platform environments
  - — Hardware compatible with IA-32 binaries
  - — AGP address space up to 32 GB supported
  - — Support for Auto Detection of SDRAM memory type and mixed memory sizes allowed between rows
  - — Supports 16-, 64-, 128- and 256-Mbit DRAM devices
  - — Full support for the PCI Configuration Space Enable (CSE) protocol to devices on all Expander channels
  - — WXB supports 3.3 volt PCI bus operation (supports universal and 3.3 volt PCI cards) and has an Integrated Hot-Plug Controller**
  - — PCI Rev. 2.2 compliant on the WXB and PXB
  - — GXB supports fast writes and 1x, 2x and 4x data rates
  - — 1 MB or greater of firmware storage provided by the 82802AC (FWH)
  - — Interrupt controller, bus-mastering IDE and Universal Serial Bus supported by the 82468GX (IFB)
  - — Support of 8259A mode, APIC mode and SAPIC mode interrupts via the UPD55566S1-016 (PID) provided by NEC*

The Intel® 460GX chipset, the first Intel chipset in the Itanium™ processor family, is optimized for 1–4 way Itanium processor platforms and offers high performance and availability for e-business. The 64 GB of system memory support and 4.2 GB/s of memory bandwidth provide outstanding performance for server transactions and workstation simulation by enabling the memory bus to feed both the full system bus and I/O bus bandwidths simultaneously. The 460GX provides high-end capabilities for web servers and graphics intensive applications thanks to the 2-GB I/O bandwidth as well as support of multiple GB ethernet cards and AGP 4X. SMBus compatibility and comprehensive reliability, availability and serviceability (RAS) features enable highly available servers for e-business applications.

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Introduction 1

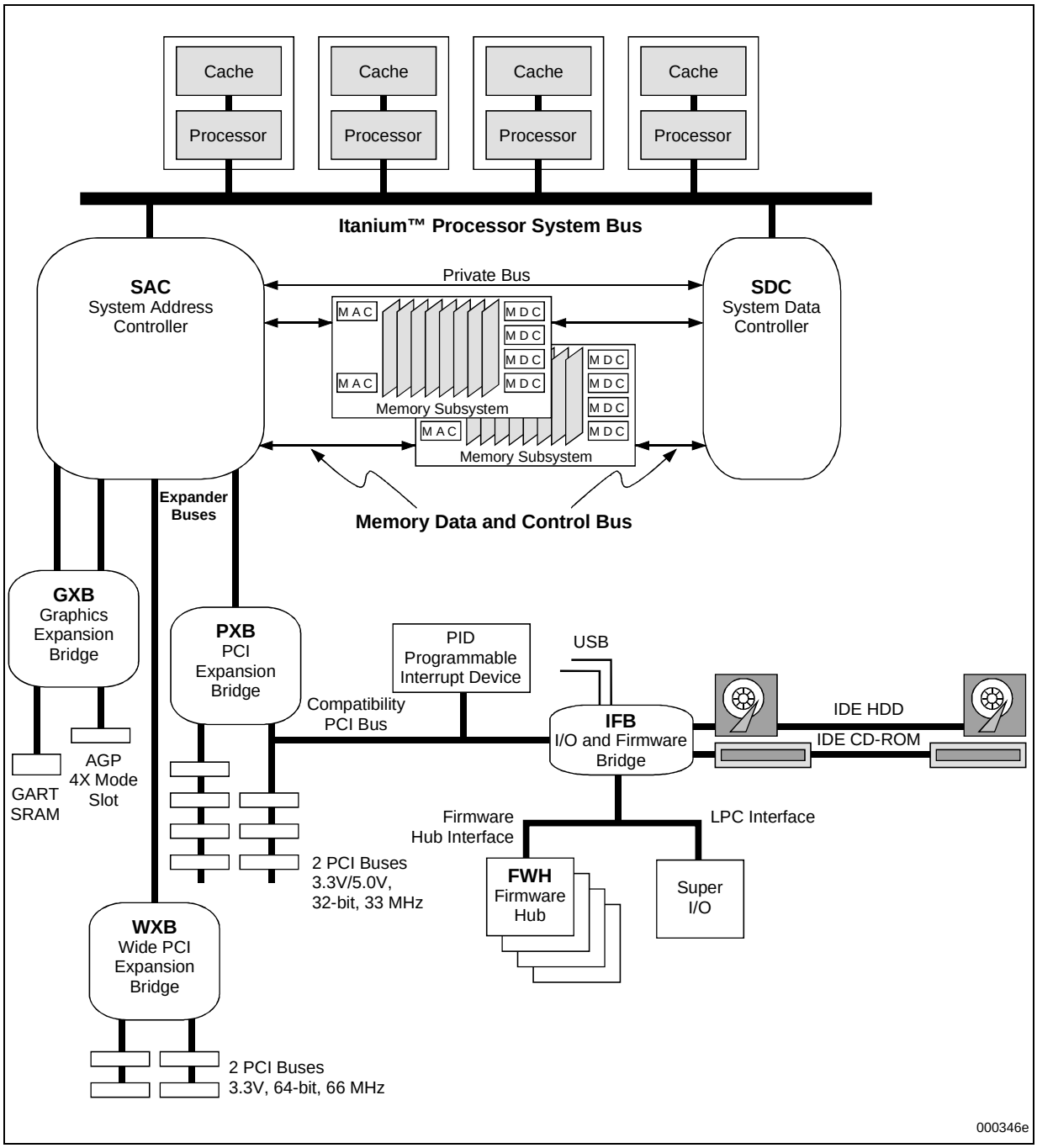
This document provides the Intel® 460GX chipset signal lists, electrical specifications, power specifications, maximum ratings, thermal specifications, ball-out lists, and package specifications for each component in the chipset. In addition, DC electrical specifications, AC timing specifications, and other design considerations are included for each interface.

Note: This document contains data that is subject to change. Intel shall have no responsibility for conflicts or incompatibilities arising from future changes to the data contained in this document. Please consult http://developer.intel.com for any changes to the components included in this documentation.

1.1 System Overview

The Intel 460GX chipset is a high performance chipset for Itanium™ processor-based systems, targeted for multiprocessor servers and high-performance workstations. It provides the memory controller interface and appropriate bridges to PCI, AGP 4X (a high-performance graphics port), and other standard I/O buses. Figure 1-1 illustrates the basic system configuration of a four-processor platform.

Figure 1-1. Diagram of a Typical Intel® 460GX Chipset-based System with AGP



1.1.1 Component Overview

Table 1-1 lists the Intel 460GX chipset components.

Table 1-1. Intel® 460GX Chipset Components

Component	Name	Function
SAC	82461GX System Address Controller	Interfaces the address and control portion of the Itanium processor system bus and the memory bus. Acts as a host bridge interface to peripheral I/O devices through four Expander channels.
SDC	82462GX System Data path Controller	Interfaces the data portion of the Itanium processor system bus and the memory bus.
MAC	82463GX Memory Address Controller	Provides the SDRAM RAS/CAS/WE/CS generation as well as redriving the address to the SDRAMs. It is capable of buffering several commands from the SAC.
MDC	82464GX Memory Data path Controller	Multiplexes the data from the SDRAM to the SDC. On reads, it latches data from the SDRAM, then transfers the data to the SDC. On writes, it latches the data from the SDC, then writes the data to the SDRAM.
GXB	82465GX Graphics eXpander Bridge	Provides the control and data interface for an AGP 4X graphics port. This device attaches to the SAC via two Expander channels which utilize a special configuration.
WXB	82466GX Wide and fast PCI eXpander Bridge	Provides the primary control and data interface for two independent 64-bit, 66 MHz PCI interfaces. This device attaches to the SAC via an Expander channel.
PXB	82467GX PCI eXpander Bridge	Provides the primary control and data interface for two independent 32-bit, 33-MHz PCI interfaces. These two 32-bit interfaces may operate together to produce a single 64-bit, 33-MHz interface via a configuration option. This device attaches to the SAC via an Expander channel.
IFB	82468GX I/O and Firmware Bridge	The IFB is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus Host/Hub function, an SMBus Interface function, Power Management function and the Firmware Hub interface.
FWH	82802AC Firmware Hub 8Mb	The FWH component interfaces to the IFB component and provides firmware storage and security features. Further FWH information can be found at http://developer.intel.com/design/chipsets/datashts or by ordering document 290658-003.
PID	NEC# UPD66566S1-016 Programmable Interrupt Device	The PID is an interrupt controller that provides interrupt steering functions. The PID contains the logic required to support 8259A mode, APIC mode, and SAPIC mode interrupt controller operations. The PID interfaces include a PCI bus interface, an APIC bus interface, a serial IRQ interface, and an interrupt input interface.

1.2 Reference Documents

In addition to this document, the reader should be familiar with the following reference documents:

- *Intel® 460GX Chipset System Software Developer's Manual*
  (Document Number: 248704)
- *Intel® Itanium™ Processor at 800 MHz and 733 MHz Datasheet*
  (Document Number: 245481)
- *Intel® Itanium™ Processor Hardware Developer's Manual*
  (Document Number: 248701)
- *Intel® 82460GX Chipset OLGA1 Package, Manufacturing, Mechanical, and Thermal Design Guide*
- *PCI Local Bus Specification*, Rev 2.2
  (http://www.pcisig.com/)
- *Accelerated Graphics Port Interface Specification*
  (http://www.intel.com/technology/agp/agp_index.htm)
- *JTAG IEEE 1149.1 Specification*
  (http://www.ieee.com)
- *Universal Serial Bus Specification*
  (http://www.usb.org)
- *System Management Bus Specification*, Rev. 1.0
- *Low Pin Count (LPC) Interface Specification*, Rev 1.0

Note: Contact your Intel representative for the latest revision of the documents without document numbers.

1.3 Revision History

Date	Description
June 2001	First release of the 460GX chipset datasheet.

Signals 2

This chapter lists the signals and descriptions for each Intel 460GX chipset component. Signal descriptions for the PID and IFB are found in Chapter 11 and Chapter 12 respectively. See Chapter 1 for locating information on the FWH.

2.1 Signal Types

Table 2-1 through Table 2-7 contain the 460GX chipset's signal names, buffer types, and signal types for each component.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bidirectional (input/output) pin

The signal description also includes the type of buffer used for the particular signal:

AGTL+	Enhanced Assisted Gunning Transceiver Logic interface
PCI	PCI-compliant 3.3V / 5V - tolerant interface
3.3V PCI	PCI-compliant 3.3V interface
3.3V CMOS	3.3V CMOS signals
1.8V CMOS	1.8V CMOS signals (also referred to as low voltage CMOS or LVC)
AGP	AGP-compliant 1.5V / 3.3V - tolerant interface
Analog	Typically a voltage reference, power supply, ground, static input, or compensation resistor
HSTL	HSTL clock signals
LVTTL	3.3V TTL-compatible signals

In addition, the signal description may include the following information about the buffer:

SS	Source Synchronous capable signal
OD	Open drain signal
ST	Schmitt Trigger
U	Internal pull-up resistor
D	Internal pull-down resistor
OT	Tristateable output

Lastly, when describing Driver/Receiver relationship, the symbol "–" may be used to indicate the signal is either driven to or received from a system agent not directly addressed in this document (i.e. clock buffer, power plane, ground plane, resistor, etc.).

2.2 Signal Conventions

The terms *assertion* and *deassertion* are used extensively when describing signals, to avoid confusion when working with a mix of active-high and active-low signals. The term *assert*, or *assertion*, indicates that the signal is active, independent of whether the active level is represented by a high or low voltage. The term *deassert*, or *deassertion*, indicates that the signal is inactive.

The "#" symbol at the end of a signal name indicates that the active, or asserted state, occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

When discussing data values used inside the chipset, the *logical* value is used (i.e., a data value described as "1101b" would appear as "1101b" on an active-high bus, and as "0010b" on an active-low bus). When discussing the assertion of a value on the actual pin, the physical value is used (i.e., asserting an active-low signal produces a "0" value on the pin).

Some signals or groups of signals have multiple versions. These signal groups may represent distinct but similar ports or interfaces, or may represent identical copies of the signal used to reduce loading effects. The following conventions are used:

RR(A,B,C)XX	expands to: RRAXX, RRBXX, and RRCXX
RR(A,...,D)XX	expands to: RRAXX, RRBXX, RRCXX, and RRDXX

Typically, *upper case* groups (e.g., "(A,B,C)") represent functionally similar but logically distinct signals; each signal provides an independent control, and may or may not be asserted at the same time as the other signals in the grouping. In contrast, *lower case* groups (e.g., "(a,b,c)") typically represent identical duplicates of a common signal; such duplicates are provided to reduce loading.

2.3 Unused Pins

For reliable operation, always connect unused inputs to an appropriate signal level:

- Unused AGTL+ inputs should be connected to the bus termination voltage.
- Unused active low 3.3V tolerant inputs should be connected to 3.3V.
- Unused active high inputs should be connected to ground (V_{SS}).

When connecting bidirectional signals to a power plane or a ground plane, a resistor must be used. When connecting *any* signal to a power plane or a ground plane, a resistor will also allow for testing of the processor and the 460GX chipset after board assembly. It is suggested that ~10KΩ resistors be used for pull-ups and ~1KΩ resistors be used as pull-downs.

2.4 Signal Lists

Table 2-1. SAC Signal List

Signal	Direction	Driver/Receiver	Type
System Bus — SAC/Processor Interface			
A[35:3]#	I/O	Bidirectional	AGTL+
ADS#	I/O	Bidirectional	AGTL+
AP[1:0]#	I/O	Bidirectional	AGTL+
BERR#	I/O	Bidirectional	AGTL+
BINIT#	I/O	Bidirectional	AGTL+
BNR#	I/O	Bidirectional	AGTL+
BP[5:0]#	I/O	Bidirectional	AGTL+
BPRI#	O	SAC/Processor	AGTL+
BR[0]#	I/O	Bidirectional	AGTL+
BR[3:1]#	I	Processor/SAC	AGTL+
DEFER#	O	SAC/Processor	AGTL+
HIT#	I/O	Bidirectional	AGTL+
HITM#	I/O	Bidirectional	AGTL+
INIT#	O	SAC/Processor	AGTL+
LOCK#	I	Processor/SAC	AGTL+
REQ[4:0]#	I/O	Bidirectional	AGTL+
RP#	I/O	Bidirectional	AGTL+
RESET#	O	SAC/Processor	AGTL+
Private Bus — SAC/SDC Interface			
PCMD[16:0]#	O	SAC/SDC	1.8V CMOS
PCMDP#	O	SAC/SDC	1.8V CMOS
PITID[5:0]#	I/O	Bidirectional	1.8V CMOS OT
PITIDP#	I/O	Bidirectional	1.8V CMOS OT
PITIDV#	I/O	Bidirectional	1.8V CMOS OT
PVGNT#	I	SDC/SAC	1.8V CMOS
PVREQ#	O	SAC/SDC	1.8V CMOS
PVD[63:0]#	I/O	Bidirectional	1.8V CMOS OT
PVDP[3:0]#	I/O	Bidirectional	1.8V CMOS OT
PVDV#	I/O	Bidirectional	1.8V CMOS OT
RITID[5:0]#	I	SDC/SAC	1.8V CMOS
RITIDP#	I	SDC/SAC	1.8V CMOS
SDCRS[3:0]#	O	SAC/SDC	1.8V CMOS
SDCRST#	O	SAC/SDC	1.8V CMOS
TOQE#	I	SDC/SAC	1.8V CMOS
Memory Data and Control (MD&C) Bus - Address and Control Signals — SAC/MAC Interface			
CMND(A, B)[1:0]#	O	SAC/MAC	1.8V CMOS
LCMPLT(A, B)#	I	MAC/SAC	1.8V CMOS
RCMPLT(A, B)#	I	MAC/SAC	1.8V CMOS
ERR(A, B)#	I	MAC/SAC	1.8V CMOS OD

Table 2-1. SAC Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
MA(A, B)[16:0]#	O	SAC/MAC	1.8V CMOS
MEMRST[1:0]#	O	SAC/MAC	1.8V CMOS
PAR(A, B)#	O	SAC/MAC	1.8V CMOS
ROW(A, B)[2:0]#	O	SAC/MAC	1.8V CMOS
Expander Bus (Expander Interface) — SAC/PXB, SAC/WXB, SAC/GXB Interface			
X(0,1,2,3)ADS#	I/O	Bidirectional	AGTL+SS
X(0,1,2,3)BE[1:0]#	I/O	Bidirectional	AGTL+SS
X(0,1,2,3)BLK#	O	SAC/Expander	AGTL+ SS
X(0,1,2,3)CLK	O	SAC/Expander	AGTL+
X(0,1,2,3)CLKB	O	SAC/SAC	AGTL+
X(0,1,2,3)CLKFB	I	SAC/SAC	AGTL+
X(0,1,2,3)D[15:0]#	I/O	Bidirectional	AGTL+SS
X(0,1,2,3)HRTS#	O	SAC/Expander	AGTL+SS
X(0,1,2,3)HSTBN#	O	SAC/Expander	AGTL+SS
X(0,1,2,3)HSTBP#	O	SAC/Expander	AGTL+SS
X(0,1,2,3)PAR#	I/O	Bidirectional	AGTL+SS
X(0,1,2,3)RST#	O	SAC/Expander	AGTL+
X(0,1,2,3)RSTB#	O	SAC/SAC	AGTL+
X(0,1,2,3)RSTFB#	I	SAC/SAC	AGTL+
X(0,1,2,3)XRTS#	I	Expander/SAC	AGTL+SS
X(0,1,2,3)XSTBP#	I	Expander/SAC	AGTL+SS
X(0,1,2,3)XSTBN#	I	Expander/SAC	AGTL+SS
JTAG Interface			
TCK	I	JTAG/SAC	AGTL+
TDI	I	JTAG/SAC	AGTL+
TDO	O	SAC/JTAG	AGTL+
TMS	I	JTAG/SAC	AGTL+
TRST#	I	JTAG/SAC	AGTL+
System Management Bus Interface			
SMBSCL	I/O	Bidirectional	1.8V CMOS OD
SMBSDA	I/O	Bidirectional	1.8V CMOS OD
MB1SCL	I/O	Bidirectional	1.8V CMOS OD
MB1SDA	I/O	Bidirectional	1.8V CMOS OD
SAC/PID Interface			
INTREQ#	O	SAC/PID	1.8V CMOS OD
Reset and Initialization			
PWRGD	I	–/SAC	1.8V CMOS ST
EXRESET#	I	–/SAC	1.8V CMOS
CRESET#	O	SAC/–	1.8V CMOS OD
XBINIT#	I	–/SAC	AGTL+
CHLNSZ#	I	–/SAC	1.8V CMOS
SAC/PCI Interface			
XSERR#	I	–/SAC	1.8V CMOS

Table 2-1. SAC Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
Compensation Resistor Pins			
F16CRES[1:0]	I	–/SAC	Analog
PVBCRES[1:0]	I	–/SAC	Analog
SMPCRES	I	–/SAC	Analog
IMPCNTL#	I	–/SAC	Analog
SWRCNTL#	I	–/SAC	Analog
Clocks			
HCLKIN	I	–/SAC	HSTL
HCLKIN#	I	–/SAC	HSTL
Power and Ground Pins			
VCTFSB[6:0]	I	–/SAC	Analog
VCTF16[14:0]	I	–/SAC	Analog
VCCA[4:0]	I	–/SAC	Analog
VSSA	I	–/SAC	Analog
VCC	I	–/SAC	Analog
VSS	I	–/SAC	Analog
Reference Voltage Pins			
VREFFSB[3:0]	I	–/SAC	Analog
VREFF16[3:0]	I	–/SAC	Analog
VREFM[1:0]	I	–/SAC	Analog
VREFPVB[1:0]	I	–/SAC	Analog
VREFOUT[1:0]	O	SAC/–	Analog

Table 2-2. SDC Signal List

Signal	Direction	Driver/Receiver	Type
System Bus — SDC/Processor Interface			
D[63:0]#	I/O	Bidirectional	AGTL+SS
DEP[7:0]#	I/O	Bidirectional	AGTL+SS
TRDY#	O	SDC/Processor	AGTL+
DRDY#	I/O	Bidirectional	AGTL+
DBSY#	I/O	Bidirectional	AGTL+
SBSY#	I/O	Bidirectional	AGTL+
STBN[3:0]#	I/O	Bidirectional	AGTL+SS
STBP[3:0]#	I/O	Bidirectional	AGTL+SS
ID[6:0]#	O	SDC/Processor	AGTL+
IDS#	O	SDC/Processor	AGTL+
RS[2:0]#	O	SDC/Processor	AGTL+
RSP#	O	SDC/Processor	AGTL+
Private Bus — SDC/SAC Interface			
PCMD[16:0]#	I	SAC/SDC	1.8V CMOS
PCMDP#	I	SAC/SDC	1.8V CMOS
PITID[5:0]#	I/O	Bidirectional	1.8V CMOS OT

Table 2-2. SDC Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
PITIDP#	I/O	Bidirectional	1.8V CMOS OT
PITIDV#	I/O	Bidirectional	1.8V CMOS OT
PVGNT#	O	SDC/SAC	1.8V CMOS
PVREQ#	I	SAC/SDC	1.8V CMOS
PVD[63:0]#	I/O	Bidirectional	1.8V CMOS OT
PVDP[3:0]#	I/O	Bidirectional	1.8V CMOS OT
PVDV#	I/O	Bidirectional	1.8V CMOS OT
RITID[5:0]#	O	SDC/SAC	1.8V CMOS
RITIDP#	O	SDC/SAC	1.8V CMOS
SDCRS[3:0]#	I	SAC/SDC	1.8V CMOS
SDCRST#	I	SAC/SDC	1.8V CMOS
TOQE#	O	SDC/SAC	1.8V CMOS
Memory Data and Control (MD&C) Bus - Address and Control Signals — SDC/MAC Interface			
FWMDA#	I	MAC/SDC	1.8V CMOS
FWMDB#	I	MAC/SDC	1.8V CMOS
FWSLA#	I	MAC/SDC	1.8V CMOS
FWSLB#	I	MAC/SDC	1.8V CMOS
HWMDAL#	O	SDC/MAC	1.8V CMOS
HWMDAR#	O	SDC/MAC	1.8V CMOS
HWMDBL#	O	SDC/MAC	1.8V CMOS
HWMDBR#	O	SDC/MAC	1.8V CMOS
LRMDA#	I	MAC/SDC	1.8V CMOS
LRMDB#	I	MAC/SDC	1.8V CMOS
Memory Data and Control (MD&C) Bus - Data Signals — SDC/MDC Interface			
MDA[71:0]#	I/O	Bidirectional	1.8V CMOS SS
MDASP[3:0]#	I/O	Bidirectional	1.8V CMOS SS
MDASN[3:0]#	I/O	Bidirectional	1.8V CMOS SS
MDB[71:0]#	I/O	Bidirectional	1.8V CMOS SS
MDBSP[3:0]#	I/O	Bidirectional	1.8V CMOS SS
MDBSN[3:0]#	I/O	Bidirectional	1.8V CMOS SS
JTAG Interface			
TCK	I	JTAG/SDC	AGTL+
TDI	I	JTAG/SDC	AGTL+
TDO	O	SDC/JTAG	AGTL+
TMS	I	JTAG/SDC	AGTL+
TRST#	I	JTAG/SDC	AGTL+
Reset and Initialization			
PWRGD	I	–/SDC	1.8V CMOS ST
DRATE#	I	–/SDC	AGTL+
CHLNSZ#	I	–/SDC	1.8V CMOS

Table 2-2. SDC Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
Compensation Resistor Pins			
CRESF[1:0]	I	–/SDC	Analog
CRESM0	I	–/SDC	Analog
Clocks			
HCLKIN	I	–/SDC	HSTL
HCLKIN#	I	–/SDC	HSTL
Power and Ground Pins			
VCT[7:0]	I	–/SDC	Analog
VCCA	I	–/SDC	Analog
VSSA	I	–/SDC	Analog
VCC	I	–/SDC	Analog
VSS	I	–/SDC	Analog
Reference Voltage Pins			
VREF[4:0]	I	–/SDC	Analog
MVREFA1:0]	I	–/SDC	Analog
MVREFB[1:0]	I	–/SDC	Analog
PVREF[1:0]	I	–/SDC	Analog

Table 2-3. MAC Signal List

Signal	Direction	Driver/Receiver	Type
Memory Data and Control (MD&C) Bus - Address and Control Signals — MAC/SAC Interface			
CMND[1:0]#	I	SAC/MAC	1.8V CMOS
CMPLT(L:R)#	O	MAC/SAC	1.8V CMOS
ERR#	O	MAC/SAC	1.8V CMOS OD
MA[16:0]#	I	SAC/MAC	1.8V CMOS
MEMRST#	I	SAC/MAC	1.8V CMOS
PAR#	I	SAC/MAC	1.8V CMOS
ROW[2:0]#	I	SAC/MAC	1.8V CMOS
Memory Data and Control (MD&C) Bus - Address and Control Signals — MAC/SDC Interface			
FWMD#	O	MAC/SDC	1.8V CMOS
FWSL#	O	MAC/SDC	1.8V CMOS
HWMD(L,R)#	I	SDC/MAC	1.8V CMOS
LRMD#	O	MAC/SDC	1.8V CMOS
Memory Data and Control (MD&C) Bus - Address and Control Signals — MAC/MDC Interface			
CORDR[1:0]#	O	MAC/MDC	1.8V CMOS
FDQ(L,R)#	O	MAC/MDC	1.8V CMOS
FRMD#	O	MAC/MDC	1.8V CMOS
LDQ (L,R)#	O	MAC/MDC	1.8V CMOS
LEFT#	O	MAC/MDC	1.8V CMOS

Table 2-3. MAC Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
LWMD#	O	MAC/MDC	1.8V CMOS
MINIT#	0	MAC/MDC	1.8V CMOS
RESET#	O	MAC/MDC	1.8V CMOS
Memory Subsystem Bus — MAC/SDRAM Interface			
ADD(L,R)(A,B,C,D)[12:0]	O	MAC/SDRAM	3.3V CMOS
BANK(L,R)(A,B,C,D)[2:0]	O	MAC/SDRAM	3.3V CMOS
CAS(L,R)(A,B,C,D)#	O	MAC/SDRAM	3.3V CMOS
RAS(L,R)(A,B,C,D)#	O	MAC/SDRAM	3.3V CMOS
WE(L,R)(A,B,C,D)#	O	MAC/SDRAM	3.3V CMOS
CS(L,R)(A,B,C,D)[3:0]#	O	MAC/SDRAM	3.3V CMOS
JTAG Interface			
TRST#	I	JTAG/MAC	LVTTL
TMS	I	JTAG/MAC	LVTTL
TDI	I	JTAG/MAC	LVTTL
TCK	I	JTAG/MAC	LVTTL
TDO	O	MAC/JTAG	LVTTL OD
System Management Bus Interface			
SCL	I/O	Bidirectional	1.8V CMOS OD
SDA	I/O	Bidirectional	1.8V CMOS OD
IDVAL[1:0]	I	–/MAC	3.3V CMOS
Compensation Resistor PIns			
CRES[2:0]	I	–/MAC	Analog
Reset and Initialization			
PWRGD	I	–/MAC	1.8V CMOS ST
Clocks			
HCLKIN	I	–/MAC	HSTL
HCLKIN#	I	–/MAC	HSTL
Power and Ground Pins			
VCCA	I	–/MAC	Analog
VCC33	I	–/MAC	Analog
VCC18	I	–/MAC	Analog
VSS	I	–/MAC	Analog
Reference Voltage Pins			
VREF33	I	–/MAC	Analog
VREF18	I	–/MAC	Analog

Table 2-4. MDC Signal List

Signal	Direction	Driver/Receiver	Type
Memory Data and Control (MD&C) Bus - Data signals MDC/SDC Interface			
MD[17:0]#	I/O	Bidirectional	1.8V CMOS SS
MDSP#	I/O	Bidirectional	1.8V CMOS SS
MDSN#	I/O	Bidirectional	1.8V CMOS SS
Memory Data and Control (MD&C) Bus - Address and Control Signals — MDC/MAC Interface			
CORDR[1:0]#	I	MAC/MDC	1.8V CMOS
FDQ(L,R)#	I	MAC/MDC	1.8V CMOS
FRMD#	I	MAC/MDC	1.8V CMOS
LDQ(L,R)#	I	MAC/MDC	1.8V CMOS
LEFT#	I	MAC/MDC	1.8V CMOS
LWMD#	I	MAC/MDC	1.8V CMOS
MINIT#	I	MAC/MDC	1.8V CMOS
RESET#	I	MAC/MDC	1.8V CMOS
Memory Subsystem Bus — MDC/SDRAM Interface			
DQ(L,R)[71:0]	I/O	Bidirectional	3.3V CMOS
MEMCLKB(L,R)[15:0]	O	MDC/SDRAM	3.3V CMOS
MEMCLK(L,R)	I	MDC/MDC	HSTL
MEMCLKIN(L,R)	O	MDC/MDC	3.3V CMOS
JTAG Interface			
TRST#	I	JTAG/MDC	LVTTL
TMS	I	JTAG/MDC	LVTTL
TDI	I	JTAG/MDC	LVTTL
TCK	I	JTAG/MDC	LVTTL
TDO	O	MDC/JTAG	LVTTL OD
System Management Bus Interface			
SCL18	I/O	Bidirectional	1.8V CMOS OD
SDA18	I/O	Bidirectional	1.8V CMOS OD
SCL33	I/O	Bidirectional	3.3V CMOS OD
SDA33	I/O	Bidirectional	3.3V CMOS OD
IDVAL[2:0]	I	–/MDC	3.3V CMOS
Compensation Resistor Pins			
CRES[2:0]	I	–/MDC	Analog
Reset and Initialization			
PWRGD	I	–/MDC	1.8V CMOS ST
Clocks			
HCLKIN	I	–/MDC	HSTL
HCLKIN#	I	–/MDC	HSTL
Power and Ground Pins			
VCCA[2:0]	I	–/MDC	Analog
VCC33	I	–/MDC	Analog

Table 2-4. MDC Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
VCC18	I	–/MDC	Analog
VSS	I	–/MDC	Analog
Reference Voltage Pins			
VREF33[4:0]	I	–/MDC	Analog
VREF18[1:0]	I	–/MDC	Analog

Table 2-5. PXB Signal List

Signal	Direction	Driver/Receiver	Type
Expander Bus — PXB/SAC Interface			
XADS#	I/O	Bidirectional	AGTL+SS
XBE[1:0]#	I/O	Bidirectional	AGTL+SS
XBLK#	I	SAC/PXB	AGTL+ SS
XCLK	I	SAC/PXB	AGTL+
XD[15:0]#	I/O	Bidirectional	AGTL+SS
XHRTS#	I	SAC/PXB	AGTL+SS
XHSTBN#	I	SAC/PXB	AGTL+SS
XHSTBP#	I	SAC/PXB	AGTL+SS
XIB#	O	PXB/-	AGTL+
XPAR#	I/O	Bidirectional	AGTL+SS
XRST#	I	SAC/PXB	AGTL+
XXRTS#	O	PXB/SAC	AGTL+SS
XXSTBN#	O	PXB/SAC	AGTL+SS
XXSTBP#	O	PXB/SAC	AGTL+SS
PCI Interface			
ACK64#	I/O	Bidirectional	PCI
MODE64#	I	PCI/PXB	PCI
PHOLD#	I	PCI/PXB	PCI
PHLDA#	O	PXB/PCI	PCI
REQ64#	I/O	Bidirectional	PCI
WSC#	O	PXB/PCI	PCI
INTRQ(A,B)#	O	PXB/PCI	PCI OD
P(A,B)AD[31:0]	I/O	Bidirectional	PCI
P(A,B)C/BE#[3:0]	I/O	Bidirectional	PCI
P(A,B)DEVSEL#	I/O	Bidirectional	PCI
P(A,B)FRAME#	I/O	Bidirectional	PCI
P(A,B)GNT[5:0]#	O	PXB/PCI	PCI
P(A,B)IRDY#	I/O	Bidirectional	PCI
P(A,B)LOCK#	I/O	Bidirectional	PCI
P(A,B)PAR	I/O	Bidirectional	PCI
P(A,B)PERR#	I/O	Bidirectional	PCI
P(A,B)REQ[5:0]#	I	PCI/PXB	PCI
P(A,B)RST#	O	PXB/PCI	PCI
P(A,B)SERR#	O	PXB/PCI	PCI OD

Table 2-5. PXB Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
P(A,B)STOP#	I/O	Bidirectional	PCI
P(A,B)TRDY#	I/O	Bidirectional	PCI
P(A,B)XARB#	I	PCI/PXB	PCI
P(A,B)MON[1:0]#	I/O	Bidirectional	3.3V CMOS OD 14mA
P(A,B)CLK	O	PXB/–	3.3V CMOS 12mA
P(A,B)CLKFB	I	–/PXB	3.3V CMOS
JTAG Interface			
TCK	I	JTAG/PXB	LVTTL
TDI	I	JTAG/PXB	LVTTL
TDO	O	PXB/JTAG	LVTTL OD
TMS	I	JTAG/PXB	LVTTL
TRST#	I	JTAG/PXB	LVTTL
PXB/IFB Interface			
PIIXOK#	I	IFB/PXB	3.3V CMOS
Reset and Initialization			
PWRGD	I	–/PXB	3.3V CMOS
XBINIT#	O	PXB/SAC	AGTL+
LONGXB[1:0]	I	–/PXB	Analog
XCLKGTL	I	–/PXB	Analog
GEAR4#	I	–/PXB	LVTTL
Compensation Resistor Pins			
CRES[1:0]	I	–/PXB	Analog
Power and Ground Pins			
VCT	I	–/PXB	Analog
VCCA[2:0]	I	–/PXB	Analog
VCC	I	–/PXB	Analog
VCC5	I	–/PXB	Analog
VSS	I	–/PXB	Analog
Reference Voltage Pins			
VREF[1:0]	I	–/PXB	Analog

Table 2-6. GXB Signal List

Signal	Direction	Driver/Receiver	Type
Expander Bus — GXB/SAC Interface			
X0BLK#	I	SAC/GXB	AGTL+ SS
X0CLK	I	SAC/GXB	AGTL+
X0RST#	I	SAC/GXB	AGTL+
X(0,1)ADS#	I/O	Bidirectional	AGTL+SS
X(0,1)BE[1:0]#	I/O	Bidirectional	AGTL+SS
X(0,1)D[15:0]#	I/O	Bidirectional	AGTL+SS
X(0,1)HSTBP#	I	SAC/GXB	AGTL+SS
X(0,1)HSTBN#	I	SAC/GXB	AGTL+SS

Table 2-6. GXB Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
X(0,1)HRTS#	I	SAC/GXB	AGTL+SS
X(0,1)PAR#	I/O	Bidirectional	AGTL+SS
X(0,1)XSTBP#	O	GXB/SAC	AGTL+SS
X(0,1)XSTBN#	O	GXB/SAC	AGTL+SS
X(0,1)XRTS#	O	GXB/SAC	AGTL+SS
AGP Interface			
TYPEDET#	I	–/GXB	3.3V CMOS U
AGPCLK[1:0]	O	GXB/–	3.3V CMOS
AGPCLKIN	I	–/GXB	3.3V CMOS
AGPRST#	O	GXB/–	3.3V CMOS
REQ#	I	–/GXB	AGP U
GNT#	O	GXB/–	AGP
ST[2:0]	O	GXB/–	AGP
WBF#	I	–/GXB	AGP U
RBF#	I	–/GXB	AGP U
PIPE#	I	–/GXB	AGP U
FRAME#	I/O	Bidirectional	AGP U
SBA[7:0]	I	–/GXB	AGP SS U
SBSTB	I	–/GXB	AGP D
SBSTB#	I	–/GXB	AGP U
AD[31:0]	I/O	Bidirectional	AGP SS
ADSTB[1:0]	I/O	Bidirectional	AGP D
ADSTB[1:0]#	I/O	Bidirectional	AGP U
CBE#[3:0]	I/O	Bidirectional	AGP SS
DEVSEL#	I/O	Bidirectional	AGP U
TRDY#	I/O	Bidirectional	AGP U
IRDY#	I/O	Bidirectional	AGP U
STOP#	I/O	Bidirectional	AGP U
PERR#	I/O	Bidirectional	AGP U
SERR#	I/O	Bidirectional	AGP U
PAR	I/O	Bidirectional	AGP
GART SRAM Interface			
SADDR[17:0]	O	GXB/–	3.3V CMOS U
SGW#	O	GXB/–	3.3V CMOS U
SOE#	O	GXB/–	3.3V CMOS U
SSE3#	O	GXB/–	3.3V CMOS U
SDATA[31:0]	I/O	Bidirectional	3.3V CMOS U
SCLK[2:0]	O	GXB/–	3.3V CMOS U
SCLKIN	I	–/GXB	3.3V CMOS U
GXB/PID Interface			
XINTR#	O	GXB/PID	3.3V CMOS
Reset and Initialization			
PWRGD	I	–/GXB	3.3V CMOS
XBINIT#	O	GXB/SAC	AGTL+

Table 2-6. GXB Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
JTAG Interface			
TCK	I	JTAG/GXB	LVTTL U
TDI	I	JTAG/GXB	LVTTL U
TDO	O	GXB/JTAG	LVTTL OD
TMS	I	JTAG/GXB	LVTTL U
TRST#	I	JTAG/GXB	LVTTL U
Compensation Resistor Pins			
CRES[5:0]	I	–/GXB	Analog
Power and Ground Pins			
VCT	I	–/GXB	Analog
VCCA[3:0]	I	–/GXB	Analog
VCCQ	I	–/GXB	Analog
VCC	I	–/GXB	Analog
VSS	I	–/GXB	Analog
Reference Voltage Pins			
VREFAGP[2:0]	I	–/GXB	Analog
VREF[2:0]	I	–/GXB	Analog
VREFOUT[1:0]	O	GXB/–	Analog

Table 2-7. WXB Signal List

Signal	Direction	Driver/Receiver	Type
Expander Bus — PXB/SAC Interface			
XADS#	I/O	Bidirectional	AGTL+ SS
XBE[1:0]#	I/O	Bidirectional	AGTL+ SS
XBLK#	I	SAC/WXB	AGTL+ SS
XCLK	I	SAC/WXB	AGTL+
XD[15:0]#	I/O	Bidirectional	AGTL+ SS
XHRTS#	I	SAC/WXB	AGTL+ SS
XHSTBN#	I	SAC/WXB	AGTL+ SS
XHSTBP#	I	SAC/WXB	AGTL+ SS
XIB#	O	WXB/-	AGTL+
XPAR#	I/O	Bidirectional	AGTL+ SS
XRST#	I	SAC/WXB	AGTL+
XXRTS#	O	WXB/SAC	AGTL+ SS
XXSTBN#	O	WXB/SAC	AGTL+ SS
XXSTBP#	O	WXB/SAC	AGTL+ SS
PCI Interface			
P(A,B)ACK64#	I/O	Bidirectional	3.3V PCI
P(A,B)AD[63:0]	I/O	Bidirectional	3.3V PCI
P(A,B)C/BE[7:0]#	I/O	Bidirectional	3.3V PCI
P(A,B)CLK[2:0]	O	WXB/PCI	LVTTL
P(A,B)CLKFB	I	WXB/WXB	1.8V CMOS

Table 2-7. WXB Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
P(A,B)CLKREF	O	WXB/WXB	LVTTL
P(A,B)DEVSEL#	I/O	Bidirectional	3.3V PCI
P(A,B)FRAME#	I/O	Bidirectional	3.3V PCI
P(A,B)GNT[5:0]#	O	WXB/PCI	3.3V PCI
P(A,B)IDSEL[18:16]#	O	WXB/PCI	3.3V PCI
P(A,B)IRDY#	I/O	Bidirectional	3.3V PCI
P(A,B)LOCK#	I/O	Bidirectional	3.3V PCI
P(A,B)M66EN	I/O	Bidirectional	3.3V PCI
P(A,B)MON[1:0]#	O	WXB/PCI	LVTTL OD
P(A,B)PAR	I/O	Bidirectional	3.3V PCI
P(A,B)PAR64	I/O	Bidirectional	3.3V PCI
P(A,B)PERR#	I/O	Bidirectional	3.3V PCI
P(A,B)REQ[5:0]#	I	PCI/WXB	3.3V PCI
P(A,B)REQ64#	I/O	Bidirectional	3.3V PCI
P(A,B)RST#	O	WXB/PCI	3.3V PCI
P(A,B)SERR#	O	WXB/PCI	3.3V PCI OD
P(A,B)STOP#	I/O	Bidirectional	3.3V PCI
P(A,B)TRDY#	I/O	Bidirectional	3.3V PCI
JTAG Interface			
TCK	I	JTAG/WXB	LVTTL
TDI	I	JTAG/WXB	LVTTL
TDO	O	WXB/JTAG	LVTTL OD
TMS	I	JTAG/WXB	LVTTL
TRST#	I	JTAG/WXB	LVTTL
Reset and Initialization			
PWRGD	I	–/WXB	1.8V CMOS ST
LONGXB[1:0]	I	–/WXB	1.8V CMOS
XBINIT#	O	WXB/SAC	AGTL+
Compensation Resistor Pins			
CRES[1:0]	I	–/WXB	Analog
Power and Ground Pins			
VCT	I	–/WXB	Analog
VCCA[2:0]	I	–/WXB	Analog
VCC	I	–/WXB	Analog
VCCP	I	–/WXB	Analog
VSSA	I	–/WXB	Analog
VSS	I	–/WXB	Analog
Reference Voltage Pins			
VREF	I	–/WXB	Analog
Integrated Hot-Plug Controller Interface			
H(A,B)SIC	I/O	Bidirectional	LVTTL
H(A,B)SID	I	–/WXB	LVTTL
H(A,B)SIL#	I/O	Bidirectional	LVTTL

Table 2-7. WXB Signal List (Continued)

Signal	Direction	Driver/Receiver	Type
H(A,B)SOC	O	WXB/–	LVTTL
H(A,B)SOD	O	WXB/–	LVTTL
H(A,B)SOL	I/O	Bidirectional	LVTTL
H(A,B)SOR#	O	WXB/–	LVTTL
H(A,B)SORR#	O	WXB/–	LVTTL
H(A,B)INTRQ#	O	WXB/PID	LVTTL OD
Interrupt Signal Interface			
SERR_OUT#	O	WXB/PID	LVTTL OD
P(A,B)INTRQ#	O	WXB/PID	LVTTL OD

2.5 Signal Descriptions

This section gives detailed signal descriptions of the Intel 460GX chipset signals.

Reference the "Intel® 460GX Chipset System Software Developer's Manual (Document Number: 248704)" for further pin descriptions than those shown in this chapter.

2.5.1 System Bus

For the processor system bus signals, please refer to the "Intel® Itanium™ Processor Hardware Developer's Manual (Document Number: 248701)".

2.5.2 Expander Interface

The Expander bus (16 bits) provides the interface between the host bridge (SAC) and the expansion bridges (PXB, GXB and WXB).

XADS# — **Address/Data Strobe**
Bidirectional signal asserted by the sending agent during every clock of a packet transmission except the last clock. In a single clock transmission it is asserted for one clock.

XBE[1:0]# — **Byte Enables**
Bidirectional signal asserted in phase with data on the Expander bus to indicate valid bytes during the data phases of a packet transmission. Reserved function during header phases.

XBLK# — **Reserved (PXB, GXB)**
This is a reserved signal that must be appropriately connected between Expander agents.

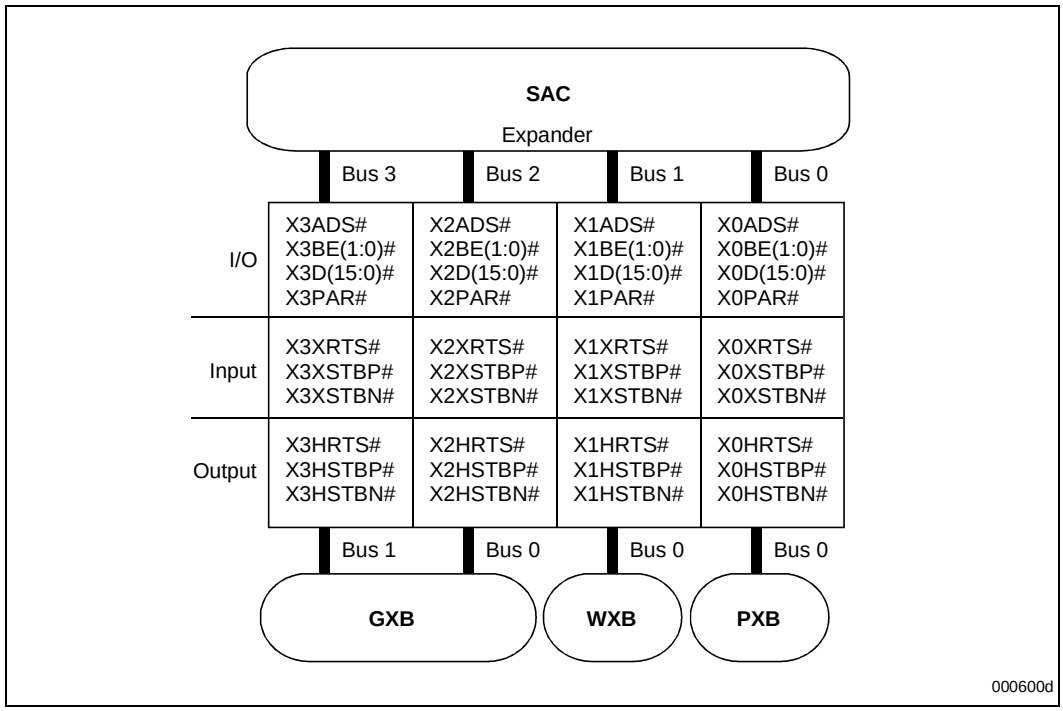
Sideband Write (WXB)
This pin is used for sideband write completion on the WXB only.

XCLK — **Clock**
XCLK is the primary clock source provided to the PXB/GXB/WXB. XCLK is a buffered and sychronized version of host clock, provided by the SAC and routed across the connector/cable alongside the other Expander signals.

XCLKB, XCLKFB	**Clock Reference** XCLKB and XCLKFB are used to align the bus clock. XCLKB is a copy of XCLK that is looped back to the XCLKFB input on the SAC. The length of the XCLKB trace should match the length of the XCLK and XRST# traces.
XD[15:0]#	**Data** This bidirectional datapath is used to transfer addresses and data between the SAC and PXB/GXB/WXB.
XHRTS#	**Host Request to Send** Request to use the bidirectional Expander bus sent from SAC to PXB/GXB/WXB. Synchronous to HCLKIN.
XHSTBP#, XHSTBN#	**Host Strobes** This pair of opposite-phase strobes is sent in phase with data transfers from the SAC to the PXB/GXB/WXB. They are used by the PXB/GXB/WXB to latch and synchronize the incoming data.
XIB#	**Inbound Transfer (PXB and WXB only)** This active-low signal is asserted by the PCI expansion bridge when it is driving data over the Expander bus. This signal serves as a logic analyzer clock qualifier for XHSTBP# and XHSTBN# as follows: when XIB is sampled active by the falling edge of XHSTBP#, the next two transfers will be driven by the PCI expansion bridge. If sampled inactive by the falling edge of XHSTBP#, and XADS# is active, the next two transfers are outbound data.
XPAR#	**Bus Parity** Bidirectional signal indicates even parity across XD[15:0] and XBE[1:0].
XRST#	**Expander Reset** This signal issues a reset to the PXB/GXB/WXB, including the dependent PCI buses.
XRSTB#, XRSTFB#	**Reset Reference** XRSTB# is a copy of XRST# that is looped back to the XRSTFB# input on the SAC. The length of the XRSTB# trace should match the length of the XRST# and XCLK traces.
XXRTS#	**Expander Request to Send** Request to use the bidirectional Expander bus sent from PXB/GXB/WXB to SAC. Synchronous to HCLKIN.
XXSTBP#, XXSTBN#	**Expander Strobes** This pair of opposite-phase strobes is sent in phase with data transfers from the PXB/GXB/WXB to the SAC. They are used by the SAC to latch and synchronize the incoming data.

Figure 2-1 shows an example of how source synchronous signals are grouped on each respective Expander bus. The system designer is ordinarily free to use any Expander bus for any Expander compliant component; however, if a GXB component is used, it must connect to Expander buses 3 and 2.

Figure 2-1. Example of Source Synchronous Groupings for the Expander Buses



2.5.3 Memory Data and Control (MD&C) Interface

The Memory Data and Control (MD&C) interface includes all of the connections between the SAC and MAC components, the SDC and MAC components, the SDC and MDC components, and the MAC and MDC components.

2.5.3.1 SAC/MAC Interface

CMND[1:0]# — **Access Command**
The CMND# signals encode the command of the next transaction requested by the SAC to the memory subsystem.

CMPLT(L:R)# — **Memory Command Completed**
The CMPLT(L,R)# signals identifies to the SAC that the memory transaction at the top of the queue has completed. The (L,R) indicates the CMPLT# signals is for the transaction completing in either the Left or Right stack. In a dual MAC system, one MAC is connected to the SAC and the second MAC pins are left unconnected.

An external 10KΩ resistor to 1.8V should be used near the SAC component for this signal.

ERR# — **MAC Error Detect**
The ERR# signal alerts the SAC that the MAC has seen some type of fatal error. In a dual MAC system, the ERR# is wired-or between the two MACs and then connected to the SAC. ERR# asserts for one clock cycle.

An external 2.2KΩ resistor to 1.8V should be used near the SAC component for this signal.

MA[16:0]# — **Command Address**
MA# is the target address of the row for the command of the next transaction requested by the SAC to the memory subsystem.

MEMRST# — **Memory Reset**
The MEMRST# signal is asserted by the SAC to alert the MAC of a software-initiated system reset. This reset signals the MAC to reset itself and the MDC. MEMRST# is also used to re-synchronize the MAC's after individually programming them during the chipset initialization sequence.

PAR# — **Command Bus Parity Bit**
PAR# is the (Odd/Even) parity bit for the CMND[1:0]#, ROW[2:0]# and MA[12:0]# command bus coming from the SAC to the MAC.

ROW[2:0]# — **Command Row Select**
ROW# encodes the target row for the command of the next transaction requested by the SAC to the memory subsystem

2.5.3.2 SDC/MAC Interface

FWMD# — **Forward Write Memory Data**
The FWMD# signals is used by the MAC to direct the SDC to drive the next memory write data to the MDC. In a dual MAC system, one MAC is connected to the SDC and the second MAC pins are left unconnected.

FWSL# — **Write Data Stack Left/Not Right**
The FWSL# signals is used in conjunction with the FWMD# signal to alert the SDC as to which stack on the MDC to send data to as requested by the MAC. In a dual MAC system, one MAC is connected to the SDC and the second MAC pins are left unconnected.

HWMD(L,R)# — **Have Write Memory Data**
The HWMD# signals is used by the SDC to alert the MAC that memory write data is available for transfer from the SDC to the MDC. The (L,R) indicates the HWMD# signals is either for the left or right stack.

LRMD# — **Load Read Memory Data**
The LRMD# signals is used by the MAC to direct the SDC to receive memory data from the MDC. In a dual MAC system, one MAC is connected to the SDC and the second MAC pins are left unconnected.

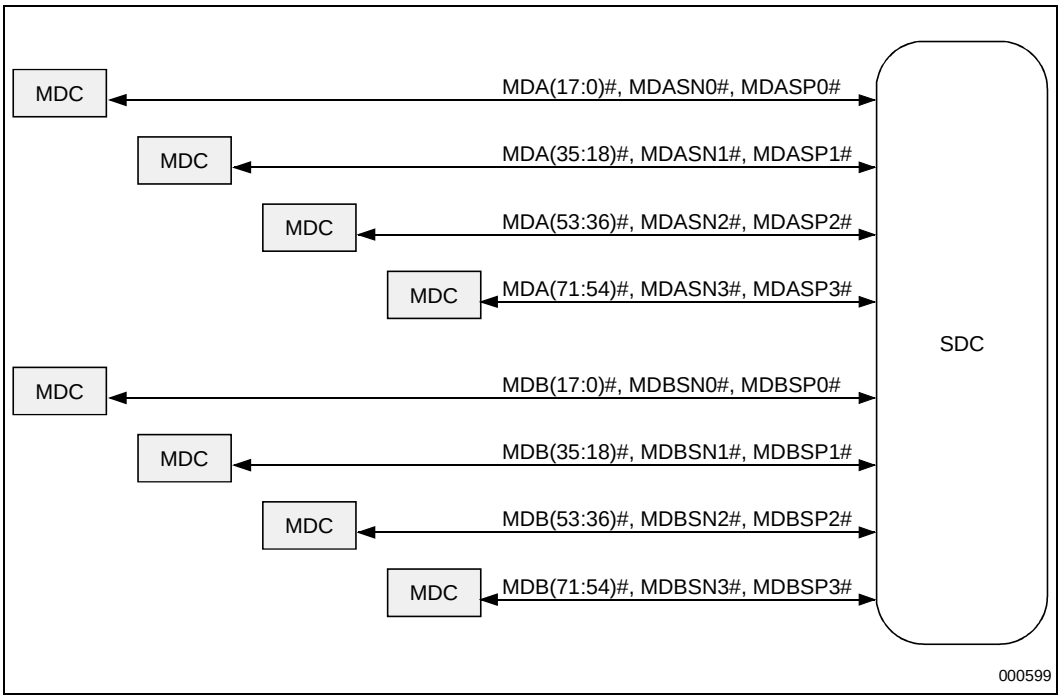
2.5.3.3 SDC/MDC Interface

MD[17:0]# — **Memory Data Bus**
The MD lines are the source synchronous data signals that move data between the MDC and the SDC.

MDSP#, MDSN# — **Memory Data Bus Strobes**
The MDSp# and MDSn# are opposite-phase strobes that are transmitted or received with the data presented on the MD ports.

Signals that are source synchronous within the same group must be routed together to achieve minimum length mismatch. Figure 2-2 shows an example of how source synchronous signals could be grouped for each respective MDC component.

Figure 2-2. Example of Source Synchronous Groupings for the MD&C Bus



2.5.3.4 MAC/MDC Interface

CORDR[1:0]# — **Critical Chuck Ordering**
The CORDR# signals are used by the MAC to direct the MDC of the correct critical chuck ordering of data movement between the SDC and the MDC. In a single MAC system, signals are connected to four MDCs. In a dual MAC system, signals are connected to two MDCs for each MAC.

FDQ(L,R)# — **Forward Write Data to SDRAM**
The FDQ(L,R)# signals are used by the MAC to direct the MDC to drive data to the SDRAM on the DQ ports. The (L,R) indicates the FDQ# signals are either for the left or right stack. In a single MAC system, these signals are connected to four MDCs. In a dual MAC system, these signals are connected to two MDCs for each MAC.

FRMD# — **Forward Read Memory Data**
The FRMD# signal is used by the MAC to direct the MDC to drive data to the SDC on the MD ports. In a single MAC system, this signals is connected to four MDCs. In a dual MAC system, this signal is connected to two MDCs for each MAC.

LDQ(L,R)# — **Load Read Data from SDRAM**
The LDQ(L,R)# signals is used by the MAC to direct the MDC to receive data from the SDRAM on the DQ ports. The (L,R) indicates the LDQ# signals is either for the left or right stack.In a single MAC system, this signals is connected to four MDCs. In a dual MAC system, this signal is connected to two MDCs for each MAC.

LEFT# — **Left Stack Select**
The LEFT# signals is used by the MAC to alert the MDC that the data moved between the SDC and MDC is either for the left or right stack. In a single MAC system, this signals is connected to four MDCs. In a dual MAC system, this signal is connected to two MDCs for each MAC.

LWMD# — **Load Write Memory Data from the SDC**
The LWMD# signal is used by the MAC to direct the MDC to receive data from the SDC on the MD ports. In a single MAC system, this signals is connected to four MDCs. In a dual MAC system, this signal is connected to two MDCs for each MAC.

MINIT# — **Memory Initialization**
This signal is no longer used by the MAC to alert the MDC that a memory initialization sequence is starting. This function now takes place via special configuration cycles between the SAC and the MDC. This signal should be connected between the MAC and MDC to ensure that the I/O is in a known state.

RESET# — **MDC Reset**
The RESET# signal is used by the MAC to send the MDC into a reset state. In a single MAC system, this signals is connected to four MDCs. In a dual MAC system, this signal is connected to two MDCs for each MAC.

2.5.4 Memory Subsystem Bus

The memory subsystem bus is the interface between the MAC, MDC, and SDRAM.

2.5.4.1 MAC/SDRAM Interface

ADD(L,R)(A,B,C,D)[12:0] — **Address Signals**
ADD defines to which address location in the DIMM the current command is directed. The ADD[12:0] outputs ports tie to the ADD[12:0] input ports on the DIMMS.The (L,R) indicates the ADD signals that go to the Left or Right stack. The (A,B,C,D) indicates the ADD signals that go either row A, B, C, or D. Each signal is capable of driving two SDRAM DIMMS per row of memory.

BANK(L,R)(A,B,C,D)[2:0] — **BANK Address**
BANK defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied within the selected DIMM. The BANK[2:0] output ports tie to the BANK[2:0] input ports on the DIMMs. The (L,R) indicates the BANK signals that go to the Left or Right stack. The (A,B,C,D) indicates the BANK signals that go either row A, B, C, or D. Each signal is capable of driving two SDRAM DIMMS per row of memory.

CAS(L,R)(A,B,C,D)# — **Column Address Strobes**
These signals are used to indicate that the column address has been broadcasted to the SDRAMs. The (L,R) indicates the CAS# signals that go to the Left or Right stack. The (A,B,C,D) indicates the CAS# signals that go either row A, B, C, or D. These eight signals are all independent signals. Each signal is capable of driving two SDRAM DIMMS.

RAS(L,R)(A,B,C,D)# **Row Address Strobes**
These signals are used to indicate that the row address has been broadcasted to the SDRAMs. The (L,R) indicates the RAS# signals that go to the Left or Right stack. The (A,B,C,D) indicates the RAS# signals that go either row A, B, C, or D. These eight signals are all independent signals. Each signal is capable of driving two SDRAM DIMMS.

WE(L,R)(A,B,C,D)# **Write Enable Signal**
WE# is asserted during writes to the SDRAMs. The (L,R) indicates the WE# signals that go to the Left or Right stack. The (A,B,C,D) indicates the WE# signals that go either row A, B, C, or D. These eight signals are all independent signals. Each signal is capable of driving two SDRAM DIMMS.

CS(L,R)(A,B,C,D)[3:0]# **Chip Select**
CS# enables and disables the command decoder within the SDRAM. The (L,R) indicates the CS# signals that go to the Left or Right stack. The (A,B,C,D) indicates the CS# signals that go either row A, B, C, or D. The [3:0] indicates a common logical signal for each row of SDRAM. Four copies of the CS are provided to improve the signal quality to each DIMM. Each signal is capable of driving two SDRAM DIMMS.

2.5.4.2 MDC/SDRAM Interface

DQ(L,R)[71:0] **SDRAM Data Bus**
The DQ lines are the data lines that run between the MDC and the four possible SDRAM DIMMS data inputs. The (L,R) indicates the DQ signals is either for the left or right stack.

MEMCLKB(L,R)[15:0] **Buffered Memory Clocks**
MEMCLKB(L,R)[15:0] are the clock source drivers for the SDRAM memory clock. Each MEMCLKB output driver is properly buffered to drive a single clock input on each DIMM. The (L,R) indicates the MEMCLKB signals is either for the left or right stack.

MEMCLKIN(L,R) **Memory Clocks Reference Output**
MEMCLKIN and MEMCLK are used to properly align the MEMCLKB with the HCLKIN input. MEMCLKIN is looped back into the MDC via the MEMCLK input. Adjustment of the trace length between the MEMCLKIN and the MEMCLK pins is used to align the half frequency MEMCLKB to the HCLKIN input. The (L,R) indicates the MEMCLKIN signals is either for the left or right stack.

MEMCLK(L,R) **Memory Clocks Reference Input**
Refer to MEMCLKIN description.

2.5.5 PCI Interface

For PCI interface signals, please refer to the “PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)”

2.5.6 AGP Interface

AGPCLK[1:0] — **AGP bus clock**
One AGPCLK pin is for the AGP bus and the other is for feedback for the internal PLL on the AGPCLKIN input.

AGPCLKIN — **AGP bus clock feedback**
This signal is connected to AGPCLK[1] at the system level, and is used to provide feedback timing information to allow an internal PLL to compensate for the I/O buffer insertion delay.

For the other AGP interface signals, please refer to the "Accelerated Graphics Port Interface Specification (http://www.intel.com/technology/agp/agp_index.htm)"

2.5.7 GART SRAM Interface

The GART SRAM interface is between the GXB and the GART SRAM.

SADDR[17:0] — **Address bus to SRAM**

SGW# — **Write enable for SRAM**

SOE# — **Output enable for SRAM**

SSE3# — **Chip enable for SRAM**

SDATA[31:0] — **Data bus to SRAM**

SCLK[2:0] — **SRAM clock**
One SCLK pin is for feedback for the internal PLL on the SCLKIN input, the other two are for point to point connections to the SRAMs.

SCLKIN — **Feedback to lock PLL for SCLK**

2.5.8 WXB Integrated Hot-Plug Controller Interface

The WXB integrates a Hot-Plug controller for each PCI bus.

H(A,B)SIC — **Hot-Plug Serial Input Clock**
Pulses low to shift external serial input shift register data one bit position. (The shift registers should be similar to standard "74x165" series).

H(A,B)SIL# — **Hot-Plug Serial Input Load**
Normally high. Pulses low to synchronously parallel load external serial input shift registers on the next rising edge of H(A,B)SIC. Also used as an (strapped) input during reset.

H(A,B)SID — **Hot-Plug Serial Input Data**
Serial input data.

H(A,B)SOR# — **Hot-Plug Serial Output Non-Reset Latch Clear**
Normally high. Asynchronously clears the power-enable, clock-enable, slot bus-enable, and LED latches.

H(A,B)SORR# — **Hot-Plug Serial Output Reset Latch Clear**
Normally high. Asynchronously clears the PCI slot reset latches.

H(A,B)SOC	**Hot-Plug Serial Output Clock** Normally high. Pulses low to shift external serial output shift register data one bit position. (The shift registers should be similar to standard “74x164” series). Also used as an (strapped) input during reset.
H(A,B)SOL	**Hot-Plug Serial Output Load** Normally high. Pulses low to shift external serial output shift register data one bit position. (The shift registers should be similar to standard “74x164” series). Also used as an (strapped) input during reset.
H(A,B)SOD	**Hot-Plug Serial Output Data** Serial output data.

2.5.9 TAP Port Boundary Scan Interface

For more information on TAP Port interface signals, please refer to the “Intel® Itanium™ Processor Hardware Developer’s Manual (Document Number: 248701)”

2.5.10 System Management Bus (SMBus) Interface

SCL	**Serial Clock Line** The SCL signals are the serial clock line for reference and control of the SMBus.
SDA	**Serial Data/Address Line** The SDA signals are the serial data and address signals of the SMBus.
IDVAL[1:0]	**Identification Select (MAC Components)** These IDVAL inputs are used to determine the SMBus address for the MAC components. The value of the IDVAL inputs are platform specific, depending on the number of MAC components in the system.
IDVAL[2:0]	**Identification Select (MDC Components)** These IDVAL inputs are used to determine the SMBus address for the MDC components. The value of the IDVAL inputs are platform specific, depending on the number of MDC components in the system.

2.5.11 PID Interface Signals

2.5.11.1 SAC/PID Interface

INTREQ#	**External Interrupt Request** INTREQ# is routed from the SAC to the PID to cause an interrupt. INTREQ# must be translated from the 1.8V to 3.3V power domain for the PID. An external 180Ω resistor to 1.8V should be used near the SAC component for this signal.

2.5.11.2 GXB/PID Interface

XINTR#	**GXB Error** This signal is asserted as the result of a non-fatal error detection in the

GXB or on specific status events. This pin should be connected to the normal interrupt delivery mechanism of the system.

2.5.12 SAC/PCI Interface Signals

XSERR# — **PCI Error Signal**
When asserted, XSERR# will cause BERR# to be asserted on the system bus. System logic should capture the SERR# signals synchronously from each PCI bus with that PCI bus's clock following standard PCI protocol. The logic should then logically OR all the PCI SERR# signals together and drive one XSERR# input into the SAC. XSERR# must be translated from the 3.3V power domain to a 1.8V input on the SAC.

2.5.13 PXB/IFB Interface Signals

PIIXOK# — **IFB Reset Complete**
When the IFB asserts PIIXOK#, it is indicating to the PXB that it has completed reset. Therefore, while PIIXOK# is deasserted, the PXB will prevent PCI compatibility bus requests directed to the IFB.

2.5.14 WXB/PID Interface Signals

SERR_OUT# — **SERR Output**
This pin forwards an SERR event (on either PCI bus or from an internal event) to an external PID. SERR_OUT# is a pulsed signal that is pulsed for eight Expander clock cycles whenever an SERR event is detected.

H(A,B)INTRQ# — **Hot-Plug Interrupt Request**
PCI-like interrupt signal indicating an Hot-Plug event.

P(A,B)INTRQ# — **Interrupt Request**
PCI interrupt signal generated by the WXB. May also be referred to as INTRQ in other sections of this specification.

2.5.15 Reset and Initialization Signals

CHLNSZ# — **Cache Line Size**
CHLNSZ# is an input on SAC and SDC and indicates a 32 or 64 byte cache line size. Active low indicates 32 bytes, inactive high indicates 64 bytes. This signal should be pulled up for an Itanium processor system with a 64 byte cache line size.

CRESET# — **CMOS Reset**
The CRESET# signal is a synchronous 1.8V CMOS level output of the SAC which tracks RESET# but is held asserted two clocks longer than RESET#. It is provided for use by external system logic.

An external 180Ω resistor to 1.8V should be used near the SAC component for this signal.

DRATE# — **System Bus Data Rate**
DRATE# is an input on SDC. A logic zero indicates common clock data transfers on the system bus, a logic one indicates source synchronous

data transfers. For optimum performance on the Itanium processor system bus, this signal should be pulled up to enable source synchronous data transfers.

EXRESET#

External Reset
An inactive to active transition of this signal causes the SAC to issue a system reset. This signal is provided to allow an external source, such as a front-panel button, to reset the system. It is necessary for the system to adequately debounce this signal to prevent invalid transitions during assertion.

To issue a system reset, this signal must be held active for a minimum of 8 system bus clock cycles before going inactive. Additionally, the signal must remain inactive for a minimum of 8 system bus clock cycles before going active again.

EXRESET# must be translated from the 3.3V power domain to the 1.8V power domain for the SAC.

GEAR4#

Expander Clock to PCI Clock Ratio
This strapping pin (static input) on the PXB is used to establish the Expander clock to PCI clock ratio. When asserted low, the PXB operates in a 4:1 Expander clock to PCI clock ratio.

LONGXB[1:0]

Expander Latency Mode
These are strapping pins (static inputs) on the PXB and WXB used to establish the desired Expander latency mode. The signals are decoded for each of these parts as indicated in Table 2-8.

Table 2-8. LONGXB Encoding

LONGXB[1]	LONGXB[0]	Expander Latency Mode (Clocks)
1	0	2
0	0	3

PWRGD

Power Good
PRWGD is a clean indication that the clocks and power supplies are within their specifications. *Clean* implies that PWRGD will remain low, (capable of sinking leakage current) without glitches, from the time that the power supplies are turned on until the clocks and power are valid. PWRGD will have a single low to high transition with a 100ns rise time.

The number of power good signals in the system is power domain dependent. All power supply and voltage regulation power good signals must be ANDed together before forming the Power Good signal (PWRGD) to the processor and Intel 460GX chipset components.

There are two different voltage requirements for PWRGD as an input to the components. The SAC, SDC, MAC, MDC, and WXB components require a 1.8V PWRGD, and the PXB and GXB components require a 3.3V PWRGD signal.

Timing between the assertion of the different PWRGD edges is not critical. However, edge separation should be limited to 1 us or less.

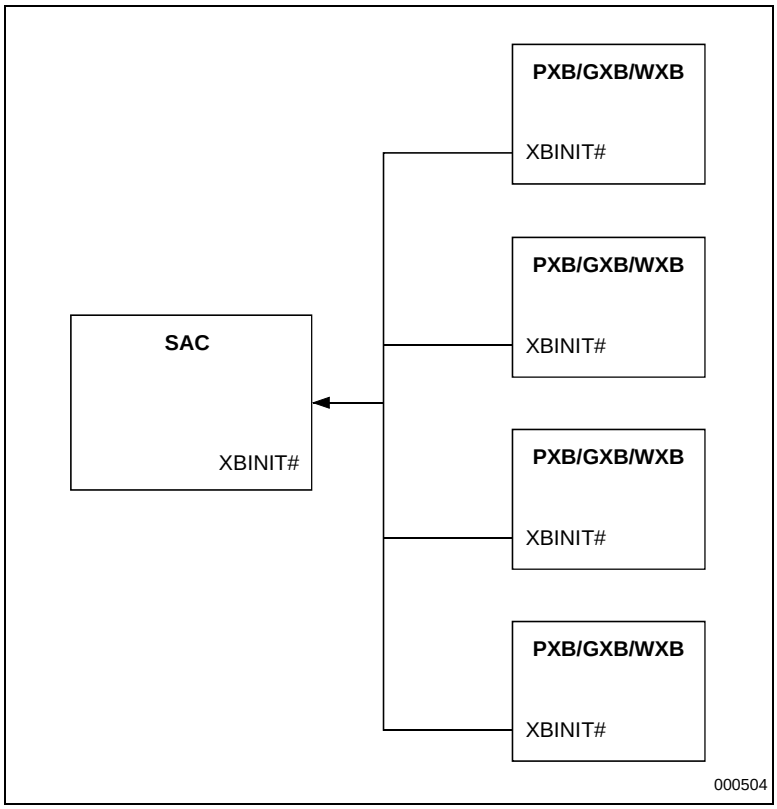
XBINIT#

Expander Bus Initialization
XBINIT# is an output from the expander bridges (PXB, GXB, WXB) and an input on the SAC. It signals a fatal error on the expander bridge

or other external component and causes a BINIT# assertion on the system bus.

Only one input is available on the SAC to receive this signal. One possible method to combine the XBINIT# signals for input on the SAC is to wire-OR them (See Figure 2-3).

Figure 2-3. XBINIT# Connections for Multiple Bridge Configurations



Note that with multiple loads, the XBINIT# signal is not guaranteed to be driven in one clock cycle. The driving agent will assert the XBINIT# signal and hold it asserted until reset. For systems which need to drive this in a deterministic fashion so that it will be seen on the same system clock over multiple nodes, external logic is required.

XCLKGTL

XCLK Buffer Type
XCLKGTL is a strapping pin (static input) on the PXB. It is normally tied to power. When XCLKGTL is high the PXB expects XCLK to be transmitted as a AGTL+, falling edge signal. When driven low, the PXB expects XLCK to be a CMOS, rising edge signal. (For compliance with 82450NX chipset systems.)

2.5.16 Clock Signals

HCLKIN

Host Clock In
HCLKIN receives a buffered host clock for SAC, SDC, MAC, and MDC. Equivalent to BCLKP# on Itanium processor.

HCLKIN# — **Host Clock in Complement**
HCLKIN# receives a complement of the buffered host clock for SAC, SDC, MAC, and MDC. Equivalent to BCLKN# on Itanium processor.

2.5.17 Compensation Resistor Pins

The Intel 460GX chipset includes I/O buffer compensation for selected pins to control the output impedance and/or slew rate. Please refer to Section 3.4 for a detailed listing of each components compensation resistor pins and corresponding recommended resistor values.

2.5.18 Power and Ground Pins

VCCA — **Analog VCC**
This is the analog VCC supply used for the PLLs. Refer to Section 3.1.3 for more information.

VSSA — **Analog VSS**
This is the analog VSS supply used for the PLLs. Refer to Section 3.1.3 for more information.

VSS — **Component Ground**
Refer to Chapter 9 for the correct number of ground pins for each component.

Table 2-9 lists the power pins for each component.

The processor system bus and Expander bus both require external termination. The "Intel® Itanium™ Processor at 800 MHz and 733 MHz Datasheet (Document Number: 245481)" describes the termination requirements for the system bus, while Chapter 5 describes the Expander bus termination requirements.

Table 2-9. Power Pins

Component	Planes	Voltage Level	Description
SAC	$VCT_{FSB[6:0]}$	1.5V	Processor system bus I/O
	$VCT_{Expander[14:0]}$	1.5V	Expander bus I/O
	VCC	1.8V	Core power
SDC	$VCT_{[7:0]}$	1.5V	Processor system bus I/O
	VCC	1.8V	Core power
MAC	VCC_{18}	1.8V	Memory data and control bus I/O
	VCC_{33}	3.3V	Memory subsystem I/O, core power
MDC	VCC_{18}	1.8V	Memory data and control bus I/O
	VCC_{33}	3.3V	Memory subsystem I/O, core power
PXB	VCT	1.5V	Expander bus I/O
	VCC	3.3V	Core power
	VCC_5	3.3V/5V	PCI bus /O
GXB	VCT	1.5V	Expander bus I/O
	VCC_Q	1.5V/3.3V	AGP bus I/O
	VCC	3.3V	Core power
WXB	VCT	1.5V	Expander bus I/O
	VCC	1.8V	Core power
	VCC_P	3.3V	PCI bus I/O

2.5.19 Reference Voltage Pins

VREFOUT[1:0] **Voltage Reference Ground Output**
These signals are internal grounds to either the SAC or GXB that may optionally be used as a ground reference for resistor divider networks generating Expander reference voltages.

Most input receivers on the Intel 460GX chipset are true differential receivers requiring a reference voltage to determine the trip point of the receiver. Table 2-10 lists the reference voltage pins.

Table 2-10. Reference Voltage Pins

Component	System Bus	Private Bus	Expander Bus	Memory Data and Control Bus	Memory Subsystem	AGP Bus
SAC	VREFFSB [3:0]	VREFPVB [1:0]	VREFF16 [3:0]	VREFM[1:0][a]		
SDC	VREF[4:0][b]	PVREF[1:0]		MVREFA [1:0][c] MVREFB [1:0]		
MAC				VREF18	VREF33	
MDC				VREF18	VREF33	
PXB			VREF[1:0]			
GXB			VREF[2:0][d]			VREFAGP [2:0]
WXB			VREF			

a. VREFM[1] is for memory board A, while VREFM[0] is for memory board B.
b. VREF[4] is for the address and control signals while VREF[3:0] are for data signals. These should be routed as two separate traces as shown in the "Intel® Itanium™ Processor at 800 MHz and 733 MHz Datasheet (Document Number: 245481)"
c. MVREFA is for memory board A, while MVREFB is for memory board B.
d. VREF2 & VREF0 reference the GXB Expander X0 bus connection to the SAC Expander X2 bus. VREF1 references the GXB Expander X1 bus connection to the SAC Expander X3 bus. See Section 5.5 for more details on GXB component connectivity.

Electrical Specifications for Components 3

3.1 DC and AC Specifications

For the detailed DC electrical specifications and AC timing specifications of a particular bus, please refer to the appropriate sections throughout the datasheet. This section is intended to provide general specifications common to each component of the Intel 460GX chipset. Electrical specification for the IFB and PID are found in Chapter 11 and Chapter 12 respectively. See Chapter 1 to locate information on the FWH.

3.1.1 Voltage Specification

Table 3-1 lists the voltage specification associated with the Intel 460GX chipset.

Table 3-1. Core and I/O Voltage Parameters

Parameter	Min	Typ	Max	Unit	Notes
1.8V core and I/O voltages	1.71	1.80	1.89	V	a
3.3V core and I/O voltages	3.13	3.30	3.47	V	a
Expander bus I/O voltage	1.42	1.50	1.58	V	a
5V PCI bus I/O voltage	4.75	5.00	5.25	V	a

a. Minimum and maximum values are based on a ±5% tolerance of the typical value.

3.1.2 Power and Power Step Specification

Table 3-2 lists the power and power set specifications for the Intel 460GX chipset components. This can be used to evaluate maximum power dissipation and determine capacitive decoupling requirements. It should be noted that since the Expander and System Bus I/O signals are always consuming power via external termination, they do not contribute to the step power.

Table 3-2. Step Power for the Intel® 460GX Chipset Components

Component	P_{Core} (W) Core Power	$P_{I/O}$ (W) I/O Power	P_{MAX} (W) Max Power[a,b]	I_{CC} (A) Max Power Supply Current[c]	I_{SS} (A) Max Ground Supply Current[d]	P_{Step} (W) Power Step in One Cycle[b]
SAC	4.6	2.6	7.2	2.5	3.5	6.4 → 7.2
SDC	1.9	3.1	5.0	2.1	2.1	2.1 → 5.0
MAC	1.5	4.0	5.5	1.3	2.0	2.3 → 5.5 [e]
MDC	1.5	4.0	5.5	2.1	1.9	3.5 → 5.5 [f]
PXB	9.1	1.9	11.0	2.9	4.4	10.0 → 11.0
GXB	8.9	2.4	11.3	2.5	4.0	10.0 → 11.3
WXB	7.7	2.1	9.8	5.3	6.1	8.7 → 9.8 [g]

a. Maximum power is assumed as a maximum average power. P_{MAX} may not equal the maximum voltage multiplied by the maximum current due to guard banding. This specification is a combination of core power (I_{CC}) and power dissipated in the AGTL+ outputs and I/O.
b. Step frequency = 133 MHz, except where otherwise noted.
c. The I_{CC} specification does not include the AGTL+ output current to VSS.
d. The I_{SS} specification is the maximum supply current consumption when all AGTL+ signals are low.
e. Out of this swing, only 10% is applicable to the 1.8V supply.
f. Out of this swing, only 27% is applicable to the 1.8V supply.
g. Out of this swing, 81% is applicable to the PCI bus. Step frequency = 66 MHz.

3.1.3 VCCA Pins

The analog power supply, VCCA, must be filtered from the board V_{CC} for the phase locked loop (PLL) to be stable. Figure 3-1 shows the recommended circuit for the SAC, SDC, and WXB components. There should be a separate filter for each VCCA pin on each component to avoid coupling noise from one analog circuit to another. The ground connection for each of these filter circuits should be made through the VCCA signal.

Figure 3-1. VCCA Filter for SAC, SDC and WXB Components

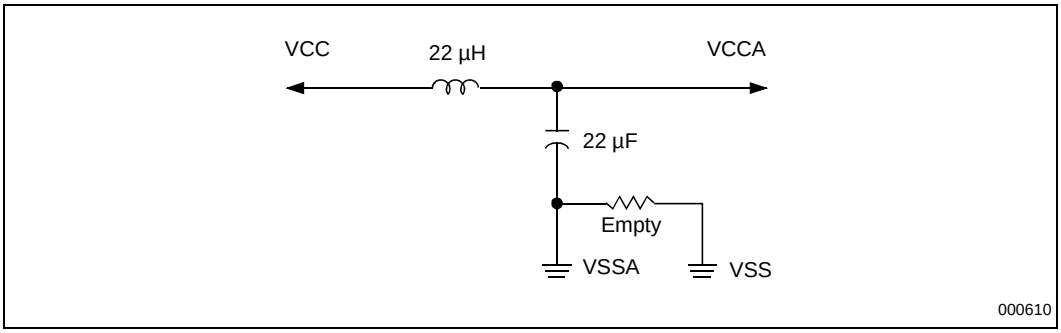
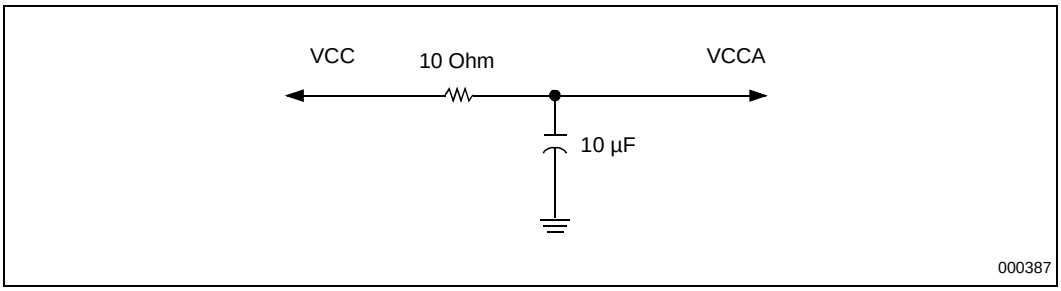


Figure 3-2 shows the recommended circuit for the MAC, MDC, GXB, and PXB components. There should be a separate filter for each VCCA pin on each component to avoid coupling noise from one analog circuit to another.

Figure 3-2. VCCA Filter for the MAC, MDC, GXB and PXB Components



3.2 Maximum Ratings

Table 3-3 contains stress ratings for the Intel 460GX chipset. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed.

Warning: *All components of the Intel 460GX chipset should not receive a clock while subjected to any of these conditions*. Functional operating conditions are given in the AC and DC tables. Extended

exposure to the maximum ratings may affect device reliability. Furthermore, although the Intel 460GX chipset contains protective circuitry to resist damage from static discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 3-3. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
1.8V Core and I/O voltage	–0.5	2.0	V	
System bus and Expander bus I/O voltage (SAC, SDC)	–0.3	V_{TT}[a]+0.7	V	
Expander bus I/O voltage (PXB, GXB)	–0.5	V_{TT}[b]+0.5 (not to exceed 2.9)	V	
3.3V Core voltage	–0.5	4.3	V	
3.3V I/O voltage		Core voltage +0.9 (not to exceed 4.7)	V	c
5V I/O voltage		V_{CC-PCI} +0.5	V	d
Storage temperature (SAC, SDC, and WXB)	–40	85	°C	
Storage Temperature (MAC, MDC, PXB, and GXB)	–65	150	°C	

a. V_{TT} is the termination voltage, see Table 4-1 for more information.
b. V_{TT} is the termination voltage, see Table 5-1 for more information.
c. Parameter applies to 3.3V tolerant and TAP Port signal groups only.
d. V_{CC-PCI} is the voltage level on the PCI bus.

Please also refer to the "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)" for the maximum AC waveforms for 5V and 3.3V PCI signals.

3.3 Transient Signal Overshoot Specification

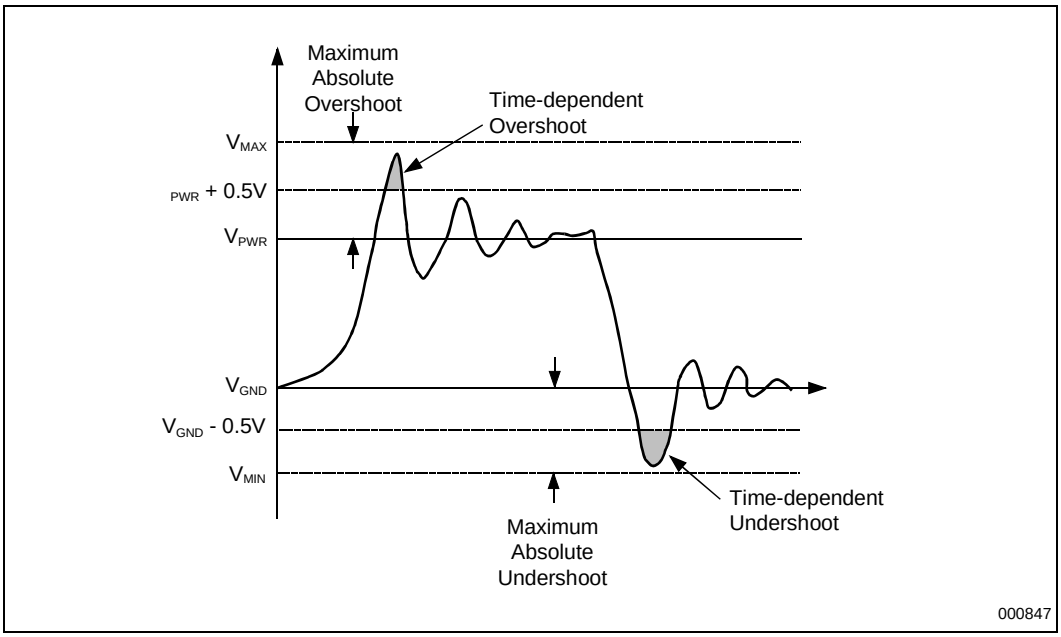
A transient electrical signal in the Intel 460GX chipset must not transition beyond the nominal power supply rail + 0.8V (V_{MAX}) or beyond the nominal ground supply rail – 0.8V (V_{MIN}).

If a transient signal transitions beyond the nominal power supply rail (V_{PWR}) + 0.5V or beyond the nominal ground supply rail (V_{GND}) – 0.5V, then it must transition back within these limits in less than one quarter of the clock period or 10ns, whichever is smaller. Please refer to Figure 3-3.

These values assume a current no greater than 10mA and measurement at the pin of the component. If these requirements are not followed, device reliability may be affected.

Furthermore, to ensure meeting AC timing requirements, a transient signal should settle within the steady state DC operating limits within seven tenths of the clock period.

Figure 3-3. Waveform Showing Signal Quality on the Receiver Pin



3.4 Compensation Resistors

The Intel 460GX chipset uses compensation resistors to control the output impedance and/or slew rate on selected signals.

All compensation resistors should be discrete elements with a precision of 1%. Connections should be made from the ball of the component to the first resistor pad, then from the second resistor pad directly to ground, unless otherwise noted. Trace lengths should not exceed 0.5 inch.

Please refer to Table 3-4 for a listing of compensation resistor pins for each component, a description of the their purpose, and the required resistor values.

Table 3-4. Compensation Resistor Pins

Component	I/O Buffer Compensation Resistor Pins	Signals Associated with Compensation Resistor Pin	Resistor Value	Notes
SAC	CRES[1:0]	Expander bus (slew rate control)	768Ω	a
	PVBCRES[1:0]	Private bus (impedance control)	110Ω	b
	SMPCRES	Memory Data and Control bus (impedance control)	110Ω	b
	IMPCNTL#	System bus (impedance control)	c	
	SWRCNTL#	System bus (slew rate control)	c	
SDC	CRESF1	System bus (slew rate control)	c	
	CRESF0	System bus (impedance control)	c	
	CRESM0	Memory Data and Control bus (impedance control)	110Ω	b

Table 3-4. Compensation Resistor Pins (Continued)

Component	I/O Buffer Compensation Resistor Pins	Signals Associated with Compensation Resistor Pin	Resistor Value	Notes
MAC	CRES2	Memory Data and Control bus (impedance control)	40Ω - 70Ω	d
	CRES1	Memory Subsystem Bus (impedance control)	40Ω - 70Ω	c,e
	CRES0	Memory Subsystem Bus - ChipSelect (impedance control)	40Ω - 70Ω	c,e
MDC	CRES2	Memory and Data Control Bus (impedance control)	40Ω - 70Ω	c
	CRES1	Memory Subsystem Bus (impedance control)	40Ω - 70Ω	c,e
	CRES0	Memory Subsystem Bus - MemCLK (impedance Control)	40Ω - 70Ω	c,e
PXB	CRES[1:0]	Expander bus (slew rate control)	768Ω	a
GXB	CRES[5:4]	AGP bus (impedance control)	60Ω	a,f
	CRES3	Other CMOS I/O (impedance control)	50Ω	f
	CRES2	GART SRAM interface (impedance control)	50Ω	f
	CRES[1:0]	Expander bus (slew rate control)	768Ω	a
WXB	CRES[1:0]	Expander bus (slew rate control)	768Ω	a

a. The resistor must be connected between the two pins.
b. The resistor is calculated to match twice the required board impedance of 55Ω.
c. Consult the "Intel® Itanium™ Processor at 800 MHz and 733 MHz Datasheet (Document Number: 245481)" for more information.
d. The resistor value should be calculated to match the impedance of the network, between 40 ohms and 70 ohms. Board measurements should be preformed to determine this value.
e. The buffer being compensated is capable of driving in regular mode (1x) or heavy mode (2x). This mode is determined by setting the appropriate component register as described in "Intel® 460GX Chipset System Software Developer's Manual (Document Number: 248704)". In regular mode (1x), the compensation resistor value will equal the output impedance of the buffer. In heavy mode (2x), the compensation resistor value will equal twice the output impedance of the buffer.
f. The resistor is calculated to match the board impedance.

System Bus Interface 4

This chapter describes the Intel 460GX chipset electrical specifications for the Itanium processor system bus interface.

4.1 DC Specifications

Table 4-1 contains the DC specifications for the system bus interface. All system bus signals, excluding clocks, are AGTL+ and require external pull-up resistors (R_{TERM}) to a termination voltage (V_{TT}) at each end of the bus. Signal receivers use a reference voltage (V_{REF}) provided by the system, which is derived from V_{TT}, to determine their switching threshold.

Table 4-1. System Bus Interface AGTL+ DC Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{TT}	Termination Voltage	1.425	1.500	1.575	V	±5%
V_{REF}	Reference Voltage		2/3 V_{TT}		V	a
R_{TERM}	Termination Resistance		40		Ω	b
V_{OH}	Driver Output High Voltage	V_{TT}			V	
V_{OL}	Driver Output Low Voltage			0.6	V	
V_{IH}	Receiver Input High Voltage	V_{REF} +0.2			V	c
V_{IL}	Receiver Input Low Voltage			V_{REF} –0.2	V	c
C_{IN}	Input Capacitance			10	pF	d
C_O	Output Capacitance			10	pF	e
$C_{I/O}$	I/O Capacitance			10	pF	e
I_{OL}	Output Low Current			45	mA	f
I_{LI}	Input Leakage Current			±50	µA	e
I_{REF}	Reference Voltage Current			±50	µA	

a. This must be a fraction of V_{TT} and cannot be derived from other sources. External resistors generating V_{REF} should have a tolerance of 1%.
b. 40Ω is a recommended termination resistance. A different termination resistance may work better in a different platform. R_{TERM} should have a tolerance of 1%.
c. STBN[3:0]# and STBP[3:0]# have a V_{IL} of V_x-0.1 and V_{IH} of V_x+0.1. V_x is the cross over voltage and can vary from 0.9 to 1.1 volts.
d. Includes package and die capacitance; but not capacitance from traces on the printed circuit board.
e. $0 \le V_{IN} \le V_{TT}$.
f. Current specified into a 25Ω load to V_{TT}.

4.2 AC Specifications

The system bus operates at a clock frequency of 133 MHz. Signals specified by “SS” in Section 2.4 use source synchronous clocking, allowing up to 266 MHz operation.

The AC timing specifications shown in this section are with respect to the ball of the component. The intent is to provide a method for verifying the component's I/O timings in a real system. These specifications reflect the I/O timings that the actual component is tested to in a tester environment under worst case conditions.

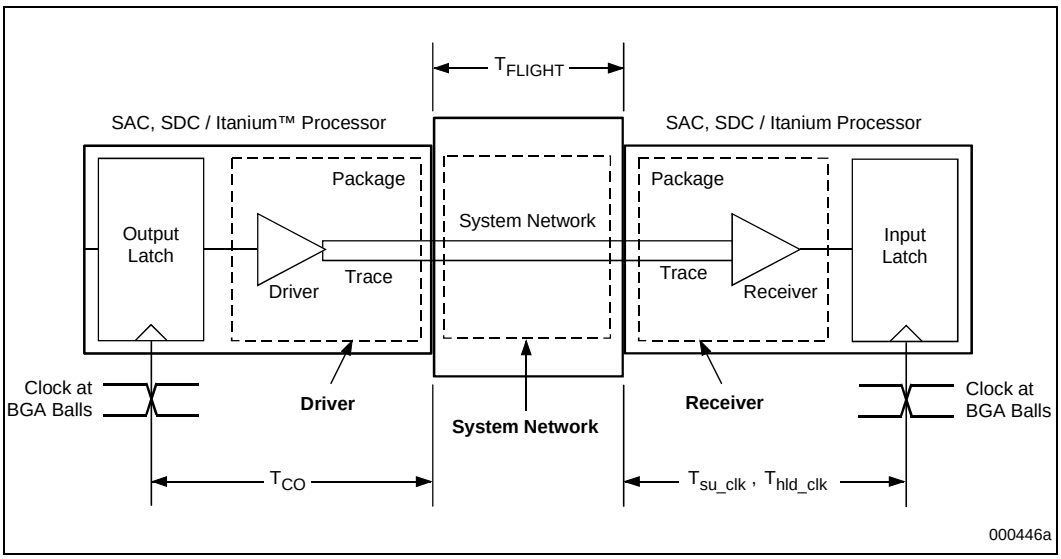
To determine system timing margins, separate timing specifications to internal nodes should be used. This enables the system designer to take into account the impact of various effects on I/O buffer behavior, such as noise and parasitics inside the part, thereby providing more margin with less guardband. Contact your local Intel Representative for further information.

4.2.1 Common Clock

The common clock timing specification for the system bus consists of three parts: clock to driver output delay (T_{CO}), flight time (T_{FLIGHT}), and receiver setup and hold to bus clock (T_{su_clk} and T_{hld_clk}). These timing parameters reference the driver and receiver components at the ball and are intended for verifying the component's I/O timings in a real system. The parameters should not be used to determine system timing margins.

Figure 4-1 illustrates these timing specifications.

Figure 4-1. Common Clock Timing Definition Overview

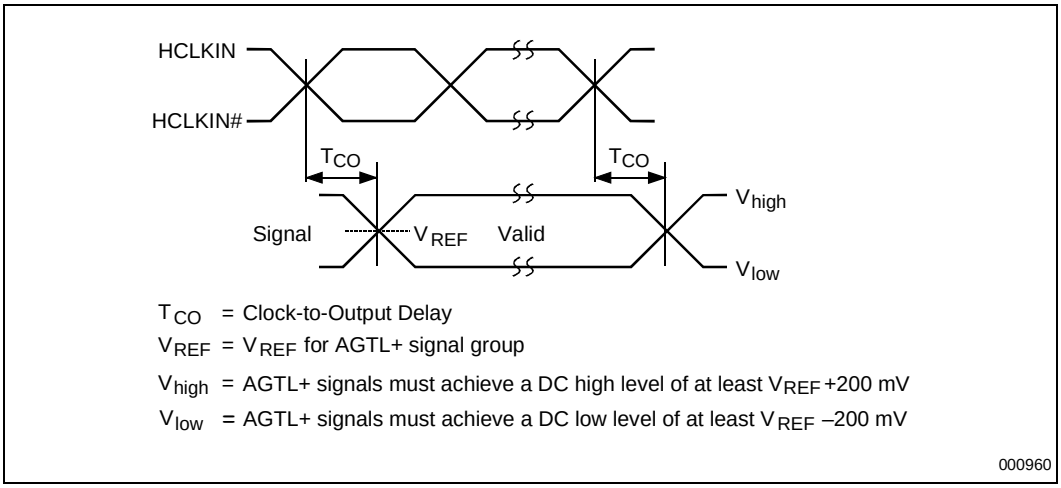


4.2.1.1 Clock to Driver Output Delay

The clock to driver output delay (T_{CO}) is defined as the time between the differential bus clock crossing at the input ball (at the driving agent) relative to the signal crossing V_{REF} at the output ball (of the driving agent) at an edge rate defined by the environment conditions. It includes the internal clock skew and tester guardband.

Figure 4-2 illustrates the T_{CO} timing definition, and Section 4.2.1.4 lists the T_{CO} values for each appropriate system bus signal in the 460GX chipset.

Figure 4-2. $T_{CO,min/max}$ Timing Diagram



4.2.1.2 Flight Time

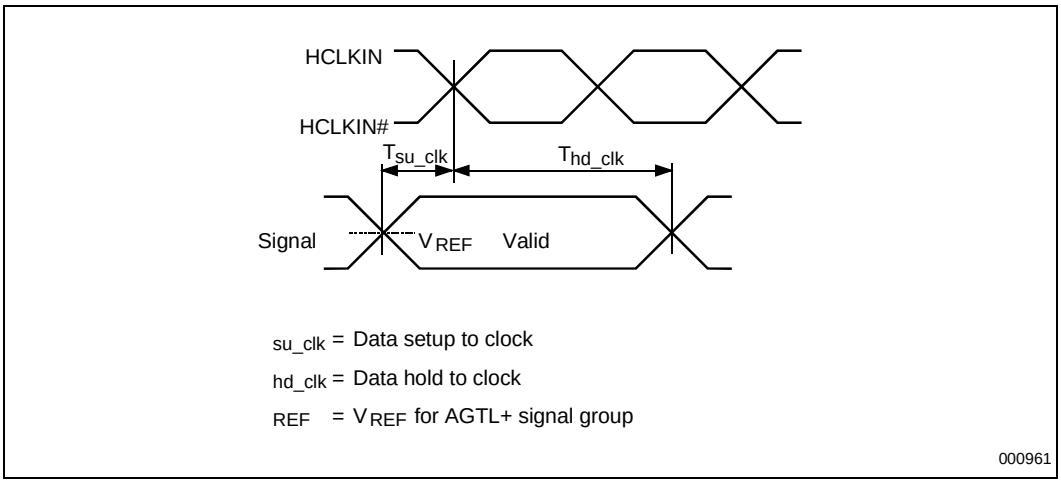
The flight time (T_{FLIGHT}) is defined as the time between the signal crossing V_{REF} at the output ball (of the driving agent) relative to the signal crossing V_{REF} at the input ball (of the receiving agent). Flight time is a system dependent timing based on the specific PCB technology, the interface routing topology, and applicable connectors.

4.2.1.3 Receiver Setup and Hold to Bus Clock

The receiver setup and hold to bus clock (T_{su_clk} and T_{hd_clk}) are defined by the signal at the input ball (of the receiving agent) crossing V_{REF} relative to the differential bus clock crossing at the input ball (of the receiving agent). T_{su_clk} and T_{hd_clk} each include the internal clock skew and tester guardband.

Figure 4-3 illustrates the T_{su_clk} and T_{hd_clk} timing definition, and Section 4.2.1.4 lists the T_{su_clk} and T_{hd_clk} values for each appropriate system bus signal in the 460GX chipset.

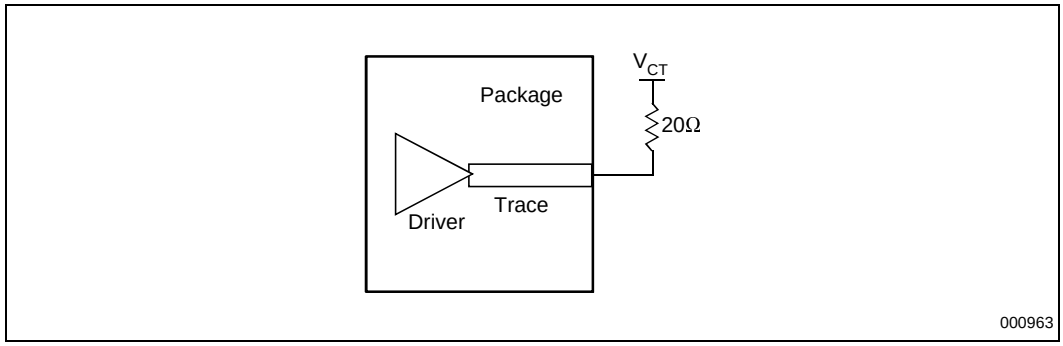
Figure 4-3. T_{su_clk} and T_{hd_clk} Timing Diagram



4.2.1.4 Component Timing Specification

The tables in this section show the common clock AC timing parameters that the actual component is tested to in a test environment under worst case conditions. These parameters are intended to provide a method for verifying the component's I/O timings in a real system. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 4-4. The voltage reference is V_{REF}.

Figure 4-4. Rated Load for Common Clock AC Timing Specification



Please refer to the preceding sections for corresponding timing diagrams.

Table 4-2. SAC Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T1	A(35:3)#	0.48	2.85	1.51	0.75	
T2	ADS#	0.37	2.68	1.51	0.75	
T2	AP[1:0]#	0.37	2.68	1.51	0.75	
T2	BERR#	0.37	2.68	1.51	0.75	
T2	BINIT#	0.37	2.68	1.51	0.75	
T2	BNR#	0.37	2.68	1.51	0.75	
T2	BPRI#	0.37	2.68			
T2	BR[0]#	0.37	2.68	1.51	0.75	
T2	BR[3:1]#			1.51	0.75	
T2	DEFER#	0.37	2.68			
T2	HIT#	0.37	2.68	1.51	0.75	
T2	HITM#	0.37	2.68	1.51	0.75	
T2	INIT#	0.37	2.68			
T2	LOCK#			1.51	0.75	
T2	REQ[4:0]#	0.37	2.68	1.51	0.75	
T2	RP#	0.37	2.68	1.51	0.75	
T3	RESET#	0.06	3.46			
T15	BP[5:0]#	0.37	2.68	1.51	0.75	

Table 4-3. SDC Component Common Clock AC Specification Timings

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T16_1X	D[63:0]#	0.4	3.05	1.60	0.65	
T16_1X	DEP[7:0]#	0.4	3.05	1.60	0.65	
T17	STBP[3:0]#	2.38	4.81			a
T17	STBN[3:0]#	2.38	4.81			a
T18	DBSY#	0.54	2.84	1.51	0.75	
T18	DRDY#	0.54	2.84	1.51	0.75	
T18	ID[6:0]#	0.54	2.84			
T18	IDS#	0.54	2.84			
T18	RS[2:0]	0.54	2.84			
T18	RSP#	0.54	2.84			
T18	SBSY#	0.54	2.84	1.51	0.75	
T18	TRDY#	0.54	2.84			

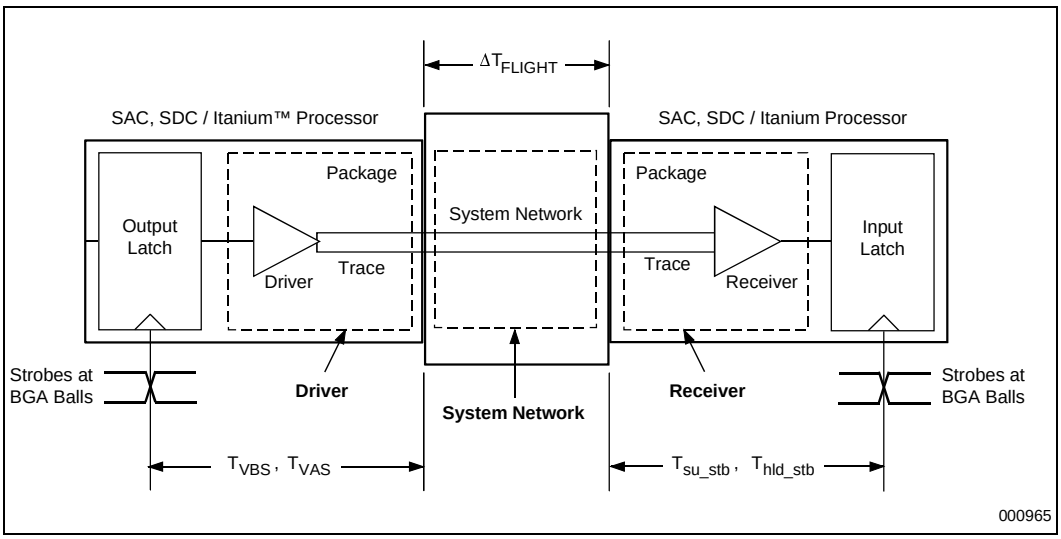
a. Includes a 1.875ns phase offset from HCLKIN/HCLKIN# by design.

4.2.2 Source Synchronous

The source synchronous timing specification for the system bus consists of three parts: driver valid before and after strobe (T_{VBS} and T_{VAS}), delta flight time (ΔT_{FLIGHT}), and receiver setup and hold to strobe (T_{su_stb} and T_{hld_stb}). These three timing parameters reference the driver and receiver components at the ball and are intended for verifying the component's I/O timings in a real system. The parameters should not be used to determine system timing margins.

Figure 4-5 illustrates these timing specifications.

Figure 4-5. Source Synchronous Timing Definition Overview

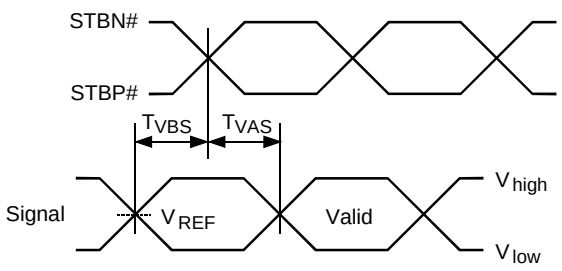


4.2.2.1 Driver Valid Before and After Strobe

The driver valid before and after strobe (T_{VBS} and T_{VAS}) are defined as the time between the signal crossing V_{REF} at the output ball (of the driving agent) relative to the differential strobe crossing at the output ball (of the driving agent). T_{VBS} and T_{VAS} each include the internal clock skew and tester guardband.

Figure 4-6 illustrates the T_{VBS} and T_{VAS} timing definition, and Section 4.2.2.4 lists the T_{VBS} and T_{VAS} values for each appropriate system bus signal of the 460GX chipset.

Figure 4-6. T_{VBS} and T_{VAS} Timing Diagram



T_{VBS} = Data output valid before strobe

T_{VAS} = Data output valid after strobe

V_{REF} = V_{REF} for AGTL+ signal group

V_{high} = AGTL+ signals must achieve a DC high level of at least V_{REF} +200 mV

V_{low} = AGTL+ signals must achieve a DC low level of at least V_{REF} –200 mV

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4.2.2.2 Delta Flight Time

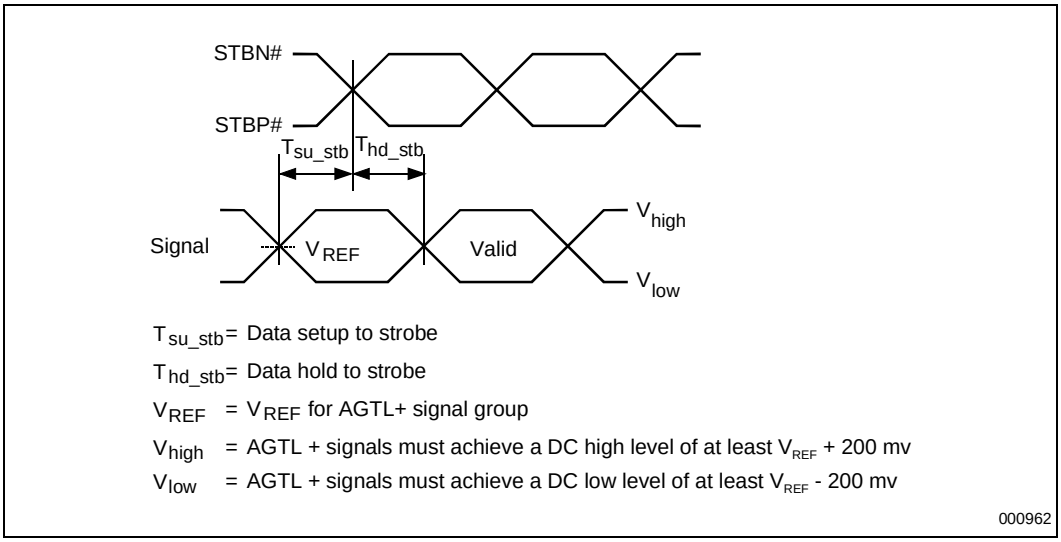
The delta flight time (ΔT_{FLIGHT}) is defined as the timing difference between the signal flight time, as measured by the signal crossing V_{REF} at the output ball (of the driving agent) relative to the signal crossing V_{REF} at the input ball (of the receiving agent), and the strobe flight time, as measured by the strobe crossing V_{REF} at the output ball (of the driving agent) relative to the strobe crossing V_{REF} at the input ball (of the receiving agent). Delta flight time is a system dependent timing based on the maximum skew due to the specific PCB technology, the interface routing topology, and applicable connectors.

4.2.2.3 Receiver Setup and Hold to Strobe

The receiver setup and hold to strobe (T_{su_stb} and T_{hd_stb}) are defined by the signal at the input ball (of the receiving agent) crossing V_{REF} relative to the differential strobe crossing at the input ball (of the receiving agent). T_{su_stb} and T_{hd_stb} each include the internal clock skew and tester guardband.

Figure 4-7 illustrates the T_{su_stb} and T_{hd_stb} timing definition, and Section 4.2.2.4 lists the T_{su_stb} and T_{hd_stb} values for each appropriate system bus signal of the 460GX chipset.

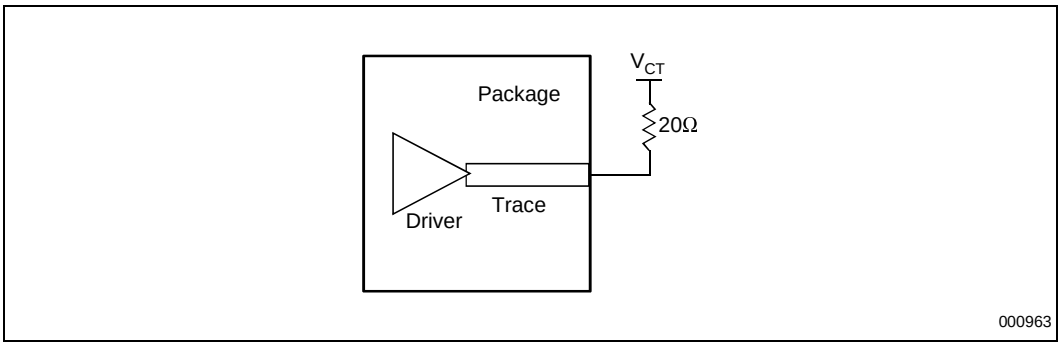
Figure 4-7. T_{su_stb} and T_{hd_stb} Timing Diagram



4.2.2.4 Component Timing Specification

The table in this section shows the source synchronous AC timing parameters under worst case conditions in a tester environment. These parameters are intended to provide a method for verifying the component's I/O timings in a real system. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 4-8. The voltage reference is V_{REF}.

Figure 4-8. Rated Load for Source Synchronous AC Timing Specification



Please refer to the preceding sections for corresponding timing diagrams.

Table 4-4. SDC Component Source Synchronous AC Timing Specification

Symbol	Parameter	T_{VBS}	T_{VAS}	T_{su_stb}	T_{hd_stb}	Notes
T16_2X	D[63:0]#	1.50	1.50	0.04	0.57	
T16_2X	DEP[7:0]#	1.50	1.50	0.04	0.57	

4.2.3 HCLKIN, HCLKIN# Skew Specification

The HCLKIN and HCLKIN# need to be routed to match the specification shown in Figure 4-5. The host clock pins are routed from the clock generator to the SAC, SDC, MDC and MAC.

Table 4-5. HCLKIN, HCLKIN# Max Skew Specification

Skew Between (at balls)	Max (ps)
SAC - SDC	100
All others	200

Expansion Interface 5

This chapter describes the Intel 460GX chipset electrical specifications of the Expansion bus interface.

5.1 DC Specifications

Table 5-1 contains the DC specifications for the Expansion bus interface. All Expansion bus signals, excluding clocks, are AGTL+ and require external pull-up resistors (R_{TERM}) to a termination voltage (V_{TT}) at each end of the bus. Signal receivers use a reference voltage (V_{REF}) provided by the system, which is derived from V_{TT}, to determine their switching threshold.

Table 5-1. Expansion Interface DC Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{TT}	Termination Voltage	1.425	1.500	1.575	V	±5%
V_{REF}	Reference Voltage		2/3 V_{TT}		V	a
R_{TERM}	Termination Resistance		50		Ω	b
V_{OH}	Driver Output High Voltage	V_{TT}			V	
V_{OL}	Driver Output Low Voltage			0.6	V	
V_{IH}	Receiver Input High Voltage	V_{REF} +0.2			V	
V_{IL}	Receiver Input Low Voltage			V_{REF} –0.2	V	
C_{IN}	Input Capacitance			10	pF	c
C_O	Output Capacitance			10	pF	d
$C_{I/O}$	I/O Capacitance			10	pF	d
I_{OL}	Output Low Current			36	mA	e
I_{LI}	Input Leakage Current			±50	µA	e
I_{REF}	Reference Voltage Current			±50	µA	f
ΔV_{cm}	DC ground difference between interconnect ends	–100		+100	mV	g

a. This must be a fraction of V_{TT} and cannot be derived from other sources. External resistors generating V_{REF} should have a tolerance of 1%.
b. R_{TERM} should have a tolerance of 1%.
c. Includes package and die capacitance; but not capacitance from traces on the Printed Circuit Board.
d. $0 \le V_{IN} \le V_{TT}$.
e. Current specified into a 25Ω load to V_{TT}.
f. Total Current for all V_{REF}
g. Exceeding this specification will compromise AC timing.

5.2 AC Specifications

The Expansion bus operates at a clock frequency of 133 MHz. Signals specified by “SS” in Section 2.4 use source synchronous clocking, allowing up to 266 MHz operation.

The AC timing specifications shown in this section are with respect to the ball of the component. The intent is to provide a method for verifying the component’s I/O timings in a real system. These specifications reflect the I/O timings that the actual component is tested to in a tester environment under worst case conditions.

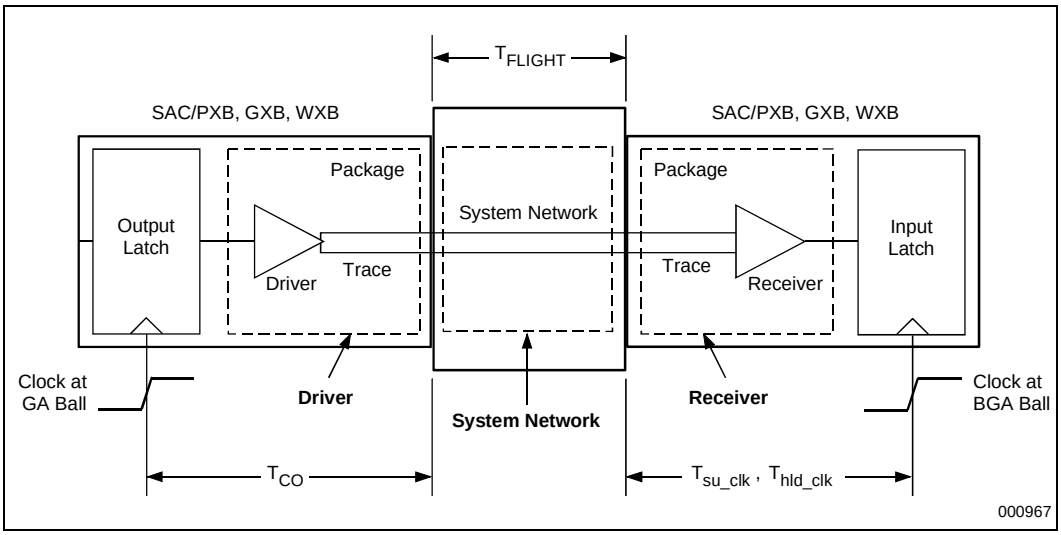
To determine system timing margins, separate timing specifications to internal nodes should be used. This enables the system designer to take into account the impact of various effects on I/O buffer behavior, such as noise and parasitics inside the part, thereby providing more margin with less guardband. Contact your local Intel Representative for further information.

5.2.1 Common Clock

The common clock timing specification for the Expansion bus consists of three parts: clock to driver output delay (T_{CO}), flight time (T_{FLIGHT}), and receiver setup and hold to bus clock (T_{su_clk} and T_{hld_clk}). These three timing parameters reference the driver and receiver components at the ball and are intended for verifying the component’s I/O timings in a real system. The parameters should not be used to determine system timing margins.

Figure 5-1 illustrates these timing specifications.

Figure 5-1. Common Clock Timing Definition Overview



5.2.1.1 Clock to Driver Output Delay

The clock to driver output delay (T_{CO}) is defined as the time between the differential bus clock crossing at the input ball (at the driving agent) relative to the signal crossing V_{REF} at the output ball (of the driving agent) at an edge rate defined by the environment conditions. For further information about this parameter, please refer to Section 4.2.1.1.

Section 5.2.1.4 lists the T_{CO} values for each appropriate Expansion bus signal in the Intel 460GX chipset.

5.2.1.2 Flight Time

The flight time (T_{FLIGHT}) is defined as the time between the signal crossing V_{REF} at the output ball (of the driving agent) relative to the signal crossing V_{REF} at the input ball (of the receiving agent). Flight time is a system dependent timing based on the specific PCB technology, the interface routing topology, and applicable connectors.

5.2.1.3 Receiver Setup and Hold to Bus Clock

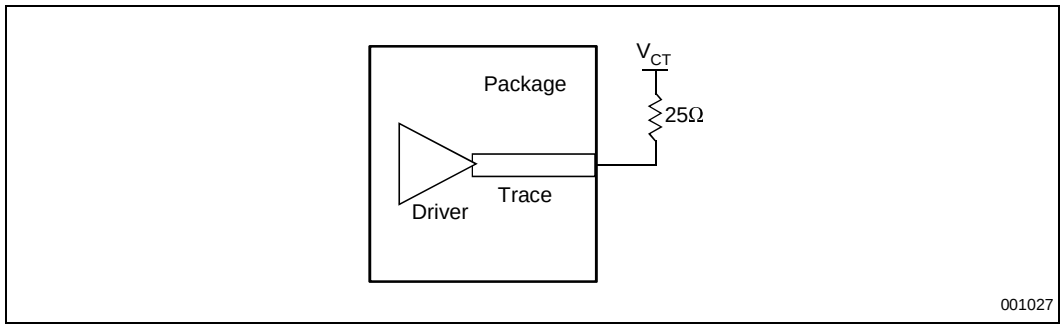
The receiver setup and hold to bus clock (T_{su_clk} and T_{hd_clk}) are defined by the signal at the input ball (of the receiving agent) crossing V_{REF} relative to the differential bus clock crossing at the input ball (of the receiving agent). For further information about this parameter, please refer to Section 4.2.1.3.

Section 5.2.1.4 lists the T_{su_clk} and T_{hd_clk} values for each appropriate Expansion bus signal in the Intel 460GX chipset.

5.2.1.4 Component Timing Specification

The tables in this section show the common clock AC timing parameters that the actual component is tested to in a test environment under worst case conditions. These parameters are intended to provide a method for verifying the component's I/O timings in a real system. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 5-2. The voltage reference is V_{REF}.

Figure 5-2. Rated Load for Common Clock AC Timing Specification



Please refer to the preceding sections for corresponding timing diagrams.

Table 5-2. SAC Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T8A	X(0,1,2,3)RST#	-0.19	1.86			a
T8A	X(0,1,2,3)RSTB#	-0.19	1.86			a
T8A	X(0,1,2,3)RSTFB#			2.11	0.61	
T9A	X(0,1,2,3)HSTBN#	1.54	3.65			b
T9A	X(0,1,2,3)HSTBP#	1.54	3.65			b
T9A	X(0,1,2,3)XSTBN#			1.88		cd
T9A	X(0,1,2,3)XSTBP#			1.88		cd

a. Referenced to XCLK
b. Includes a 1.875ns phase offset from HCLKIN/HCLKIN# by design
c. Guaranteed by design.
d. AC timings is used for determining the maximum length of the Expansion bus.

Table 5-3. WXB Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T8A	XRST#			2.18	1.9[a]	
T9A	XHSTBN#			1.58	1.875	a
T9A	XHSTBP#			1.58	1.875	a
T9A	XXSTBN#	1.72	4.39			b
T9A	XXSTBP#	1.72	4.39			b

a. Guaranteed by design.
b. Includes a 1.875ns phase offset from HCLKIN/HCLKIN# by design.

Table 5-4. PXB Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T40	XRST#			1.99	1.5	
T99	XHSTBN#			1.5		a
T99	XHSTBP#			1.5		a
T65	XXSTBN#	2.5	2.875			b
T63	XXSTBP#	2.6	2.875			b
T11a	XIB#	0.61	1.69			

a. Guaranteed by design.
b. Includes a 1.875ns phase offset from HCLKIN/HCLKIN# by design.

Table 5-5. GXB Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T8B	X0RST#			2.09	0.18	
T9B	X(0,1)HSTBN#			3.36	1.875	a
T9B	X(0,1)HSTBP#			3.36	1.875	a
T9B	X(0,1)XSTBN#	2.22	3.98			b
T9B	X(0,1)XSTBP#	2.22	3.98			b

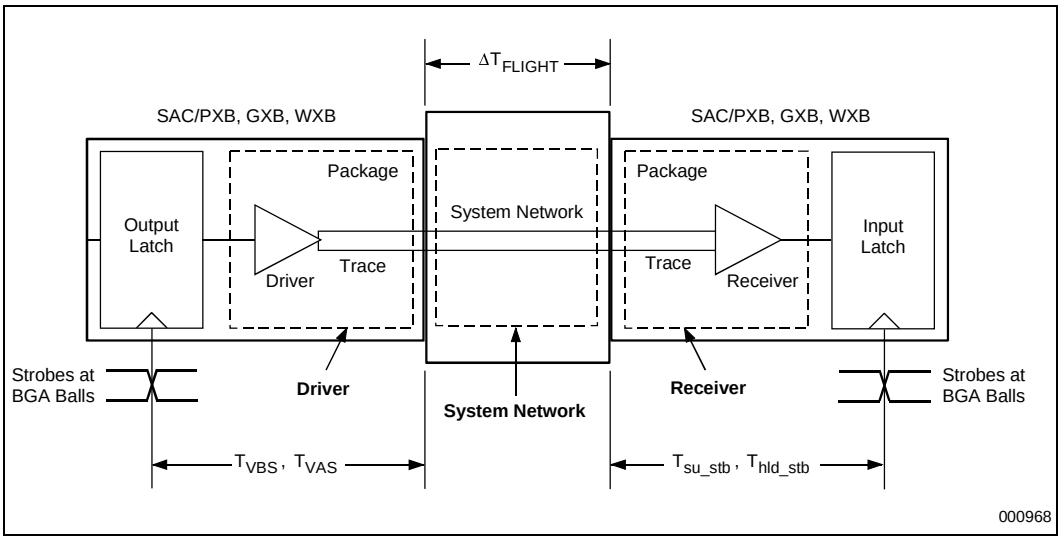
a. Guaranteed by design.
b. Includes a 1.875ns phase offset from HCLKIN/HCLKIN# by design.

5.2.2 Source Synchronous

The source synchronous timing specification for the Expansion bus consists of three parts: driver valid before and after strobe (T_{VBS} and T_{VAS}), delta flight time (ΔT_{FLIGHT}), and receiver setup and hold to strobe (T_{su_stb} and T_{hld_stb}). These three timing parameters reference the driver and receiver components at the ball and are intended for verifying the component's I/O timings in a real system. The parameters should not be used to determine system timing margins.

Figure 5-3 illustrates these timing specifications.

Figure 5-3. Source Synchronous Timing Definition Overview



5.2.2.1 Driver Valid Before and After Strobe

The driver valid before and after strobe (T_{VBS} and T_{VAS}) are defined as the time between the signal crossing V_{REF} at the output ball (of the driving agent) relative to the differential strobe crossing at the output ball (of the driving agent). For further information about this parameter, please refer to Section 4.2.2.1.

Section 5.2.2.4 lists the T_{VBS} and T_{VAS} values for each appropriate Expansion bus signal of the Intel 460GX chipset.

5.2.2.2 Delta Flight Time

The delta flight time (ΔT_{FLIGHT}) is defined as the timing difference between the signal flight time, as measured by the signal crossing V_{REF} at the output ball (of the driving agent) relative to the signal crossing V_{REF} at the input ball (of the receiving agent), and the strobe flight time, as measured by the strobe crossing V_{REF} at the output ball (of the driving agent) relative to the strobe crossing V_{REF} at the input ball (of the receiving agent). Delta flight time is a system dependent timing based on the maximum skew due to the specific PCB technology, the interface routing topology, and applicable connectors.

5.2.2.3 Receiver Setup and Hold to Strobe

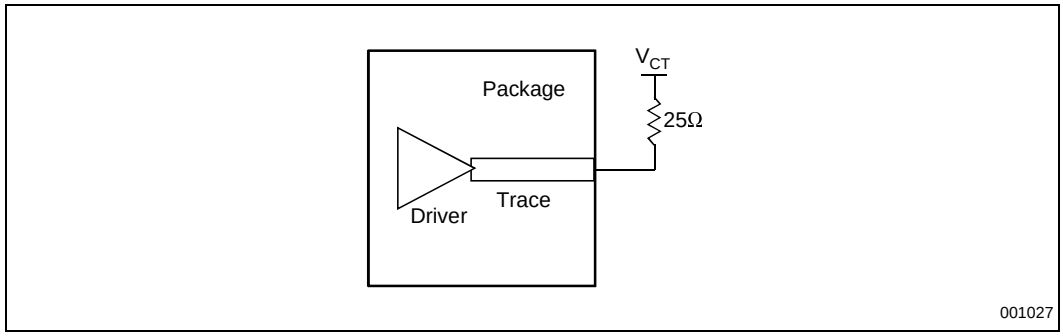
The receiver setup and hold to strobe (T_{su_stb} and T_{hd_stb}) are defined by the signal at the input ball (of the receiving agent) crossing V_{REF} relative to the differential strobe crossing at the input ball (of the receiving agent). For further information about this parameter, please refer to Section 4.2.2.3.

Section 5.2.2.4 lists the T_{su_stb} and T_{hd_stb} values for each appropriate Expansion bus signal of the Intel 460GX chipset.

5.2.2.4 Component Timing Specification

The tables in this section show the source synchronous AC timing parameters under worst case conditions in a tester environment. These parameters are intended to provide a method for verifying the component's I/O timings in a real system. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 5-4. The voltage reference is V_{REF}.

Figure 5-4. Rated Load for Source Synchronous AC Timing Specification



Please refer to the preceding sections for corresponding timing diagrams.

Table 5-6. SAC Component Source Synchronous AC Timing Specification

Symbol	Parameter	T_{VBS}	T_{VAS}	T_{su_stb}	T_{hd_stb}	Notes
T7A	X(0,1,2,3)ADS#	1.85	1.41	-0.18	0.81	
T7A	X(0,1,2,3)BE[1:0]#	1.85	1.41	-0.18	0.81	
T7A	X(0,1,2,3)D[15:0]#	1.85	1.41	-0.18	0.81	
T7A	X(o,1,2,3)BLK#	1.85	1.41			
T7A	X(0,1,2,3)HRTS#	1.85	1.41			
T7A	X(0,1,2,3)PAR#	1.85	1.41	-0.18	0.81	
T7A	X(0,1,2,3)XRTS#			-0.18	0.81	

Table 5-7. WXB Component Source Synchronous AC Timing Specification

Symbol	Parameter	T_{VBS}	T_{VAS}	T_{su_stb}	T_{hd_stb}	Notes
T7A	XADS#	1.57	1.17	0.22	0.92	
T7A	XBE[1:0]#	1.57	1.17	0.22	0.92	
T7A	XBLK#			0.22	0.92	
T7A	XD[15:0]#	1.57	1.17	0.22	0.92	
T7A	XHRTS#			0.22	0.92	
T7A	XPAR#	1.57	1.17	0.22	0.92	
T7A	XXRTS#	1.57	1.17			
T7A	XIB#	1.57	1.17			

Table 5-8. PXB Component Source Synchronous AC Timing Specification

Symbol	Parameter	T_{VBS}	T_{VAS}	T_{su_stb}	T_{hd_stb}	Notes
T22_ads	XADS#	0.82	1.10	0.44	0.38	
T22	XBE[1:0]#	0.82	1.10	0.94	0.40	
T22	XBLK#			0.94	0.40	
T22	XD[15:0]#	0.82	1.10	0.94	0.40	
T11	XHRTS#			0.94	0.40	
T22	XPAR#	0.82	1.10	0.94	0.40	
T13	XXRTS#	0.82	1.10			

Table 5-9. GXB Component Source Synchronous AC Timing Specification

Symbol	Parameter	T_{VBS}	T_{VAS}	T_{su_stb}	T_{hd_stb}	Notes
T7B	X(0,1)ADS#	1.71	2.13	0.33	0.60	
T7B	X(0,1)BE[1:0]#	1.71	2.13	0.33	0.60	
T7B	X0BLK#			0.33	0.60	
T7B	X(0,1)D[15:0]#	1.71	2.13	0.33	0.60	
T7B	X(0,1)HRTS#			0.33	0.60	
T7B	X(0,1)PAR#	1.71	2.13	0.33	0.60	
T7B	X(0,1)XRTS#	1.71	2.13			

5.3 XCLK Duty Cycle Requirement

The component driving XCLK to the Expansion expansion bridge must meet a duty cycle requirement as indicated in Table 5-10. The SAC component is designed to comply with this requirement.

Table 5-10. External Clock Duty Cycle Requirement

Parameter	Minimum	Maximum	Notes
XCLK duty cycle	48%	52%	a

a. Assumes a nominal duty cycle of 50%. Guaranteed by design.

5.4 Clock and Reset Signal Distribution

Two copies of the bus clock, XCLK and XCLKB, are driven by the SAC on the Expansion bus. XCLK goes to the expansion bridge (PXB, GXB, or WXB). XCLKB loops back to the SAC on the XCLKFB input. The XCLK and XCLKB signal interconnects must be length matched so both components receive the same phase of the clock. The same is done for the reset signals, XRST#, XRSTB#, and XRSTFB# (see Figure 5-5).

Figure 5-5. Signal Topology

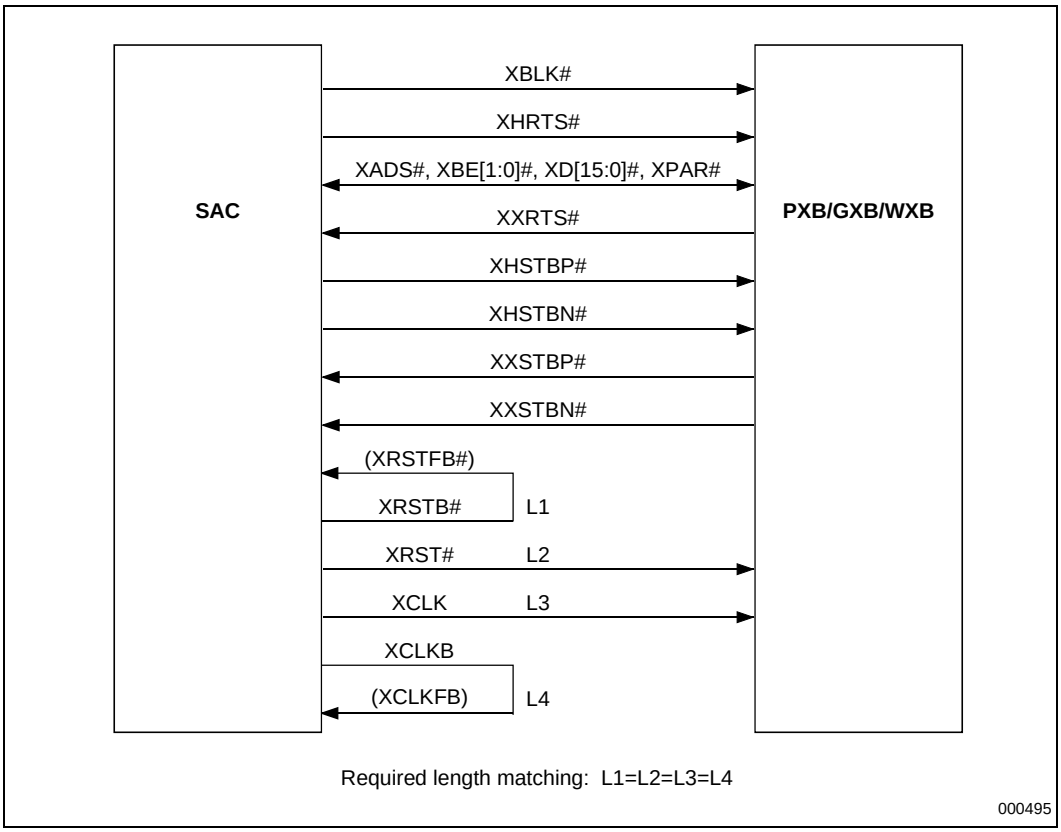


Table 5-11 shows the parameters necessary for XCLK skew determination with the various expansion components.

Table 5-11. Expansion Bridge Component XCLK Parameters

Driver	Value	Unit	Notes
XCLK jitter	125	ps	a
XCLK to XCLKB pin skew	±75	ps	b
Feedback clock to source clock skew	±175	ps	c

a. Jitter is specified at the X(0,1,2,3)CLK pin. Guaranteed by design.
b. Skew is from the pin of each corresponding expansion channel, i.e. X(0)CLK to X(0)CLKFB, X(3)CLK to X(3)CLKFB and so on, the skew does not go across expansion bridges. Guaranteed by design.
c. Feedback clock to source clock skew is specified between the input pin of HCLKIN and the input pin of X(0,1,2,3)CLKFB. Guaranteed by design.

5.5 GXB Component Specific Requirements

The GXB component connects to the SAC component uniquely in that it uses two Expansion buses. The listing below indicates the requirements that must be met when connecting the GXB component to the SAC component:

- The SAC and GXB components must connect via the SAC X2 and X3 Expansion buses.
- The X2 and X3 Expansion buses must operate in the same latency mode.

- The X2 and X3 Expansion buses must meet common clock and source synchronous timing requirements.
- X2CLK and X2RST# on the SAC component must connect to X0CLK and X0RST# on the GXB component.
- X3CLK and X3RST# on the SAC component must connect to valid AGTL+ termination.
- The feedback loops X2CLKB to X2CLKFB and X2RSTB# to X2RSTFB# must each match in length to the X2CLK and X2RST# nets, as shown in Figure 5-5.

Memory Data & Control Interface 6

This chapter describes the Intel 460GX chipset electrical specifications of the Memory Data and Control (MD&C) interface. This interface is actually composed of multiple interfaces, each of which can be classified as one of two bus types. The **memory address bus** includes all address and control signals between the SAC and MAC and between the MAC and MDC components. The **memory data bus** includes all data and strobe signals between the SDC and MDC components. The **memory data bus** is source synchronous capable.

6.1 DC Specifications

The following tables contain the DC specifications for the MD&C interface. All MD&C signals are 1.8V CMOS, therefore external pull-up resistors are not required. Signal receivers use a reference voltage (V_{REF}) provided by the system, which is derived from V_{CC18}, to determine their switching threshold.

Table 6-1. DC Specifications for MAC and MDC

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{REF}	Reference Voltage		1/2 V_{CC18}		V	a
V_{IL}	Input Low Voltage			V_{REF} - 0.2	V	
V_{IH}	Input High Voltage	V_{REF} + 0.2			V	b
V_{OL}	Output Low Voltage			0.9	V	cd
V_{OH}	Output High Voltage	0.9			V	d
C_{IN}	Input Capacitance			10	pF	
C_O	Output Capacitance			10	pF	
$C_{I/O}$	I/O Capacitance			10	pF	
I_{REF}	Reference Voltage Current			50	µA	
I_{OL}	Output Low Current	18.0			mA	ed
I_{OH}	Output High Current	18.0			mA	d
I_{LI}	Input Leakage Current			±50	µA	f
I_{LO}	Output Leakage Current			±50	µA	g

a. This must be a fraction of V_{CC18}, the 1.8V power supply, and cannot be derived from other sources. External resistors generating V_{REF} should have a tolerance of 1%.
b. $V_{IH} = V_{REF} + 0.25V$ for the MDC.
c. For open drain outputs, $V_{OL, MAX} = 0.4V$.
d. I_{OH}=0mA at V_{OH} of $0.99*V_{CC}$; I_{OL}=0mA at V_{OL} of $0.01*V_{CC}$
e. For open drain outputs, $I_{OL, MIN} = 3mA$.
f. $0 \le V_{IN} \le V_{CC18}$.
g. Tri-state only or logic high for open drain outputs.

Table 6-2. DC Specifications for SAC and SDC

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{REF}	Reference Voltage		1/2 V_{CC18}		V	a
V_{IL}	Input Low Voltage			V_{ref} - 0.2	V	
V_{IH}	Input High Voltage	V_{ref} + 0.2			V	
V_{OL}	Output Low Voltage			0.9	V	bd
V_{OH}	Output High Voltage	0.9			V	d
C_{IN}	Input Capacitance			10	pF	
C_O	Output Capacitance			10	pF	
$C_{I/O}$	I/O Capacitance			10	pF	
I_{REF}	Reference Voltage Current			50	µA	
I_{OL}	Output Low Current	18			mA	cd
I_{OH}	Output High Current	18			mA	d
I_{LI}	Input Leakage Current			±50	µA	e
I_{LO}	Output Leakage Current			±50	µA	f

a. This must be a fraction of V_{CC18}, the 1.8V power supply, and cannot be derived from other sources. External resistors generating V_{REF} should have a tolerance of 1%.
b. For open drain outputs, $V_{OL, MAX}$ = 0.4V.
c. For open drain outputs, $I_{OL, MIN}$ = 3mA.
d. I_{OH}=0mA at V_{OH} of 0.99*V_{CC}; I_{OL}=0mA at V_{OL} of 0.01*V_{CC}.
e. $0 \le V_{IN} \le V_{CC18}$.
f. Tri-state only or logic high for open drain outputs.

6.2 AC Specifications

The **memory address bus** operates at a clock frequency of 133 MHz. The **memory data bus** contains signals specified by “SS” in Section 2.4 that use source synchronous clocking, allowing up to 266 MHz operation.

The AC timing specifications shown in this section are with respect to the ball of the component. These specifications reflect the I/O timings that the actual component must meet under worst case conditions.

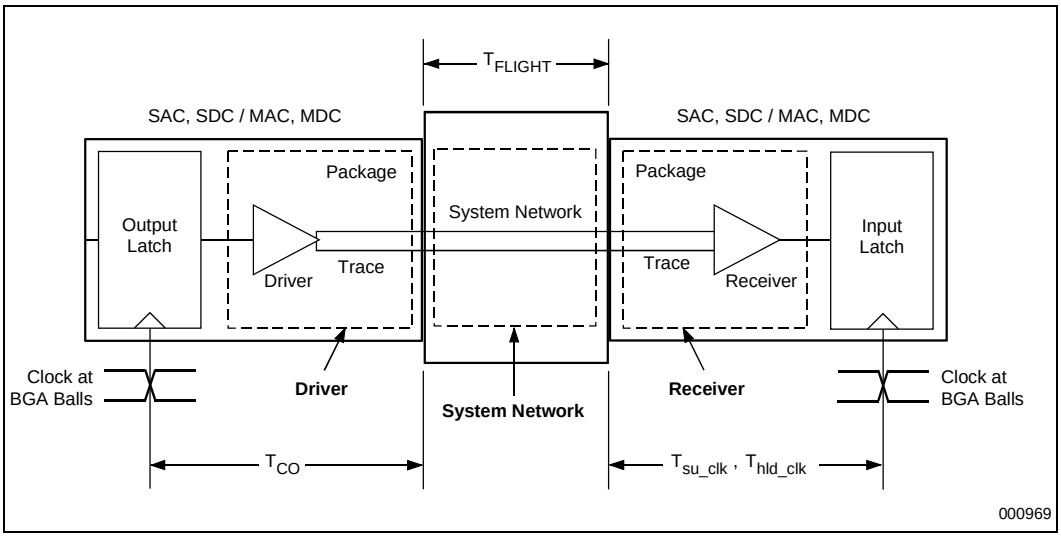
To determine system timing margins, measurements of the specific PCB technology and routing topology being implemented are required to find the minimum and maximum flight times (T_{FLIGHT}) between the driver ball and the receiver ball. Care must be taken when measuring flight times to ensure that the worst case conditions for all of the critical parameters are considered. Refer to Section 7.1 for further details.

6.2.1 Common Clock

The common clock timing specification for the MD&C interface consists of three parts: clock to driver output delay (T_{CO}), flight time (T_{FLIGHT}), and receiver setup and hold to bus clock (T_{su_clk} and T_{hld_clk}). These three timing parameters reference the driver and receiver components at the ball.

Figure 6-1 illustrates these timing specifications.

Figure 6-1. Timing Definition Overview



6.2.1.1 Clock to Driver Output Delay

The clock to driver output delay (T_{CO}) is defined as the time between the differential bus clock crossing at the input ball (at the driving agent) relative to the signal crossing V_{REF} at the output ball (of the driving agent) at an edge rate defined by the environment conditions. For further information about this parameter, please refer to Section 4.2.1.1.

Section 6.2.1.4 lists the T_{CO} values for each appropriate MD&C interface signal in the Intel 460GX chipset.

6.2.1.2 Flight Time

The flight time (T_{FLIGHT}) is defined as the time between the signal crossing V_{REF} at the output ball (of the driving agent) relative to the signal crossing V_{REF} at the input ball (of the receiving agent). Flight time is a system dependent timing based on the specific PCB technology, the interface routing topology, and applicable connectors.

6.2.1.3 Receiver Setup and Hold to Bus Clock

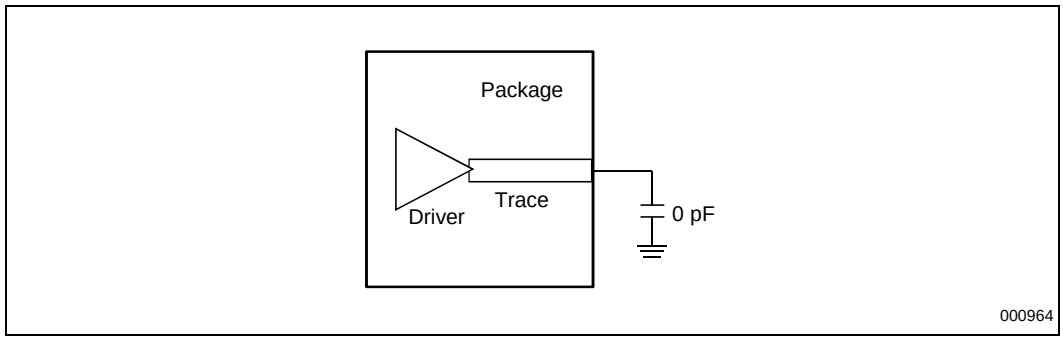
The receiver setup and hold to bus clock (T_{su_clk} and T_{hd_clk}) is defined by the signal at the input ball (of the receiving agent) crossing V_{REF} relative to the differential bus clock crossing at the input ball (of the receiving agent). For further information about this parameter, please refer to Section 4.2.1.3.

Section 6.2.1.4 lists the T_{su_clk} and T_{hd_clk} values for each appropriate MD&C interface signal in the Intel 460GX chipset.

6.2.1.4 Component Timing Specification

The tables in this section show the common clock AC timing parameters that the actual component is tested to in a test environment under worst case conditions. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 6-2. The voltage reference is V_{REF}.

Figure 6-2. Rated Load for Common Clock AC Timing Specification



Please refer to the preceding sections for corresponding timing diagrams.

Table 6-3. SAC Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T6A	CMND(A,B)[1:0]	-0.43	1.60			
T6A	ERR(A,B)#			1.57	0.49	
T6A	LCMPLT(A,B)#			1.57	0.49	
T6A	MA(A,B)[16:0]#	-0.43	1.60			
T6A	PAR(A,B)#	-0.43	1.60			
T6A	RCMPLT(A,B)#			1.57	0.49	
T6A	ROW(A,B)[2:0]#	-0.43	1.60			
T12	MEMRST[1:0]#	-0.43	1.60			

Table 6-4. SDC Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T21A	MD(A,B)SP[3:0]#	1.57	3.88			a
T21A	MD(A,B)SN[3:0]#	1.57	3.88			a
T19A	FWMD(A,B)#			1.53	0.49	
T19A	FWSLA(A,B)#			1.53	0.49	
T19A	HWMD(A,B)(L,R)#	-0.43	1.73			
T19A	LRMD(A,B)#			1.53	0.49	

a. Includes a 1.875ns phase offset from HCLKIN/HCLKIN# by design

Table 6-5. MAC Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T6B	CMND[1:0]#			1.54	0.66	
T6B	CMPLT(L,R)#	– 0.03	3.26			
T6B	MA[16:0]#			1.54	0.66	
T6B	MEMRST#			1.54	0.66	

Table 6-5. MAC Component Common Clock AC Timing Specification (Continued)

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T6B	PAR#			1.54	0.66	
T6B	ROW[2:0]#			1.54	0.66	
T6C	ERR#	– 0.13	3.20			
T19B	FWMD#	– 0.03	3.27			
T19B	FWSL#	– 0.03	3.27			
T19B	HWMD(L,R)#			1.54	0.66	
T19B	LRMD#	– 0.03	3.27			
T24	CORDR[1:0]#	– 0.03	3.23			
T24	FDQ(L,R)#	– 0.03	3.23			
T24	FRMD#	– 0.03	3.23			
T24	LDQ(L,R)#	– 0.03	3.23			
T24	LEFT1#	– 0.03	3.23			
T24	LWMD#	– 0.03	3.23			
T24	MINIT#	– 0.03	3.23			
T24	RESET#	– 0.03	3.23			

Table 6-6. MDC Component Common Clock AC Timing Specification

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T21B	MDSP#	1.75	5.20			a
T21B	MDSN#	1.75	5.20			a
T24	CORDR[1:0]#			1.54	0.75	
T24	FDQ(L,R)#			1.54	0.75	
T24	FRMD#			1.54	0.75	
T24	LDQ(L,R)#			1.54	0.75	
T24	LEFT#			1.54	0.75	
T24	LWMD#			1.54	0.75	
T24	MINIT#			1.54	0.75	
T24	RESET#			1.54	0.75	

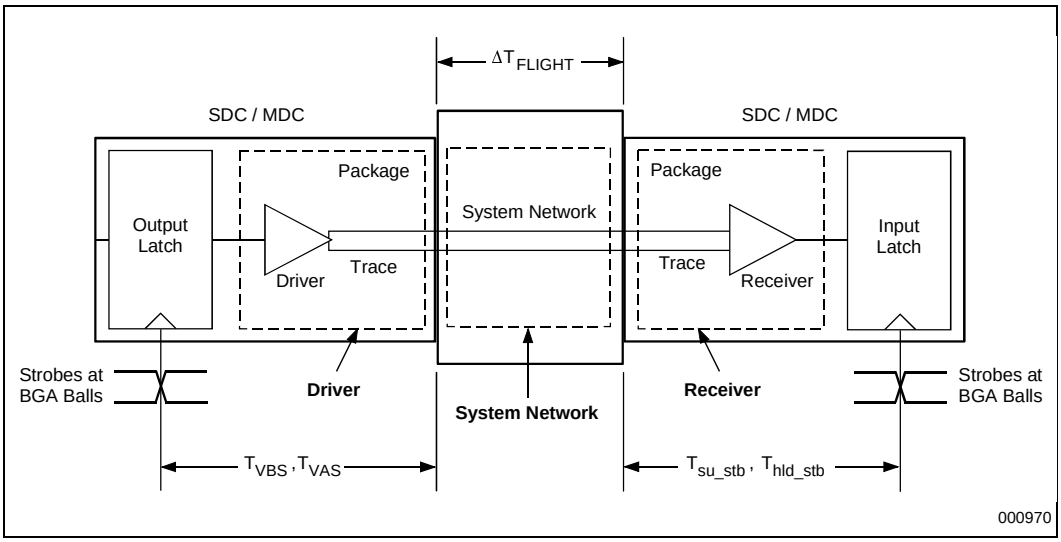
a. $T_{CO,\ min/max}$ each include a 1.875ns phase offset from HCLKIN/HCLKIN# by design

6.2.2 Source Synchronous

The source synchronous timing specification for the **memory data bus** consists of three parts: driver valid before and after strobe (T_{VBS} and T_{VAS}), delta flight time (ΔT_{FLIGHT}), and receiver setup and hold to strobe (T_{su_stb} and T_{hld_stb}). These three timing parameters reference the driver and receiver components at the ball.

Figure 6-3 illustrates these timing specifications.

Figure 6-3. Timing Definition Overview



6.2.2.1 Driver Valid Before and After Strobe

The driver valid before and after strobe (T_{VBS} and T_{VAS}) is defined as the time between the signal crossing V_{REF} at the output ball (of the driving agent) relative to the differential strobe crossing at the output ball (of the driving agent). For further information about this parameter, please refer to Section 4.2.2.1.

Section 6.2.2.4 lists the T_{VBS} and T_{VAS} values for each appropriate **memory data bus** signal of the Intel 460GX chipset.

6.2.2.2 Delta Flight Time

The delta flight time (ΔT_{FLIGHT}) is defined as the timing difference between the signal flight time, as measured by the signal crossing V_{REF} at the output ball (of the driving agent) relative to the signal crossing V_{REF} at the input ball (of the receiving agent), and the strobe flight time, as measured by the strobe crossing V_{REF} at the output ball (of the driving agent) relative to the strobe crossing V_{REF} at the input ball (of the receiving agent). Delta flight time is a system dependent timing based on the maximum skew due to the specific PCB technology, the interface routing topology, and applicable connectors.

6.2.2.3 Receiver Setup and Hold to Strobe

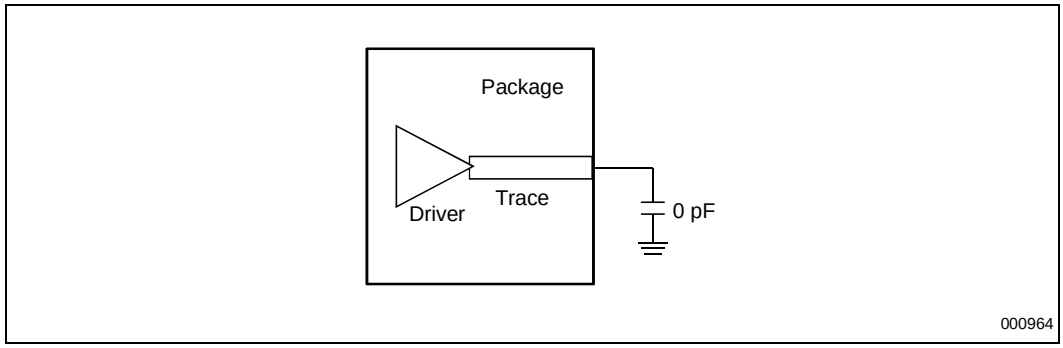
The receiver setup and hold to strobe (T_{su_stb} and T_{hd_stb}) is defined by the signal at the input ball (of the receiving agent) crossing V_{REF} relative to the differential strobe crossing at the input ball (of the receiving agent). For further information about this parameter, please refer to Section 4.2.2.3.

Section 6.2.2.4 lists the T_{su_stb} and T_{hd_stb} values for each appropriate **memory data bus** signal of the Intel 460GX chipset.

6.2.2.4 Component Timing Specification

The tables in this section show the source synchronous AC timing parameters under worst case conditions in a tester environment. These parameters are intended to provide a method for verifying the component's I/O timings in a real system. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 6-4. The voltage reference is V_{REF}.

Figure 6-4. Rated Load for Source Synchronous AC Timing Specification



Please refer to the preceding sections for corresponding timing diagrams.

Table 6-7. SDC Component Source Synchronous AC Timing Specification

Symbol	Parameter	T_{VBS}	T_{VAS}	T_{su_stb}	T_{hd_stb}	Notes
T20A	MD(A,B)[71:0]#	1.07	1.84	0.50	0.86	

Table 6-8. MDC Component Source Synchronous AC Timing Specification

Symbol	Parameter	T_{VBS}	T_{VAS}	T_{su_stb}	T_{hd_stb}	Notes
T20B	MD[17:0]#	1.00	2.00	0.58	0.52	

6.2.2.5 Trace Length Requirement

The source synchronous MD&C bus length must be within the limits shown in Table 6-9.

Table 6-9. MD&C Source Synchronous Bus Length Maximum

Bus	Maximum (ns)
MD&C Source Synchronous	0.55 * Bus Clock

Subsystem Bus Specifications 7

This chapter describes the Intel 460GX chipset electrical specifications for the memory subsystem, I/O subsystem, and other interfaces.

7.1 Calculating AC Timing Margins

To determine AC timing margins for these various interfaces, measurements of the specific PCB technology and routing topology are required to find the minimum and maximum flight times (T_{FLIGHT}) between the driver pin and the receiver pin. Care must be taken when measuring the flight times to ensure that the worst case conditions for all of the critical parameters are considered. The setup and hold time margin calculations are given by:

Setup time margin = Cycle time – ($T_{CO,max}$ + $T_{FLIGHT,max}$ + T_{su_clk} + $T_{ext\_clk\_skew}$)

Hold time margin = $T_{CO,min}$ + $T_{FLIGHT,min}$ – T_{hld_clk} – $T_{ext\_clk\_skew}$

T_{CO} is the clock at the pin to valid data at the pin parameter specific to the component driving the signal. T_{su_clk} and T_{hld_clk} are the data setup to clock at the pin and data hold to clock at the pin parameters specific to the component receiving the signal. $T_{ext\_clk\_skew}$ is the clock skew external to the components.

7.2 MAC and MDC – Memory Subsystem Specification

The memory subsystem includes the 3.3V CMOS interface between the MAC / MDC components and SDRAM DIMMs. This bus has a clock frequency of 66 MHz, yielding a cycle time of 15ns. All signals are common clock signals.

7.2.1 Memory Subsystem DC Specifications

Table 7-1 lists the DC specifications for the 3.3V CMOS memory subsystem signals.

Table 7-1. Memory Subsystem DC Specifications for 2x Mode

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{REF}	Reference Voltage		1/2 V_{CC33}			a
V_{IL}	Input Low Voltage			V_{REF}-0.2	V	
V_{IH}	Input High Voltage	V_{REF}+0.2			V	
V_{OL}	Output Low Voltage			1.65	V	b
V_{OH}	Output High Voltage	1.65			V	b
C_{IN}	Input Capacitance			10	pF	
C_O	Output Capacitance			10	pF	
$C_{I/O}$	I/O Capacitance			10	pF	
I_{REF}	Reference Voltage Current			50	µA	

Table 7-1. Memory Subsystem DC Specifications for 2x Mode (Continued)

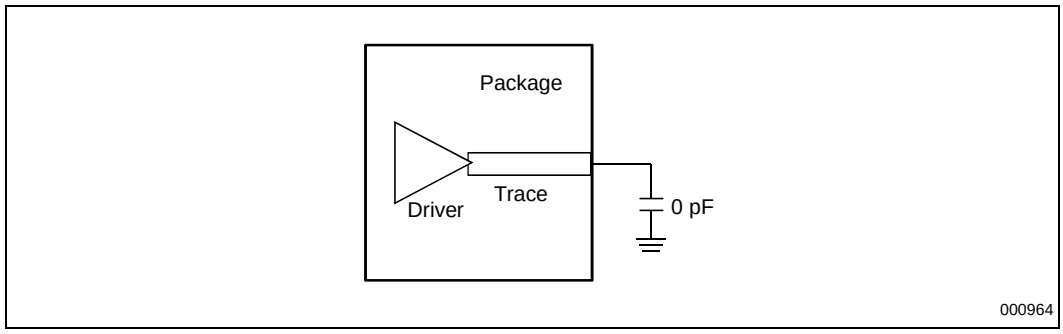
Symbol	Parameter	Min	Nom	Max	Unit	Notes
I_{OL}	Output Low Current	66			mA	b
I_{OH}	Output High Current	66			mA	b
I_{LI}	Input Leakage Current			±50	µA	c
I_{LO}	Output Leakage Current			±50	µA	d

a. This must be a fraction of V_{CC33}, the 3.3V power supply, and cannot be derived from other sources. External resistors generating V_{REF} should have a tolerance of 1%.
b. I_{OH}=0mA at V_{OH} of 0.99*V_{CC}; I_{OL}=0mA at V_{OL} of 0.01*V_{CC}.
c. $0 \le V_{IN} \le V_{CC33}$.
d. Tri-state only or logic high for open drain outputs.

7.2.2 Memory Subsystem AC Specifications

Table 7-2 and Table 7-3 consist of the AC timing parameters for the SDRAM interface. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 7-1. The voltage reference is V_{REF}.

Figure 7-1. MAC and MDC Component SDRAM Interface Rated Load for AC Timings



The system designer must find the specifications for the SDRAM used in the system in order to calculate the timing margins.

Table 7-2. MDC Component AC Timings at 66 MHz

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T25_1x	DQ(L,R)[71:0]	0.85	3.24	1.64	0.68	
T25_2x	DQ(L,R)[71:0]	0.85	3.24	1.64	0.68	

Table 7-3. MAC Component AC Timings at 66 MHz [a]

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T25_2x	ADD(L,R)(A,B,C,D)[12:0]	– 0.10	2.95			
T25_2x	BANK(L,R)(A,B,C,D)[2:0]	– 0.10	2.95			
T25_2x	RAS(L,R)(A,B,C,D)#	– 0.10	2.95			
T25_2x	CAS(L,R)(A,B,C,D)#	– 0.10	2.95			
T25_2x	WE(L,R)(A,B,C,D)#	– 0.10	2.95			
T25_2x	CS(L,R)(A,B,C,D)#	– 0.10	2.95			

a. The buffer is capable of driving in regular mode (1x) or heavy mode (2x). This mode is determined by setting the appropriate component register as described in "Intel® 460GX Chipset System Software Developer's Manual (Document Number: 248704)". In regular mode (1x), the compensation resistance will equal the output impedance. In heavy mode (2x), the compensation resistance will be twice the output impedance. Operation in 1x mode for the MAC is tested for functionality but not tested for AC or DC.

Note: The AC timings shown in Table 7-2 and Table 7-3 are specified relative to the HCLK crossing at the input of the component. These timings are not related to MEMCLK.

Table 7-4 shows the parameters necessary to account for clock skew with the MDC component.

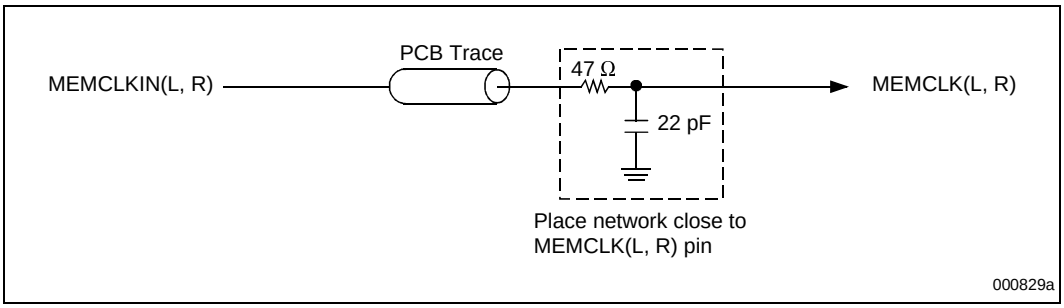
Table 7-4. MDC Component Memory Subsystem Bus Clock Parameters[a]

Driver	Value	Unit	Notes
Clock source jitter	125	ps	b
Clock pin to pin skew	250	ps	c
Feedback clock to source clock skew	+200 to +800	ps	d

a. MEMCLK(L,R) are measured at the point that they cross 50% of 3.3V Vcc. These specifications only apply if the circuit in Figure 7-2 is used.
b. Jitter is specified at the pin for MEMCLKB(L,R)[15:0] or MEMCLKIN(L,R) relative to the differential crossing of HCLKIN/HCLKIN# at the pin. The jitter for all pins should center around the HCLKIN/HCLKIN# differential crossing. Guaranteed by design.
c. Clock buffer pin to pin skew is specified between one pin of MEMCLKB(L,R)[15:0] or MEMCLKIN(L,R) and any other pin of MEMCLKB(L,R)[15:0] or MEMCLKIN(L,R). Guaranteed by design.
d. Feedback clock to source clock skew is specified between the input pin of MEMCLK(L,R) and the voltage crossing at the input pins of HCLKIN/HCLKIN#. Guaranteed by design.

The MDC component clock feedback trace must contain a filter network near the MEMCLK(L,R) input signals. Figure 7-2 shows the recommended circuit.

Figure 7-2. MDC Component SDRAM Feedback Clock Termination



7.3 PXB – PCI Interface Specification

For more information on the PCI bus specific signals and corresponding waveforms, please refer to the 5V tolerant, 33MHz sections of the "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)".

Table 7-5 lists the AC timings for the PCI interface and PIIXOK# signal for the PXB. These timings are specified with respect to the rising edge of XCLK. The XCLK is four times the PCICLK. All timings are taken from the "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)".

Table 7-5. PXB Component PCI Interface AC Specifications

Parameter	T_{su_clk} Min	T_{hld_clk} Min	T_{CO} Min	T_{CO} Max	Unit	Notes
P(A,B)AD[31:0], P(A,B)C/BE[3:0]#, P(A,B)TRDY#, P(A,B)STOP#, P(A,B)LOCK#, P(A,B)DEVSEL#, P(A,B)PAR, P(A,B)IRDY#, P(A,B)FRAME#, P(A,B)PERR#, P(A,B)XARB#	7.0	0.0	2.0	11.0	ns	a, b
P(A,B)REQ[5:0]#	12.0	0.0			ns	a
P(A,B)GNT[5:0]#			2.0	12.0	ns	a, b
INTRQ(A,B)#, P(A,B)RST#, P(A,B)SERR#			2.0	11.0	ns	a, b
REQ64#, ACK64#	7.0	0.0	2.0	11.0	ns	a, b
PHOLD#	7.0	0.0			ns	a
PHLDA#, WSC#			2.0	12.0	ns	a, b
P(A,B)MON[1:0]#	5.0	0.5	1.0	6.0	ns	c
PIIXOK#	7.0	0.0			ns	a

a. 5V tolerant signal levels.
b. Min and max timings are referenced with a rated load. Please refer to the "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)".
c. Min and Max timings are measured with a 0pF rated load.

XCLK divided by four is internally phase-lock looped to generate low skew P(A,B)CLK output signals. These output signals drive an independent clock generator which is used to generate PCI clock signals for each PCI device on the bus. All PCI clock traces driven by the independent clock generator, including the feedback trace, should have closely matched lengths. This will ensure low clock skew between PCI devices. Table 7-6 shows the parameters necessary for clock skew determination with the PXB component.

Table 7-6. PXB Component PCI Bus Clock Parameters

Driver	Value	Unit	Notes
Clock source jitter	125	ps	a
PCI clock buffer pin to pin skew	System Dependent	ps	b
Feedback clock to source clock skew	50	ps	c

a. Jitter is specified at the pin for P(A,B)CLK. Guaranteed by design.
b. Clock buffer pin to pin skew is specified between one PCI clock pin and any other PCI clock pin at the clock buffer. Guaranteed by design.
c. Feedback clock to source clock skew is specified between the input pin of P(A,B)CLKFB and the input pin of XCLK#. Guaranteed by design.

7.4 WXB – PCI Interface Specification

For more information on the PCI bus specific signals and corresponding waveforms, please refer to the 3.3 V, 66 MHz sections of the "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)"

Table 7-7 lists the AC timings for the PCI interface of the WXB. These timings are specified with respect to the P(A,B)CLK[2:0] at the PCI component or the rising edge of 'XCLK - 500ps' at the WXB pin. The XCLK is 2x/4x of the PCICLK 66/33 MHz clock respectively. All timings are taken from the "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)".

Table 7-7. WXB Component PCI Interface AC Specifications

Parameter	T_{su_clk} Min	T_{hld_clk} Min	T_{CO} Min	T_{CO} Max	Unit	Notes
P(A,B)AD[63:0], P(A,B)C/BE[7:0]#, P(A,B)TRDY#, P(A,B)STOP#, P(A,B)LOCK#, P(A,B)DEVSEL#, P(A,B)PAR, P(A,B)PAR64, P(A,B)IRDY#, P(A,B)FRAME#, P(A,B)PERR#, P(A,B)M66EN, P(A,B)REQ64#, P(A,B)ACK64#,	3.0	0.0	2.0	6.0	ns	a
P(A,B)REQ[5:0]#	3.0	0.0			ns	
P(A,B)GNT[5:0]#, P(A,B)INTRQ#, P(A,B)RST#, P(A,B)SERR#			2.0	6.0	ns	a

a. Min and max timing values are referenced to a rated load. Please refer to the "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)".

XCLK divided by two is internally phase-lock looped to generate low skew P(A,B)CLK[2:0] output signals. These output signals drive PCI clock input signals for each PCI device on the bus. All PCI clock traces, including the feedback trace, should have closely matched lengths. This will ensure low clock skew between PCI devices. Table 7-8 shows the parameters necessary for clock skew determination with the WXB component.

Table 7-8. WXB Component PCI Bus Clock Parameters

Driver	Value	Unit	Notes
Clock source jitter	125	ps	a
PCI clock buffer pin to pin skew	50	ps	b
Feedback clock to source clock skew	135	ps	c

a. Jitter is specified at the pin for P(A,B)CLK[2:0] and P(A,B)CLKREF. Guaranteed by design.
b. Clock buffer pin to pin skew is specified between one PCI clock pin and any other PCI clock. Guaranteed by design.
c. Feedback clock to source clock skew is specified between the input pin of P(A,B)CLKFB and the input pin of XCLK#. Guaranteed by design.

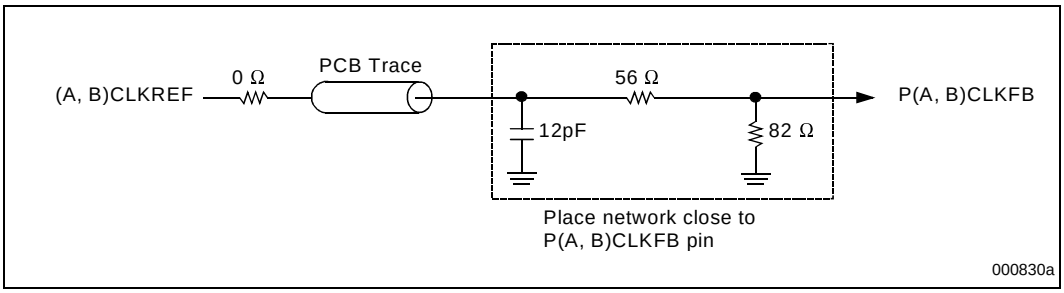
Table 7-9. WXB PCI Feedback Clock Specification

Driver	Min	Max	Unit	Notes
P(A,B)CLKFB delay skew after the earliest P(A,B)CLK[2:0] at the PCI component	0.50	1.0	ns	abc

a. This is a system controlled parameter that can be adjusted by the P(A,B)CLKFB loop and RC termination as shown in Figure 7-3
b. Probing P(A,B)CLKFB changes the RC attributes and results in unreliable timings, therefore the "Feedback Clock Specification" timings adjustment should be made with respect to the XCLK# rising edge input pin.
c. All system PCI timings measurements for the WXB should be made with respect to 'XCLK# - 500ps' at the WXB pin.

The WXB component PCI clock feedback loop must contain a filter network, typically within an inch of the P(A,B)CLKFB input signals. The total length of the loop should match the corresponding PCI clock length being matched, including both the motherboard and the expansion card lengths. Refer to "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)" for required clock length on expansion cards. Figure 7-3 shows the filter network.

Figure 7-3. WXB Component PCI Feedback Clock Termination



A series termination resistor near each PCI clock driver is also required. System measurements should be performed to determine the precise value in a particular system. Timing studies should be done on the feedback network to satisfy Table 7-9.

7.5 GXB – Graphics Subsystem Specification

For DC and AC specifications of the AGP interface, please refer the "Accelerated Graphics Port Interface Specification (http://www.intel.com/technology/agp/agp_index.htm)" located at http://www.agp.forum.

7.5.1 Voltage Reference

When the TYPEDET# signal on the GXB component is deasserted, or electrically high, a 3.3V V_{DDQ} is assumed to be present. The GXB component will then generate its own internal reference voltage as the reference for the receivers on the AGP interface.

When the TYPEDET# signal is asserted, or electrically low, a 1.5V V_{DDQ} is assumed to be present. The GXB component will then use the voltage driven on the VREFAGP[2:0] pins as the reference voltage for the receivers on the AGP interface.

7.5.2 Clock

To achieve proper timing, the GXB component's feedback clock, AGPCLKIN, must be closely matched in trace length to each AGPCLK total trace length. The AGPCLK total trace length includes the length from the GXB component to the connector plus the targeted length from the connector through the adapter card.

7.5.3 Graphics Subsystem AGP Interface Specification

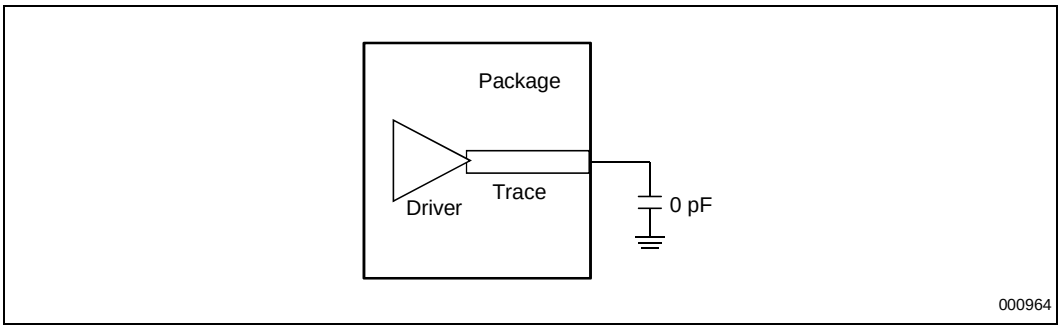
For DC and AC specifications of the AGP interface, please refer the "Accelerated Graphics Port Interface Specification (http://www.intel.com/technology/agp/agp_index.htm)".

7.5.4 Graphics Subsystem GART SRAM Interface Specification

All GART SRAM signals on the GXB are 3.3V CMOS. Please refer to Section 7.2 for DC specifications.

Table 7-10 in this section consists of the AC timing parameters for the GART SRAM interface. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 7-4.

Figure 7-4. GXB Component GART SRAM Rated Load for AC Timings



The system designer must find the specifications for the SRAM devices used in the system in order to calculate the timing margins.

Table 7-10. GXB Component GART SRAM AC Timings

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T36	SADDR[17:0]	0.60	2.43			
T31B	SCLK[2:0]	NA	NA			
T36	SDATA[31:0]	0.60	2.43	1.64	0.68	
T36	SGW#	0.60	2.43			
T36	SOE#	0.60	2.43			
T36	SSE3#	0.60	2.43			

Furthermore, to achieve proper timing, the GXB component's feedback clock, SCLKIN, must be closely matched in trace length to each SCLK trace from the GXB component to each GART SRAM. Table 7-11 shows the parameters necessary for clock skew determination with the GXB component.

Table 7-11. GXB Component GART SRAM Bus Clock Parameters

Driver	Value	Unit	Notes
Clock source jitter	150	ps	a
SRAM clock buffer pin to pin skew	200	ps	b
Feedback clock to source clock skew	280	ps	c

a. Jitter is specified at the pin for SCLK[2:0] and SCLKIN. Guaranteed by design.
b. Guaranteed by design.
c. Feedback clock to source clock skew is specified between the input pin of SCLKIN and the input pin of X0CLK#. Guaranteed by design.

7.6 Private Bus Specification

The private bus is the interface between the SAC and SDC components.

7.6.1 Private Bus DC Specification

The signals on the private bus are 1.8 V CMOS.

7.6.2 Private Bus AC Specification

The AC timing specification is guaranteed by placement of the SAC and SDC components. Table 7-12 provides the trace length specification for the private bus. In addition, the PCB must meet the physical requirements listed in the "Intel® Itanium™ Processor at 800 MHz and 733 MHz Datasheet (Document Number: 245481)".

Table 7-12. Private Bus AC Specification

Parameter	Min	Max	Unit	Notes
Private Bus Length	0.7	2.0	inch	a

a. Minimum of 1.78cm and a maximum of 5.08cm. Please follow the clock skew requirement found in the "*RS-Intel® Itanium™ Processor/Intel 460GX Platform Design Guide*".

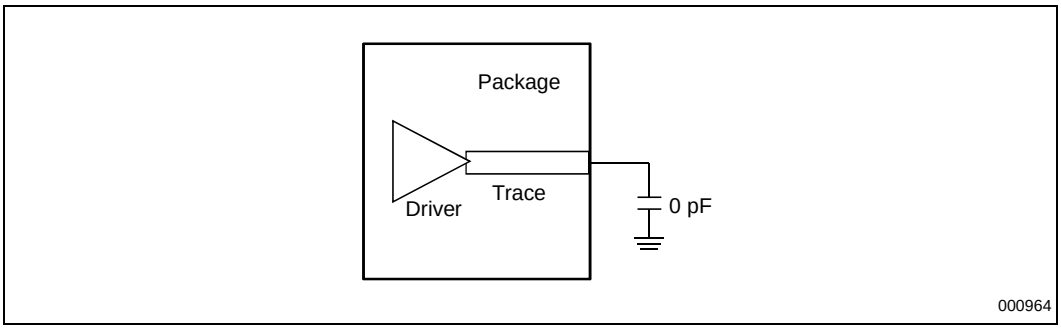
7.7 WXB – Integrated Hot-Plug Controller Interface

The WXB integrates a Hot-Plug controller for each PCI bus. Consult "Intel® 460GX Chipset System Software Developer's Manual (Document Number: 248704)" further hot-plug interface details.

The DC specification for the WXB Hot-Plug signals are PCI compliant. Refer "PCI Local Bus Specification, Rev 2.2 (http://www.pcisig.com/)" for the specific DC specifications.

Table 7-13 in this section consist of the AC timing parameters for the Integrated Hot-Plug Controller interface. All timings are specified in nanoseconds (ns) to the ball of the component at the rated load illustrated in Figure 7-5.

Figure 7-5. WXB Integrated Hot-Plug Controller Interface Rated Load for AC Timings



The system designer must find the specifications for the PCI devices used in the system in order to calculate the timing margins.

Table 7-13. WXB Integrated Hot-Plug Controller Interface AC Timings[a]

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T38	H(A,B)SIC	12.9	14.4			
T38	H(A,B)SID			6.4	2.4	
T38	H(A,B)SIL#	12.9	14.4	6.4	2.4	
T38	H(A,B)SOC	12.9	14.4	6.4	2.4	
T38	H(A,B)SOD	12.9	14.4			
T38	H(A,B)SOL	12.9	14.4	6.4	2.4	
T38	H(A,B)SOR#	12.9	14.4			
T38	H(A,B)SORR#	12.9	14.4			
T38	H(A,B)INTRQ#	12.9	14.4			

a. These times are guaranteed by design.

7.8 Test Access Port (TAP) Interface Specification

7.8.1 TAP Interface DC Specification

The TAP signal DC specifications are shown in Table 7-14.

Table 7-14. TAP DC Specifications [a]

Symbol	Parameter	SAC,SDC	WXB	MAC, MDC, GXB, PXBC	Units	Notes
V_{OL} Max	Driver Output Low Voltage	0.49	1.27	2.42	V	
V_{IH} Min	Receiver Input High Voltage	V_{REF}[b] + 0.2	1.52	2.31	V	
V_{IL} Max	Receiver Input Low Voltage	V_{REF}[b] - 0.2	1.06	0.68	V	
C_{IN}	Input Capacitance	10	10	10	pF	
C_O	Output Capacitance	10	10	10	pF	
$C_{I/O}$	I/O Capacitance	10	10	10	pF	
I_{Lo}	Output Leakage Current	50	50	50	µA	
I_{LI}	Input Leakage Current	50	50	50	µA	

a. These signals are tested to a 50 ohm pull-up.
b. V_{REF} is defined in Table 4-1.

The SAC and SDC TAP signals are AGTL+. The TAP signals on the MAC, MDC, PXB, WXB and GXB are LVTTL. They require a AGTL+ to LVTTL translation device in order to connect to the AGTL+ TAP loop.

7.8.2 TAP Interface AC Specification

The Intel 460GX chipset TAP clock must run with a minimum HCLKIN/HCLKIN# frequency to TCK frequency ratio of 12:1 or greater. Table 7-15 lists the AC specifications for the TAP interface.

Table 7-15. TAP Interface AC Specification

Symbol	Parameter	Min	Max	Units	Notes
t_{suRST}	TRST# setup			ns	a, b
t_{hldRST}	TRST# hold			ns	a, b
t_{suMS}	TMS setup	1.62		ns	c
t_{hldMS}	TMS hold		17.04	ns	c
t_{suDI}	TDI setup	1.62		ns	c
t_{hldDI}	TDI hold		17.04	ns	c
t_{DO}	TDO delay	0.60	11.93	ns	c, d
t_{DOD}	TDO on/off delay		25.0	ns	c, d

a. TRST# requires a pulse width of 40 ns.
b. This input is asynchronous. Therefore, there is no associated setup or hold time.
c. 3.3V tolerant signals on the MAC, MDC, PXB, GXB, WXB, and PID components. Inputs are referenced to TCK rising, outputs are referenced to TCK falling.
d. Min and Max timings are measured with 0pF load.

7.8.3 TAP Connections

Refer to the "Intel® Itanium™ Processor Hardware Developer's Manual (Document Number: 248701)" for an example of the TAP loop for the processor(s), SAC, and SDC.

All TAP connections are AGTL+, with the exception of the MAC, MDC, PXB, GXB and WXB. The MAC, MDC, PXB, Expand WXB use 3.3V level TAP I/O and require a AGTL+ to LVTTL translation device in order to connect to the AGTL+ TAP loop. AGTL+ to LVTTL translation can be accomplished using an SN74GTL16612 or equivalent device.

To ensure "JTAG IEEE 1149.1 Specification (http://www.ieee.com)" compliance, the TAP Controller will only be reset by a TRST# assertion or a TMS assertion for 5 TCK periods. If the user does not intend to test the PWRGD connection via boundary scan, it is advisable to tie TRST# to the PWRGD signal such that the TAP Controller will be reset whenever power is not good. If the user does intend to test the PWRGD connection via boundary scan, the user should not connect TRST# to PWRGD. If the user were to connect these signals, it would result in the TAP Controller resetting when PWRGD is forced to its inactive state under conditions such as an EXTEST or CLAMP command. In order to ensure system reliability, if TRST# is not connected to PWRGD, TRST# must be held asserted during initial power up by some other means. On systems where the JTAG logic will not be used, TRST# should always be pulled down to its asserted state.

When testing PWRGD via boundary scan, if PWRGD = 0, the boundary scan commands EXTEST and CLAMP will not be functional. All other boundary scan commands will be functional, so the user can use Sample/Preload to capture the value on the pin and shift out the data.

The 3.3V TAP TDO outputs on the MAC, MDC, PXB, GXB, WXB, and PID are not slew rate compensated and may require an external series termination resistor to limit signal overshoot on the electrical High to electrical Low transition.

7.9 System Management Bus (SMBus) Interface Specification

The SMBus signals meet the AC specifications required by standard-mode I^2C interfaces. Figure 7-6 shows an example of the various connections of the Intel 460GX chipset SMBuses. It should be noted that the way each SMBus is connected and used is largely system dependent. The Microcontroller shown in Figure 7-6 is a generic controller capable of operating an I^2C interface.

Please refer to Table 7-16, Table 7-17 and Table 7-18 for the SMBus interface DC specifications for each applicable Intel 460GX chipset component.

Table 7-16. Electrical Specifications for the 1.8V SMBus Interface on the SAC Component

Symbol	Parameter	Minimum	Maximum	Unit	Notes
$V_{DD\ 18}$	1.8 V Bus Termination Voltage	1.60	2.00	V	
V_{OL}	Driver Output Low Voltage		1.18	V	a
V_{IH}	Receiver Input High Voltage	0.8 $V_{DD\ 18}$		V	
V_{IL}	Receiver Input Low Voltage		0.6 $V_{DD\ 18}$	V	
T_{RISE}	Driver Output Rise Time	1.7	300.0	ns	b
T_{FALL}	Driver Output Fall Time	0.8	60.0	ns	c

a. V_{OL} is specified with a current of 3mA.
b. Output values are specified under worst case voltage, temperature, and process conditions, with an external 450Ω pull-up resistor and a capacitive load ranging from 5pF to 400pF.

Table 7-17. Electrical Specifications for the 1.8 V SMBus Interface on the MAC and MDC Components

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{DD18}	1.8V Bus Termination Voltage	1.60	2.00	V	
V_{OL}	Driver Output Low Voltage		0.4	V	a
V_{IH}	Receiver Input High Voltage	0.7 V_{DD18}		V	
V_{IL}	Receiver Input Low Voltage		0.3 V_{DD18}	V	
T_{RISE}	Driver Output Rise Time	1.7	220.0	ns	b
T_{FALL}	Driver Output Fall Time	4.2	106.0	ns	b

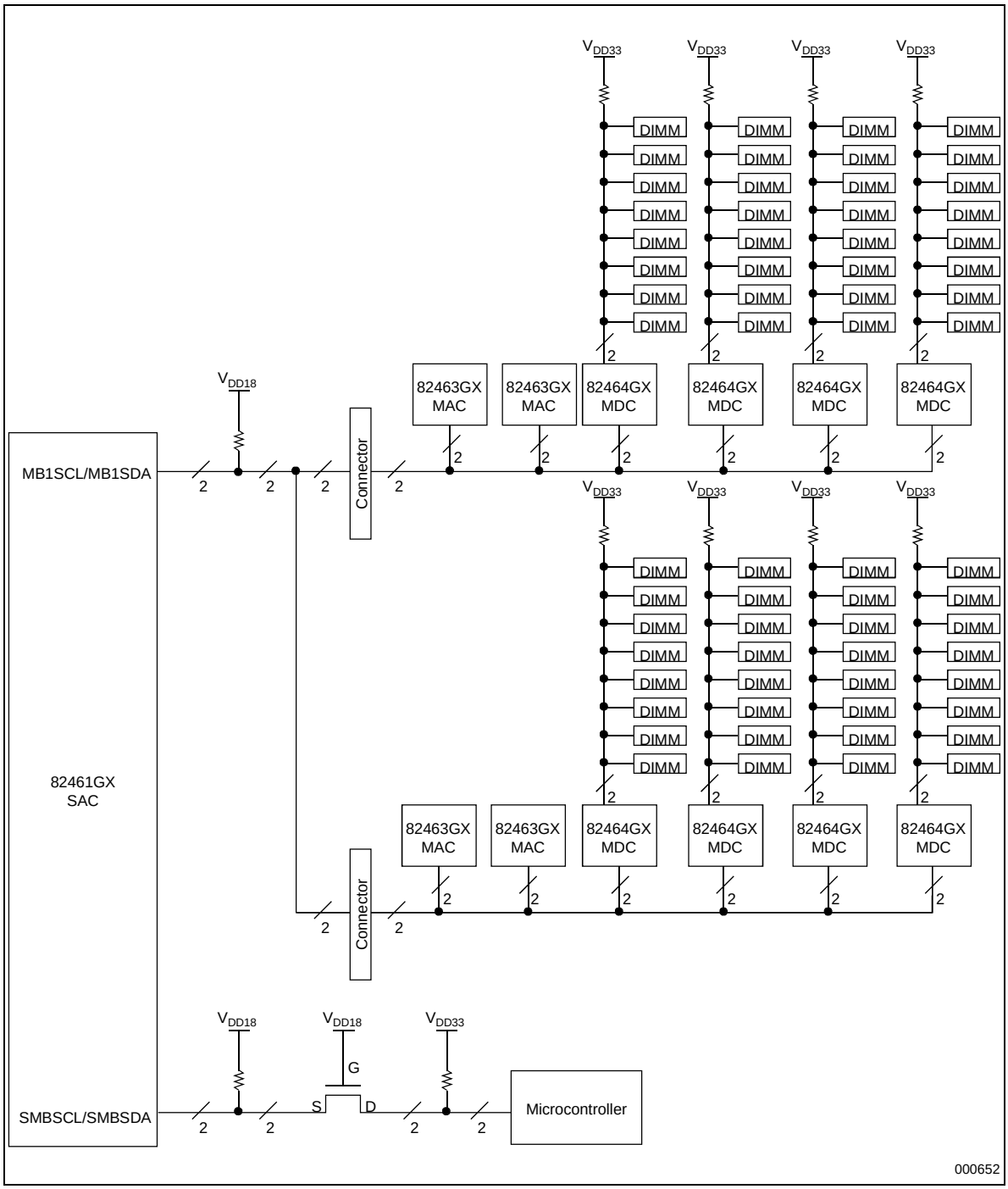
a. V_{OL} is specified assuming a current of 3mA.
b. Output values are specified under worst case voltage, temperature, and process conditions, with an external 450Ω pull-up resistor and a capacitive load ranging from 5pF to 400pF.

Table 7-18. Electrical Specifications for the 3.3 V SMBus Interface on the MDC Component

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{DD33}	1.8V Bus Termination Voltage	3.00	3.60	V	
V_{OL}	Driver Output Low Voltage		0.4	V	a
V_{IH}	Receiver Input High Voltage	0.7 $V_{DD\ 33}$		V	
V_{IL}	Receiver Input Low Voltage		0.3 $V_{DD\ 33}$	V	
T_{RISE}	Driver Output Rise Time	2.9	460.0	ns	b
T_{FALL}	Driver Output Fall Time	4.7	124.0	ns	b

a. V_{OL} is specified assuming a current of 3mA.
b. Output values are specified under worst case voltage, temperature, and process conditions, with an external 900Ω pull-up resistor and a capacitive load ranging from 5pF to 400pF.

Figure 7-6. Example of Intel® 460GX Chipset SMBus Connections



7.10 Other Signals

The signals listed in Table 7-19 meet the DC specifications given by a JEDEC standard or another document.

Table 7-19. DC Specifications for Other Signals

Component	Signals	Reference
SAC	INTREQ#, CRESET	JEDEC *JESD8-7* standard.
SAC	XSERR#, EXRESET#	$V_{IL} = V_{REF} - 0.2$, $V_{IH} = V_{REF} + 0.2$
SAC	PWRGD	$V_{IL} = 0.05*V_{CC}$, $V_{OH} = 0.95*V_{CC}$
SDC	PWRGD	$V_{IL} = 0.05*V_{CC}$, $V_{OH} = 0.95*V_{CC}$
SDC	SDCRST#	JEDEC *JESD8-7* standard
GXB	XBINIT#	JEDEC *JESD8-A* standard
GXB	PWRGD	$V_{IL} = 0.10*V_{CC}$, $V_{OH} = 0.90*V_{CC}$
MDC	PWRGD	$V_{IL} = 0.09*V_{CC}$, $V_{OH} = 0.92*V_{CC}$
MAC	PWRGD	$V_{IL} = 0.09*V_{CC}$, $V_{OH} = 0.92*V_{CC}$
PXB	PWRGD	$V_{IL} = 0.20*V_{CC}$, $V_{OH} = 0.70*V_{CC}$
WXB	PWRGD	$V_{IL} = 0.05*V_{CC}$, $V_{OH} = 0.95*V_{CC}$

The signals listed in Table 7-20 through Table 7-24 show the AC specifications for these signals.

Table 7-20. SAC Component Common Clock AC Specification Timings

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T3	RESET#	-0.04	3.26			a
T14	XBINIT			1.77	c	d
T12	SDCRST#	-0.43	1.60			
T13	CRESET#	-0.44	1.46			b
T12	XSERR#			c	c	d
T13	INTREQ#	-0.44	1.46			
T29	PWRGD			c	c	e

a. Measured into rated load of 20 ohms into Vct.
b. Measured into rated load of 50 ohms into Vct.
c. This pin is asynchronous.
d. This pin must have a pulse width of five clock cycles.
e. Must be active for a minimum of eight clock cycles and inactive for eight clock cycles before going active.

Table 7-21. MAC Component AC Specification Timings

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T24	RESET	-0.03	3.23			

Table 7-22. PXB Component AC Specification Timings

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T11_a	XBINIT#	0.61	1.69			

Table 7-23. GXB Component AC Specification Timings

Symbol	Parameter	$T_{co,min}$	$T_{co,max}$	T_{su_clk}	T_{hd_clk}	Notes
T14B	XBINIT#	0.03	2.31			
T37	XINTR#	-0.16	2.07			

Table 7-24. WXB Component AC Specification Timings

Symbol	Parameter	T_{VAS}	T_{VBS}	T_{su_clk}	T_{hd_clk}	Notes
T14A	XBINIT#	0.87	1.15			

Thermal Specifications 8

To ensure functionality and reliability, the Intel 460GX chipset is specified for proper operation when the case temperature T_C is within the specified range shown in Table 8-1. Table 8-2 shows the target maximum power dissipation and thermal coefficients for each Intel 460GX chipset component.

Table 8-1. Intel® 460GX Chipset Component Operating Case Temperature

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Operating case temperature	0	85	°C	a

a. For the SAC, SDC, and WXB components using an OLGA1 package, the die temperature should not exceed 105°C.

Table 8-2. Intel® 460GX Chipset Component Thermal Specifications

Component	Package	Max Power (W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Notes
SAC	567 OLGA1	7.2	a	NA	b
SDC	567 OLGA1	3.8	a	NA	b
MAC	324 BGA	5.5	22.5	2.03	c
MDC	324 BGA	7.9	22.5	2.03	c
PXB	540 PLGA	9.3	11	0.9	d
GXB	540 PLGA	11.3	11	0.9	d
WXB	567 OLGA1	9.8	a	NA	b

a. Please refer to the "Intel® 82460GX Chipset OLGA1 Package, Manufacturing, Mechanical, and Thermal Design Guide".
b. θ_{JC} cannot be specified for an OLGA1 component as the die on the substrate is exposed.
c. θ_{JA} is indicated at 0 LFM airflow. θ_{JA} would be reduced by 10% at 100 LFM airflow.
d. θ_{JA} and θ_{JC} are indicated at 0 LFM airflow. θ_{JA} would be reduced by 12% at 200 LFM airflow.

Ball-out Specifications 9

9.1 Ball-out Lists

Table 9-1 through Table 9-7 list the respective ball-outs for each Intel 460GX chipset component. Ball-out Specifications for the PID and IFB are found in Chapter 12 and Chapter 11 respectively. See Chapter 1 for locating information on the FWH.

All ball locations marked “NC” or “N/C” are no-connects. All ball locations marked “RSVD” are reserved. Both of these ball location types must remain unconnected. This restriction forbids any chipset connection, including floating conductors, to be attached.

All ball locations marked “VCC (RSVD)” or “VSS (RSVD)” should be connected to VCC or VSS as indicated. However, these ball locations should not be considered power or ground supplies.

All ball locations marked “P/U” or “P/D” should be pulled-up to the core VCC or pulled-down to VSS through the specified resistor value.

Table 9-1. SAC Ball List

Ball Number	Signal
A01	N/C
A02	X0RST#
A03	VSS
A04	X0D[15]#
A05	VSS
A06	X0HSTBN#
A07	X1BE[1]#
A08	X1BE[0]#
A09	X1RST#
A10	X1RSTFB#
A11	N/C
A12	N/C
A13	X1HSTBN#
A14	X2BE[1]#
A15	X2BE[0]#
A16	X2RST#
A17	X2RSTFB#
A18	X2D[15]#
A19	X2HSTBN#
A20	X2HSTBP#
A21	X3BE[1]#
A22	VSS
A23	X3RSTFB#
A24	X3HSTBN#
B01	X0BE[1]#
B02	X0BE[0]#
B03	X0PAR#
B04	X0RSTFB#
B05	X0D[12]#
B06	VSS
B07	X0HSTBP#
B08	VCTF16
B09	X1D[11]#
B10	VSS
B11	X1D[2]#
B12	VCTF16
B13	X1HSTBP#
B14	VSS

Ball Number	Signal
B15	X2D[4]#
B16	VCTF16
B17	X2D[12]#
B18	VSS
B19	X2D[7]#
B20	VCTF16
B21	X3BE[0]#
B22	X3RST#
B23	X3D[15]#
B24	X3HSTBP#
C01	X3CLKFB
C02	X3CLKB
C03	VCTF16
C04	X0D[13]#
C05	VSS
C06	X0D[11]#
C07	X1RSTB#
C08	X1D[4]#
C09	X1D[9]#
C10	X1D[12]#
C11	X1D[1]#
C12	X1D[15]#
C13	X2RSTB#
C14	X2PAR#
C15	VREFF16[2]
C16	X2D[9]#
C17	X2D[11]#
C18	X2D[2]#
C19	X3D[14]#
C20	X3PAR#
C21	X3D[4]#
C22	X3D[13]#
C23	VSS
C24	VCC (RSVD)
D01	X3CLK
D02	VSS
D03	X0ADS#
D04	X0D[10]#

Table 9-1. SAC Ball List (Continued)

Ball Number	Signal
D05	X0XSTBN#
D06	X0XSTBP#
D07	X0HRTS#
D08	VSS
D09	X1PAR#
D10	X1D[13]#
D11	VSS
D12	X1D[6]#
D13	VCTF16
D14	X2D[8]#
D15	VSS
D16	X2HRTS#
D17	VSS
D18	VREFOUT[1]
D19	VCTF16
D20	VREFF16[3]
D21	VSS
D22	X3D[7]#
D23	P/U 100Ω
D24	MB1SCL
E01	X2CLKFB
E02	X2CLKB
E03	VSS
E04	X0BLK#
E05	X0XRTS#
E06	VCTF16
E07	X0D[9]#
E08	X0D[7]#
E09	X1D[14]#
E10	X1D[10]#
E11	X1XSTBN#
E12	X1D[0]#
E13	X2D[14]#
E14	X2XSTBN#
E15	X2XSTBP#
E16	X3RSTB#
E17	X3ADS#
E18	X3XSTBN#
E19	X3XSTBP#

Ball Number	Signal
E20	X3D[9]#
E21	X3D[2]#
E22	VCTF16
E23	INTREQ#
E24	VSS
F01	X1CLKFB
F02	VSS
F03	X2CLK
F04	VSS
F05	X0D[14]#
F06	F16CRES[0]
F07	X0D[1]#
F08	VSS
F09	VREFOUT[0]
F10	VCTF16
F11	X1XSTBP#
F12	VSS
F13	X2ADS#
F14	VCTF16
F15	X2D[0]#
F16	VSS
F17	X3D[5]#
F18	VCTF16
F19	X3D[12]#
F20	X3HRTS#
F21	X3D[0]#
F22	VSS
F23	MEMRST[0]#
F24	XSERR#
G01	IMPCNTL#
G02	X1CLK
G03	X1CLKB
G04	X0CLK
G05	VSS
G06	X0RSTB#
G07	X0D[8]#
G08	X0D[4]#
G09	X0D[0]#
G10	X1ADS#

Table 9-1. SAC Ball List (Continued)

Ball Number	Signal
G11	VREFF16[1]
G12	X1D[7]#
G13	X2BLK#
G14	X2D[1]#
G15	X2D[6]#
G16	X3XRTS#
G17	X3D[8]#
G18	X3D[1]#
G19	F16CRES[1]
G20	VSS
G21	XBINIT#
G22	CRESET#
G23	SMBSDA
G24	ROWB[2]#
H01	AP[0]#
H02	VSS
H03	VREFFSB[0]
H04	VSS
H05	X0CLKFB
H06	PWRGD
H07	X0D[5]#
H08	X0D[3]#
H09	VSS
H10	X0D[2]#
H11	VCTF16
H12	X1HRTS#
H13	VSS
H14	X2D[13]#
H15	VSS
H16	X3D[10]#
H17	VSS
H18	X3D[6]#
H19	VCTF16
H20	P/U 10KΩ
H21	SMBSCL
H22	MB1SDA
H23	VSS
H24	ROWB[1]#
J01	A[4]#

Ball Number	Signal
J02	A[3]#
J03	VSS
J04	AP[1]#
J05	X0CLKB
J06	HCLKIN#
J07	VSSA
J08	VCCA[1]
J09	VCCA[2]
J10	VREFF16[0]
J11	X1BLK#
J12	X1D[3]#
J13	X1D[8]#
J14	X2D]5]#
J15	X2D[3]#
J16	VCTF16
J17	X3D[11]#
J18	P/U 100Ω
J19	EXRESET#
J20	CHLNSZ#
J21	VSS
J22	MAB[16]#
J23	MAB[15]#
J24	ROWB[0]#
K01	A[8]#
K02	VSS
K03	A[7]#
K04	VSS
K05	A[6]#
K06	N/C
K07	HCLKIN
K08	VCCA[0]
K09	VCCA[3]
K10	VCCA[4]
K11	X0D[6]#
K12	X1XRTS#
K13	X1D[5]#
K14	X2XRTS#
K15	X2D[10]#
K16	X3BLK#

Table 9-1. SAC Ball List (Continued)

Ball Number	Signal
K17	VSS
K18	SDCRST#
K19	MEMRST[1]#
K20	MAB[14]#
K21	MAB[13]#
K22	MAB[12]#
K23	PARB#
K24	VSS
L01	A[13]#
L02	A[12]#
L03	A[11]#
L04	A[10]#
L05	VSS
L06	A[9]#
L07	VCC (RSVD)
L08	VCC
L09	VSS
L10	VCC
L11	VSS
L12	VCC
L13	VSS
L14	VCC
L15	VSS
L16	X3D[3]#
L17	MAB[11]#
L18	MAB[10]#
L19	MAB[9]#
L20	VSS
L21	MAB[8]#
L22	VSS
L23	LCMPLTB#
L24	RCMPLTB#
M01	N/C
M02	VSS
M03	A[15]#
M04	VSS
M05	A[14]#
M06	A[5]#
M07	VCTFSB

Ball Number	Signal
M08	VCTFSB
M09	VCC
M10	VSS
M11	VCC
M12	VSS
M13	VCC
M14	VSS
M15	VCC
M16	SMPCRES
M17	MAB[7]#
M18	MAB[6]#
M19	MAB[5]#
M20	VCC
M21	VREFM[0]
M22	MAB[4]#
M23	CMNDB[1]#
M24	N/C
N01	N/C
N02	A[19]#
N03	VSS
N04	A[18]#
N05	A[17]#
N06	A[16]#
N07	VCTFSB
N08	VCC
N09	VSS
N10	VCC
N11	VSS
N12	VCC
N13	VSS
N14	VCC
N15	VSS
N16	MAA[4]#
N17	MAA[10]#
N18	VSS
N19	MAB[3]#
N20	MAB[2]#
N21	MAB[1]#
N22	MAB[0]#

Table 9-1. SAC Ball List (Continued)

Ball Number	Signal
N23	VCC
N24	N/C
P01	A[23]#
P02	VSS
P03	A[22]#
P04	VSS
P05	A[21]#
P06	A[20]#
P07	VCTFSB
P08	VSS
P09	VCC
P10	VSS
P11	VCC
P12	VSS
P13	VCC
P14	VSS
P15	VCC
P16	MAA[0]#
P17	MAA[6]#
P18	LCMPLTA#
P19	MAA[13]#
P20	MAA[16]#
P21	VSS
P22	MAA[14]#
P23	CMNDB[0]#
P24	ERRB#
R01	A[28]#
R02	A[27]#
R03	A[26]#
R04	A[25]#
R05	VSS
R06	A[24]#
R07	VREFFSB[1]
R08	TRST#
R09	TDI
R10	TMS
R11	PITID[0]#
R12	PITID[1]#
R13	VSS

Ball Number	Signal
R14	VCC
R15	PVD[9]#
R16	PVD[10]#
R17	MAA[3]#
R18	MAA[2]#
R19	VCC
R20	MAA[12]#
R21	MAA[9]#
R22	MAA[15]#
R23	ROWA[2]#
R24	VSS
T01	A[31]#
T02	VSS
T03	A[30]#
T04	VSS
T05	A[29]#
T06	BNR#
T07	VCTFSB
T08	VSS
T09	VCC
T10	RITID[3]#
T11	PITID[2]#
T12	VCC
T13	PVD[4]#
T14	VSS
T15	PVD[8]#
T16	PVD[11]#
T17	VSS
T18	PVD[13]#
T19	MAA[1]#
T20	VREFM[1]
T21	MAA[8]#
T22	VCC
T23	ROWA[0]#
T24	ROWA[1]#
U01	A[35]#
U02	A[34]#
U03	VSS
U04	A[33]#

Table 9-1. SAC Ball List (Continued)

Ball Number	Signal
U05	A[32]#
U06	REQ[0]#
U07	VCTFSB
U08	TCK
U09	PCMD[12]#
U10	VSS
U11	RITID[4]#
U12	PITID[3]#
U13	PITID[5]#
U14	PVD[6]#
U15	VCC
U16	PVD[14]#
U17	PVD[18]#
U18	PVDP[1]#
U19	RESERVED[0]
U20	VSS
U21	MAA[11]#
U22	MAA[5]#
U23	RCMPLTA#
U24	PARA#
V01	BR[3]#
V02	VSS
V03	HIT#
V04	VSS
V05	HITM#
V06	VCTFSB
V07	VREFFSB[2]
V08	VCC
V09	PCMD[10]#
V10	RITID[1]#
V11	RITID[2]#
V12	VREFPVB[0]
V13	VSS
V14	PITIDP#
V15	PVD[12]#
V16	PVD[21]#
V17	PVD[23]#
V18	VCC
V19	PVD[29]#

Ball Number	Signal
V20	PVDV#
V21	RESERVED[1]
V22	MAA[7]#
V23	VSS
V24	CMNDA[1]#
W01	RP#
W02	BR[0]#
W03	BR[1]#
W04	BR[2]#
W05	VREFFSB[3]
W06	VSS
W07	TDO
W08	PCMD[0]#
W09	PCMDP#
W10	RITID[0]#
W11	VCC
W12	RITID[5]#
W13	PITIDV#
W14	PVD[7]#
W15	PVD[16]#
W16	VSS
W17	PVD[19]#
W18	PVD[22]#
W19	PVD[27]#
W20	PVD[34]#
W21	VCC
W22	PVD[38]#
W23	CMNDA[0]#
W24	ERRA#
Y01	BINIT#
Y02	VSS
Y03	INIT#
Y04	REQ[3]#
Y05	SWRCNTL#
Y06	BP[0]#
Y07	BP[3]#
Y08	PCMD[1]#
Y09	VSS
Y10	PCMD[7]#

Table 9-1. SAC Ball List (Continued)

Ball Number	Signal
Y11	PCMD[13]#
Y12	RITIDP#
Y13	PVD[1]#
Y14	VCC
Y15	PVD[17]#
Y16	PVD[26]#
Y17	PVD[24]#
Y18	PVD[36]#
Y19	VSS
Y20	PVD[35]#
Y21	PVD[25]#
Y22	PVD[33]#
Y23	PVBCRES1
Y24	VCC
AA01	RESET#
AA02	REQ[4]#
AA03	VSS
AA04	REQ[2]#
AA05	VSS
AA06	BP[1]#
AA07	VCC
AA08	PCMD[9]#
AA09	PCMD[5]#
AA10	PCMD[8]#
AA11	PCMD[3]#
AA12	VSS
AA13	PVD[0]#
AA14	PVD[3]#
AA15	PVD[20]#
AA16	PVD[28]#
AA17	VCC
AA18	PVD[32]#
AA19	PVD[31]#
AA20	PVD[52]#
AA21	PVD[41]#
AA22	VSS
AA23	PVD[37]#
AA24	PVD[42]#
AB01	DEFER#

Ball Number	Signal
AB02	VSS
AB03	LOCK#
AB04	BP[4]#
AB05	VCC
AB06	BP[2]#
AB07	PVBCRES0
AB08	PCMD[11]#
AB09	PCMD[16]#
AB10	VCC
AB11	PCMD[14]#
AB12	PITID[4]#
AB13	PVD[15]#
AB14	PVD[2]#
AB15	VSS
AB16	PVDP[2]#
AB17	PVD[39]#
AB18	PVD[47]#
AB19	VREFPVB[1]
AB20	VCC
AB21	PVD[45]#
AB22	PVD[44]#
AB23	PVD[40]#
AB24	PVDP[3]#
AC01	BERR#
AC02	REQ[1]#
AC03	BP[5]#
AC04	VSS
AC05	PCMD[4]#
AC06	PCMD[15]#
AC07	PVGNT#
AC08	VSS
AC09	SDCRS[1]#
AC10	SDCRS[3]#
AC11	PVD[5]#
AC12	PVD[54]#
AC13	VCC
AC14	PVDP[0]#
AC15	PVD[30]#
AC16	PVD[53]#

Table 9-1. SAC Ball List (Continued)

Ball Number	Signal
AC17	PVD[43]#
AC18	VSS
AC19	PVD[58]#
AC20	PVD[48]#
AC21	PVD[60]#
AC22	PVD[56]#
AC23	VCC
AC24	PVD[51]#
AD01	ADS#
AD02	BPRI#
AD03	VSS
AD04	PCMD[6]#
AD05	PVREQ#
AD06	VCC
AD07	SDCRS[2]#
AD08	TOQE#

Ball Number	Signal
AD09	SDCRS[0]#
AD10	PCMD[2]#
AD11	VSS
AD12	N/C
AD13	N/C
AD14	PVD[61]#
AD15	PVD[59]#
AD16	VCC
AD17	PVD[55]#
AD18	PVD[63]#
AD19	PVD[57]#
AD20	PVD[46]#
AD21	VSS
AD22	PVD[62]#
AD23	PVD[50]#
AD24	PVD[49]#

Table 9-2. SDC Ball List

Ball Number	Signal
A01	N/C
A02	ID[5]#
A03	VSS
A04	PCMD[1]#
A05	VSS
A06	PCMD[9]#
A07	PCMD[11]#
A08	PCMD[12]#
A09	RITID[3]#
A10	PITID[0]#
A11	N/C
A12	N/C
A13	PVD[6]#
A14	PVD[9]#
A15	PVD[10]#
A16	PVD[18]#
A17	PVD[13]#
A18	PVD[29]#
A19	PVDV#
A20	PVD[25]#
A21	PVD[33]#
A22	PVD[38]#
A23	PVD[37]#
A24	PVD[42]#
B01	ID[2]#
B02	ID[6]#
B03	PCMD[0]#
B04	VCC
B05	PCMD[4]#
B06	VSS
B07	PCMD[15]#
B08	VCC
B09	RITID[1]#
B10	VSS
B11	PITID[1]#
B12	VCC
B13	PITIDP#
B14	VSS

Ball Number	Signal
B15	PVD[11]#
B16	VCC
B17	PVDP[1]#
B18	VSS
B19	PVD[34]#
B20	VCC
B21	PVD[44]#
B22	VSS
B23	PVD[40]#
B24	PVDP[3]#
C01	DBSY#
C02	SBSY#
C03	VREF[4]
C04	ID[0]#
C05	VSS
C06	PVGNT#
C07	PCMD[6]#
C08	PCMD[10]#
C09	RITID[0]#
C10	PITID[2]#
C11	PITID[3]#
C12	PVD[4]#
C13	PVD[7]#
C14	PVD[8]#
C15	PVD[14]#
C16	PVD[23]#
C17	PVD[22]#
C18	PVD[27]#
C19	PVD[35]#
C20	PVD[41]#
C21	PVD[56]#
C22	CRESM0
C23	PVD[50]#
C24	PVD[51]#
D01	RS[1]#
D02	VSS
D03	RSP#
D04	VSS

Table 9-2. SDC Ball List (Continued)

Ball Number	Signal
D05	VCC
D06	PVREQ#
D07	VSS
D08	PCMDP#
D09	VCC
D10	RITID[4]#
D11	VSS
D12	PITID[5]#
D13	VCC
D14	PVD[12]#
D15	VSS
D16	PVD[19]#
D17	VCC
D18	PVD[31]#
D19	VSS
D20	PVD[45]#
D21	VCC
D22	PVD[62]#
D23	VSS
D24	PVD[49]#
E01	D[48]#
E02	RS[0]#
E03	VSS
E04	DRDY#
E05	IDS#
E06	SDCRS[2]#
E07	TOQE#
E08	PCMD[5]#
E09	PCMD[7]#
E10	RITID[2]#
E11	PVREF[0]
E12	PITIDV#
E13	PVD[3]#
E14	PVD[16]#
E15	PVD[21]#
E16	PVD[24]#
E17	PVD[36]#
E18	PVREF[1]
E19	PVD[52]#

Ball Number	Signal
E20	PVD[48]#
E21	PVD[60]#
E22	MDA[58]#
E23	MDA[62]#
E24	MVREFA[1]
F01	D[49]#
F02	VSS
F03	D[50]#
F04	VSS
F05	ID[1]#
F06	VCC
F07	SDCRS[0]#
F08	VSS
F09	PCMD[8]#
F10	VCC
F11	RITID[5]#
F12	VSS
F13	PVD[2]#
F14	VCC
F15	PVD[26]#
F16	VSS
F17	PVD[32]#
F18	VCC
F19	PVD[46]#
F20	VSS
F21	MDA[60]#
F22	VCC
F23	MDA[59]#
F24	MDA[64]#
G01	D[52]#
G02	D[53]#
G03	D[54]#
G04	D[51]#
G05	VSS
G06	RS[2]#
G07	ID[3]#
G08	SDCRS[1]#
G09	SDCRS[3]#
G10	PCMD[13]#

Table 9-2. SDC Ball List (Continued)

Ball Number	Signal
G11	RITIDP#
G12	PVD[1]#
G13	PVDP[0]#
G14	PVD[17]#
G15	PVD[28]#
G16	PVD[39]#
G17	PVD[47]#
G18	PVD[57]#
G19	PVD[58]#
G20	MDASN[3]#
G21	MDA[66]#
G22	MDA[61]#
G23	MDA[67]#
G24	MDA[65]#
H01	D[55]#
H02	VSS
H03	STBP[3]#
H04	VSS
H05	DEP[6]#
H06	TRDY#
H07	VCT
H08	ID[4]#
H09	VSS
H10	PCMD[3]#
H11	VCC
H12	PVD[0]#
H13	VSS
H14	PVD[20]#
H15	VCC
H16	PVD[43]#
H17	VSS
H18	PVD[63]#
H19	VCC
H20	MDASP[3]#
H21	VSS
H22	MDA[68]#
H23	VCC
H24	MDA[56]#
J01	DEP[7]#

Ball Number	Signal
J02	STBN[3]#
J03	VSS
J04	D[58]#
J05	D[56]#
J06	VCT
J07	VCT
J08	D[59]#
J09	PCMD[16]#
J10	PCMD[2]#
J11	PCMD[14]#
J12	PITID[4]#
J13	PVD[15]#
J14	PVD[30]#
J15	PVDP[2]#
J16	PVD[53]#
J17	PVD[55]#
J18	MDA[63]#
J19	MDA[57]#
J20	MDA[52]#
J21	MDA[71]#
J22	MDA[53]#
J23	MDA[50]#
J24	MDA[48]#
K01	D[35]#
K02	VSS
K03	D[57]#
K04	VSS
K05	D[61]#
K06	D[62]#
K07	VREF[3]
K08	D[60]#
K09	VCC
K10	VSS
K11	PVD[5]#
K12	VSS
K13	PVD[54]#
K14	PVD[61]#
K15	PVD[59]#
K16	VCC

Table 9-2. SDC Ball List (Continued)

Ball Number	Signal
K17	MDA[69]#
K18	VSS
K19	MDASP[2]#
K20	VCC
K21	MDA[70]#
K22	VSS
K23	MDA[47]#
K24	MDA[46]#
L01	D[39]#
L02	D[38]#
L03	DEP[4]#
L04	DEP[5]#
L05	VSS
L06	D[36]#
L07	D[63]#
L08	VCC
L09	VSS
L10	VCC
L11	VSS
L12	VCC
L13	VSS
L14	VCC
L15	MDA[55]#
L16	MDA[54]#
L17	VSS
L18	MDA[42]#
L19	MDASN[2]#
L20	MDA[45]#
L21	VSS
L22	MDA[49]#
L23	MDA[44]#
L24	MDA[18]#
M01	N/C
M02	VSS
M03	STBP[2]#
M04	VSS
M05	STBN[2]#
M06	D[37]#
M07	D[32]#

Ball Number	Signal
M08	VSS
M09	VCC
M10	VSS
M11	VCC
M12	VSS
M13	VCC
M14	VSS
M15	MDA[51]#
M16	MDA[38]#
M17	MDA[43]#
M18	MDA[41]#
M19	VCC
M20	MDA[40]#
M21	MDA[20]#
M22	VCC
M23	MDA[39]#
M24	N/C
N01	N/C
N02	D[40]#
N03	VSS
N04	D[34]#
N05	VREF[2]
N06	VCT
N07	VCT
N08	VCC
N09	VSS
N10	VCC
N11	VSS
N12	VCC
N13	VSS
N14	VCC
N15	MDA[29]#
N16	MDA[36]#
N17	MDA[26]#
N18	MDA[30]#
N19	VCC
N20	MDA[19]#
N21	MDASN[1]#
N22	MDA[37]#

Table 9-2. SDC Ball List (Continued)

Ball Number	Signal
N23	MDA[33]#
N24	N/C
P01	D[43]#
P02	VSS
P03	D[42]#
P04	VSS
P05	D[33]#
P06	D[29]#
P07	D[28]#
P08	VSS
P09	VCC
P10	VSS
P11	VCC
P12	VSS
P13	VCC
P14	VSS
P15	MDA[28]#
P16	MDA[5]#
P17	VSS
P18	MDA[31]#
P19	MDA[24]#
P20	MDASP[1]#
P21	VSS
P22	MDA[23]#
P23	MDA[25]#
P24	MDA[34]#
R01	D[44]#
R02	D[45]#
R03	D[47]#
R04	D[41]#
R05	VSS
R06	D[26]#
R07	D[31]#
R08	VCC (RSVD)
R09	VSS
R10	CHLNSZ#
R11	VCC (RSVD)
R12	MDB[0]#
R13	MDB[44]#

Ball Number	Signal
R14	MVREFB[1]
R15	MDB[62]#
R16	VSS
R17	MDA[3]#
R18	VCC
R19	MDA[10]#
R20	VSS
R21	MDA[21]#
R22	VCC
R23	MDA[0]#
R24	MDA[35]#
T01	D[46]#
T02	VSS
T03	D[24]#
T04	VSS
T05	STBN[1]#
T06	STBP[1]#
T07	D[30]#
T08	D[1]#
T09	VCCA
T10	PWRGD
T11	MDB[2]#
T12	MDB[35]#
T13	MDB[28]#
T14	MDB[46]#
T15	MDB[57]#
T16	FWMDB#
T17	MDA[13]#
T18	FWSLA#
T19	MDA[11]#
T20	MDASP[0]#
T21	MDA[27]#
T22	MDA[32]#
T23	MDA[22]#
T24	MDA[1]#
U01	DEP[3]#
U02	D[25]#
U03	VSS
U04	D[27]#

Table 9-2. SDC Ball List (Continued)

Ball Number	Signal
U05	VREF[1]
U06	VCT
U07	VCT
U08	VSS
U09	VCC
U10	VSSA
U11	VCC
U12	MDB[30]#
U13	VSS
U14	MDB[45]#
U15	VCC
U16	MDB[63]#
U17	VSS
U18	MDB[64]#
U19	VCC
U20	MDASN[0]#
U21	VSS
U22	MDA[8]#
U23	VCC
U24	MDA[2]#
V01	DEP[2]#
V02	VSS
V03	D[23]#
V04	VSS
V05	STBN[0]#
V06	STBP[0]#
V07	VCT
V08	TRST#
V09	DRATE#
V10	MDB[5]#
V11	MDB[15]#
V12	MDB[29]#
V13	MDB[26]#
V14	MDB[27]#
V15	MDB[36]#
V16	MDB[49]#
V17	MDB[60]#
V18	FWSLB#
V19	MDB[65]#

Ball Number	Signal
V20	HWMDAL#
V21	MVREFA[0]
V22	MDA[9]#
V23	MDA[4]#
V24	MDA[7]#
W01	D[22]#
W02	D[20]#
W03	D[18]#
W04	D[19]#
W05	VSS
W06	D[3]#
W07	D[0]#
W08	VCC
W09	VSS
W10	MDB[16]#
W11	MDB[6]#
W12	VCC
W13	MDBSN[1]#
W14	VSS
W15	MDB[38]#
W16	VCC
W17	MDB[47]#
W18	VSS
W19	MDB[67]#
W20	VCC
W21	MDA[12]#
W22	VSS
W23	LRMDA#
W24	MDA[15]#
Y01	D[21]#
Y02	VSS
Y03	D[17]#
Y04	D[6]#
Y05	D[5]#
Y06	D[2]#
Y07	TDO
Y08	CRESF0
Y09	P/U 180Ω
Y10	MDB[10]#

Table 9-2. SDC Ball List (Continued)

Ball Number	Signal
Y11	MDB[4]#
Y12	MDB[31]#
Y13	MDBSP[1]#
Y14	MDB[21]#
Y15	MDB[18]#
Y16	MDBSN[2]#
Y17	MDB[39]#
Y18	MDB[48]#
Y19	MDB[61]#
Y20	MDB[66]#
Y21	FWMDA#
Y22	HWMDBL#
Y23	MDA[17]#
Y24	MDA[6]#
AA01	D[16]#
AA02	D[14]#
AA03	VSS
AA04	DEP[1]#
AA05	D[4]#
AA06	VSS
AA07	TDI
AA08	P/U 10KΩ
AA09	VCC
AA10	MDB[8]#
AA11	VSS
AA12	MDB[9]#
AA13	VCC
AA14	MDB[34]#
AA15	VSS
AA16	MDBSP[2]#
AA17	VCC
AA18	MDB[50]#
AA19	VSS
AA20	MDB[71]#
AA21	VCC
AA22	MDA[14]#
AA23	VSS
AA24	MDA[16]#
AB01	D[15]#

Ball Number	Signal
AB02	VSS
AB03	D[11]#
AB04	VSS
AB05	D[7]#
AB06	TMS
AB07	VSS (RSVD)
AB08	HCLKIN#
AB09	MDB[11]#
AB10	MDBSP[0]#
AB11	MDBSN[0]#
AB12	MDB[3]#
AB13	MDB[7]#
AB14	MDB[22]#
AB15	MDB[23]#
AB16	MDB[20]#
AB17	MDB[40]#
AB18	MDB[41]#
AB19	MDB[53]#
AB20	MDBSN[3]#
AB21	MDBSP[3]#
AB22	MDB[68]#
AB23	HWMDAR#
AB24	LRMDB#
AC01	D[12]#
AC02	D[13]#
AC03	VSS
AC04	VREF[0]
AC05	TCK
AC06	CRESF1
AC07	VSS
AC08	HCLKIN
AC09	MDB[17]#
AC10	VCC
AC11	MVREFB[0]
AC12	VSS
AC13	MDB[32]#
AC14	VCC
AC15	MDB[33]#
AC16	VSS

Table 9-2. SDC Ball List (Continued)

Ball Number	Signal	Ball Number	Signal
AC17	MDB[19]#	AD09	MDB[12]#
AC18	VCC	AD10	MDB[13]#
AC19	MDB[52]#	AD11	MDB[14]#
AC20	VSS	AD12	N/C
AC21	MDB[55]#	AD13	N/C
AC22	MDB[69]#	AD14	MDB[1]#
AC23	MDB[70]#	AD15	MDB[24]#
AC24	HWMDBR#	AD16	MDB[42]#
AD01	D[10]#	AD17	MDB[25]#
AD02	D[8]#	AD18	MDB[43]#
AD03	D[9]#	AD19	MDB[37]#
AD04	DEP[0]#	AD20	MDB[51]#
AD05	N/C	AD21	MDB[58]#
AD06	VSS (RSVD)	AD22	MDB[59]#
AD07	SDCRST#	AD23	MDB[56]#
AD08	P/U 180Ω	AD24	MDB[54]#

Table 9-3. MAC Ball List

Ball Number	Signal
A01	VCC33
A02	TRST#
A03	IDVAL1
A04	HCLKIN
A05	VCC18
A06	CMND1#
A07	MA16#
A08	MA13#
A09	MA8#
A10	VCC18
A11	VCC18
A12	PAR#
A13	CMPLTL#
A14	PWRGD
A15	CORDR1#
A16	VCC18
A17	N/C
A18	FDQR#
A19	FRMD#
A20	VCC18
B01	ADDLD7
B02	TDI
B03	SCL
B04	IDVAL0
B05	HCLKIN#
B06	CMND0#
B07	ROW0#
B08	MA14#
B09	MA9#
B10	MA5#
B11	MA2#
B12	ERR#
B13	CMPLTR#
B14	HWMDR#
B15	FWMD#
B16	N/C
B17	LDQL#
B18	LRMD#

Ball Number	Signal
B19	ADDRD10
B20	ADDRD5
C1	ADDLD6
C2	ADDLD9
C3	VSS
C4	TCK
C5	VCC33 (RSVD)
C6	VSS
C7	ROW1#
C8	VCC18
C9	MA10#
C10	VSS
C11	VSS
C12	N/C
C13	VCC18
C14	HWMDL#
C15	VSS
C16	FDQL#
C17	LDQR#
C18	VSS
C19	ADDRD7
C20	ADDRD4
D1	ADDLD1
D2	ADDLD4
D3	ADDLD10
D4	ADDLD12
D5	SDA
D6	VCC33 (RSVD)
D7	ROW2#
D8	MA12#
D9	MA11#
D10	MA4#
D11	MA3#
D12	N/C
D13	VREF18
D14	FWSL#
D15	MINIT#
D16	LWMD#

Table 9-3. MAC Ball List (Continued)

Ball Number	Signal
D17	LEFT#
D18	ADDRD8
D19	ADDRD2
D20	CRES0
E01	VCC33
E02	ADDLD0
E03	ADDLD8
E04	ADDLD11
E05	TDO
E06	VSS (RSVD)
E07	VCCA
E08	MA15#
E09	MA7#
E10	MA6#
E11	MA1#
E12	MA0#
E13	MEMRST#
E14	CORDR0#
E15	RESET#
E16	ADDRD11
E17	ADDRD9
E18	ADDRD6
E19	ADDRD1
E20	VCC33
F01	RASLD#
F02	BANKLD2
F03	VSS
F04	ADDLD3
F05	TMS
F06	VCC33
F14	VCC33
F15	VCC33
F16	ADDRD12
F17	CRES2
F18	VSS
F19	ADDRD0
F20	BANKRD0
G01	WELD#
G02	CASLD#

Ball Number	Signal
G03	BANKLD0
G04	ADDLD2
G05	ADDLD5
G06	VCC33
G16	ADDRD3
G17	CRES1
G18	BANKRD1
G19	RASRD#
G20	CASRD#
H01	CSLD2#
H02	CSLD1#
H03	VCC33
H04	CSLD3#
H05	BANKLD1
H16	BANKRD2
H17	WERD#
H18	VCC33
H19	CSRD2#
H20	CSRD3#
J01	ADDLC9
J02	ADDLC10
J03	ADDLC11
J04	ADDLC12
J05	CSLD0#
J09	VSS
J10	VSS
J11	VSS
J12	VSS
J16	CSRD1#
J17	CSRD0#
J18	ADDRC12
J19	ADDRC11
J20	ADDRC10
K01	VCC33
K02	ADDLC6
K03	VSS
K04	ADDLC7
K05	ADDLC8
K09	VSS

Table 9-3. MAC Ball List (Continued)

Ball Number	Signal
K10	VSS
K11	VSS
K12	VSS
K16	ADDRC9
K17	ADDRC8
K18	VSS
K19	ADDRC7
K20	VCC33
L01	VCC33
L02	ADDLC5
L03	VSS
L04	ADDLC3
L05	ADDLC4
L09	VSS
L10	VSS
L11	VSS
L12	VSS
L16	ADDRC5
L17	ADDRC4
L18	VSS
L19	ADDRC6
L20	VCC33
M01	ADDLC2
M02	ADDLC0
M03	ADDLC1
M04	BANKLC2
M05	BANKLC1
M09	VSS
M10	VSS
M11	VSS
M12	VSS
M16	BANKRC2
M17	ADDRC0
M18	ADDRC2
M19	ADDRC1
M20	ADDRC3
N01	BANKLC0
N02	RASLC#
N03	VCC33

Ball Number	Signal
N04	CSLC2#
N05	CSLC1#
N16	CSRC2#
N17	CSRC3#
N18	VCC33
N19	BANKRC0
N20	BANKRC1
P01	WELC#
P02	CASLC#
P03	CSLC3#
P04	CSLC0#
P05	ADDLB10
P15	VCC33
P16	ADDRB11
P17	CSRC1#
P18	WERC#
P19	RASRC#
P20	CASRC#
R01	ADDLB12
R02	ADDLB11
R03	VSS
R04	VREF33
R05	ADDLB1
R06	VCC33
R07	VCC33
R15	VCC33
R16	ADDRB1
R17	ADDRB9
R18	VSS
R19	ADDRB12
R20	CSRC0#
T01	VCC33
T02	ADDLB9
T03	ADDLB7
T04	BANKLB1
T05	BANKLB2
T06	ADDLA11
T07	ADDLA8
T08	ADDLA1

Table 9-3. MAC Ball List (Continued)

Ball Number	Signal
T09	CSLA3#
T10	CSLA2#
T11	CSRA2#
T12	CSRA3#
T13	ADDRA1
T14	ADDRA8
T15	ADDRA11
T16	BANKRB2
T17	BANKRB1
T18	ADDRB7
T19	ADDRB10
T20	VCC33
U01	ADDLB8
U02	ADDLB5
U03	ADDLB2
U04	BANKLB0
U05	WELB#
U06	ADDLA12
U07	ADDLA5
U08	BANKLA1
U09	BANKLA0
U10	CSLA0#
U11	CSRA0#
U12	BANKRA0
U13	BANKRA1
U14	ADDRA5
U15	ADDRA12
U16	WERB#
U17	BANKRB0
U18	ADDRB2
U19	ADDRB5
U20	ADDRB8
V01	ADDLB6
V02	ADDLB3
V03	VSS
V04	CSLB3#
V05	CSLB0#
V06	VSS
V07	ADDLA4

Ball Number	Signal
V08	VCC33
V09	RASLA#
V10	VSS
V11	VSS
V12	RASRA#
V13	VCC33
V14	ADDRA4
V15	VSS
V16	CSRB0#
V17	CSRB3#
V18	VSS
V19	ADDRB3
V20	ADDRB6
W01	ADDLB4
W02	ADDLB0
W03	RASLB#
W04	CSLB2#
W05	ADDLA10
W06	ADDLA6
W07	ADDLA3
W08	ADDLA0
W09	CASLA#
W10	CSLA1#
W11	CSRA1#
W12	CASRA#
W13	ADDRA0
W14	ADDRA3
W15	ADDRA6
W16	ADDRA10
W17	CSRB2#
W18	RASRB#
W19	ADDRB0
W20	ADDRB4
Y01	VCC33
Y02	CASLB#
Y03	CSLB1#
Y04	ADDLA9
Y05	VCC33
Y06	ADDLA7

Table 9-3. MAC Ball List (Continued)

Ball Number	Signal	Ball Number	Signal
Y07	ADDLA2	Y14	ADDRA2
Y08	BANKLA2	Y15	ADDRA7
Y09	WELA#	Y16	VCC33
Y10	VCC33	Y17	ADDRA9
Y11	VCC33	Y18	CSRB1#
Y12	WERA#	Y19	CASRB#
Y13	BANKRA2	Y20	VCC33

Table 9-4. MDC Ball List

Ball Number	Signal
A01	VCC33
A02	DQR51
A03	DQR49
A04	DQR67
A05	VCC33
A06	DQR15
A07	DQR13
A08	DQR43
A09	DQR41
A10	VCC33
A11	VCC33
A12	DQR36
A13	DQR1
A14	IDVAL0
A15	MEMCLKBR13
A16	VCC33
A17	MEMCLKBR11
A18	MEMCLKBR6
A19	MEMCLKBR2
A20	VCC33
B01	DQR20
B02	DQR18
B03	DQR16
B04	DQR71
B05	DQR69
B06	DQR47
B07	DQR45
B08	DQR10
B09	DQR8
B10	DQR39
B11	DQR5
B12	DQR3
B13	DQR33
B14	VREF334
B15	MEMCLKBR14
B16	MEMCLKBR10
B17	MEMCLKBR5
B18	MEMCLKBR1

Ball Number	Signal
B19	MEMCLKR
B20	VREF180
C01	DQR52
C02	DQR50
C03	VSS
C04	DQR66
C05	DQR64
C06	VSS
C07	DQR12
C08	VCC33
C09	DQR40
C10	VSS
C11	VSS
C12	DQR35
C13	VCC33
C14	IDVAL1
C15	VSS
C16	MEMCLKBR7
C17	MEMCLKBR4
C18	VSS
C19	VSS (RSVD)
C20	N/C
D01	DQR19
D02	DQR17
D03	DQR48
D04	DQR70
D05	DQR68
D06	DQR14
D07	DQR44
D08	DQR42
D09	DQR65
D10	DQR6
D11	DQR37
D12	DQR2
D13	DQR0
D14	MEMCLKBR15
D15	MEMCLKBR8
D16	MEMCLKBR3

Table 9-4. MDC Ball List (Continued)

Ball Number	Signal
D17	MEMCLKBR0
D18	VCC33 (RSVD)
D19	RESET#
D20	FDQR#
E01	VCC33
E02	DQR53
E03	DQR21
E04	DQR54
E05	DQR22
E06	DQR46
E07	DQR11
E08	DQR9
E09	DQR7
E10	DQR38
E11	DQR4
E12	DQR34
E13	DQR32
E14	MEMCLKBR12
E15	MEMCLKBR9
E16	MEMCLKINR
E17	VCC33 (RSVD)
E18	VSS (RSVD)
E19	LEFT#
E20	VCC18
F01	DQR55
F02	DQR23
F03	VSS
F04	VREF333
F05	DQR56
F06	VCC33
F14	VCC18
F15	VCC18
F16	IDVAL2
F17	MINIT#
F18	VSS
F19	FRMD#
F20	LDQL#
G01	DQR24
G02	DQR57

Ball Number	Signal
G03	DQR25
G04	N/C
G05	DQR58
G06	VCC33
G16	PWRGD
G17	FDQL#
G18	LDQR#
G19	CORDR1#
G20	CORDR0#
H01	DQR26
H02	DQR59
H03	VCC33
H04	DQR27
H05	DQR60
H16	LWMD#
H17	VCCA2
H18	VCC18
H19	MD16#
H20	MD17#
J01	DQR28
J02	DQR61
J03	DQR29
J04	DQR62
J05	DQR30
J09	VSS
J10	VSS
J11	VSS
J12	VSS
J16	MD15#
J17	MD14#
J18	MD13#
J19	MD12#
J20	MD11#
K01	VCC33
K02	VREF332
K03	VSS
K04	DQR63
K05	DQR31
K09	VSS

Table 9-4. MDC Ball List (Continued)

Ball Number	Signal
K10	VSS
K11	VSS
K12	VSS
K16	MD10#
K17	VCCA0
K18	VSS
K19	MDSN#
K20	VCC18
L01	VCC33
L02	DQL61
L03	VSS
L04	DQL27
L05	DQL60
L09	VSS
L10	VSS
L11	VSS
L12	VSS
L16	MD9#
L17	MD8#
L18	VSS
L19	MDSP#
L20	VCC18
M01	DQL26
M02	DQL3
M03	DQL24
M04	DQL59
M05	DQL23
M09	VSS
M10	VSS
M11	VSS
M12	VSS
M16	MD3#
M17	MD4#
M18	MD6#
M19	MD5#
M20	MD7#
N01	DQL57
N02	DQL22
N03	VCC33

Ball Number	Signal
N04	DQL56
N05	N/C
N16	HCLKIN#
N17	HCLKIN
N18	VCC18
N19	MD1#
N20	MD2#
P01	DQL55
P02	DQL21
P03	DQL54
P04	DQL9
P05	DQL10
P15	VCC33
P16	SDA18
P17	VCCA1
P18	VREF181
P19	MD0#
P20	N/C
R01	DQL53
R02	DQL20
R03	VSS
R04	VREF331
R05	DQL52
R06	VCC33
R07	VCC33
R15	VCC33
R16	N/C
R17	CRES1
R18	VSS
R19	SCL18
R20	N/C
T01	VCC33
T02	N/C
T03	DQL32
T04	DQL69
T05	DQL64
T06	DQL62
T07	DQL6
T08	DQL40

Table 9-4. MDC Ball List (Continued)

Ball Number	Signal
T09	DQL39
T10	DQL68
T11	DQL34
T12	DQL37
T13	DQL29
T14	MEMCLKBL12
T15	MEMCLKBL9
T16	MEMCLKINL
T17	N/C
T18	N/C
T19	CRES2
T20	VCC18
U01	DQL51
U02	DQL2
U03	DQL50
U04	DQL65
U05	DQL67
U06	DQL44
U07	DQL42
U08	DQL5
U09	DQL4
U10	DQL35
U11	DQL47
U12	DQL30
U13	DQL11
U14	MEMCLKBL15
U15	MEMCLKBL8
U16	MEMCLKBL3
U17	MEMCLKBL0
U18	TRST#
U19	TCK
U20	CRES0
V01	DQL19
V02	DQL49
V03	VSS
V04	DQL70
V05	DQL63
V06	VSS
V07	DQL14

Ball Number	Signal
V08	VCC33
V09	DQL38
V10	VSS
V11	VSS
V12	DQL25
V13	VCC33
V14	SDA33
V15	VSS
V16	MEMCLKBL7
V17	MEMCLKBL4
V18	VSS
V19	TMS
V20	TDO
W01	DQL18
W02	DQL48
W03	DQL16
W04	DQL45
W05	DQL66
W06	DQL15
W07	DQL41
W08	DQL1
W09	DQL71
W10	DQL58
W11	DQL33
W12	DQL0
W13	DQL28
W14	VREF330
W15	MEMCLKBL14
W16	MEMCLKBL10
W17	MEMCLKBL5
W18	MEMCLKBL1
W19	MEMCLKL
W20	TDI
Y01	VCC33
Y02	DQL17
Y03	DQL46
Y04	DQL7
Y05	VCC33
Y06	DQL43

Table 9-4. MDC Ball List (Continued)

Ball Number	Signal
Y07	DQL13
Y08	DQL12
Y09	DQL36
Y10	VCC33
Y11	VCC33
Y12	DQL8
Y13	DQL31

Ball Number	Signal
Y14	SCL33
Y15	MEMCLKBL13
Y16	VCC33
Y17	MEMCLKBL11
Y18	MEMCLKBL6
Y19	MEMCLKBL2
Y20	VCC33

Table 9-5. GXB Ball List

Ball Number	Signal
A1	VCC
A2	VCC
A3	VCC
A4	VCC
A5	VCT
A6	X1D11#
A7	VSS
A8	X1D9#
A9	VCC
A10	X1HSTBN#
A11	VSS
A12	X1D4#
A13	VCC
A14	X1ADS#
A15	VSS
A16	VCT
A17	X0D15#
A18	VSS
A19	X0D14#
A20	VCC
A21	X0D6#
A22	VSS
A23	X0XSTBP#
A24	VCC
A25	X0D3#
A26	VSS
A27	X0BE1#
A28	VCT
A29	VSS
A30	VSS
A31	VSS
A32	VSS
B1	VCC
B2	VCC
B3	VCC
B4	VSS
B5	NC514
B6	VSS

Ball Number	Signal
B7	X1D13#
B8	VCC
B9	X1XRTS#
B10	VSS
B11	X1HSTBP#
B12	VCC
B13	X1D2#
B14	VSS
B15	X1D1#
B16	VCC
B17	NC450
B18	X0D12#
B19	VCC
B20	X0HRTS#
B21	VSS
B22	X0HSTBP#
B23	VCC
B24	X0D5#
B25	VSS
B26	X0D00#
B27	VSS
B28	VCC
B29	VCC
B30	VSS
B31	VSS
B32	VSS
C1	VCC
C2	VCC
C3	VSS
C4	VCT
C5	VCC
C6	X1D10#
C7	VCT
C8	X1D8#
C9	VCT
C10	X1D7#
C11	VREF1
C12	X1XSTBN#

Table 9-5. GXB Ball List (Continued)

Ball Number	Signal
C13	VCT
C14	X1PAR#
C15	VCT
C16	X1BE0#
C17	X0D10#
C18	VCT
C19	X0D8#
C20	VCT
C21	X0HSTBN#
C22	VREFOUT0
C23	X0XSTBN#
C24	VCT
C25	X0PAR#
C26	VCT
C27	X0BE0#
C28	VSS
C29	VCT
C30	VCC
C31	VSS
C32	VSS
D1	VCC
D2	VSS
D3	VCT
D4	VSS
D5	XBINIT#
D6	VCC
D7	X1D12#
D8	VSS
D9	X1HRTS#
D10	VCC
D11	VREFOUT1
D12	VSS
D13	X1D5#
D14	VCC
D15	X1D00#
D16	VSS
D17	VCC
D18	X0D13#
D19	VSS

Ball Number	Signal
D20	X0XRTS#
D21	VCC
D22	VREF0
D23	VSS
D24	X0D2#
D25	VCC
D26	X0D1#
D27	VCC
D28	VCT
D29	VCC
D30	VSS
D31	VCC
D32	VSS
E1	VSS
E2	VCC
E3	VSS
E4	VCT
E5	VSS
E6	X1D15#
E7	VCC
E8	X1D14#
E9	VSS
E10	X1D6#
E11	VCT
E12	X1XSTBP#
E13	VSS
E14	X1D3#
E15	VCC
E16	X1BE1#
E17	X0D11#
E18	VCC
E19	X0D9#
E20	VSS
E21	X0D7#
E22	VCT
E23	X0D4#
E24	VSS
E25	X0ADS#
E26	VCC

Table 9-5. GXB Ball List (Continued)

Ball Number	Signal
E27	X0BLK#
E28	VSS
E29	VCT
E30	VCC
E31	VSS
E32	VCC
F1	VCC
F2	VSS
F3	VCC
F4	N/C
F5	VSS
F28	VSS
F29	CRES0
F30	VSS
F31	VCC
F32	VSS
G1	N/C
G2	VCC
G3	N/C
G4	VSS
G5	N/C
G28	VCC
G29	CRES1
G30	VCC
G31	VSS
G32	VCC
H1	VCC
H2	N/C
H3	VSS
H4	N/C
H5	VCC
H28	VSS
H29	VCC
H30	VSS
H31	VCC
H32	VSS
J1	VCC (RSVD)
J2	VCC
J3	N/C

Ball Number	Signal
J4	VSS
J5	N/C
J28	VCC
J29	VSS
J30	VCC
J31	VSS
J32	VCC
K1	VSS
K2	VSS (RSVD)
K3	VCC
K4	PWRGD
K5	VSS
K28	VSS
K29	VCC
K30	VSS
K31	VCC
K32	VSS
L1	AGPCLKIN
L2	VSS
L3	VCCA1
L4	VCC
L5	VCCA0
L28	VCC
L29	XINTR#
L30	VSS
L31	SDATA1
L32	VCC
M1	SCLKIN
M2	X0CLK
M3	VREF2
M4	X0RST#
M5	VCCA2
M28	SDATA00
M29	VSS
M30	SDATA2
M31	VSS
M32	SDATA4
N1	VCC
N2	AGPCLK0

Table 9-5. GXB Ball List (Continued)

Ball Number	Signal
N3	VSS
N4	VCCA3
N5	VCC
N28	SDATA3
N29	SDATA5
N30	SDATA8
N31	SDATA6
N32	SDATA7
P1	SCLK1
P2	VCC
P3	SCLK0
P4	VSS
P5	AGPCLK1
P28	VCC
P29	SDATA9
P30	VSS
P31	SDATA10
P32	VCC
R1	VSS
R2	SCLK2
R3	VCC
R4	VSS (RSVD)
R5	VSS
R28	VSS
R29	SDATA14
R30	SDATA13
R31	SDATA11
R32	SDATA12
T1	VCC
T2	VSS
T3	N/C
T4	VSS (RSVD)
T5	N/C
T28	SDATA18
T29	VSS
T30	SDATA15
T31	VSS
T32	SDATA16
U1	VSS

Ball Number	Signal
U2	VCC
U3	N/C
U4	VCC (RSVD)
U5	N/C
U28	VCC
U29	SDATA23
U30	VSS
U31	SDATA17
U32	VCC
V1	TDO
V2	VSS
V3	TRST#
V4	VCC
V5	VSS
V28	SDATA29
V29	SDATA24
V30	SDATA21
V31	SDATA20
V32	SDATA19
W1	TMS
W2	TCK
W3	VCC
W4	TDI
W5	VSS
W28	SDATA31
W29	VSS
W30	SDATA27
W31	VCC
W32	SDATA22
Y1	VSS
Y2	VCC
Y3	VSS
Y4	VCC
Y5	VSS
Y28	SADDR3
Y29	SDATA30
Y30	SDATA28
Y31	SDATA26
Y32	SDATA25

Table 9-5. GXB Ball List (Continued)

Ball Number	Signal
AA1	N/C
AA2	VSS
AA3	N/C
AA4	VCC
AA5	N/C
AA28	VCC
AA29	SADDR2
AA30	VSS
AA31	SADDR1
AA32	VCC
AB1	VSS
AB2	N/C
AB3	VCC
AB4	N/C
AB5	VSS
AB28	SADDR5
AB29	SADDR00
AB30	SADDR4
AB31	SOE#
AB32	SGW#
AC1	N/C
AC2	VSS
AC3	N/C
AC4	VCC
AC5	N/C
AC28	VSS
AC29	SADDR6
AC30	SADDR8
AC31	SADDR9
AC32	VSS
AD1	VCCQ
AD2	TYPEDET#
AD3	VCC
AD4	AGPRST#
AD5	VSS
AD28	VCC
AD29	SADDR11
AD30	VSS
AD31	SADDR7

Ball Number	Signal
AD32	VCC
AE1	REQ#
AE2	VCCQ
AE3	GNT#
AE4	VSS
AE5	ST0
AE28	SADDR15
AE29	SADDR14
AE30	SADDR12
AE31	SADDR10
AE32	SSE3#
AF1	VSS
AF2	ST1
AF3	VCC
AF4	ST2
AF5	VCCQ
AF28	SADDR17
AF29	VCC
AF30	SADDR16
AF31	VSS
AF32	SADDR13
AG1	RBF#
AG2	VSS
AG3	PIPE#
AG4	VCCQ
AG5	WBF#
AG28	VCC
AG29	VSS
AG30	VSS
AG31	CRES5
AG32	VCC
AH1	VCC
AH2	VCCQ
AH3	VSS
AH4	VCC
AH5	VSS
AH6	SBSTB
AH7	VCCQ
AH8	SBA5

Table 9-5. GXB Ball List (Continued)

Ball Number	Signal
AH9	VSS
AH10	AD31
AH11	VCC
AH12	AD26
AH13	VSS
AH14	AD23
AH15	VCCQ
AH16	AD18
AH17	VCC
AH18	TRDY#
AH19	VCCQ
AH20	VSS
AH21	AD14
AH22	VCC
AH23	AD9
AH24	VSS
AH25	ADSTB0#
AH26	VCCQ
AH27	AD1
AH28	VSS
AH29	VCC
AH30	CRES4
AH31	VCC
AH32	VSS
AJ1	VSS
AJ2	VCC
AJ3	VREFAGP0
AJ4	VSS
AJ5	SBA0
AJ6	VSS
AJ7	SBSTB#
AJ8	VCCQ
AJ9	VREFAGP1
AJ10	VSS
AJ11	AD28
AJ12	VCCQ
AJ13	ADSTB1
AJ14	VSS
AJ15	AD20

Ball Number	Signal
AJ16	VCCQ
AJ17	CBE2#
AJ18	VSS
AJ19	SERR#
AJ20	VREFAGP2
AJ21	VCCQ
AJ22	AD12
AJ23	VSS
AJ24	ADSTB0
AJ25	VCCQ
AJ26	AD4
AJ27	VSS
AJ28	CBE0#
AJ29	VSS
AJ30	CRES3
AJ31	VSS
AJ32	VCCQ
AK1	VSS
AK2	VSS
AK3	VCC
AK4	VCCQ
AK5	VSS
AK6	SBA3
AK7	VCC
AK8	SBA6
AK9	VCC
AK10	AD30
AK11	VCCQ
AK12	AD25
AK13	VCC
AK14	AD22
AK15	VCC
AK16	AD17
AK17	VSS
AK18	DEVSEL#
AK19	VSS
AK20	VCC
AK21	AD15
AK22	VCCQ

Table 9-5. GXB Ball List (Continued)

Ball Number	Signal
AK23	AD10
AK24	VCC
AK25	AD6
AK26	VCC
AK27	AD2
AK28	VCCQ
AK29	CRES2
AK30	VCC
AK31	VCCQ
AK32	VCCQ
AL1	VSS
AL2	VSS
AL3	VSS
AL4	VCC
AL5	SBA1
AL6	VCCQ
AL7	SBA4
AL8	VSS
AL9	CBE3#
AL10	VCCQ
AL11	AD27
AL12	VSS
AL13	ADSTB1#
AL14	VCCQ
AL15	AD19
AL16	VSS
AL17	IRDY#
AL18	VCCQ
AL19	PERR#
AL20	PAR
AL21	VSS
AL22	AD13
AL23	VCCQ
AL24	AD8
AL25	VSS
AL26	AD5
AL27	VCCQ

Ball Number	Signal
AL28	AD00
AL29	VCC
AL30	VCCQ
AL31	VCCQ
AL32	VCCQ
AM1	VSS
AM2	VSS
AM3	VSS
AM4	VSS
AM5	VCCQ
AM6	SBA2
AM7	VSS
AM8	SBA7
AM9	VCCQ
AM10	AD29
AM11	VSS
AM12	AD24
AM13	VCCQ
AM14	AD21
AM15	VSS
AM16	AD16
AM17	VCCQ
AM18	FRAME#
AM19	STOP#
AM20	VCCQ
AM21	CBE1#
AM22	VSS
AM23	AD11
AM24	VCCQ
AM25	AD7
AM26	VSS
AM27	AD3
AM28	VSS
AM29	VCCQ
AM30	VCCQ
AM31	VCCQ
AM32	VCCQ

Table 9-6. PXB Ball List

Ball Number	Signal
A1	N/C
A2	N/C
A3	VCC
A4	VCC
A5	VCC
A6	VCC
A7	VCC
A8	VCC
A9	VCC
A10	VCC
A11	N/C
A12	VREF[1]
A13	N/C
A14	VCC
A15	XD[10]#
A16	VCC
A17	XHSTBN#
A18	VCC
A19	XD[04]#
A20	VCC
A21	XBLK#
A22	VCC
A23	N/C
A24	VREF[0]
A25	N/C
A26	VCC
A27	VCCA[0]
A28	VCC
A29	VCC
A30	N/C
A31	N/C
A32	N/C
B1	N/C
B2	VCC
B3	VCC
B4	VCC
B5	N/C
B6	N/C
C13	N/C

Ball Number	Signal
B7	N/C
B8	N/C
B9	N/C
B10	N/C
B11	N/C
B12	N/C
B13	N/C
B14	XD[15]#
B15	XD[11]#
B16	XD[08]#
B17	N/C
B18	XHRTS#
B19	XD[05]#
B20	XD[02]#
B21	XPAR#
B22	XBE[1]#
B23	N/C
B24	N/C
B25	N/C
B26	N/C
B27	N/C
B28	VCC
B29	LONGXB1
B30	VCC
B31	VCC
B32	N/C
C1	N/C
C2	N/C
C3	N/C
C4	N/C
C5	N/C
C6	VSS
C7	VSS
C8	VSS
C9	N/C
C10	VSS
C11	N/C
C12	VSS
D20	XD[03]#

Table 9-6. PXB Ball List (Continued)

Ball Number	Signal
C14	VSS
C15	XD[12]#
C16	VSS
C17	XHSTBP#
C18	VSS
C19	XXSTBN#
C20	VSS
C21	XADS#
C22	VSS
C23	N/C
C24	XCLKGTL
C25	XCLK
C26	VSS
C27	VCCA[1]
C28	N/C
C29	N/C
C30	N/C
C31	N/C
C32	N/C
D1	N/C
D2	VSS
D3	N/C
D4	VCT
D5	N/C
D6	N/C
D7	XBINIT#
D8	N/C
D9	CRES1
D10	N/C
D11	N/C
D12	N/C
D13	N/C
D14	N/C
D15	XD[13]#
D16	XD[09]#
D17	XD[06]#
D18	XXRTS#
D19	N/C
E27	VCCA[2]

Ball Number	Signal
D21	XD[00]#
D22	XRST#
D23	N/C
D24	N/C
D25	N/C
D26	N/C
D27	LONGXB0
D28	VCT
D29	PWRGD
D30	N/C
D31	VSS
D32	N/C
E1	N/C
E2	N/C
E3	N/C
E4	N/C
E5	N/C
E6	VCT
E7	N/C
E8	VCT
E9	CRES0
E10	VCT
E11	N/C
E12	VCT
E13	XIB#
E14	VCT
E15	XD[14]#
E16	VCT
E17	XD[07]#
E18	VCT
E19	XXSTBP#
E20	VCT
E21	XD[01]#
E22	VCT
E23	XBE[0]#
E24	VCT
E25	N/C
E26	VCT
J4	N/C

Table 9-6. PXB Ball List (Continued)

Ball Number	Signal
E28	N/C
E29	N/C
E30	N/C
E31	N/C
E32	N/C
F1	VSS
F2	N/C
F3	VCC
F4	N/C
F5	VSS
F28	VSS
F29	PIIXOK#
F30	N/C
F31	N/C
F32	N/C
G1	N/C
G2	N/C
G3	N/C
G4	N/C
G5	N/C
G28	N/C
G29	N/C
G30	GEAR4#
G31	N/C
G32	N/C
H1	VCC
H2	N/C
H3	VSS
H4	N/C
H5	VCC
H28	N/C
H29	N/C
H30	VSS
H31	N/C
H32	N/C
J1	N/C
J2	N/C
J3	N/C
N3	N/C

Ball Number	Signal
J5	N/C
J28	N/C
J29	N/C
J30	PBCLKFB
J31	N/C
J32	PACLKFB
K1	VSS
K2	N/C
K3	VCC
K4	N/C
K5	VSS
K28	VSS
K29	N/C
K30	VCC
K31	N/C
K32	VSS
L1	N/C
L2	N/C
L3	N/C
L4	N/C
L5	N/C
L28	N/C
L29	N/C
L30	PBCLK
L31	N/C
L32	PACLK
M1	VCC
M2	N/C
M3	VSS
M4	JTTCK
M5	VCC
M28	VCC
M29	N/C
M30	VSS
M31	N/C
M32	VCC
N1	JTTDI
N2	JTTDO
U2	N/C

Table 9-6. PXB Ball List (Continued)

Ball Number	Signal
N4	JTTMS
N5	JTTRST#
N28	N/C
N29	N/C
N30	N/C
N31	N/C
N32	N/C
P1	VCC
P2	N/C
P3	VSS
P4	N/C
P5	VCC
P28	VSS
P29	N/C
P30	VCC
P31	N/C
P32	VSS
R1	VCC
R2	N/C
R3	VSS
R4	N/C
R5	VCC
R28	VSS
R29	N/C
R30	VCC
R31	N/C
R32	VSS
T1	VCC
T2	N/C
T3	VSS
T4	N/C
T5	VCC
T28	VSS
T29	N/C
T30	VCC
T31	N/C
T32	VSS
U1	N/C
AA1	PBAD[25]#

Ball Number	Signal
U3	N/C
U4	N/C
U5	N/C
U28	N/C
U29	N/C
U30	VCC
U31	N/C
U32	VSS
V1	VSS
V2	N/C
V3	VCC5D
V4	N/C
V05	VSS
V28	VCC
V29	N/C
V30	VCC5D
V31	N/C
V32	VSS
W1	PBAD[31]#
W2	PBAD[30]#
W3	PBAD[29]#
W4	PBAD[28]#
W5	VSS
W28	VCC
W29	PAAD[28]#
W30	PAAD[29]#
W31	PAAD[30]#
W32	PAAD[31]#
Y1	VCC
Y2	PBAD[27]#
Y3	VSS
Y4	PBAD[26]#
Y5	VCC
Y28	VCC
Y29	PAAD[26]#
Y30	VSS
Y31	PAAD[27]#
Y32	VCC
AD32	VCC

Table 9-6. PXB Ball List (Continued)

Ball Number	Signal
AA2	PBAD[24]#
AA3	PBAD[23]#
AA4	PBAD[22]#
AA5	PBAD[21]#
AA28	PAAD[21]#
AA29	PAAD[22]#
AA30	PAAD[23]#
AA31	PAAD[24]#
AA32	PAAD[25]#
AB1	VSS
AB2	PBAD[20]#
AB3	VCC5D
AB4	PBAD[19]#
AB5	VSS
AB28	VSS
AB29	PAAD[19]#
AB30	VCC5D
AB31	PAAD[20]#
AB32	VSS
AC1	PBAD[18]#
AC2	PBAD[17]#
AC3	PBAD[16]#
AC4	PBAD[15]#
AC5	PBAD[14]#
AC28	PAAD[14]#
AC29	PAAD[15]#
AC30	PAAD[16]#
AC31	PAAD[17]#
AC32	PAAD[18]#
AD1	VCC
AD2	PBAD[13]#
AD3	VSS
AD4	PBAD[12]#
AD5	VCC
AD28	VCC
AD29	PAAD[12]#
AD30	VSS
AD31	PAAD[13]#
AH9	VCC

Ball Number	Signal
AE1	PBAD[11]#
AE2	PBAD[10]#
AE3	PBAD[09]#
AE4	PBAD[08]#
AE5	PBAD[07]#
AE28	PAAD[07]#
AE29	PAAD[08]#
AE30	PAAD[09]#
AE31	PAAD[10]#
AE32	PAAD[11]#
AF1	VSS
AF2	PBAD[06]#
AF3	VCC5D
AF4	PBAD[05]#
AF5	VSS
AF28	VSS
AF29	PAAD[05]#
AF30	VCC5D
AF31	PAAD[06]#
AF32	VSS
AG1	PBAD[04]#
AG2	PBAD[03]#
AG3	PBAD[02]#
AG4	PBAD[01]#
AG5	PBAD[00]#
AG28	PAAD[00]#
AG29	PAAD[01]#
AG30	PAAD[02]#
AG31	PAAD[03]#
AG32	PAAD[04]#
AH1	N/C
AH2	N/C
AH3	VCC5D
AH4	VCC
AH5	N/C
AH6	N/C
AH7	VSS
AH8	PBMON[1]#
AJ16	PBCBE[1]#

Table 9-6. PXB Ball List (Continued)

Ball Number	Signal
AH10	PBGNT[2]#
AH11	VSS
AH12	PBREQ[1]#
AH13	VCC
AH14	PBDEVSEL#
AH15	VSS
AH16	PBCBE[0]#
AH17	VCC
AH18	PACBE[0]#
AH19	VSS
AH20	PADEVSEL#
AH21	VCC
AH22	PAREQ[1]#
AH23	VSS
AH24	PAGNT[2]#
AH25	VCC
AH26	PAMON[1]#
AH27	VSS
AH28	N/C
AH29	VCC
AH30	VCC5D
AH31	N/C
AH32	N/C
AJ1	N/C
AJ2	N/C
AJ3	N/C
AJ4	VCC
AJ5	N/C
AJ6	N/C
AJ7	PBXARB#
AJ8	N/C
AJ9	PBRST#
AJ10	PBGNT[3]#
AJ11	PBGNT[0]#
AJ12	PBREQ[2]#
AJ13	PBCBE[3]#
AJ14	PBTRDY#
AJ15	PBLOCK#
AK23	VCC5D

Ball Number	Signal
AJ17	REQ64#
AJ18	PACBE[1]#
AJ19	PALOCK#
AJ20	PATRDY#
AJ21	PACBE[3]#
AJ22	PAREQ[2]#
AJ23	PAGNT[0]#
AJ24	PAGNT[3]#
AJ25	PARST#
AJ26	MODE64#
AJ27	PAXARB#
AJ28	N/C
AJ29	VCC
AJ30	N/C
AJ31	N/C
AJ32	N/C
AK1	N/C
AK2	VSS
AK3	N/C
AK4	VCC5D
AK5	N/C
AK6	N/C
AK7	VCC
AK8	N/C
AK9	VSS
AK10	PBGNT[4]#
AK11	VCC5D
AK12	PBREQ[3]#
AK13	VSS
AK14	PBIRDY#
AK15	VCC5D
AK16	PBPAR
AK17	VSS
AK18	PAPAR
AK19	VCC5D
AK20	PAIRDY#
AK21	VSS
AK22	PAREQ[3]#
AL28	N/C

Table 9-6. PXB Ball List (Continued)

Ball Number	Signal
AK24	PAGNT[4]#
AK25	VSS
AK26	PHOLD#
AK27	VCC
AK28	N/C
AK29	VCC5D
AK30	N/C
AK31	VSS
AK32	N/C
AL1	N/C
AL2	N/C
AL3	N/C
AL4	N/C
AL5	N/C
AL6	N/C
AL7	PBINTRQ#
AL8	N/C
AL9	PBMON[0]#
AL10	PBGNT[5]#
AL11	PBGNT[1]#
AL12	PBREQ[4]#
AL13	PBREQ[0]#
AL14	PBFRAME#
AL15	PBSTOP#
AL16	PBSERR#
AL17	ACK64#
AL18	PASERR#
AL19	PASTOP#
AL20	PAFRAME#
AL21	PAREQ[0]#
AL22	PAREQ[4]#
AL23	PAGNT[1]#
AL24	PAGNT[5]#
AL25	PAMON[0]#
AL26	PHLDA#
AL27	PAINTRQ#

Ball Number	Signal
AL29	N/C
AL30	N/C
AL31	N/C
AL32	N/C
AM1	N/C
AM2	N/C
AM3	VSS
AM4	VSS
AM5	VSS
AM6	N/C
AM7	VSS
AM8	N/C
AM9	VCC
AM10	N/C
AM11	VSS
AM12	PBREQ[5]#
AM13	VCC
AM14	PBCBE[2]#
AM15	VSS
AM16	PBPERR#
AM17	VCC
AM18	PAPERR#
AM19	VSS
AM20	PACBE[2]#
AM21	VCC
AM22	PAREQ[5]#
AM23	VSS
AM24	N/C
AM25	VCC
AM26	WSC#
AM27	VSS
AM28	VSS
AM29	VSS
AM30	VSS
AM31	N/C
AM32	VSS

Table 9-7. WXB Ball List

Ball Number	Signal
A01	N/C
A02	RSVD
A03	VCCP
A04	PAAD[17]
A05	PAAD[13]
A06	VCCP
A07	PACBE[0]#
A08	PAAD[6]
A09	VCCP
A10	PAAD[2]
A11	N/C
A12	N/C
A13	PBIDSEL[18]
A14	VSS
A15	PBAD[2]
A16	VCCP
A17	PBAD[6]
A18	PBCBE[0]#
A19	VCCP
A20	PBAD[13]
A21	PBAD[17]
A22	VCCP
A23	RSVD
A24	VSS
B01	RSVD
B02	VSS
B03	PAAD[23]
B04	PAAD[16]
B05	VSS
B06	PAAD[14]
B07	PAAD[11]
B08	VSS
B09	PAAD[4]
B10	PAAD[3]
B11	VSS
B12	PBIDSEL[16]
B13	PBIDSEL[17]
B14	VSS

Ball Number	Signal
B15	PBAD[3]
B16	PBAD[4]
B17	VSS
B18	PBAD[11]
B19	PBAD[14]
B20	VSS
B21	PBAD[16]
B22	PBAD[23]
B23	VSS
B24	RSVD
C01	VCC
C02	PAAD[27]
C03	PAAD[28]
C04	VCCP
C05	PAAD[22]
C06	PAAD[18]
C07	VCC
C08	PAAD[9]
C09	PAAD[7]
C10	VCCP
C11	PAAD[1]
C12	PAIDSEL[16]
C13	RSVD
C14	PBAD[1]
C15	VCCP
C16	PBAD[7]
C17	PBAD[9]
C18	VCC
C19	PBAD[18]
C20	PBAD[22]
C21	VCCP
C22	PBAD[28]
C23	PBAD[27]
C24	VCC
D01	PAGNT[0]#
D02	PAGNT[3]#
D03	VSS
D04	PAAD[29]

Table 9-7. WXB Ball List (Continued)

Ball Number	Signal
D05	PAAD[24]
D06	VSS
D07	PAAD[19]
D08	PACBE[1]#
D09	VSS
D10	PAAD[5]
D11	PAAD[0]
D12	VSS
D13	VSS
D14	PBAD[0]
D15	PBAD[5]
D16	VSS
D17	PBCBE[1]#
D18	PBAD[19]
D19	VSS
D20	PBAD[24]
D21	PBAD[29]
D22	VSS
D23	PBGNT[3]#
D24	PBGNT[0]#
E01	PAREQ[1]#
E02	VCCP
E03	PAPAR64
E04	PAREQ64#
E05	VCC
E06	PAAD[26]
E07	PACBE[2]#
E08	VCCP
E09	PAAD[15]
E10	PAAD[10]
E11	VCC
E12	PAIDSEL[18]
E13	RSVD
E14	VCC
E15	PBAD[10]
E16	PBAD[15]
E17	VCCP
E18	PBCBE[2]#
E19	PBAD[26]

Ball Number	Signal
E20	VCC
E21	PBREQ64#
E22	PBPAR64
E23	VCCP
E24	PBREQ[1]#
F01	VSS
F02	PAREQ[5]#
F03	PAGNT[2]#
F04	VSS
F05	PASERR#
F06	PAAD[30]
F07	VSS
F08	PAAD[25]
F09	PAAD[21]
F10	VSS
F11	PAAD[8]
F12	PAIDSEL[17]
F13	RSVD
F14	PBAD[8]
F15	VSS
F16	PBAD[21]
F17	PBAD[25]
F18	VSS
F19	PBAD[30]
F20	PBSERR#
F21	VSS
F22	PBGNT[2]#
F23	PBREQ[5]#
F24	VSS
G01	PASTOP#
G02	PAREQ[2]#
G03	VCC
G04	PAGNT[1]#
G05	PAACK64#
G06	VCCP
G07	PAAD[31]
G08	PACBE[3]#
G09	VCCP
G10	PAAD[20]

Table 9-7. WXB Ball List (Continued)

Ball Number	Signal
G11	PAAD[12]
G12	VCCP
G13	VCCP
G14	PBAD[12]
G15	PBAD[20]
G16	VCCP
G17	PBCBE[3]#
G18	PBAD[31]
G19	VCCP
G20	PBACK64#
G21	PBGNT[1]#
G22	VCC
G23	PBREQ[2]#
G24	PBSTOP#
H01	PAM66EN
H02	VSS
H03	PAREQ[0]#
H04	PAREQ[3]#
H05	VSS
H06	PAPERR#
H07	PAINTRQ#
H08	VSS
H09	VCC
H10	VSS
H11	VCC
H12	VSS
H13	VCC
H14	VSS
H15	VCC
H16	VSS
H17	VCC
H18	PBINTRQ#
H19	PBPERR#
H20	VSS
H21	PBREQ[3]#
H22	PBREQ[0]#
H23	VSS
H24	PBM66EN
J01	VCCP

Ball Number	Signal
J02	PAPAR
J03	PAFRAME#
J04	VCCP
J05	PAREQ[4]#
J06	PAGNT[5]#
J07	VCCP
J08	VCC
J09	VSS
J10	VCC
J11	VSS
J12	VCC
J13	VSS
J14	VCC
J15	VSS
J16	VCC
J17	VSS
J18	VCCP
J19	PBGNT[5]#
J20	PBREQ[4]#
J21	VCCP
J22	PBFRAME#
J23	PBPAR
J24	VCCP
K01	PAAD[33]
K02	PARST#
K03	VSS
K04	PALOCK#
K05	PATRDY#
K06	VSS
K07	PAGNT[4]#
K08	VSS
K09	VCC
K10	VSS
K11	VCC
K12	VSS
K13	VCC
K14	VSS
K15	VCC
K16	VSS

Table 9-7. WXB Ball List (Continued)

Ball Number	Signal
K17	VCC
K18	PBGNT[4]#
K19	VSS
K20	PBTRDY#
K21	PBLOCK#
K22	VSS
K23	PBRST#
K24	PBAD[33]
L01	PAAD[37]
L02	VCCP
L03	PAAD[35]
L04	PAAD[32]
L05	VCC
L06	PAIRDY#
L07	PADEVSEL#
L08	VCC
L09	VSS
L10	VCC
L11	VSS
L12	VCC
L13	VSS
L14	VCC
L15	VSS
L16	VCC
L17	VSS
L18	PBDEVSEL#
L19	PBIRDY#
L20	VCC
L21	PBAD[32]
L22	PBAD[35]
L23	VCCP
L24	PBAD[37]
M01	N/C
M02	PAAD[38]
M03	PAAD[39]
M04	VSS
M05	PAAD[36]
M06	PAAD[34]
M07	VSS

Ball Number	Signal
M08	VSS
M09	VCC
M10	VSS
M11	VCC
M12	VSS
M13	VCC
M14	VSS
M15	VCC
M16	VSS
M17	VCC
M18	VSS
M19	PBAD[34]
M20	PBAD[36]
M21	VSS
M22	PBAD[39]
M23	PBAD[38]
M24	N/C
N01	N/C
N02	PACBE[4]#
N03	VCC
N04	PAAD[42]
N05	PAAD[46]
N06	VCCP
N07	PAAD[45]
N08	VCC
N09	VSS
N10	VCC
N11	VSS
N12	VCC
N13	VSS
N14	VCC
N15	VSS
N16	VCC
N17	VSS
N18	PBAD[45]
N19	VCCP
N20	PBAD[46]
N21	PBAD[42]
N22	VCC

Table 9-7. WXB Ball List (Continued)

Ball Number	Signal
N23	PBCBE[4]#
N24	N/C
P01	PAAD[40]
P02	VSS
P03	PAAD[41]
P04	PACBE[5]#
P05	VSS
P06	PAAD[52]
P07	PAAD[55]
P08	VSS
P09	VCC
P10	VSS
P11	VCC
P12	VSS
P13	VCC
P14	VSS
P15	VCC
P16	VSS
P17	VCC
P18	PBAD[55]
P19	PBAD[52]
P20	VSS
P21	PBCBE[5]#
P22	PBAD[41]
P23	VSS
P24	PBAD[40]
R01	VCCP
R02	PAAD[44]
R03	PAAD[47]
R04	VCC
R05	PAAD[53]
R06	PAAD[60]
R07	VCCP
R08	VCC
R09	VSS
R10	VCC
R11	VSS
R12	VCC
R13	VSS

Ball Number	Signal
R14	VCC
R15	VSS
R16	VCC
R17	VSS
R18	VCCP
R19	PBAD[60]
R20	PBAD[53]
R21	VCC
R22	PBAD[47]
R23	PBAD[44]
R24	VCCP
T01	PAAD[43]
T02	PAAD[49]
T03	VSS
T04	PAAD[51]
T05	PAAD[59]
T06	VSS
T07	HASIL#
T08	VSS
T09	VCC
T10	VSS
T11	VCT
T12	VSS
T13	VCT
T14	VSS
T15	VCT
T16	VSS
T17	VCC
T18	HBSIL#
T19	VSS
T20	PBAD[59]
T21	PBAD[51]
T22	VSS
T23	PBAD[49]
T24	PBAD[43]
U01	PAAD[48]
U02	VCCP
U03	PAAD[50]
U04	PAAD[61]

Table 9-7. WXB Ball List (Continued)

Ball Number	Signal
U05	VCCP
U06	HASOD
U07	HASOL
U08	VCC
U09	VSS
U10	VCT
U11	VSS
U12	VCT
U13	VSS
U14	VCT
U15	VSS
U16	VCT
U17	VSS
U18	VSS
U19	HBSOD
U20	VCCP
U21	PBAD[61]
U22	PBAD[50]
U23	VCCP
U24	PBAD[48]
V01	VSS
V02	PAAD[54]
V03	PAAD[57]
V04	VSS
V05	HASID
V06	HASOC
V07	VSS
V08	RSVD
V09	PACLK[0]
V10	VSS
V11	XBINIT#
V12	XD[15]#
V13	VCT
V14	VSS
V15	TRST#
V16	VSS
V17	TDI
V18	TCK
V19	VSS

Ball Number	Signal
V20	HBSIC
V21	VSS
V22	PBAD[57]
V23	PBAD[54]
V24	VSS
W01	PACBE[6]#
W02	PAAD[58]
W03	VCC
W04	HAINTRQ#
W05	HASIC
W06	VCCP
W07	RSVD
W08	PACLKREF
W09	VCCP
W10	PACLK[1]
W11	XRST#
W12	VCT
W13	XIB#
W14	XD[0]#
W15	VCT
W16	VSS (RSVD)
W17	PAMON(1)#
W18	VCCP
W19	TDO
W20	HBSOL
W21	HBSID
W22	VCC
W23	PBAD[58]
W24	PBCBE[6]#
Y01	PAAD[56]
Y02	VSS
Y03	PAAD[63]
Y04	HASOR#
Y05	VSS
Y06	N/C
Y07	PWRGD
Y08	VSS
Y09	PACLK[2]
Y10	XD[10]#

Table 9-7. WXB Ball List (Continued)

Ball Number	Signal
Y11	VSS
Y12	XD[12]#
Y13	XD[1]#
Y14	VSS
Y15	XD[3]#
Y16	LONGXB[0]#
Y17	VSS
Y18	VSS (RSVD)
Y19	VSS (RSVD)
Y20	VSS
Y21	HBSOR#
Y22	PBAD[63]
Y23	VSS
Y24	PBAD[56]
AA01	VCCP
AA02	PACBE[7]#
AA03	HASORR#
AA04	VCCP
AA05	N/C
AA06	PACLKFB
AA07	VCC
AA08	XCLK
AA09	XPAR#
AA10	VCT
AA11	XD[11]#
AA12	VREF
AA13	VCT
AA14	XD[6]#
AA15	XHRTS#
AA16	VCT
AA17	CRES[1]
AA18	SERROUT#
AA19	VCC
AA20	VCCP (RSVD)
AA21	HBSOC
AA22	VCCP
AA23	PBCBE[7]#
AA24	VCCP
AB01	PAAD[62]

Ball Number	Signal
AB02	VCCA[2]
AB03	VSS
AB04	VSS (RSVD)
AB05	PBCLKREF
AB06	VSS
AB07	PBCLKFB
AB08	XADS#
AB09	VSS
AB10	XBE[0]#
AB11	XD[9]#
AB12	VSS
AB13	XHSTBP#
AB14	VSS
AB15	VSS
AB16	XD[8]#
AB17	XD[5]#
AB18	VSS
AB19	VSS (RSVD)
AB20	PBMON(1)#
AB21	VSS
AB22	HBINTRQ#
AB23	HBSORR#
AB24	PBAD[62]
AC01	VCCA[1]
AC02	VCC
AC03	VCCP (RSVD)
AC04	PBCLK[0]
AC05	VCCP
AC06	PBCLK[2]
AC07	XBLK#
AC08	VCT
AC09	XBE[1]#
AC10	VSS
AC11	VCT
AC12	XD[2]#
AC13	XHSTBN#
AC14	VCT
AC15	XXSTBN#
AC16	XXSTBP#

Table 9-7. WXB Ball List (Continued)

Ball Number	Signal
AC17	VCT
AC18	CRES[0]
AC19	VSS (RSVD)
AC20	VCCP
AC21	TMS
AC22	VSS (RSVD)
AC23	VCC
AC24	VCCP (RSVD)
AD01	VSS
AD02	VSSA
AD03	VCCA[0]
AD04	VSS
AD05	PBCLK[1]
AD06	XXRTS#
AD07	VSS
AD08	XD[14]#

Ball Number	Signal
AD09	XD[4]#
AD10	VSS
AD11	XD[13]#
AD12	N/C
AD13	N/C
AD14	VSS
AD15	XD[7]#
AD16	VSS
AD17	LONGXB[1]#
AD18	VSS (RSVD)
AD19	VSS
AD20	PAMON(0)#
AD21	PBMON(0)#
AD22	VSS
AD23	RSVD
AD24	VCCP (RSVD)

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10.1 567-ball OLGA1 Package Information (SAC, SDC and WXB Components)

The 567-ball OLGA1 package has an exposed die mounted on a PCB substrate. A heatsink, with appropriate interface material and retention capabilities, is required for proper operation. For heatsink suggestions, please refer to the "Intel® 82460GX Chipset OLGA1 Package, Manufacturing, Mechanical, and Thermal Design Guide"

Figure 10-1. 567-ball OLGA1 Package Dimensions – Top View

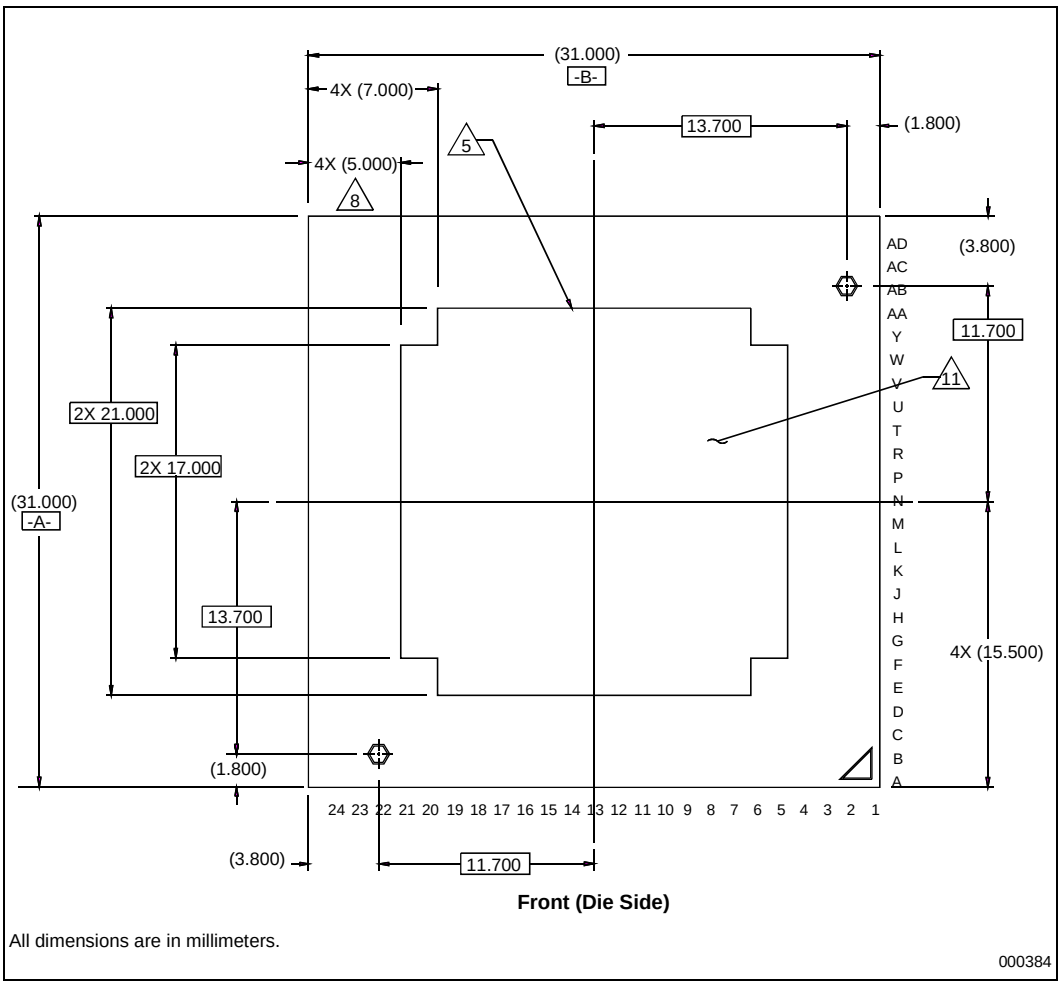


Figure 10-2. 567-ball OLGA1 Package Dimensions – Bottom View

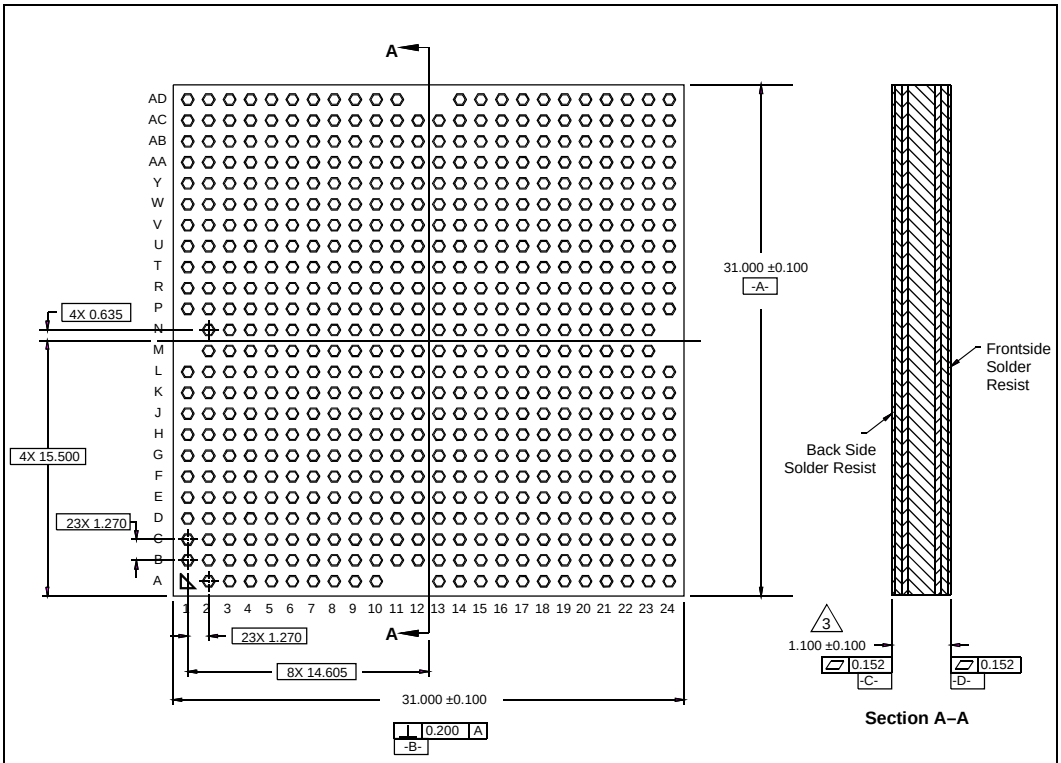


Table 10-1. Surface-Mount OLGA1 Package Specifications

Parameter	Min	Max	Unit
Overall height, as delivered (top of die to bottom of ball)	2.29	2.79	mm
Substrate height, as delivered	1.0	1.2	mm
Substrate Flatness	–	0.152	mm
Die Height	0.84 REF		mm
Ball Diameter	0.78 REF		mm
Package Width	30.90	31.10	mm
Die Width per Component			
SAC	12.24534 REF		mm
SDC	8.99414 REF		mm
WXB	10.69848 REF		mm
Die Length per Component			
SAC	10.62482 REF		mm
SDC	8.9916 REF		mm
WXB	12.41044 REF		mm
Package Length	30.90	31.10	mm
Ball Pitch	1.27		mm
Exclusion Outline to Edge of Substrate	5.00 REF		mm

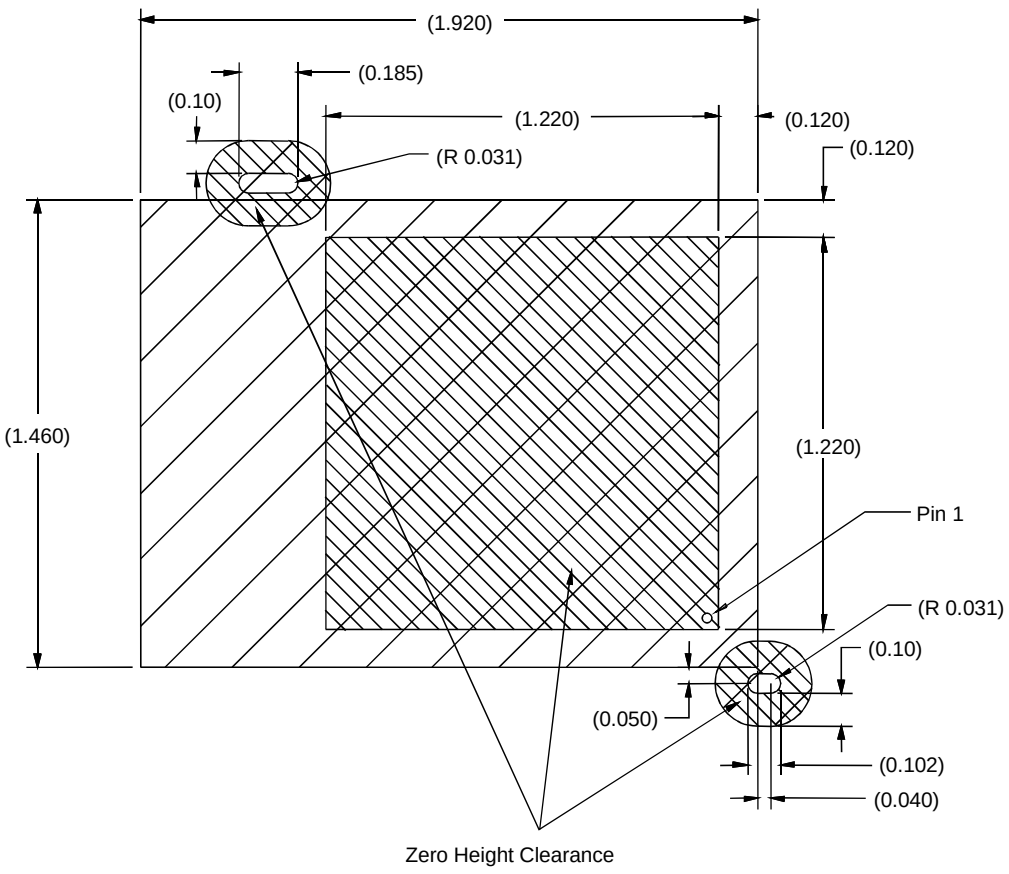
Table 10-1. Surface-Mount OLGA1 Package Specifications (Continued)

Parameter	Min	Max	Unit
Exclusion Outline to Edge of Substrate at Corner	7.00 REF		mm
Ball Count	567		ea.
Outer Ball Center to Edge of Package	0.895 REF		mm
Maximum Allowable Pressure on the Die for Thermal Solution	–	689	kPa

10.2 Keepout Areas

The PCB, designed to receive the OLGA1 package, should provide adequate clearance for thermal attachment around the OLGA1 package. To permit such an assembly, it is recommended that the PCB area reserved for the OLGA1 package and thermal solutions be defined as shown in Figure 10-3 for the SAC/SDC and Figure 10-4 for the WXB. The double cross-hatched area indicates locations where there is a zero height clearance. These areas are made up of the OLGA1 package dimensions and the keepout area around the through holes. The single cross-hatched area indicates a non-zero height clearance where passive components can be placed underneath the heatsink. The maximum component height in this non-zero height clearance area is 0.050”[1.27mm]. Since the retention wire clip is designed to protrude from the through holes, a keepout area on the secondary side of the PCB (opposite of the OLGA1 package) is required to prevent interference. This keepout area is illustrated in Figure 10-5. The clearance areas define only final position clearances, and do not reflect additional space required for tools and manufacturing procedures.

Figure 10-3. PCB Keepout Area for SAC and SDC



NOTES:

1. Reference dimensions are in inches.

000891

Figure 10-4. PCB Keepout Area for WXB

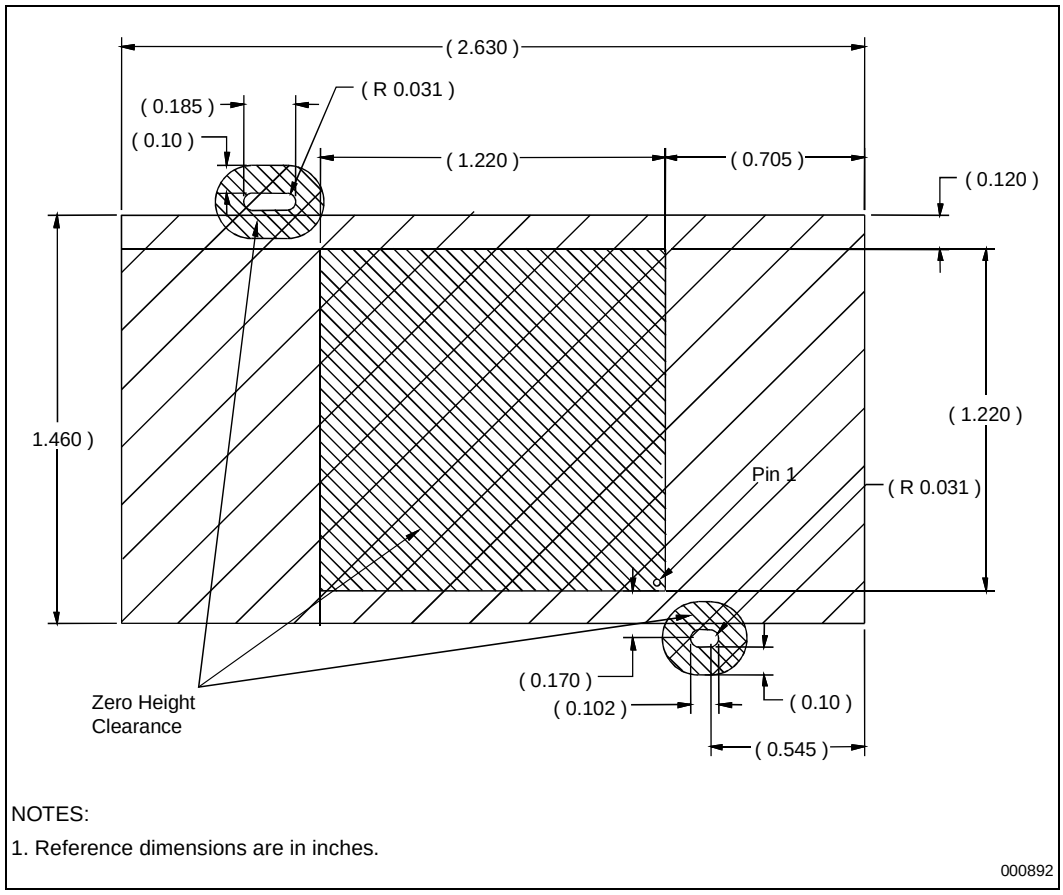
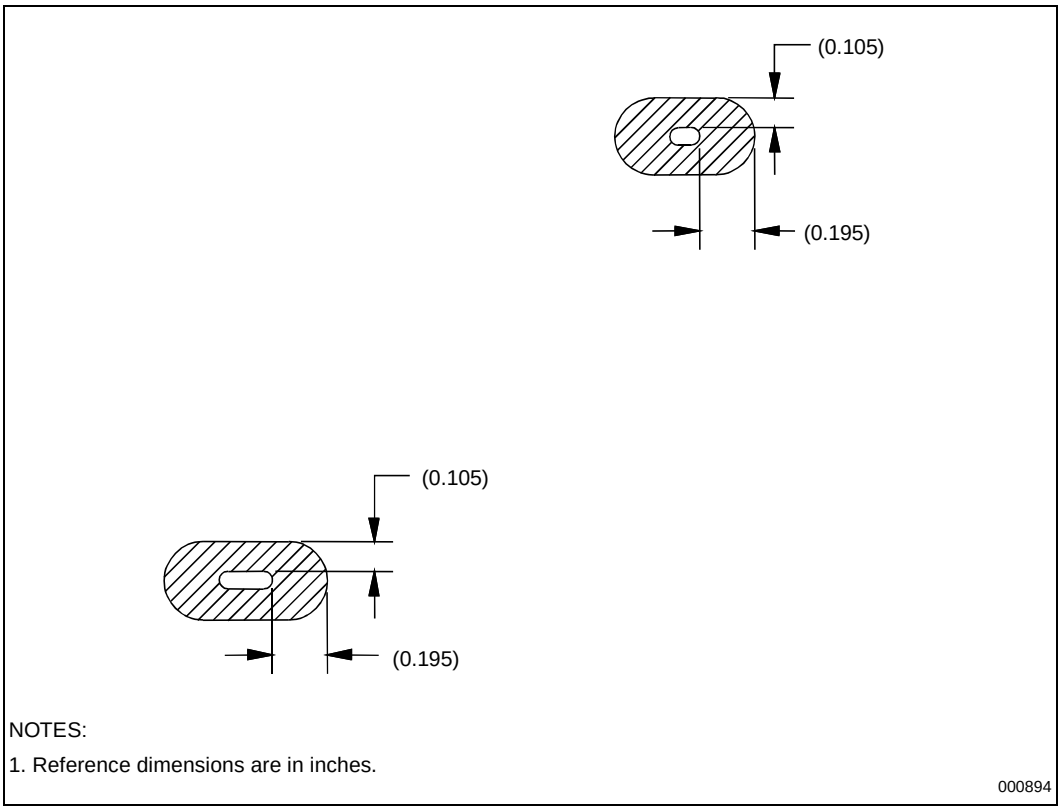


Figure 10-5. Board Keepout Area Around Through Holes (Secondary Side)



NOTES:
1. Reference dimensions are in inches.

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10.3 540-ball PLGA Package Information (PXB and GXB Components)

Figure 10-6. 540-ball PLGA Package Dimensions – Top View of Exposed Vias

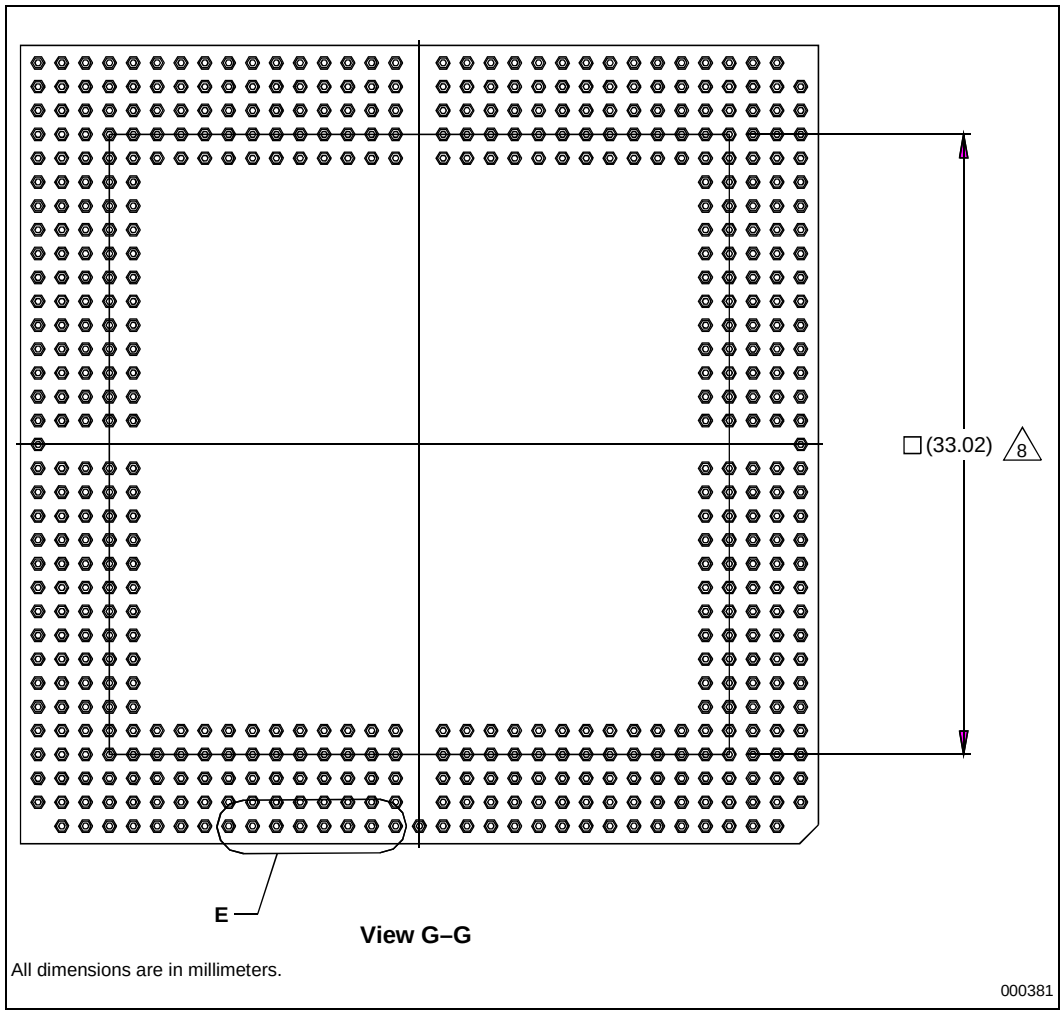
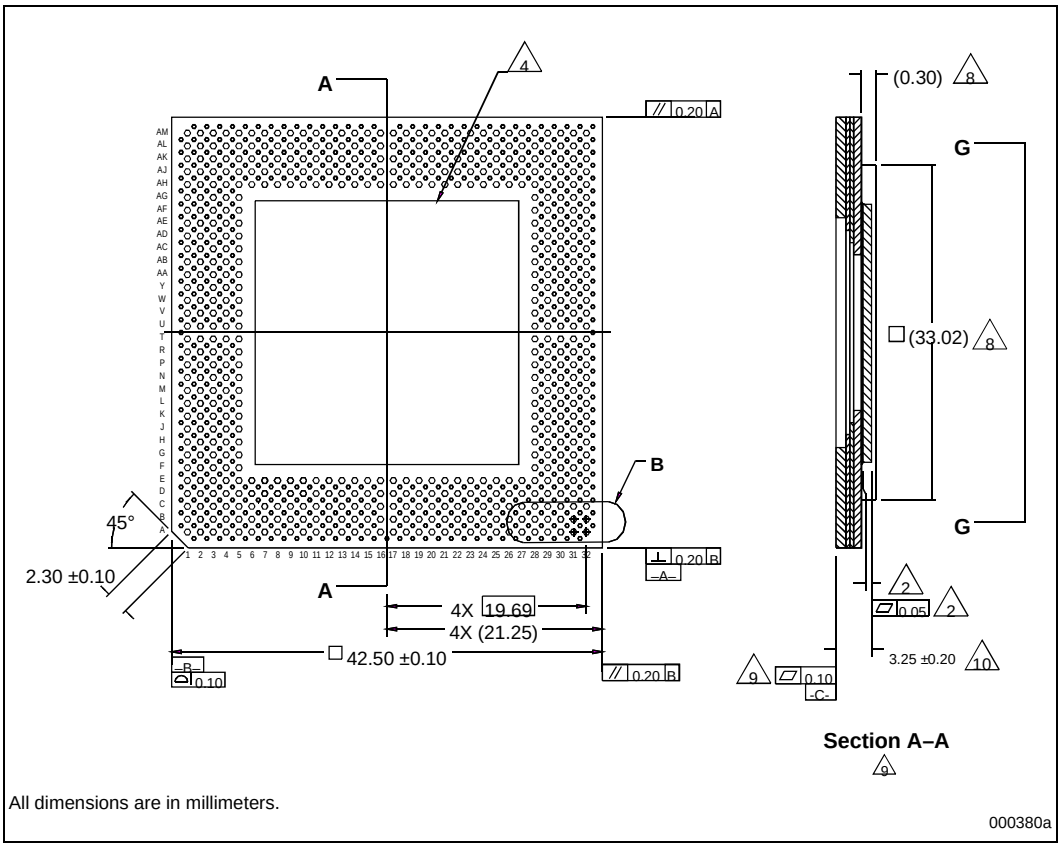


Figure 10-7. 540-ball PLGA Package Dimensions – Bottom View of Exposed Balls and Vias



10.4 324-ball BGA Package Information (MAC and MDC Components)

Figure 10-8 and Figure 10-9 provide the mechanical dimensions of the 324-ball BGA package.

Figure 10-8. 324-ball BGA Package Dimensions – Top View

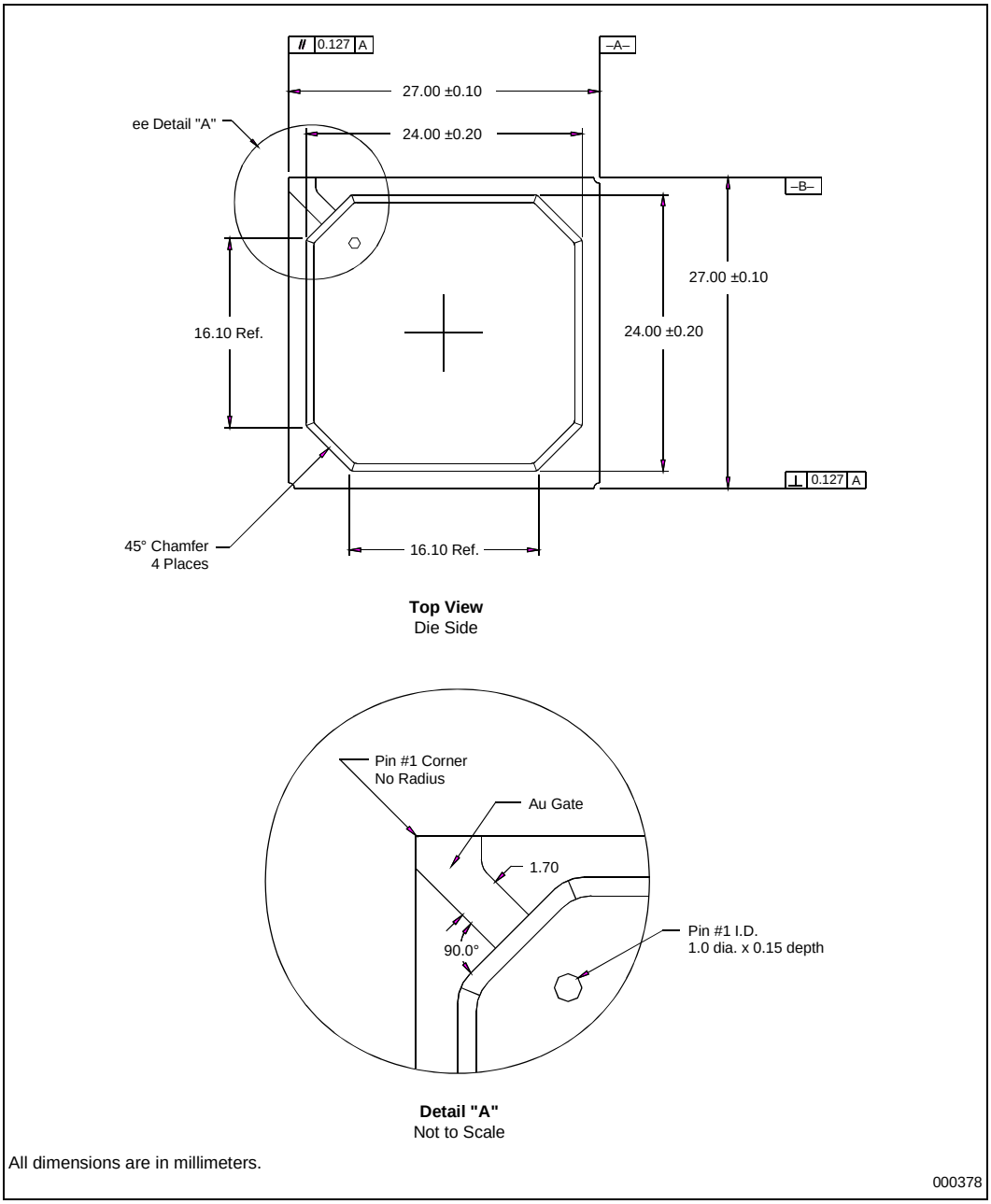
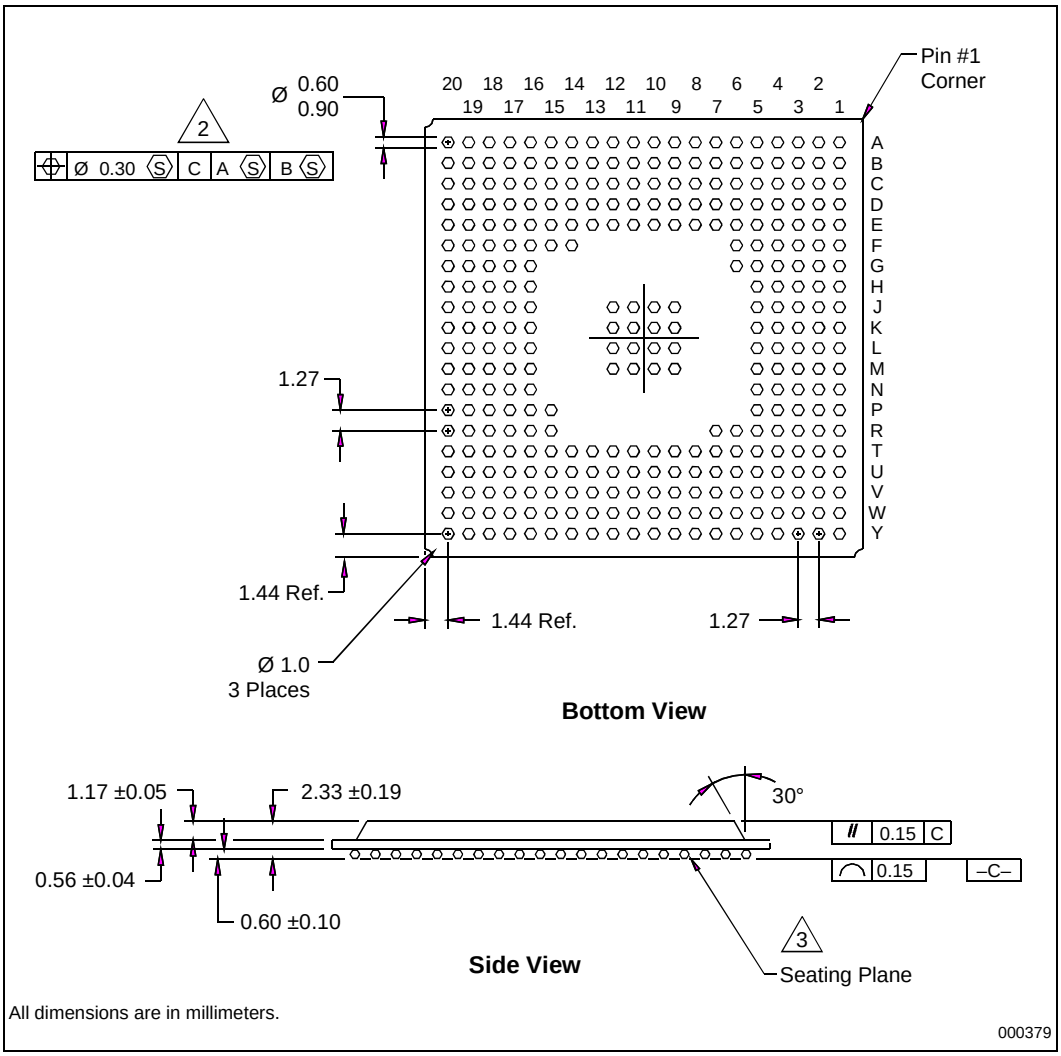


Figure 10-9. 324-ball BGA Package Dimensions – Bottom and Side Views



I/O Firmware Bridge (IFB) 11

This chapter contains the electrical and thermal specifications for the IFB. The IFB is a multi-function PCI device implementing a PCI IDE function, a universal serial bus host/hub function, an SMBus interface function, and power management functions.

11.1 Electrical Characteristics

11.2 Absolute Maximum Ratings

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only. Operating beyond the "Operating Conditions" is not recommended and extended exposure beyond "Operating Conditions" may affect reliability.

Table 11-1. Absolute Maximum Ratings

Parameter	Maximum Rating
Case Temperature under Bias	0^{o}C to +85^{o}C
Storage Temperature	–55^{o}C to +150^{o}C
Voltage on Any 3.3V Pin with Respect to Ground	0.3V to Vcc +0.3V
Voltage on Any 5V Tolerant Pin with Respect to Ground (V_{REF}=5V)	–0.3V to V_{REF} +0.3V
3.3V Supply Voltage with Respect to Vss	–0.3V to +4.6V
5.0V Supply Voltage with Respect to Vss (Vref)	–0.3V to +5.5V
Maximum Power Dissipation	1W

11.3 Thermal Characteristics

The 82468GX IFB (BGA) is designed for operation at case temperatures between 0^{o}C and 85^{o}C. The thermal resistances of the package are given in Table 11-2.

Table 11-2. Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0(0)	1.0 (196.9)
θ_{JC} (^{0}C/Watt)	29	24.5

11.4 DC Characteristics

Table 11-3. DC Characteristics

Functional Operating Range (VREF = 5V ±5%, VCC = 3.3v ±0.3V, T_{CASE} = 0°C to 85°C)					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes/Conditions**
Vcc(RTC)	Battery Voltage	2.0	3.6	V	
Vcc(SUS)	Battery Voltage	3.0	3.6	V	
V_{IL1}	Input Low Voltage	-0.5	0.3Vcc	V	a
V_{IH1}	Input High Voltage	0.5Vcc	Vcc + 0.5	V	a
V_{IL2}	Input Low Voltage	–0.3	0.6	V	a
V_{IH2}	Input High Voltage	1.4	Vcc+0.3	V	a
V_{IL3}	Input Low Voltage	–0.5	0.8	V	a
V_{IH3}	Input High Voltage	2.0	Vcc5 + 0.5	V	a
V_{OL1}	Output Low Voltage		0.4	V	a, @ I_{OL}=4mA
V_{OH1}	Output High Voltage	Vcc - 0.5		V	a, @ I_{OH}=-1mA
V_{OL2}	Output Low Voltage		0.4	V	a, @ I_{OL}=3mA
V_{OH2}	Output High Voltage	Vcc - 0.5		V	a, @ I_{OH}=-2mA
V_{OL3}	Output Low Voltage		0.4	V	a, @ I_{OL}=6mA
V_{OH3}	Output High Voltage	Vcc - 0.5		V	a, @ I_{OH}=-2mA
V_{OL4}	Output Low Voltage		0.4	V	a, @ I_{OL}=7mA
V_{OH4}	Output High Voltage	Vcc - 0.5		V	a, @ I_{OH}=-2mA
V_{OL5}	Output Low Voltage		0.3	V	a, b, @ I_{OL}=2mA
V_{OH5}	Output High Voltage	2.8	3.6	V	a, b, @ I_{OH}=-0.25mA
V_{DI}	Differential Input Sensitivity	0.2		V	|(USBPX+,USBPX-)|
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Includes V_{DI}
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V	Figure 11-18.
V_{SE}	Single Ended Rcvr Threshold	0.8	2.0	V	
I_{LI1}	Input Leakage Current		± 1	uA	
I_{LI2}	Hi-Z State Data Line Leakage	–10	+10	uA	(0V< V_{IN}< 3.3V)
C_{IN}	Input Capacitance		12	pF	F_C = 1MHz
C_O	Output Capacitance		12	pF	F_C = 1MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1MHz
C_L	Crystal Load Capacitance	NA	NA	pF	c

a. Refer to Table 11-5 for the signals associated with this specification.
b. V_{OL5} assumes R_L of 1.5KΩ to 3.6V and V_{OH5} assumes R_L of 15KΩ to GND.
c. The IFB requires an external oscillator.

Table 11-4. DC Current Characteristics

Functional Operating Range (VREF = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)					
Symbol	**Parameter**	**Typ**	**Max**	**Unit**	**Notes**
Icc(3V)	Vcc Supply Current	110	155	mA	
Icc(SUS) ON	Suspend Well Supply Current - Full On	3	5	mA	
Icc(SUS) POS/ STR	Suspend Well Supply Current - Power On Suspend or Suspend to RAM	30	150	µA	
Icc(SUS) STD/Soff	Suspend Well Supply Current - Suspend to Disk or Soft Off	9	150	µA	
Icc(RTC)	Battery Standby Current	4	6	µA	Vcc(RTC)=3.0v Mech. Off

Table 11-5. DC Characteristic Signal Association

Symbol	Associated Signals
V_{IL1} / V_{IH1}[a]	**USB Signals:** USBP[1:0]+, USBP[1:0]- **Power Management Signals:** RI#, PWRBTN# **CPU Signals:** FERR# **RTC Signals**([b])**:** RTCX1, RTCX2 **Misc. Signals:** RSMRST#, PWROK, TEST#, RTEST, GPIO[8:0], ECCINT#
V_{IL2} / V_{IH2}	**SMBus Signals:** SMBDATA, SMBCLK
V_{IL3} / V_{IH3} (5V Tolerant)[c]	**PCI Signals:** AD[31:0], C/BE[3:0]#, IDSEL, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PHLDA#, PCICLK, SERR# **IDE Signals:** PDD[15:0], PDDRQ, PIORDY, SDD[15:0], SDDRQ, SIORDY **Interrupt Signals:** IRQ[1,3:7,9:11,14:15], IRQ12/M, SERIRQ, PIRQ[A:D]#, IRQ8#, FEMPTY#, IRQ0, SCI **USB Signals:** USBCLK, OC[1:0]# **Power Management Signals:** THRM# **CPU Signals:** RCIN#, A20GATE **LPC Signals:** LFRAME#, LAD[3:0], LDRQ[1:0]# **Misc. Signals:** OSC, GPIO[22:10]
V_{OL1} / V_{OH1}	**IDE Signals:** PDCS1#, PDCS3#, PDA[2:0], PDD[15:0], PDDAK#, PDIOR#, PDIOW#, SDCS1#, SDCS3#, SDA[2:0], SDD[15:0], SDDAK#, SDIOR#, SDIOW#
V_{OL2} / V_{OH2}	**Power Management Signals:** SUS[B:C]#, SUS_STAT#, SUSCLK **CPU Signals:** IGNNE#, INTR, NMI, A20M# **SMBus Signals:** SMBCLK, SMBDATA **Misc. Signals:** SPKR, GPIO[21:0]
V_{OL3} / V_{OH3}	**PCI Signals:** AD[31:0], C/BE[3:0]#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, PHOLD#, PCIRST#, SERR# **Interrupt Signals:** SERIRQ, PIRQ[A:D]# **CPU Signals:** SMI#, STPCLK# **LPC Signals:** LFRAME#, LAD[3:0]
V_{OL4} / V_{OH4}	**USB Signals:** USBP[1:0]+, USBP[1:0]-
V_{OL5} / V_{OH5}	**CPU Signals:** INIT#, SLP#

a. This voltage specification applies to all signals listed as 5V tolerant (VIL3/VIH3) when Vref = 3V.
b. The voltage to the RTCVB pin should be match the vendor's external oscillator specifications.
c. These signals are 5V tolerant when Vref = 5V.

11.5 AC Characteristics

System Power Management Timings
Refer to the "Intel® 460GX Chipset System Software Developer's Manual (Document Number: 248704)" for system power management timings.

Table 11-6. Clock Timings

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Unit**	**Notes**	**Figure**
PCI Clock (PCICLK)						
t1a	Period	30	33.3	ns		Figure 11-2
t1b	High Time	12		ns		Figure 11-2
t1c	Low Time	12		ns		Figure 11-2
t1d	Rise Time		3	ns		Figure 11-2
t1e	Fall Time		3	ns		Figure 11-2
Oscillator Clock (OSC)						
t1l	Period	67	70	ns		Figure 11-2
t1m	High Time	20				Figure 11-2
t1n	Low time	20		ns		Figure 11-2
USB Clock (USBCLK)						
f_{clk48}	Operating Frequency	48		MHz		
t1p	Frequency Tolerance		±2500	ppm	a	
t1q	High Time	7		ns		Figure 11-2
t1r	Low time	7		ns		Figure 11-2
t1s	Rise Time		1.2	ns		Figure 11-2
t1t	Fall Time		1.2	ns		Figure 11-2
Suspend Clock (SUSCLK)						
f_{susclk}	Operating Frequency	32		KHz		
t1v	High time	10		µs		Figure 11-2
t1w	Low Time	10		µs		Figure 11-2
SMBus Clock (SMBCLK)						
f_{smb}	Operating Frequency	10	16	KHz		
t2b	High time	4.0	50	µs	b	Figure 11-20
t2c	Low time	4.7		µs		Figure 11-20
t2d	Rise time		1000	ns		Figure 11-20
t2e	Fall time		300	ns		Figure 11-20

a. The USBCLK is a 48Mhz that expects a 40/60% duty cycle.
b. The maximum high time (t2b Max) provide a simple method for devices to detect bus idle conditions.

Table 11-7. Reset Timings

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Figure**
t3a	PCIRST# Driven Inactive After SUS_STATx# is Driven Inactive.		1	RTCCLK		Figure 11-3
t3b	PCIRST# Active Pulse Width. Initiated via the RC Register.	1		ms		Figure 11-4
t3c	PWROK Rise Time		10	ns	a	

a. t3c is measured as a transition time through the threshold region Vol=0.8V and Voh=2.0V

Table 11-8. Interrupt, NMI and Miscellaneous Timings

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)								
Sym	**Parameter**	**Min**	**Max**	**Units**	**Type**	**Size**	**Notes**	**Figure**
INTERRUPT AND NMI TIMINGS								
	NMI Timing							
t23a	SERR# Active to NMI Driven Active		200	ns				Figure 11-5
	Interrupt Timing							
t24a	FEMPTY# Inactive Pulse Width	30		ns				Figure 11-6
t24a	IRQx, SCI Inactive Pulse Width	100		ns				Figure 11-6
MISCELLANEOUS TIMINGS								
	Mouse Timing Support							
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns				Figure 11-7
	Coprocessor Error Support							
t73b	IGNNE# Inactive from FERR# Inactive		230	ns				Figure 11-7
	Speaker Timing							
t76a	SPKR Valid Delay from OSC Rising		200	ns				Figure 11-8

Table 11-9. PCI Interface Timing

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Figure**
t77	AD[31:0] Valid Delay	2	11	ns	Min: 0pF Max: 50pF	Figure 11-9
t78	AD[31:0] Setup Time to PCICLK Rising	7		ns		Figure 11-10
t79	AD[31:0] Hold Time from PCICLK Rising	0		ns		Figure 11-10
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL#, Valid Delay from PCICLK Rising	2	11	ns	Min: 0pF Max: 50pF	Figure 11-9
t81	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL#, Output Enable Delay from PCICLK Rising	2		ns		Figure 11-13

Table 11-9. PCI Interface Timing (Continued)

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Figure**
t82	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL#, Float Delay from PCICLK Rising	2	28	ns		Figure 11-11
t83	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL#, Setup Time to PCICLK Rising	7		ns		Figure 11-10
t84	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, IDSEL, DEVSEL#, Hold Time from PCLKIN Rising	0		ns		Figure 11-10
t85	PHLD# Valid Delay from PCICLK Rising	2	12	ns	0pF	Figure 11-9
t86	PHLDA# Setup Time to PCICLK Rising	10		ns		Figure 11-10
t87	PHLDA# Hold Time from PCICLK Rising	0		ns		Figure 11-10
t88	PCIRST# Low Pulse Width	1		ms		Figure 11-12

Table 11-10. PCI Bus IDE Timing

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Figure**
Primary IDE Timing						
t102	PDIOW# Active From PCICLK Rising	2	20	ns		Figure 11-14, Figure 11-15
t103	PDIOW# Inactive From PCICLK Rising	2	20	ns	4	Figure 11-14, Figure 11-15
t104	PDIOR# Active From PCICLK Rising	2	20	ns		Figure 11-14, Figure 11-15
t105	PDIOR# Inactive From PCICLK Rising	2	20	ns		Figure 11-14, Figure 11-15
t106	PDA[2:0] Valid Delay From PCICLK Rising	2	30	ns		Figure 11-14
t107	PDCS1#, PDCS3# Active From PCICLK Rising	2	30	ns		Figure 11-14
t108	PDCS1#, PDCS3# Inactive From PCICLK Rising	2	30	ns		Figure 11-14
t113	PDDACK# Active From PCICLK Rising	2	20	ns		Figure 11-15
t114	PDDACK# Inactive From PCICLK Rising	2	20	ns		
t114a	PDDREQ Setup Time to PCICLK Rising	7		ns		Figure 11-15
t114b	PDDREQ Hold From PCICLK Rising	7		ns		Figure 11-15
t115	PDD[15:0] Valid Delay From PCICLK Rising	2	30	ns		Figure 11-14, Figure 11-15
t115a	PDD[15:0] Setup Time to PCICLK Rising	10		ns		Figure 11-14, Figure 11-15
t115b	PDD[15:0] Hold From PCICLK Rising	8		ns		Figure 11-14, Figure 11-15
t116	PIORDY Setup Time to PCICLK Rising	7		ns	1	Figure 11-14
t117	PIORDY Hold From PCICLK Rising	7		ns	1	Figure 11-14
t117a	PIORDY Inactive Pulse Width	48		ns	2,3	

Table 11-10. PCI Bus IDE Timing (Continued)

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Figure**
Secondary IDE Timing						
t102	SDIOW# Active From PCICLK Rising	2	20	ns		Figure 11-14, Figure 11-15
t103	SDIOW# Inactive From PCICLK Rising	2	20	ns		Figure 11-14, Figure 11-15
t104	SDIOR# Active From PCICLK Rising	2	20	ns		Figure 11-14, Figure 11-15
t105	SDIOR# Inactive From PCICLK Rising	2	20	ns		Figure 11-14, Figure 11-15
t106	SDA[2:0] Valid Delay From PCICLK Rising	2	30	ns		Figure 11-14
t107	SDCS1#, PDCS3# Active From PCICLK Rising	2	30	ns		Figure 11-14
t108	SDCS1#, PDCS3# Inactive From PCICLK Rising	2	30	ns		Figure 11-14
t113	SDDACK# Active From PCICLK Rising	2	20	ns		Figure 11-15
t114	SDDACK# Inactive From PCICLK Rising	2	20	ns		
t114a	SDDREQ Setup Time to PCICLK Rising	7		ns		Figure 11-15
t114b	SDDREQ Hold From PCICLK Rising	7		ns		Figure 11-15
t115	SDD[15:0] Valid Delay From PCICLK Rising	2	30	ns		Figure 11-14, Figure 11-15
t115a	SDD[15:0] Setup Time to PCICLK Rising	10		ns		Figure 11-14, Figure 11-15
t115b	SDD[15:0] Hold From PCICLK Rising	8		ns		Figure 11-14, Figure 11-15
t116	SIORDY Setup Time to PCICLK Rising	7		ns	1	Figure 11-14
t117	SIORDY Hold From PCICLK Rising	7		ns	1	Figure 11-14
t117a	SIORDY Inactive Pulse Width	48		ns		

NOTES:

1. IORDY is internally synchronized. This timing is to ensure recognition on the next clock.
2. PIORDY sample point from (P,S)DIOR#/(P,S)DIOW# assertion and PDIOR#/PDIOW# active pulse width is programmable from 2-5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register
3. PIORDY sample point from (P,S)DIOR#/(P,S)DIOW# assertion, PDIOR#/PDIOW# active pulse width and PDIOR#/PDIOW# inactive pulse width cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIM0/1 field in the IDE timing register.
4. PDIOR#/PDIOW# inactive pulse width is programmable from 1-4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.

Table 11-11. Universal Serial Bus Timing

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
Full Speed Source (Note [a])						
t122f	USBPx+, USBPx- Driver Rise Time	4	20	ns	[b], C_L = 50pF	Figure 11-16
t123f	USBPx+, USBPx- Driver Fall Time	4	20	ns	b, C_L = 50pF	Figure 11-16
t124f	Source Differential Driver Jitter To Next Transition For Paired Transitions	 –2 –1	 2 1	 ns ns	[c], [d]	Figure 11-17

Table 11-11. Universal Serial Bus Timing (Continued)

Functional Operating Range (V_{REF} = 5V ±5%, VCC = 3.3V ±0.3V, T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t125f	Source EOP Width	160	175	ns	e	Figure 11-18
t126l	Differential to SE0 Transition Skew	–2	5	ns	f	
t127f	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 –20 –10	 20 10	 ns ns	d	Figure 11-17
t128f	EOP Width Must reject as EOP Must accept as EOP	 40 85		 ns ns	e	Figure 11-18
t129f	Differential to SE0 Transition Skew	–2	5	ns	f	
Low Speed Source (Note g)						
t122l	USBPx+, USBPx- Driver Rise Time	75	 300	 ns ns	b, h C_L = 50pF C_L = 350pF	Figure 11-16
t123l	USBPx+, USBPx- Driver Fall Time	75	 300	 ns ns	b, h C_L = 50pF C_L = 350pF	Figure 11-16
t124l	Source Differential Driver Jitter To Next Transition For Paired Transitions	 –2 –1	 2 1	 ns ns	c, d	Figure 11-17
t125l	Source EOP Width	160	175	ns	e	Figure 11-18
t126l	Differential to SE0 Transition Skew	–2	5	ns	f	
t127l	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 –20 –10	 20 10	 ns ns	d	Figure 11-17
t128l	EOP Width Must reject as EOP Must accept as EOP	 40 85		 ns ns	e	Figure 11-18
t129l	Differential to SE0 Transition Skew	-2	5	ns	f	

a. Full Speed Data Rate has minimum of 11.97Mbps and maximum of 12.03Mbps
b. Driver output resistance under steady state drive is specified at 28 ohms at minimum and 43 ohms at maximum
c. Timing difference between the differential data signals
d. Measured at crossover point of differential data signals
e. Measured at 50% swing point of data signals
f. Measured from last crossover point to 50% swing point of data line at leading edge of EOP
g. Low Speed Data Rate has a minimum of 1.48Mbps and a maximum of 1.52Mbps
h. Measured from 10% to 90% of the data signal

Table 11-12. SMBUS Timing

Functional Operating Range (V_{REF} = 5V ±5%, Vcc=3.3V ±0.3V T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t141	Bus Tree Time Between Stop and Start Condition	4.7		µs		Figure 11-19
t142	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0		µs		Figure 11-19
t143	Repeated Start Condition Setup Time	4.7		µs		Figure 11-19
t144	Stop Condition Setup Time	4.0		µs		Figure 11-19
t145	Data Hold Time	300		ns		Figure 11-19

Table 11-12. SMBUS Timing (Continued)

Functional Operating Range (V_{REF} = 5V ±5%, Vcc=3.3V ±0.3V T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t146	Data Setup Time	250		ns		Figure 11-19
t147	Device Time Out	25	35	ms	a	Figure 11-19
t148	Cumulative Clock Low Extend Time (slave device)		25	ms	b	Figure 11-20
t149	Cumulative Clock Low Extend Time (master device)		10	ms	c	Figure 11-20

a. A device will timeout when any clock low exceeds this value.
b. t148 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
c. t149 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack or ack-to-stop.

Table 11-13. LPC Timing

Functional Operating Range (V_{REF} = 5V ±5%, Vcc=3.3V ±0.3V T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t180	LAD[3:0] Valid Delay from PCICLK Rising	2	11	ns		Figure 11-9
t181	LAD[3:0] Output Enable Delay from PCICLK Rising	2		ns		Figure 11-13
t182	LAD[3:0] Float Delay from PCICLK Rising		28	ns		Figure 11-11
t183	LAD[3:0] Setup Time to PCICLK Rising	7		ns		Figure 11-10
t184	LAD[3:0] Hold Time from PCICLK Rising	0		ns		Figure 11-10
t185	LDRQ[1:0]# Setup Time to PCICLK Rising	12		ns		Figure 11-10
t186	LDRQ[1:0]# Hold Time from PCICLK Rising	0		ns		Figure 11-10
t187	LFRAME# Valid Delay from PCICLK Rising	2	12	ns		Figure 11-9

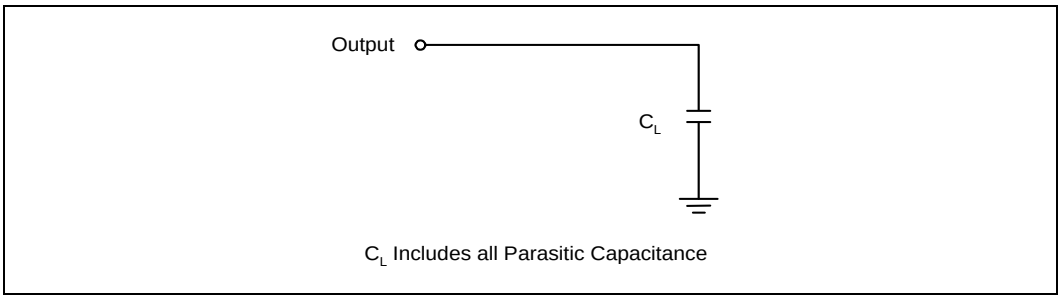
Table 11-14. General Purpose I/O Timing

Functional Operating Range (V_{REF} = 5V ±5%, Vcc=3.3v±0.3V T_{CASE} = 0°C to +85°C)						
Sym	**Parameter**	**Min**	**Max**	**Units**	**Notes**	**Fig**
t190	GPIO[8:0] Pulse Width	2		RTCC LK		Figure 11-12

Table 11-15. AC Test Loads

Capacitive Load	Signals
120pf	PCI
50pf	IDE, USB

Figure 11-1. Test Load



11.6 Clock and Reset Timing Diagrams

Figure 11-2. General Clock Timing

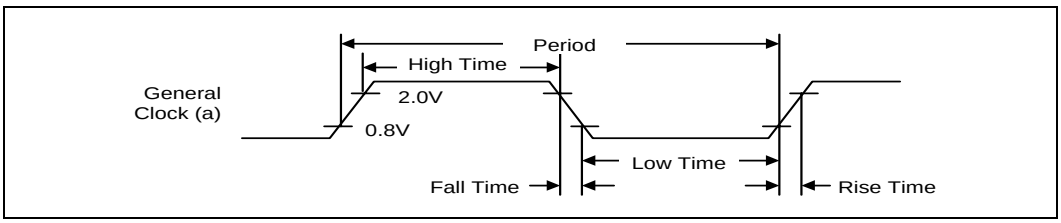


Figure 11-3. Reset Inactive Timing

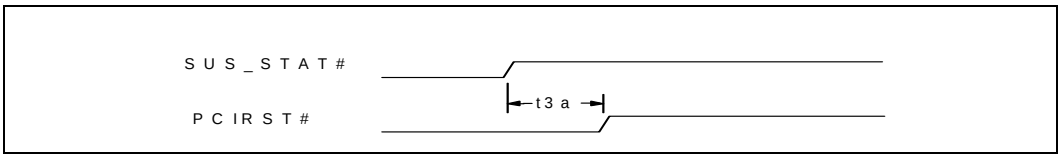
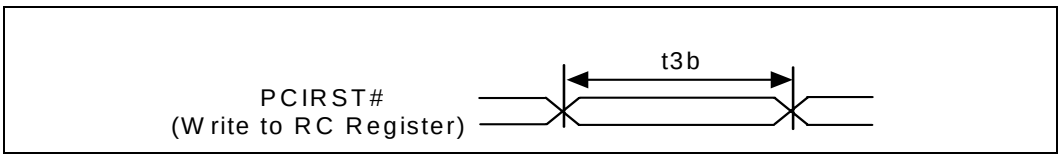


Figure 11-4. Reset Active Pulse Width



11.7 Miscellaneous Timing Diagrams

Figure 11-5. NMI Timing

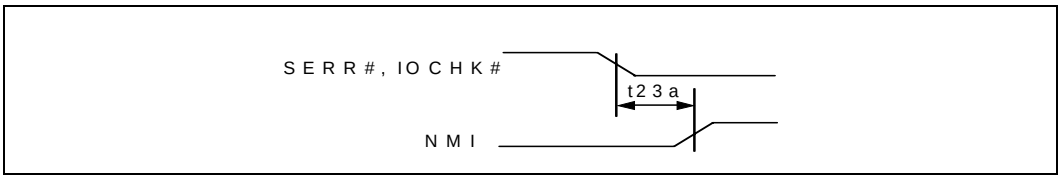


Figure 11-6. Interrupt Timing

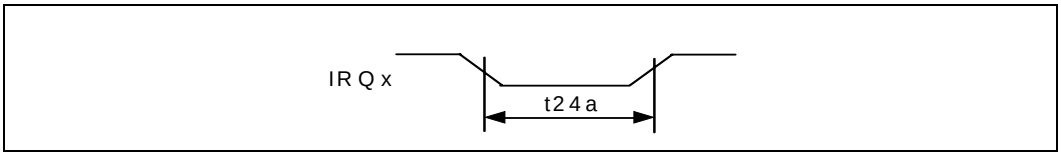


Figure 11-7. Coprocessor Error and Mouse Support Timing

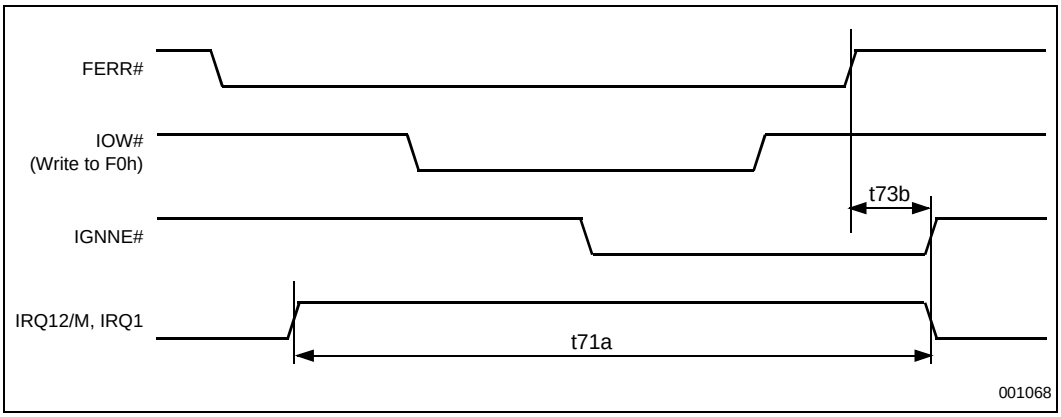
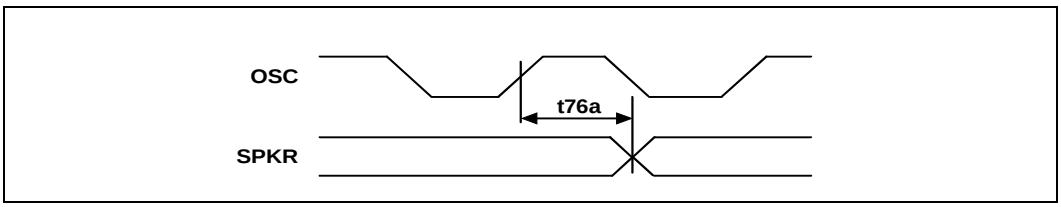


Figure 11-8. Speaker Timing



11.8 PCI, LPC and Serial IRQ Timing Diagrams

Figure 11-9. Valid Delay from Rising Clock Edge

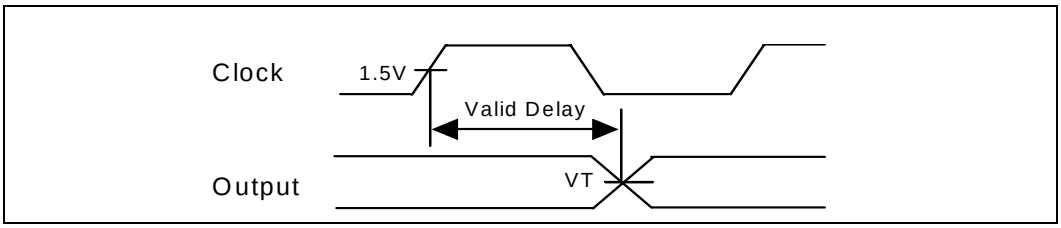


Figure 11-10. Setup and Hold Times

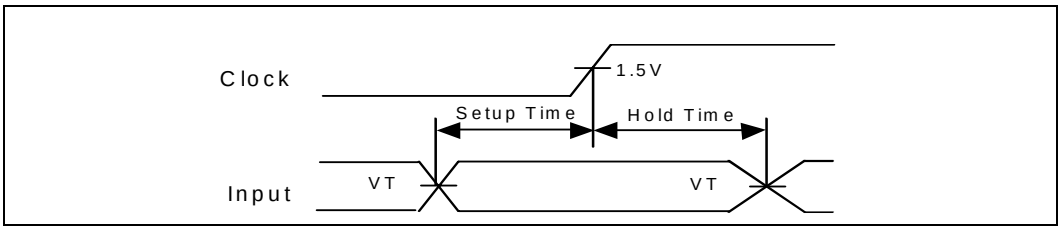


Figure 11-11. Float Delay

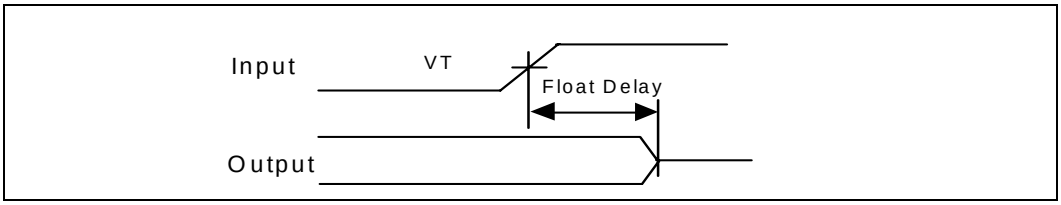


Figure 11-12. Pulse Width

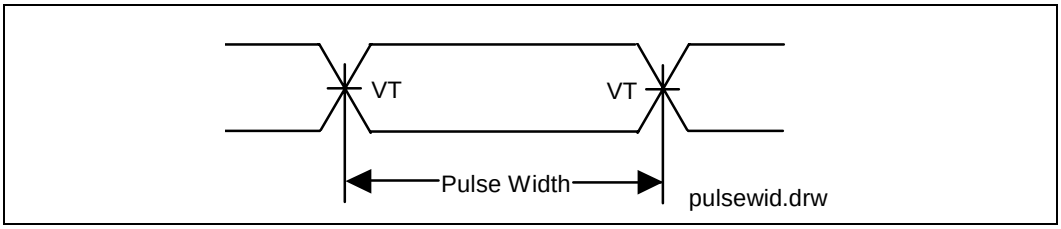
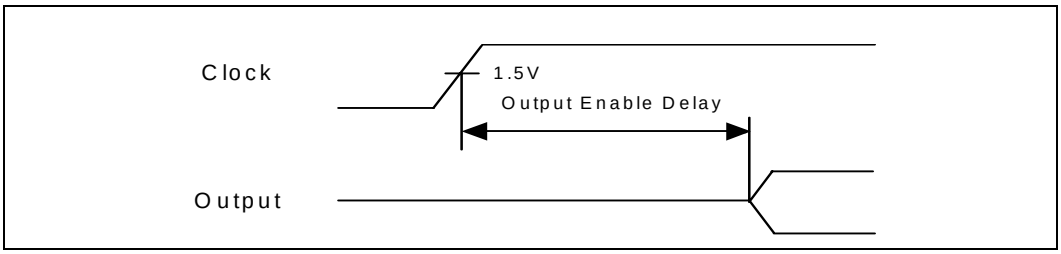


Figure 11-13. Output Enable Delay



11.9 IDE Timing Diagrams

Figure 11-14. IDE PIO Mode

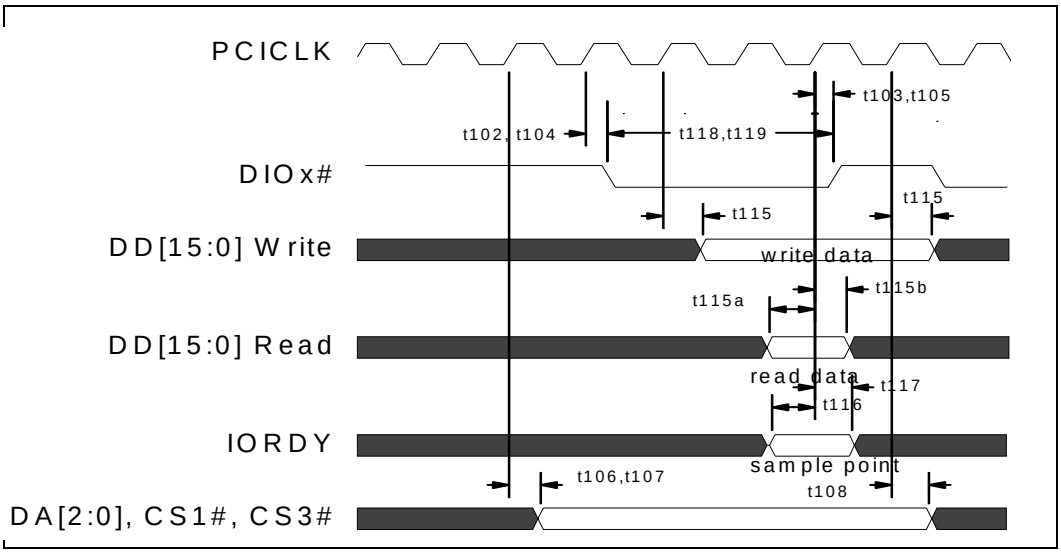
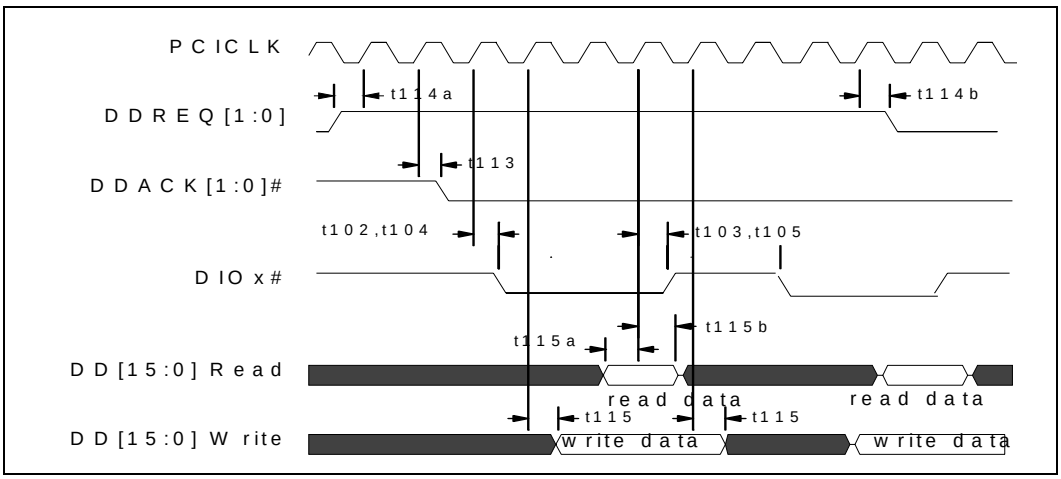


Figure 11-15. IDE Multiword DMA Mode



11.10 USB Timing Diagrams

Figure 11-16. Data Signal Rise and Fall Time

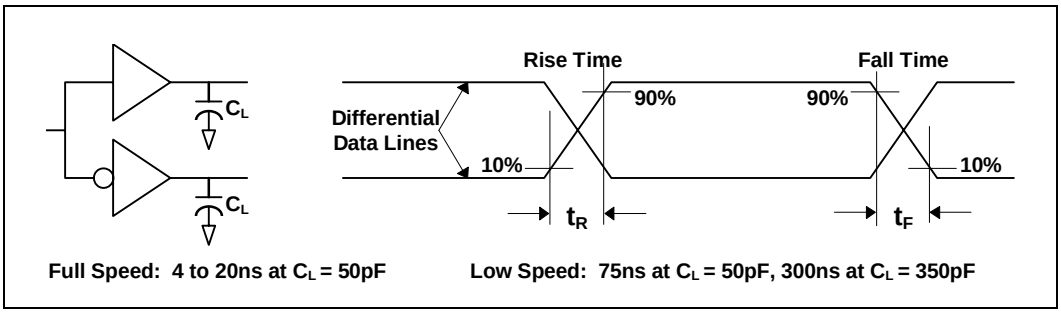


Figure 11-17. Data Jitter

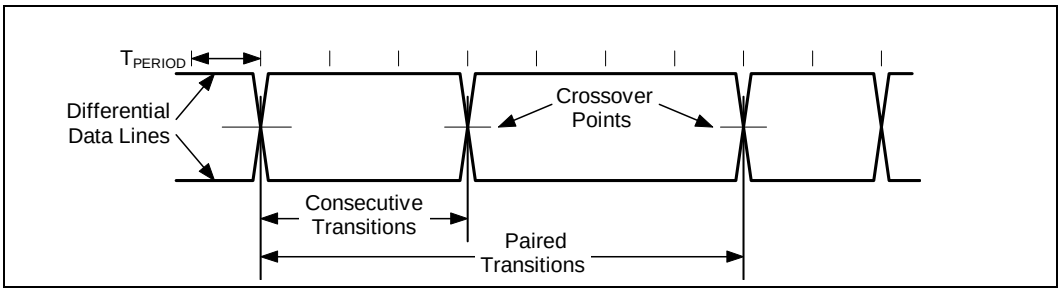
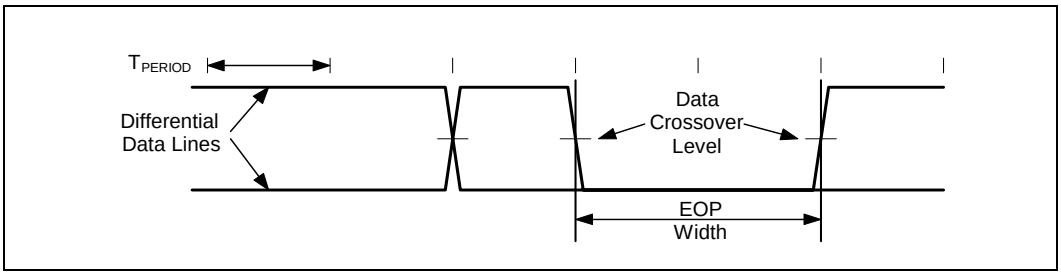


Figure 11-18. EOP Width Timing



11.11 SMBus Timing Diagrams

Figure 11-19. SMBus Timing

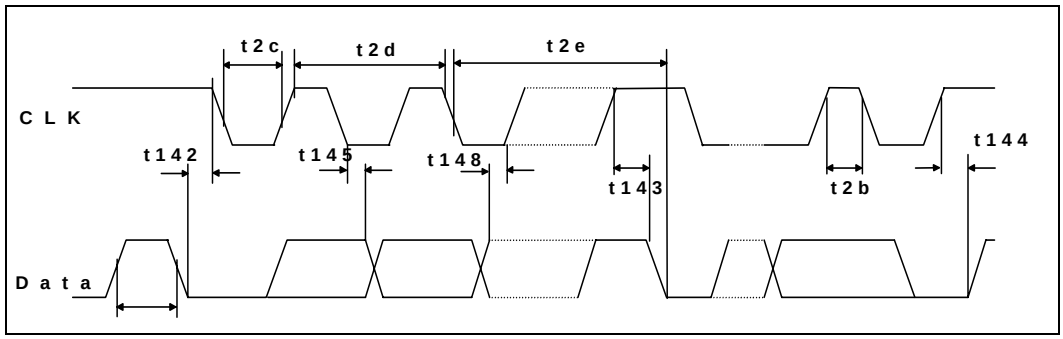
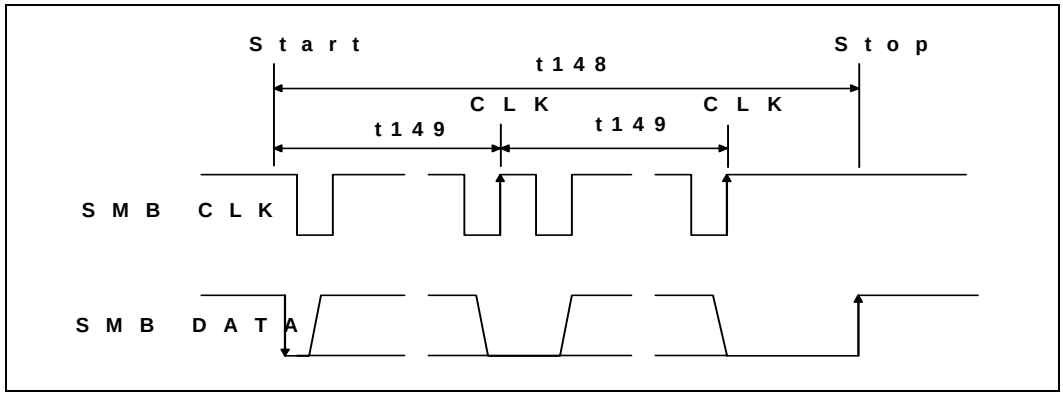


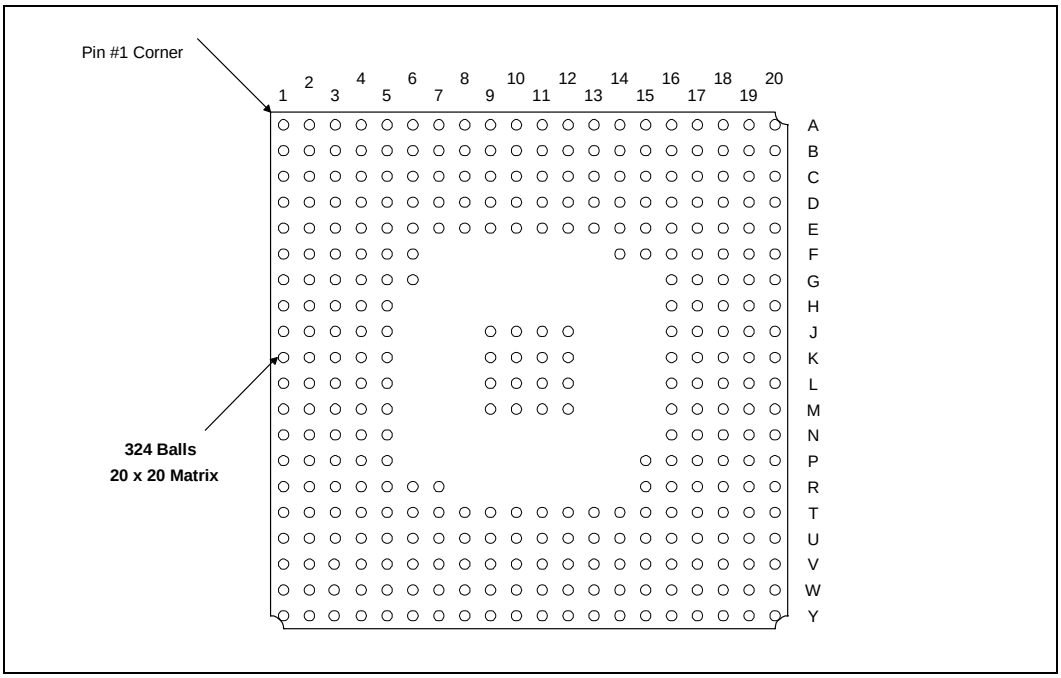
Figure 11-20. SMBus Timeout Timing



11.12 IFB Pinout and Package Information

11.12.1 Pinout Information

Figure 11-21. Pinout Diagram



11.12.2 IFB Package Information

This specification outlines the mechanical dimensions for the IFB. The package is a 324 pin ball grid array (BGA).

Figure 11-22. 324-pin BGA (Top View)

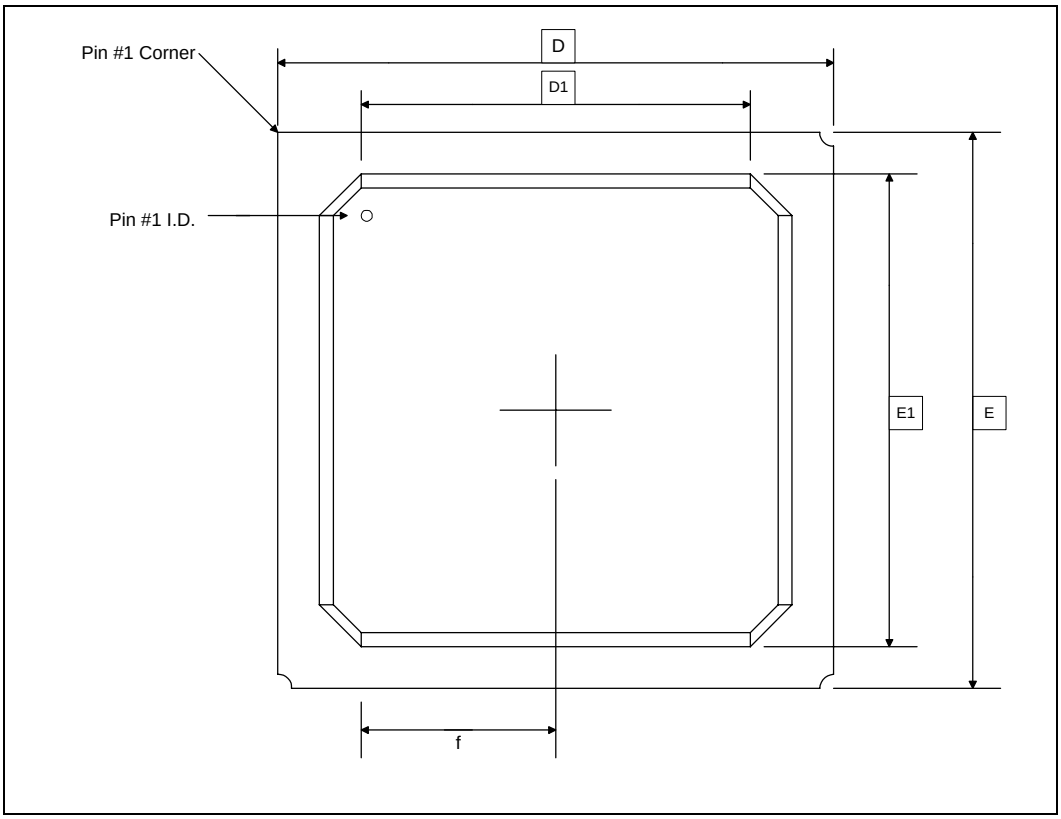


Figure 11-23. 324-pin BGA (Side View)

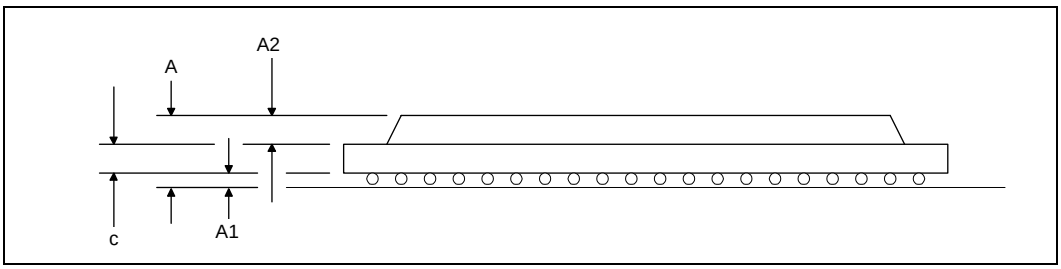


Figure 11-24. 324-pin BGA (Ball View)

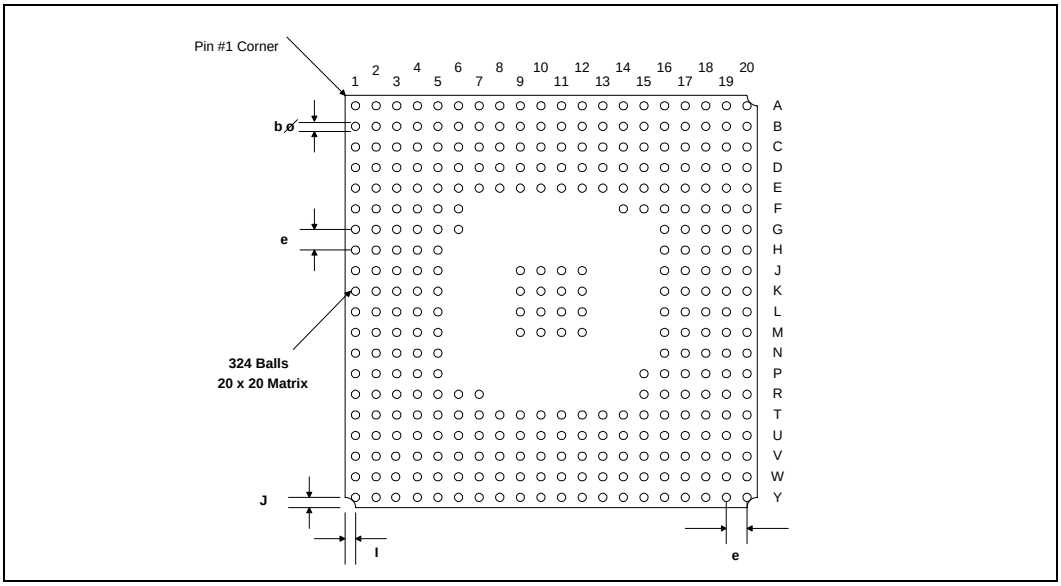
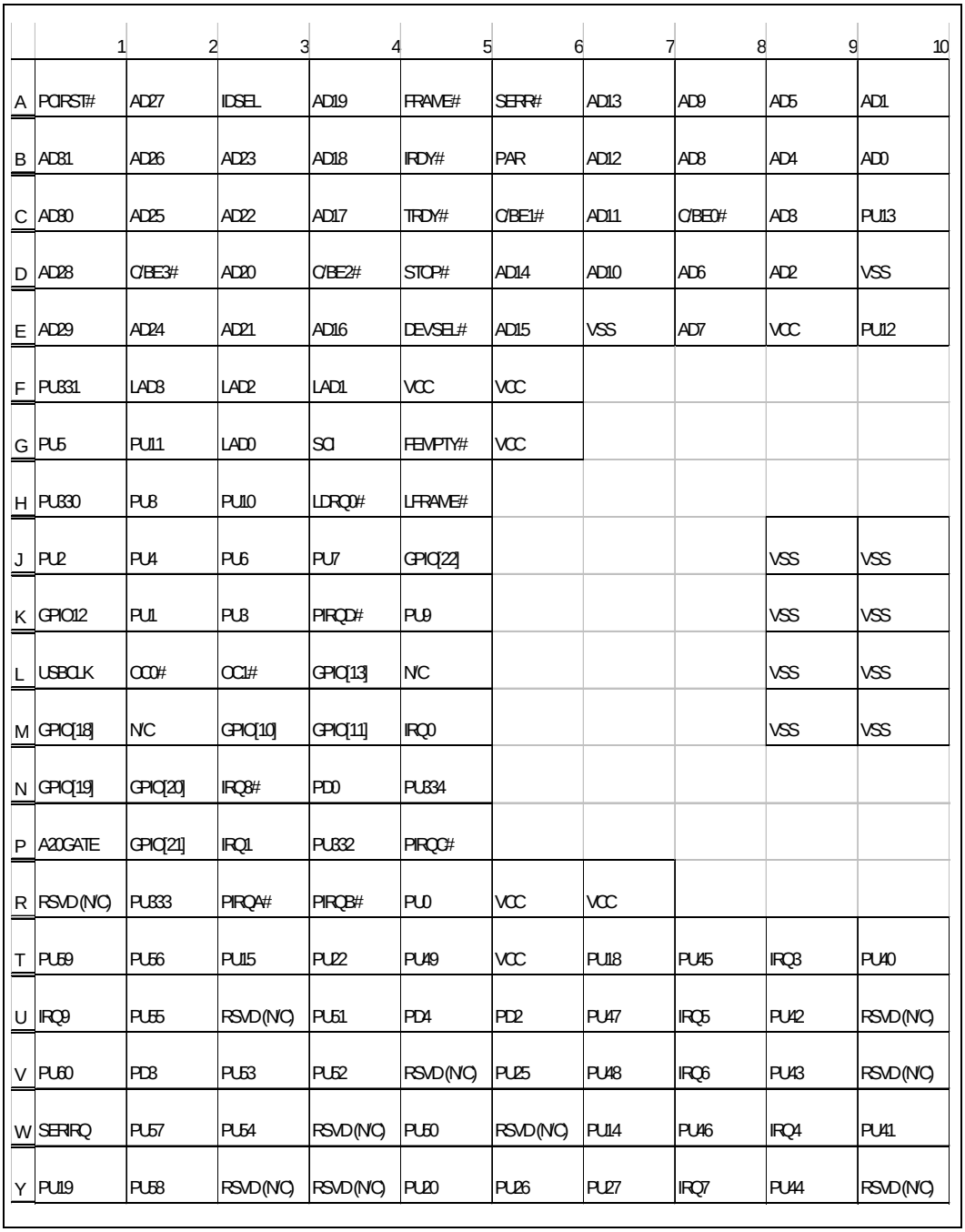


Table 11-16. IFB 324-pin Ball Grid Array

Sym	Dimension - 2 Layer (4 Layer)			Notes
	Min	Nom	Max	a
A	1.90(2.06)	2.09(2.29)	2.30(2.52)	
A1	0.50	0.60	0.70	
A2	1.12	1.17	1.22	
D	26.80	27.00	27.20	
D1		24.00	24.70	
E	26.80	27.00	27.20	
E1		24.00	24.70	
I	1.44 REF.			
J	1.44 REF.			
M	20 (DEPOPULATED)			b
N	324			c
b	0.60	0.76	0.90	
c	0.28(0.44)	0.32(0.52)	0.38(0.60)	
e	1.27			
f	8.05 REF.			

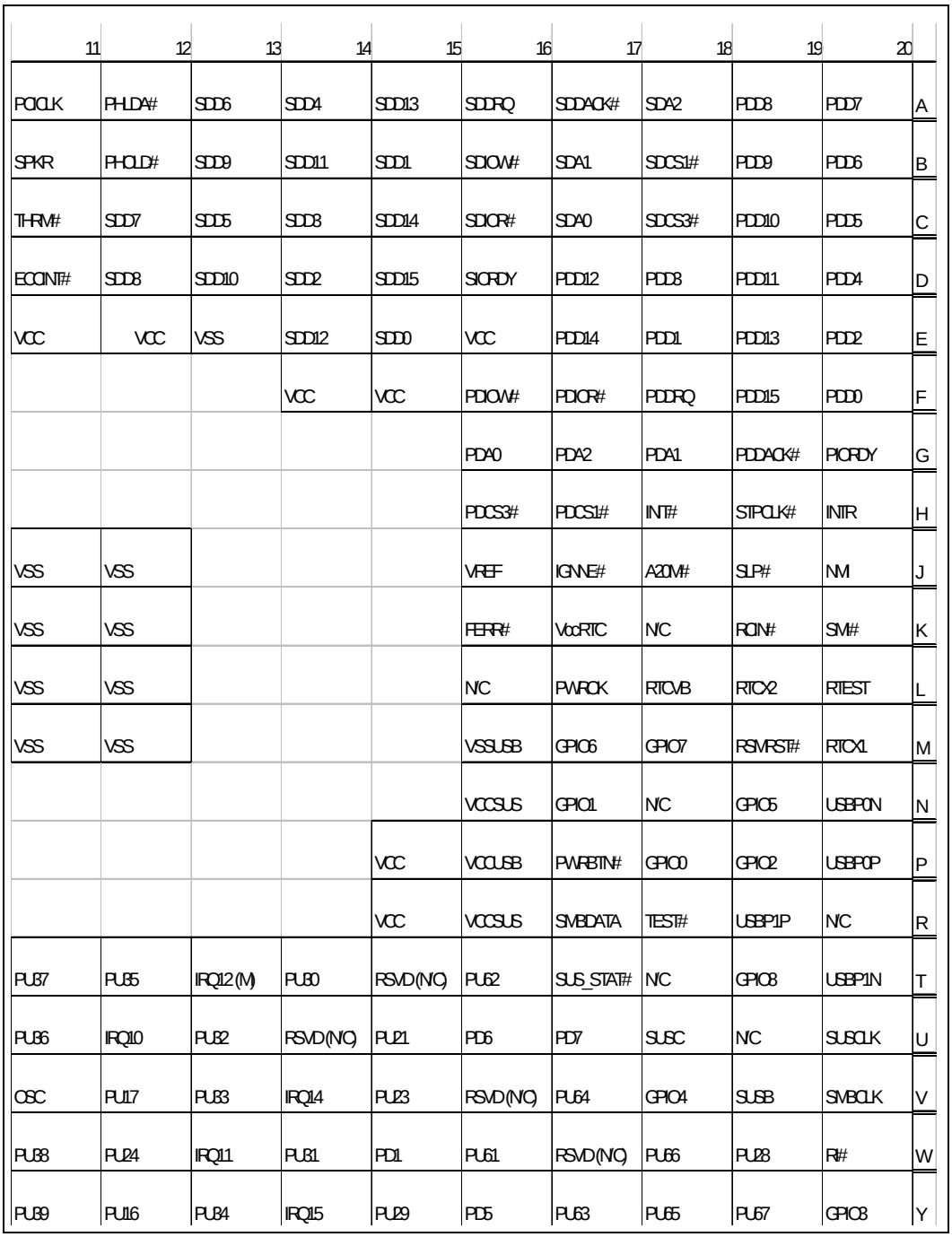
a. All dimensions are in millimeters.
b. ‘M’ represents the maximum solder ball matrix size.
c. ‘N’ Represents the maximum allowable number of solder balls.

Figure 11-25. Pinout (1/2)



	1	2	3	4	5	6	7	8	9	10
A	PCIRST#	AD27	IDSEL	AD19	FRAME#	SERR#	AD13	AD9	AD5	AD1
B	AD31	AD26	AD23	AD18	IRDY#	PAR	AD12	AD8	AD4	AD0
C	AD30	AD25	AD22	AD17	TRDY#	C/BE1#	AD11	C/BE0#	AD3	PU13
D	AD28	C/BE3#	AD20	C/BE2#	STOP#	AD14	AD10	AD6	AD2	VSS
E	AD29	AD24	AD21	AD16	DEVSEL#	AD15	VSS	AD7	VCC	PU12
F	PU33	LAD3	LAD2	LAD1	VCC	VCC				
G	PU5	PU11	LAD0	SCI	FEMPTY#	VCC				
H	PU30	PU8	PU10	LDRQ0#	LFRAME#					
J	PU2	PU4	PU6	PU7	GPIO[22]				VSS	VSS
K	GPIO12	PU1	PU3	PIRQD#	PU9				VSS	VSS
L	USBCLK	OC0#	OC1#	GPIO[13]	N/C				VSS	VSS
M	GPIO[18]	N/C	GPIO[10]	GPIO[11]	IRQ0				VSS	VSS
N	GPIO[19]	GPIO[20]	IRQ3#	PD0	PU34					
P	A20GATE	GPIO[21]	IRQ1	PU32	PIRQC#					
R	RSVD (N/C)	PU33	PIRQA#	PIRQB#	PU0	VCC	VCC			
T	PU39	PU56	PU15	PU22	PU49	VCC	PU18	PU45	IRQ3	PU40
U	IRQ9	PU55	RSVD (N/C)	PU51	PD4	PD2	PU47	IRQ5	PU42	RSVD (N/C)
V	PU60	PD3	PU53	PU52	RSVD (N/C)	PU25	PU48	IRQ6	PU43	RSVD (N/C)
W	SERIRQ	PU57	PU54	RSVD (N/C)	PU50	RSVD (N/C)	PU14	PU46	IRQ4	PU41
Y	PU19	PU58	RSVD (N/C)	RSVD (N/C)	PU20	PU26	PU27	IRQ7	PU44	RSVD (N/C)

Figure 11-26. Pinout (2/2)



11	12	13	14	15	16	17	18	19	20	
PCICLK	PHLDA#	SDD6	SDD4	SDD13	SDDRQ	SDDACK#	SDA2	PDD8	PDD7	A
SPKR	PHOLD#	SDD9	SDD11	SDD1	SDIOW#	SDA1	SDCS1#	PDD9	PDD6	B
THRM#	SDD7	SDD5	SDD3	SDD14	SDIOR#	SDA0	SDCS3#	PDD10	PDD5	C
ECCINT#	SDD8	SDD10	SDD2	SDD15	SIORDY	PDD12	PDD3	PDD11	PDD4	D
VCC	VCC	VSS	SDD12	SDD0	VCC	PDD14	PDD1	PDD13	PDD2	E
			VCC	VCC	PDIOW#	PDIOR#	PDDRQ	PDD15	PDD0	F
					PDA0	PDA2	PDA1	PDDACK#	PIORDY	G
					PDCS3#	PDCS1#	INIT#	STPCLK#	INTR	H
VSS	VSS				VREF	IGNNE#	A20M#	SLP#	NMI	J
VSS	VSS				FERR#	VccRTC	NC	RCIN#	SMI#	K
VSS	VSS				NC	PWROK	RTCVB	RTCX2	RTEST	L
VSS	VSS				VSSUSB	GPIO6	GPIO7	RSMRST#	RTCX1	M
					VCCSUS	GPIO1	NC	GPIO5	USBP0N	N
				VCC	VCCUSB	PWRBTN#	GPIO0	GPIO2	USBP0P	P
				VCC	VCCSUS	SMBDATA	TEST#	USBP1P	NC	R
PUI37	PUI35	IRQ12 (M)	PUI30	RSVD (NC)	PUI62	SUS_STAT#	NC	GPIO8	USBP1N	T
PUI36	IRQ10	PUI32	RSVD (NC)	PUI21	PD6	PD7	SUSC	NC	SUSCLK	U
OSC	PUI17	PUI33	IRQ14	PUI23	RSVD (NC)	PUI64	GPIO4	SUSB	SMBCLK	V
PUI38	PUI24	IRQ11	PUI31	PD1	PUI61	RSVD (NC)	PUI66	PUI28	RI#	W
PUI39	PUI16	PUI34	IRQ15	PUI29	PD5	PUI63	PUI65	PUI67	GPIO3	Y

Programmable Interrupt Device (PID) 12

12.1 Introduction

This document provides the programmable interrupt device (PID) electrical, mechanical and thermal specifications.

Note: NEC Corporation is responsible for the manufacturing, quality and reliability of the Programmable Interrupt Device. Intel assumes responsibility for the design of the PID. Please consult NEC if deviations from this provided specification are found.

12.2 Electrical Specifications

12.2.1 Absolute Maximum Ratings

Case temperature under bias	–55°C to +125°C
Storage temperature	–55°C to +150°C
Voltage on any 3.3V TTL input pin with respect to V_{SS}	–0.3 to V_{DD} +0.3V
Voltage on any 5V PCI input pin with respect to V_{SS}	–0.3 to V_{CC} +0.5V
Power supply voltage V_{DD} with respect to V_{SS}	–0.3 to +4.6V
Power supply voltage V_{CC} with respect to V_{SS}	–0.3 to +7.0V

Note: Stresses higher than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12.2.2 DC Characteristics

Table 12-1. Functional Operating Range
(V_{CC} = 5 V ±5%; V_{DD} = 3.3 V ±5%; T_{AMB} = 0°C to +70°C; T_{JCT} = 0 to 100°C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input voltage low (TTL) Input voltage low (5V PCI)	0 0		0.8 0.8	V V	
V_{IH}	Input voltage high (TTL) Input voltage high (5V PCI)	2.0 2.0		V_{DD} V_{CC}	V V	
V_{OL}	Output voltage low			0.4	V	
V_{OH}	Output voltage high	V_{DD} –0.2		V_{DD}	V	
V_{OH}	Output voltage high (5V PCI)	+2.4		V_{DD}	V	
I_{DD}	Power supply current		75	100	mA	Current only comes from the 3.3V power supply (V_{DD})

Table 12-1. Functional Operating Range (Continued)
(V_{CC} = 5 V ±5%; V_{DD} = 3.3 V ±5%; T_{AMB} = 0°C to +70°C; T_{JCT} = 0 to 100°C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{OZ}	Off-state output current	–14		14	µA	$V_O = V_{DD}$ or GND
I_{OS}	Output short circuit current			250	mA	V_O = GND, time ≤1 second
I_I	Input leakage current: 5V PCI Normal input With 50K ohms pull-up resistor With 5K ohms pull-up resistor With 50k ohms pull-down resistor	 –70 –10 –55 –0.42 55	 $\pm 10^{-5}$ –131 –1 131	 70 10 –238 –1.72 238	 µA µA µA mA µA	 $V_I = V_{DD}$ or GND V_I = GND V_I = GND $V_I = V_{DD}$
I_{IL}	Low-level input current	–10		+10	µA	V_I = GND
I_{OL}	Low-level output current: 6 mA 9 mA 24 mA	 6 9 24			mA	V_{OL} = 0.4V
I_{OH}	High-level output current: 6 mA 9 mA 24 mA	 –3 –3 –4			mA	V_{OH} = VDD –0.4V
C_I	Input capacitance	3	5	7	pF	V_{DD} = 0 V, T_J = 25 C, f = 1MHz
C_O	Output capacitance	3	5	7	pF	V_{DD} = 0 V, T_J = 25 C, f = 1MHz
$C_{I/O}$	Input/output capacitance	3	5	7	pF	V_{DD} = 0 V, T_J = 25 C, f = 1MHz

12.2.3 I/O Buffer Specifications

The table below lists the I/O buffer specifications for the PID signals.

Table 12-2. I/O Buffer Specifications

Pin Name	Description	Output Drive
PCICLK	3.3V TTL input	
PCIRST#	5V-tolerance TTL input	
AD[31:00]	5V-tolerance TTL input, tristate output	±24mA
CBE[3:0]#	5V-tolerance TTL input, tristate output	±24mA
PAR	5V-tolerance TTL input, tristate output	±24mA
FRAME#	5V-tolerance TTL input, tristate output	±24mA
IRDY#	5V-tolerance TTL input, tristate output	±24mA
TRDY#	5V-tolerance TTL input, tristate output	±24mA
STOP#	5V-tolerance TTL input, tristate output	±24mA
DEVSEL#	5V-tolerance TTL input, tristate output	±24mA
IDSEL	5V-tolerance TTL input	
PLOCK#	5V-tolerance TTL input, tristate output	±24mA
PCIREQ#	TTL tristate output	±9mA
PCIGNT#	5V-tolerance TTL input	

Table 12-2. I/O Buffer Specifications (Continued)

Pin Name	Description	Output Drive
PERR#	5V-tolerance TTL input, tristate output	±24mA
SERR#	5V-tolerance TTL input, open-drain output	24ma
SI_BO0	5V-tolerance TTL input, tristate output	±24 A
SERR7N_SI7	5V-tolerance TTL input	
SERR6N_SI6	5V-tolerance TTL input	
SERR5N_SI5	5V-tolerance TTL input	
SERR4N_SI4	5V-tolerance TTL input	
SERR3N_SI3	5V-tolerance TTL input	
SERR2N_SI2	5V-tolerance TTL input	
SERR1N_SI1	5V-tolerance TTL input	
SERR0N_SI0	5V-tolerance TTL input	
INTIO[15:0]	5V-tolerance TTL schmitt input, open-drain output	6mA
INTIN[47:0]	5V-tolerance TTL schmitt input	
SMI#	5V-tolerance TTL schmitt input	
NMI	5V-tolerance TTL schmitt input	
SMI_OUT#	Open-drain output	9mA
NMI_OUT	Open-drain output	9mA
I2O_INT[1:0]#	TTL tristate output	±18mA
I2BCLK	3.3V TTL input	
I2B_DATA	5V-tolerance TTL input, open-drain output	24mA
APICCLK	3.3V TTL input	
APICD[1:0]	5V-tolerance TTL input, open-drain output	24mA
APICREQ#	TTL tristate output	±9mA
APICACK[1:0]#	5V-tolerance TTL input	
I2BMST	5V-tolerance TTL input	
PICMODE	5V-tolerance TTL input	
GPIO[31:0]	5V-tolerance TTL input, tristate output	±9mA
PWRGOOD	5V-tolerance TTL input	
TRST#	5V-tolerance TTL input	
TDI	5V-tolerance TTL input	
TDO	Open-drain output	9mA
TMS	5V-tolerance TTL input	
TCK	3.3 TTL input	

12.3 Timing Specifications

12.3.1 AC Characteristics

The AC specifications given in the following table consists of output delays, input setup, and input hold requirements. These specifications are given for the functional operating range of the device. Timing specifications are given in nanoseconds (ns) unless otherwise specified.

Table 12-3. AC Characteristics (V_{CC} = 5V ±5%; V_{DD} = 3.3V ±5%; T_{AMB} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Notes
Clock Signals					
t1	APICCLK rise/fall time	1	4		
t2	APICCLK high time	11			
t3	APICCLK low time	11			
t4	APICCLK period		30		33.3MHz
t5	PCICLK rise/fall time	1	4		
t6	PCICLK high time	11			
t7	PCICLK low time	11			
t8	PCICLK period		30		33.3MHz
t9	I2BCLK rise/fall time	1	4		
t10	I2BCLK high time	56			
t11	I2BCLK low time	56			
t12	I2BCLK period		120		8.25MHz
t13	TCK rise/fall time	1	4		
t14	TCK high time	11			
t15	TCK low time	11			
t16	TCK period		30		33.3MHz

Symbol	Parameter	Setup Min	Hold Min	Delay Min	Delay Max	Unit	Notes
Reset Signals (PCICLK Rising)							
tx/ty	PCIRST#	7	2				
	PWRGOOD						ASYNC
APIC Bus Interface (APICLK Rising)							
tx/ty	APICD[1:0]	6	2	2	8		CL = 15pf
tx/ty	APICREQ#			2	7		CL = 15pf
tx/ty	APICACK[1:0]#	7	2				
Interrupt Interface (PCICLK Rising)							
tx/ty	INTIO[15:0]			2	7		CL = 15pf
	INTIN[47:0]						ASYNC
	SMI#						ASYNC
tx/ty	SMI_OUT#			2	7		CL = 15pf
	NMI						ASYNC
tx/ty	NMI_OUT			2	7		CL = 15pf
tx/ty	I2O_INT[1:0]#			2	7		CL = 15pf

Symbol	Parameter	Setup Min	Hold Min	Delay Min	Delay Max	Unit	Notes
I2B Bus Interface (I2BCLK Rising)							
tx/ty	I2B_DATA	7	2	7	18		CL = 15pf
PCI Interface (PCICLK Rising)							
tx/ty	FRAME#, AD[31:0], C/BE[3:0]#, IRDY#, TRDY#, STOP#, LOCK# DEVSEL#, PAR, PERR#, SERR#, SI_BO0, SERR7N_SI7 ... SERR0N_SI0	7	0	2	11		CL = 50pf
tx/ty	PCIREQ#			2	12		CL = 50pf
tx/ty	PCIGNT#	10	0				
JTAG Signal Interface (TCLK Rising)							
tx/ty	TDI, TMS	7	2				
tx/ty	TDO			2	10		CL = 15pf
	TRST#						ASYNC
GPIO Signal Interface							
	GPIO[31:0]						ASYNC
Misc. Signal Interface (RST# Rising)							
	PICMODE						ASYNC
	I2BMST						ASYNC

12.3.2 General Timing Diagrams

Figure 12-1. APICCLK Signal Timing

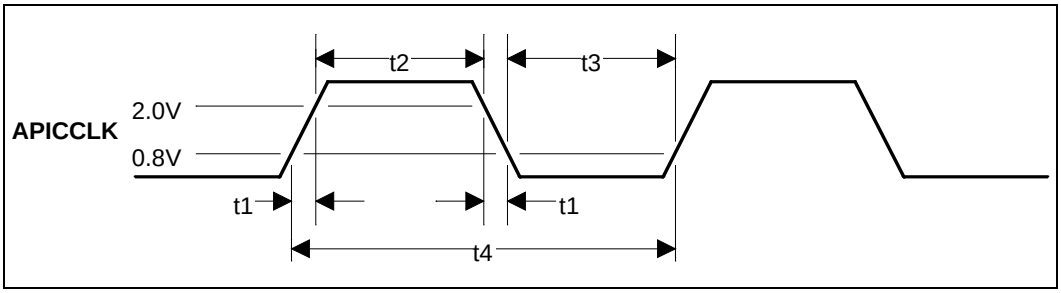


Figure 12-2. PCICLK Signal Timing

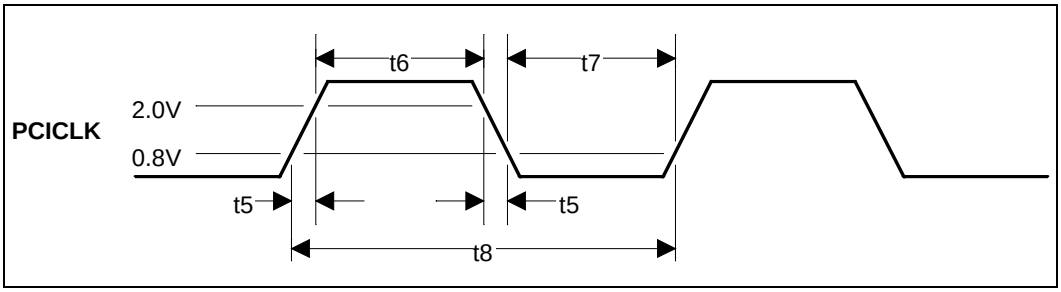


Figure 12-3. I2BCLK Signal Timing

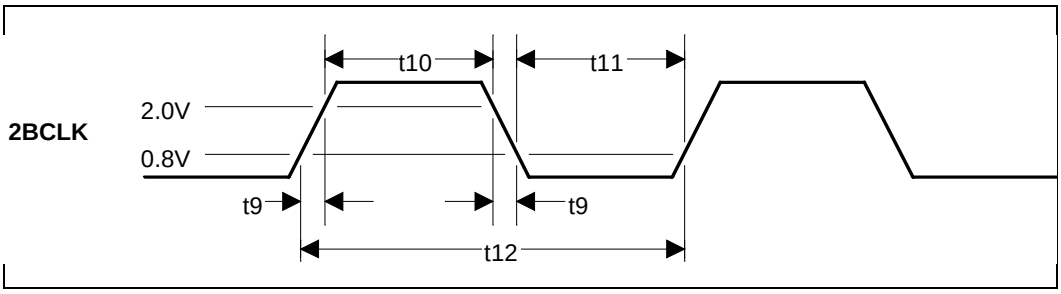


Figure 12-4. TCLK Signal Timing

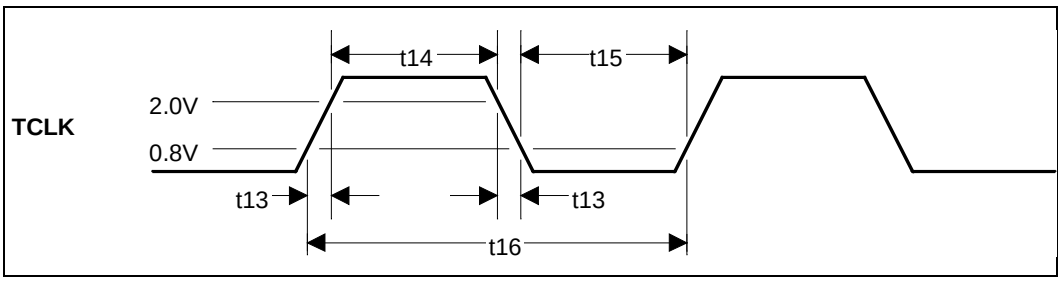
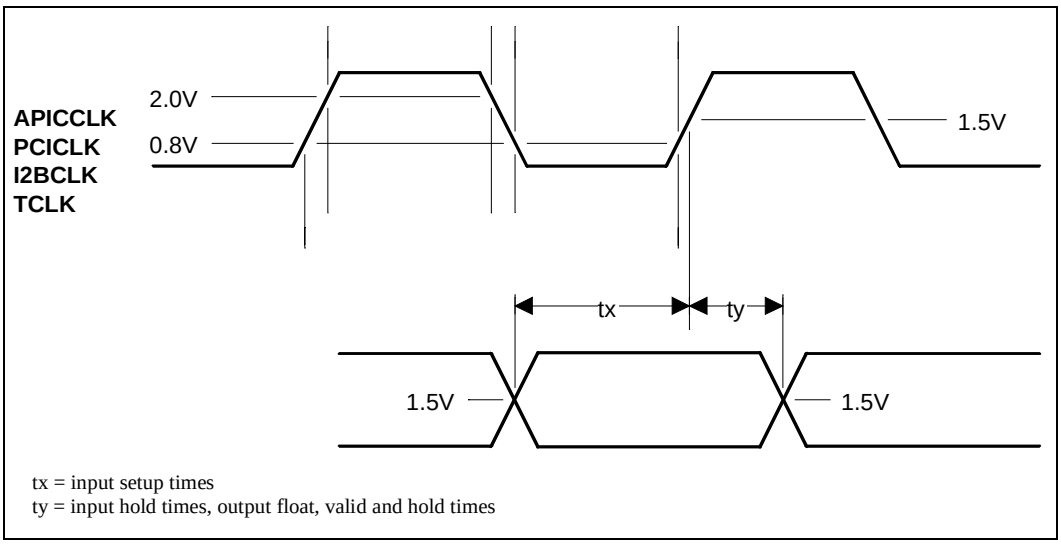


Figure 12-5. General Setup, Hold and Valid Timings Diagram

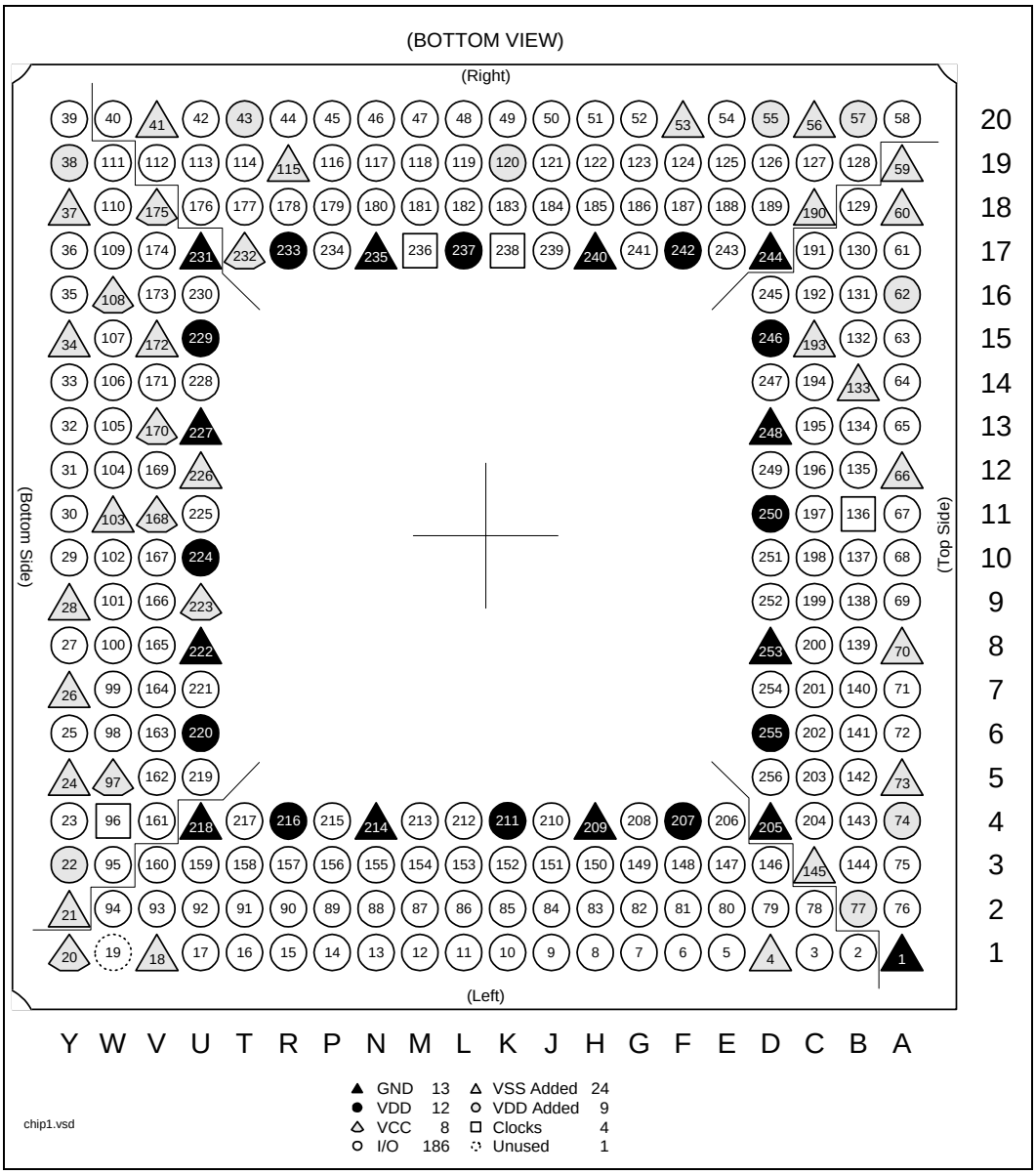


12.4 Pin, Package and Thermal Specifications

12.4.1 Pinout Diagram

The figure below shows the pin assignments of the PID.

Figure 12-6. PID Pin Assignments



12.4.2 PID Signal and Power Pin Assignments (Sorted by Pin #)

Table 12-4. PID Signal and Power Pin Assignments (Sorted by Pin Number)

Pin #	Ref #	Signal Name
1	A1	VSS
2	B1	SMI_OUT#
3	C1	INTIN46
4	D1	VSS
5	E1	INTIN43
6	F1	INTIN39
7	G1	INTIN36
8	H1	INTIN33
9	J1	INTIN29
10	K1	INTIN26
11	L1	INTIN25
12	M1	INTIN21
13	N1	INTIN17
14	P1	INTIN14
15	R1	INTIN12
16	T1	INTIN9
17	U1	INTIN5
18	V1	VSS
19	W1	NO CONNECT
20	Y1	VCC
21	Y2	VSS
22	Y3	VDD
23	Y4	AD30
24	Y5	VSS
25	Y6	AD25
26	Y7	VSS
27	Y8	AD22
28	Y9	VSS
29	Y10	AD17
30	Y11	AD16
31	Y12	FRAME#
32	Y13	DEVSEL#
33	Y14	PERR#
34	Y15	VSS
35	Y16	AD15
36	Y17	AD13
37	Y18	VSS
38	Y19	VDD
39	Y20	AD7
40	W20	AD6
41	V20	VSS
42	U20	AD2
43	T20	VDD
44	R20	INTIO13
45	P20	INTIO10
46	N20	INTIO7
47	M20	APICD1
48	L20	APICACK0#
49	K20	I2BDATA
50	J20	INTIO6
51	H20	INTIO2
52	G20	GPIO31
53	F20	VSS
54	E20	GPIO27
55	D20	VDD
56	C20	VSS
57	B20	VDD
58	A20	GPIO17
59	A19	VSS
60	A18	VSS
61	A17	GPIO12
62	A16	VDD
63	A15	GPIO7
64	A14	GPIO5
65	A13	GPIO2
66	A12	VSS
67	A11	NO CONNECT
68	A10	NO CONNECT
69	A9	NO CONNECT
70	A8	VSS
71	A7	SERR3N_SI8
72	A6	SERR1N_SI1
73	A5	VSS
74	A4	VDD
75	A3	TDO
76	A2	TRST#
77	B2	VDD
78	C2	NMI_OUT
79	D2	SMI#
80	E2	INTIN44
81	F2	INTIN40
82	G2	INTIN37
83	H2	INTIN34
84	J2	INTIN30
85	K2	INTIN28
86	L2	INTIN24
87	M2	INTIN20
88	N2	INTIN16
89	P2	INTIN13
90	R2	INTIN10
91	T2	INTIN6
92	U2	INTIN3
93	V2	INTIN0
94	W2	PRST#
95	W3	PCIGNT#
96	W4	PCICLK
97	W5	VCC
98	W6	AD26
99	W7	CBE3#
100	W8	AD23
101	W9	AD20
102	W10	AD19
103	W11	VSS
104	W12	IRDY#
105	W13	STOP#
106	W14	SERR#
107	W15	CBE1#
108	W16	VCC
109	W17	AD11
110	W18	AD8
111	W19	CBE0#
112	V19	AD5
113	U19	AD4
114	T19	AD0
115	R19	VSS
116	P19	INTIO11
117	N19	INTIO8
118	M19	I2O_INT1#
119	L19	APICD0
120	K19	VDD
121	J19	INTIO5
122	H19	INTIO1
123	G19	GPIO30
124	F19	GPIO28
125	E19	GPIO24
126	D19	GPIO22
127	C19	GPIO19
128	B19	GPIO18
129	B18	GPIO16
130	B17	GPIO15
131	B16	GPIO10
132	B15	GPIO8
133	B14	VSS
134	B13	GPIO3
135	B12	NO CONNECT
136	B11	TCK
137	B10	NO CONNECT
138	B9	NO CONNECT
139	B8	SERR5N_SI5
140	B7	SERR2N_SI2
141	B6	VDD
142	B5	PICMOD
143	B4	TDI
144	B3	VDD

Table 12-4. PID Signal and Power Pin Assignments (Sorted by Pin Number) (Continued)

Pin #	Ref #	Signal Name
145	C3	VSS
146	D3	NMI
147	E3	INTIN45
148	F3	INTIN42
149	G3	INTIN38
150	H3	INTIN35
151	J3	INTIN31
152	K3	INTIN27
153	L3	INTIN23
154	M3	INTIN19
155	N3	INTIN15
156	P3	INTIN11
157	R3	INTIN7
158	T3	INTIN4
159	U3	INTIN1
160	V3	PLOCK#
161	V4	PCIREQ#
162	V5	AD29
163	V6	AD28
164	V7	AD24
165	V8	IDSEL
166	V9	AD21
167	V10	AD18
168	V11	VCC
169	V12	TRDY#
170	V13	VCC
171	V14	PAR
172	V15	VSS
173	V16	AD12
174	V17	AD9
175	V18	VCC
176	U18	AD3
177	T18	AD1
178	R18	INTIO15
179	P18	INTIO12
180	N18	INTIO9
181	M18	APICREQ#
182	L18	APICACK1#
183	K18	I2O_INT0#
184	J18	INTIO4
185	H18	INTIO0
186	G18	GPIO29
187	F18	GPIO25
188	E18	GPIO23
189	D18	GPIO20
190	C18	VSS
191	C17	GPIO14
192	C16	GPIO11
193	C15	VSS
194	C14	GPIO6
195	C13	GPIO4
196	C12	GPIO0
197	C11	NO CONNECT
198	C10	NO CONNECT
199	C9	SERR7N_SI7
200	C8	SERR4N_SI4
201	C7	SERR0N_SI0
202	C6	I2BMST
203	C5	PWRGOOD
204	C4	SI_BO0
205	D4	VSS (G1)
206	E4	INTIN47
207	F4	VDD (V1)
208	G4	INTIN41
209	H4	VSS (G1)
210	J4	INTIN32
211	K4	VDD (V1)
212	L4	INTIN22
213	M4	INTIN18
214	N4	VSS (G1)
215	P4	INTIN8
216	R4	VDD (V1)
217	T4	INTIN2
218	U4	VSS (G1)
219	U5	AD31
220	U6	VDD (V1)
221	U7	AD27
222	U8	VSS (G1)
223	U9	VCC
224	U10	VDD (V1)
225	U11	CBE2#
226	U12	VSS
227	U13	VSS (G1)
228	U14	AD14
229	U15	VDD (V1)
230	U16	AD10
231	U17	VSS (G1)
232	T17	VCC
233	R17	VDD (V1)
234	P17	INTIO14
235	N17	VSS (G1)
236	M17	APICCLK
237	L17	VDD (V1)
238	K17	I2BCLK
239	J17	INTIO3
240	H17	VSS (G1)
241	G17	GPIO26
242	F17	VDD (V1)
243	E17	GPIO21
244	D17	VSS (G1)
245	D16	GPIO13
246	D15	VDD (V1)
247	D14	GPIO9
248	D13	VSS (G1)
249	D12	GPIO1
250	D11	VDD (V1)
251	D10	NO CONNECT
252	D9	SERR6N_SI6
253	D8	VSS (G1)
254	D7	VDD
255	D6	VDD (V1)
256	D5	TMS

12.4.3 PID Signal and Power Pin Assignments (Sorted by Ref #)

Table 12-5. PID Signal and Power Pin Assignments (Sorted by Reference Number)

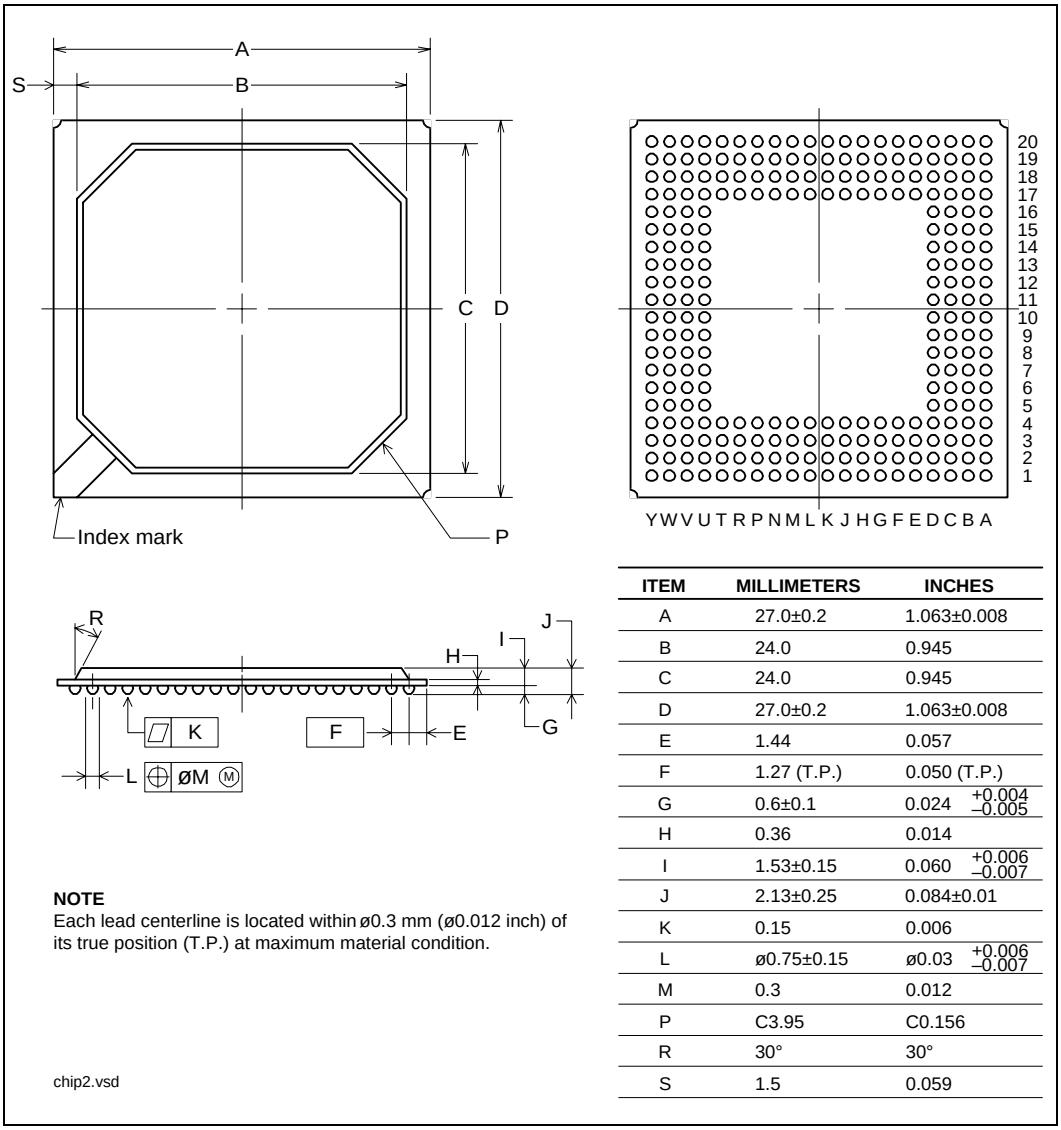
Pin #	Ref #	Signal Name
1	A1	VSS
76	A2	TRST#
75	A3	TDO
74	A4	VDD
73	A5	VSS
72	A6	SERR1N_SI1
71	A7	SERR3N_SI3
70	A8	VSS
69	A9	NO CONNECT
68	A10	NO CONNECT
67	A11	NO CONNECT
66	A12	VSS
65	A13	GPIO2
64	A14	GPIO5
63	A15	GPIO7
62	A16	VDD
61	A17	GPIO12
60	A18	VSS
59	A19	VSS
58	A20	GPIO17
2	B1	SMI_OUT#
77	B2	VDD
144	B3	VDD
143	B4	TDI
142	B5	PICMOD
141	B6	VDD
140	B7	SERR2N_SI2
139	B8	SERR5N_SI5
138	B9	NO CONNECT
137	B10	NO CONNECT
136	B11	TCK
135	B12	NO CONNECT
134	B13	GPIO3
133	B14	VSS
132	B15	GPIO8
131	B16	GPIO10
130	B17	GPIO15
129	B18	GPIO16
128	B19	GPIO18
57	B20	VDD
3	C1	INTIN46
78	C2	NMI_OUT
145	C3	VSS
204	C4	SI_BO0
203	C5	PWRGOOD
202	C6	I2BMST
201	C7	SERR0N_SI0
200	C8	SERR4N_SI4
199	C9	SERR7N_SI7
198	C10	NO CONNECT
197	C11	NO CONNECT
196	C12	GPIO0
195	C13	GPIO4
194	C14	GPIO6
193	C15	VSS
192	C16	GPIO11
191	C17	GPIO14
190	C18	VSS
127	C19	GPIO19
56	C20	VSS
4	D1	VSS
79	D2	SMI#
146	D3	NMI
205	D4	VSS (G1)
256	D5	TMS
255	D6	VDD (V1)
254	D7	VDD
253	D8	VSS (G1)
252	D9	SERR6N_SI6
251	D10	NO CONNECT
250	D11	VDD (V1)
249	D12	GPIO1
248	D13	VSS (G1)
247	D14	GPIO9
246	D15	VDD (V1)
245	D16	GPIO13
244	D17	VSS (G1)
189	D18	GPIO20
126	D19	GPIO22
55	D20	VDD
5	E1	INTIN43
80	E2	INTIN44
147	E3	INTIN45
206	E4	INTIN47
243	E17	GPIO21
188	E18	GPIO23
125	E19	GPIO24
54	E20	GPIO27
6	F1	INTIN39
81	F2	INTIN40
148	F3	INTIN42
207	F4	VDD (V1)
242	F17	VDD (V1)
187	F18	GPIO25
124	F19	GPIO28
53	F20	VSS
7	G1	INTIN36
82	G2	INTIN37
149	G3	INTIN38
208	G4	INTIN41
241	G17	GPIO26
186	G18	GPIO29
123	G19	GPIO30
52	G20	GPIO31
8	H1	INTIN33
83	H2	INTIN34
150	H3	INTIN35
209	H4	VSS (G1)
240	H17	VSS (G1)
185	H18	INTIO0
122	H19	INTIO1
51	H20	INTIO2
9	J1	INTIN29
84	J2	INTIN30
151	J3	INTIN31
210	J4	INTIN32
239	J17	INTIO3
184	J18	INTIO4
121	J19	INTIO5
50	J20	INTIO6
10	K1	INTIN26
85	K2	INTIN28
152	K3	INTIN27
211	K4	VDD (V1)
238	K17	I2BCLK
183	K18	I2O_INT0#
120	K19	VDD
49	K20	I2BDATA
11	L1	INTIN25
86	L2	INTIN24
153	L3	INTIN23
212	L4	INTIN22
237	L17	VDD (V1)
182	L18	APICACK1#
119	L19	APICD0
48	L20	APICACK0#
12	M1	INTIN21
87	M2	INTIN20
154	M3	INTIN19
213	M4	INTIN18
236	M17	APICCLK
181	M18	APICREQ#
118	M19	I2O_INT1#
47	M20	APICD1

Table 12-5. PID Signal and Power Pin Assignments (Sorted by Reference Number)

Pin #	Ref #	Signal Name
13	N1	INTIN17
88	N2	INTIN16
155	N3	INTIN15
214	N4	VSS (G1)
235	N17	VSS (G1)
180	N18	INTIO9
117	N19	INTIO8
46	N20	INTIO7
14	P1	INTIN14
89	P2	INTIN13
156	P3	INTIN11
215	P4	INTIN8
234	P17	INTIO14
179	P18	INTIO12
116	P19	INTIO11
45	P20	INTIO10
15	R1	INTIN12
90	R2	INTIN10
157	R3	INTIN7
216	R4	VDD (V1)
233	R17	VDD (V1)
178	R18	INTIO15
115	R19	VSS
44	R20	INTIO13
16	T1	INTIN9
91	T2	INTIN6
158	T3	INTIN4
217	T4	INTIN2
232	T17	VCC
177	T18	AD1
114	T19	AD0
43	T20	VDD
17	U1	INTIN5
92	U2	INTIN3
159	U3	INTIN1
218	U4	VSS (G1)
219	U5	AD31
220	U6	VDD (V1)
221	U7	AD27
222	U8	VSS (G1)
223	U9	VCC
224	U10	VDD (V1)
225	U11	CBE2#
226	U12	VSS
227	U13	VSS (G1)
228	U14	AD14
229	U15	VDD (V1)
230	U16	AD10
231	U17	VSS (G1)
176	U18	AD3
113	U19	AD4
42	U20	AD2
18	V1	VSS
93	V2	INTIN0
160	V3	PLOCK#
161	V4	PCIREQ#
162	V5	AD29
163	V6	AD28
164	V7	AD24
165	V8	IDSEL
166	V9	AD21
167	V10	AD18
168	V11	VCC
169	V12	TRDY#
170	V13	VCC
171	V14	PAR
172	V15	VSS
173	V16	AD12
174	V17	AD9
175	V18	VCC
112	V19	AD5
41	V20	VSS
19	W1	NO CONNECT
94	W2	PRST#
95	W3	PCIGNT#
96	W4	PCICLK
97	W5	VCC
98	W6	AD26
99	W7	CBE3#
100	W8	AD23
101	W9	AD20
102	W10	AD19
103	W11	VSS
104	W12	IRDY#
105	W13	STOP#
106	W14	SERR#
107	W15	CBE1#
108	W16	VCC
109	W17	AD11
110	W18	AD8
111	W19	CBE0#
40	W20	AD6
20	Y1	VCC
21	Y2	VSS
22	Y3	VDD
23	Y4	AD30
24	Y5	VSS
25	Y6	AD25
26	Y7	VSS
27	Y8	AD22
28	Y9	VSS
29	Y10	AD17
30	Y11	AD16
31	Y12	FRAME#
32	Y13	DEVSEL#
33	Y14	PERR#
34	Y15	VSS
35	Y16	AD15
36	Y17	AD13
37	Y18	VSS
38	Y19	VDD
39	Y20	AD7

12.5 Mechanical Specifications

Figure 12-7. PID Mechanical Specifications

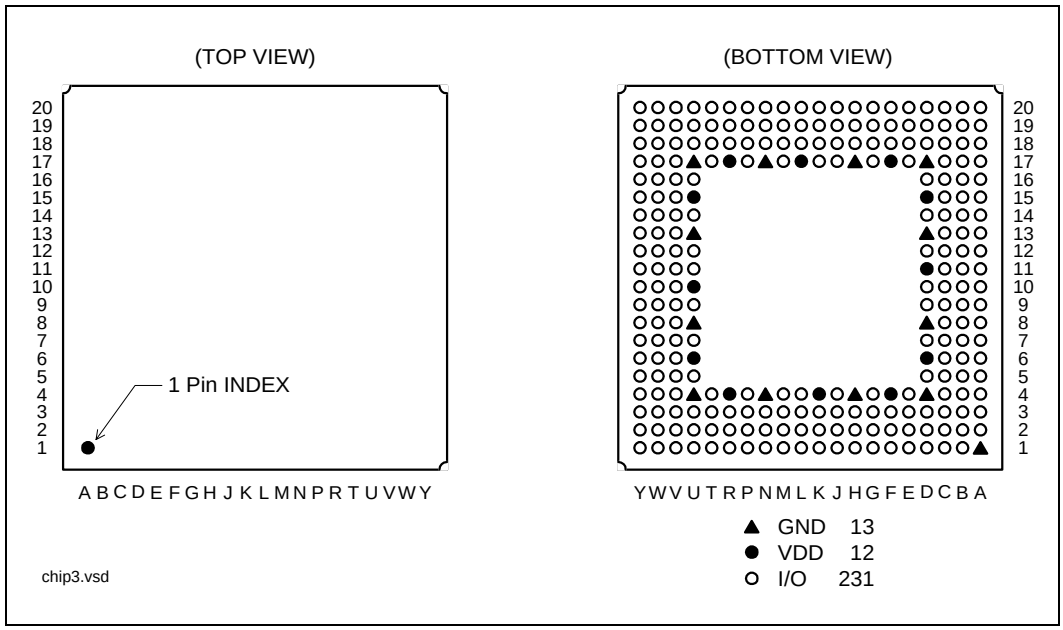


ITEM	MILLIMETERS	INCHES
A	27.0±0.2	1.063±0.008
B	24.0	0.945
C	24.0	0.945
D	27.0±0.2	1.063±0.008
E	1.44	0.057
F	1.27 (T.P.)	0.050 (T.P.)
G	0.6±0.1	0.024 +0.004 –0.005
H	0.36	0.014
I	1.53±0.15	0.060 +0.006 –0.007
J	2.13±0.25	0.084±0.01
K	0.15	0.006
L	ø0.75±0.15	ø0.03 +0.006 –0.007
M	0.3	0.012
P	C3.95	C0.156
R	30°	30°
S	1.5	0.059

NOTE
Each lead centerline is located within ø0.3 mm (ø0.012 inch) of its true position (T.P.) at maximum material condition.

chip2.vsd

Figure 12-8. 256-pin BGA Package Footprint, Top and Bottom View



12.6 Thermal Specifications

12.6.1 Thermal Resistance

For the 256-pin BGA package based on a power dissipation of 1W:

Θ_{JA} = 30°C/watt (still air)

Θ_{JA} = 26°C/watt (1.0 m/s airflow)

12.6.2 Maximum Ambient Temperature

T_A = 55°C (still air)

T_A = 70°C (1.0 m/s airflow)

12.6.3 Maximum Power Dissipation

P_D = 330mW at 3.3V