Chapter II

Monolithic Instrumentation Amplifiers

ADVANTAGES OVER OP-AMP IN-AMPS

To satisfy the demand for in-amps that would be easier to apply, monolithic IC instrumentation amplifiers were developed. These circuits incorporate variations in the three op-amp and two op-amp in-amp circuits previously described, while providing laser-trimmed resistors and other benefits of monolithic IC technology. Since both active and passive components are now within the same die they can be closely matched—this will ensure that the device provides a high CMR. In addition, these components will stay matched over temperature, assuring excellent performance over a wide temperature range. IC technologies such as laser wafer trimming allow monolithic integrated circuits to be "tuned-up" to very high accuracy and provide low cost, high volume manufacturing. A final advantage of monolithic devices is that they are available in very small, very low cost SOIC, or microSOIC packages designed for use in high volume production. Table II provides a quick performance summary of Analog Devices' in-amps.

Table II. Latest Generation Analog Devices In-Amps Summarized

Product	Features	Supply Current (Typ)	BW kHz (G = 1)	Input Offset Voltage (Max)	Input Offset Drift	RTI Noise nV/√Hz (G = 10)	Input Bias Current (Max)
AD620	General Purpose	0.9 mA	800	125 µV	1 µV/°C	12 Typ	2 nA
AD622	Low Cost	0.9 mA	800	125 µV	1 µV/°C	14 Typ	5 nA
AD621	Precise Gain	0.9 mA	800	250 µV (RTI)	2.5 µV/°C (RTI)	13 Typ (RTI)	2 nA
AD623	Low Cost, Single Supply	375 µA	800	200 µV	2 µV/°C	35 Typ	25 nA
AD627	Micropower	60 µA	80	250 µV	3 µV/°C	42 Typ	10 nA
AD626	High CMV	1.5 mA	100	500 µV	1 µV/°C	250 Typ	NS
AD830	Video In-Amp	15 mA	85 MHz	1500 µV	70 µV/°C	27 Typ	10 µA
AD629	High CMV Diff Amp	0.9 mA	500 kHz	1 mV	6 µV/°C	550 Typ (G = 1)	NA
AMP03	High BW, G = 1	3.5 mA	3 MHz	400 µV	NS	750 (RTO)	NS

NS: Not Specified.
NA: Not Applicable.

MONOLITHIC IN-AMP DESIGN—THE INSIDE STORY

Monolithic In-Amps Optimized for High Performance

Analog Devices introduced the first high performance monolithic instrumentation amplifier, the AD520, in 1971.

In 1992, the **AD620** was introduced and has now become the industry standard high-performance, low cost in-amp. The AD620 is a complete monolithic instrumentation amplifier offered in both 8-lead DIP and SOIC packages. The user can program any desired gain from 1 to 1000 using a single external resistor. By design, the required resistor values for gains of 10 and 100 are standard 1% metal film resistor values.

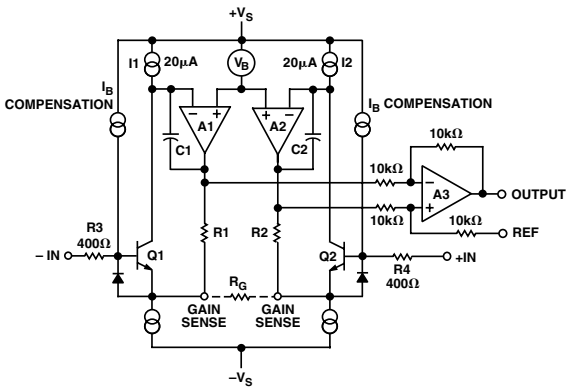

Figure 12. A Simplified Schematic of the AD620

The AD620 is a second-generation version of the classic AD524 in-amp and embodies a modification of the classic three op-amp circuit. Laser trimming of on-chip thin film resistors R1 and R2 allows the user to accurately set the gain—to 100 within ±0.5% max error, using only one external resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components.

A preamp section comprised of Q1 and Q2 provides additional gain up front. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains a constant collector current through the input devices Q1, Q2, thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity gain subtractor A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: First, the open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors.

Next, the gain bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing the amplifier's frequency response. Figure 13 shows the AD620's closed-loop gain vs. frequency.

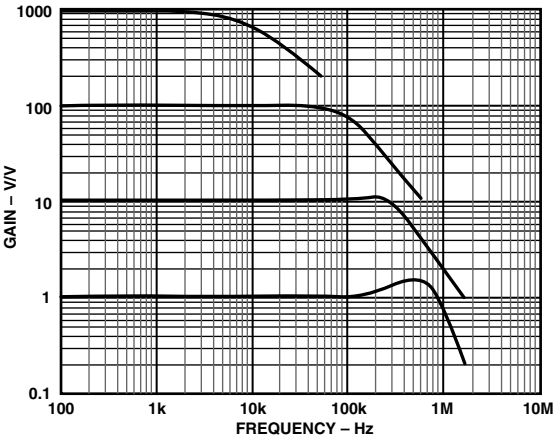

Figure 13. AD620 Closed-Loop Gain vs. Frequency

The AD620 also has superior CMR over a wide frequency range as shown by Figure 14.

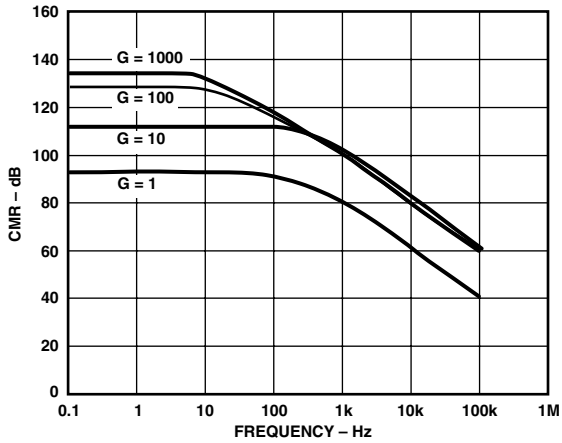

Figure 14. AD620 CMR vs. Frequency

Figures 15 and 16 show the AD620's gain nonlinearity and small signal pulse response.

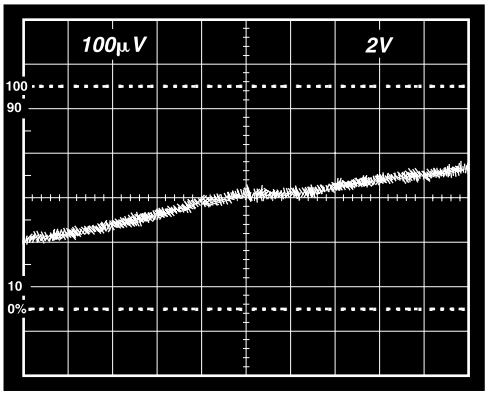

Figure 15. The AD620's Gain Nonlinearity. G = 100, R_L = 10 kΩ, Vert Scale: 100 µV = 10 ppm, Horiz Scale 2 V/Div.

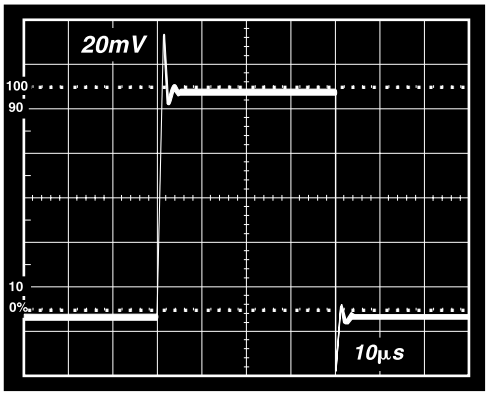

Figure 16. The Small Signal Pulse Response of the AD620. G = 10, R_L= 2 kΩ, C_L = 100 pF.

Finally, the input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2 are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor. The gain equation is then:

$$G = \frac{49.4\,k\Omega}{R_G}$$

So that:

$$R_G = \frac{49.4\,k\Omega}{G - 1}$$

Where resistor R_G is in kΩ.

The value of 24.7 kΩ was chosen so that standard 1% resistor values could be used to set the most popular gains.

The AD620 was the first in a series of high performance, low cost monolithic in-amps. Table III provides a brief comparison of the basic performance of the AD620 in-amp family.

Table III. AD620 Series In-Amps

Model	Max Input Voltage Noise	Max Input Bias Current	Input Stage Operating Current (Typ)
AD620	13 nV/√Hz	2 nA	20 µA
AD621	13 nV/√Hz	2 nA	20 µA
AD622	14 nV/√Hz	5 nA	20 µA
AD623	35 nV/√Hz	25 nA*	1.5 µA
AD627	42 nV/√Hz	10 nA*	0.8 µA

*Note that the AD623 and AD627 are single supply devices. Because of this, they do not include input current compensation in their design.

The **AD622** is a low cost version of the AD620 (see AD620 simplified schematic). The AD622 uses streamlined production methods to provide most of the performance of the AD620, at lower cost.

Figures 17, 18, and 19 show the AD622's CMR vs. frequency, gain nonlinearity, and closed-loop gain vs. frequency.

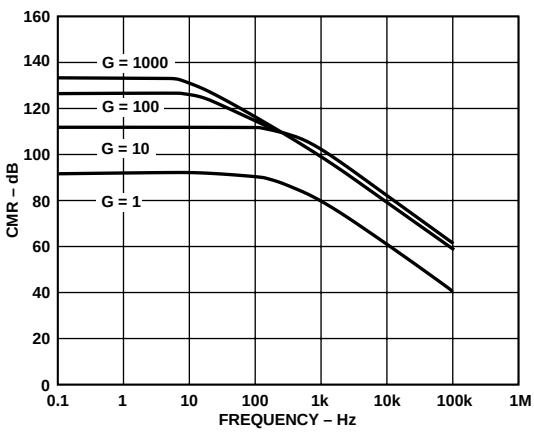

Figure 17. AD622 CMR vs. Frequency (RTI) 0 to 1 kΩ Source Imbalance

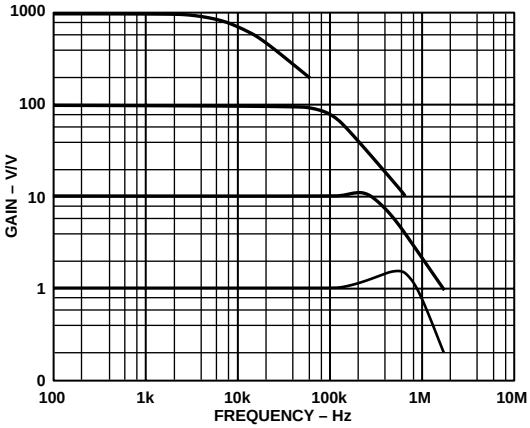

Figure 18. AD622 Closed-Loop Gain vs. Frequency

The **AD621** is also similar to the AD620, except that for gains of 10 and 100, the gain setting resistors are on the die—no external resistors are used. A single external jumper (between Pins 1 and 8) is all that is needed to select a gain of 100. For a gain of 10, leave Pin 1 and Pin 8 open. This provides excellent gain stability over temperature, as the on-chip gain resistor tracks the TC of the feedback resistor. Figure 20 is a simplified schematic of the AD621. With a max total gain error of 0.15% and ±5 ppm/°C gain drift, the AD621 has much greater built-in accuracy than the AD620.

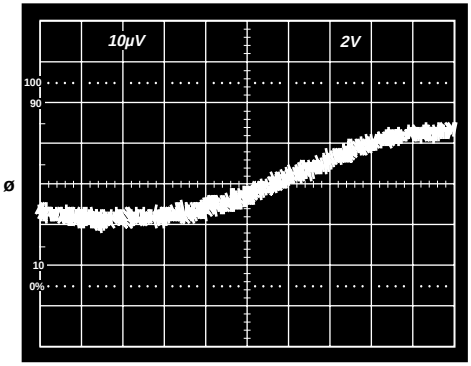

Figure 19. The AD622's Gain Nonlinearity
$G = 1$, $R_L = 10\ k\Omega$, Vert Scale: $20\ \mu V = 2$ ppm

The AD621 may also be operated at gains between 10 and 100 by using an external gain resistor, although gain error and gain drift over temperature will be degraded. Using external resistors, device gain is equal to:

$$G = (R1 + R2) / R_G + 1$$

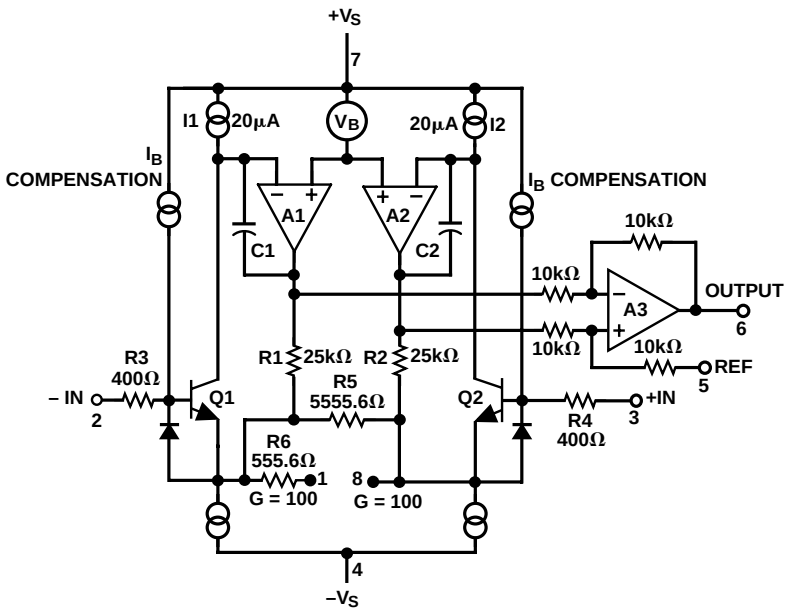

Figure 20. A Simplified Schematic of the AD621

Figures 21 and 22 show the AD621's CMR vs. frequency and closed-loop gain vs. frequency.

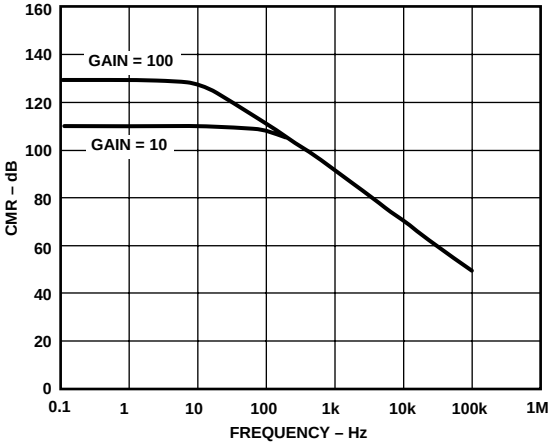

Figure 21. AD621 CMR vs. Frequency.

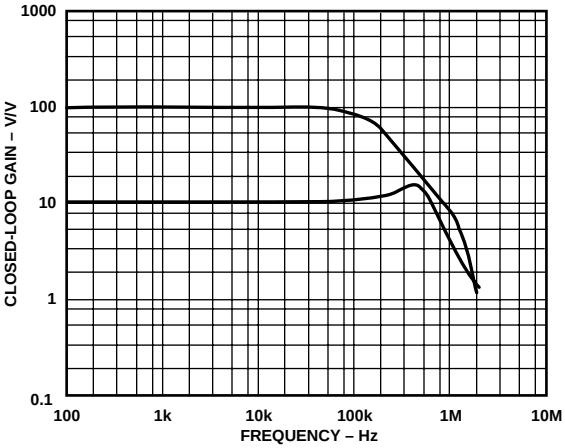

Figure 22. AD621 Closed-Loop Gain vs. Frequency

Figures 23 and 24 show the AD621's gain nonlinearity and small signal pulse response.

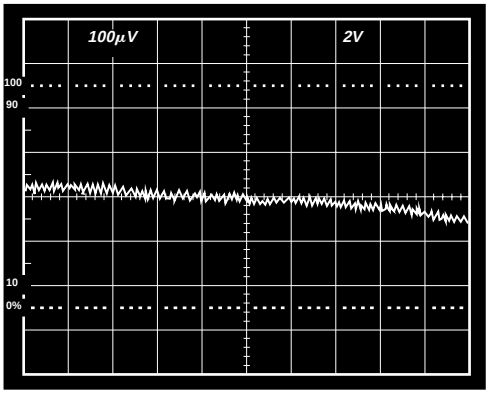

Figure 23. The AD621's Gain Nonlinearity. G = 10, R_L = 10 kΩ, Vert Scale: 100 µV/ Div = 100 ppm/Div, Horiz Scale 2 V/Div.

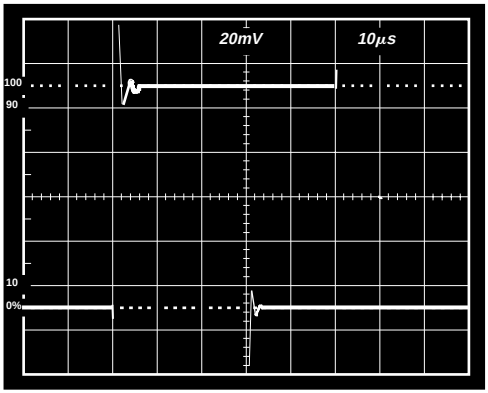

Figure 24. The Small Signal Pulse Response of the AD621. G = 10, R_L = 2 kΩ, C_L = 100 pF.

Monolithic In-Amps Optimized for Single Supply Operation

Single supply in-amps have special design problems that need to be addressed. The input stage needs to be able to amplify signals that are at ground potential (or very close to ground), and the output stage needs to be able to swing to within a few millivolts of ground or the supply rail. Low power supply current is also important. And, when operating from low power supply voltages, the in-amp needs to have an adequate gain-bandwidth product, low offset voltage drift, and good CMR vs. gain and frequency.

The **AD623** is an instrumentation amplifier based on the three op-amp in-amp circuit, modified to assure operation on either single or dual power supplies, even at common-mode voltages at or even below the negative supply rail (or below "ground" in single supply operation). Other features include: rail-to-rail output voltage swing, low supply current, microSOIC packaging, low input and output voltage offset, microvolt/dc offset level drift, high common-mode rejection, and only one external resistor to set the gain.

As shown in Figure 25, the input signal is applied to PNP transistors acting as voltage buffers and dc level-shifters. A resistor trimmed to within 0.1% of 50 kΩ in each amplifiers' (A1 and A2) feedback path assures accurate gain programmability.

The differential output is:

$$V_O = \left(1 + \frac{100\ k\Omega}{R_G}\right) + V_C$$

where R_G is in kΩ.

The differential voltage is then converted to a single-ended voltage using the output difference amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

Since all the amplifiers can swing to either supply rail, as well as have their common-mode range extended to below the negative supply rail, the range over which the AD623 can operate is further enhanced.

Note that the base currents of Q1 and Q2 flow directly "out" of the input terminals, unlike dual supply input-current compensated in-amps such as the AD620. Since the inputs (i.e., the bases of Q1 and Q2) can operate at "ground" i.e., 0 V (or, more correctly, at 200 mV below ground), it was not possible to provide input current compensation for the AD623. However, the input bias current of the AD623 is still very small: only 25 nA max.

The output voltage at Pin 6 is measured with respect to the "reference" potential at Pin 5. The impedance of the reference pin is 100 kΩ. Internal ESD clamping diodes allow the input, reference, output, and gain terminals of the AD623 to safely withstand overvoltages of 0.3 V above or below the supplies. This is true for all gains, and with power on or off. This last case is particularly important since the signal source and the in-amp may be powered separately. If the overvoltage is expected to exceed this value, the current through these diodes should be limited to 10 mA, using external current limiting resistors (see Input Protection section). The value of these resistors is defined by the in-amp's noise level, the supply voltage, and the required overvoltage protection needed.

The bandwidth of the AD623 is reduced as the gain is increased, since A1 and A2 are voltage feedback op-amps. However, even at higher gains, the AD623 still has enough bandwidth for many applications.

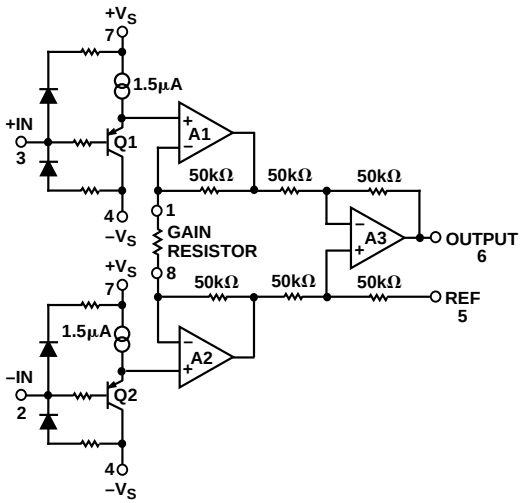

Figure 25. AD623 Simplified Schematic

The AD623's gain is resistor-programmed by R_G or, more precisely, by whatever impedance appears between Pins 1 and 8. Figure 26 shows the gain vs. frequency of the AD623. The AD623 is laser-trimmed to achieve accurate gains using 0.1% to 1% tolerance resistors.

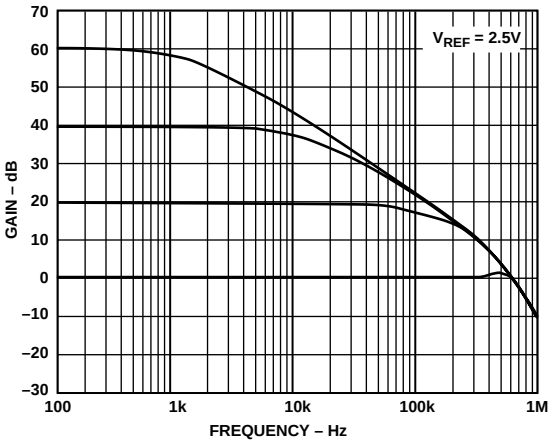

Figure 26. AD623 Closed-Loop Gain vs. Frequency

Table IV. Required Value of Gain Resistor

Desired Gain	1% Std Table Value of R_G, Ω	Calculated Gain Using 1% Resistors
2	100 k	2
5	24.9 k	5.02
10	11 k	10.09
20	5.23 k	20.12
33	3.09 k	33.36
40	2.55 k	40.21
50	2.05 k	49.78
65	1.58 k	64.29
100	1.02 k	99.04
200	499	201.4
500	200	501
1000	100	1001

Table IV shows required values of R_G for various gains. Note that for G = 1, the R_G terminals are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula:

$$R_G = 100\ k\Omega/(G - 1)$$

Figure 27 shows the AD623's CMR vs. Frequency. Note that the CMR increases with gain up to a gain of 100 and that CMR also remains high over frequency, up to 200 Hz. This ensures the attenuation of power line common-mode signals (and their harmonics).

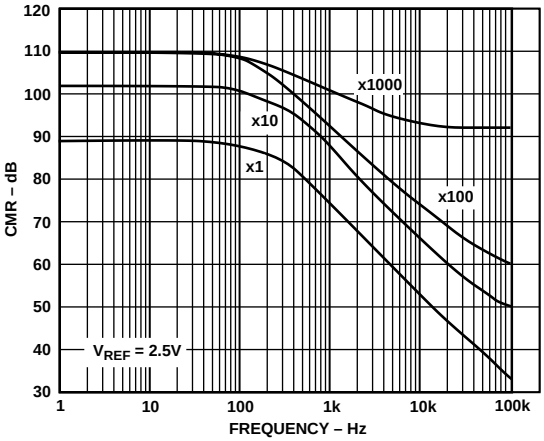

Figure 27. AD623 CMR vs. Frequency, $V_S = \pm 5$ V

The **AD627** is a single supply, micropower instrumentation amplifier that can be configured for gains between 5 and 1,000, using just a single external resistor. It provides a rail-to-rail output voltage swing, using a single +3 V to +30 V power supply. With a quiescent supply current of only 60 µA (typical), its total power consumption is less than 180 µW, operating from a +3 V supply.

Figure 28 shows the gain nonlinearity of the AD623.

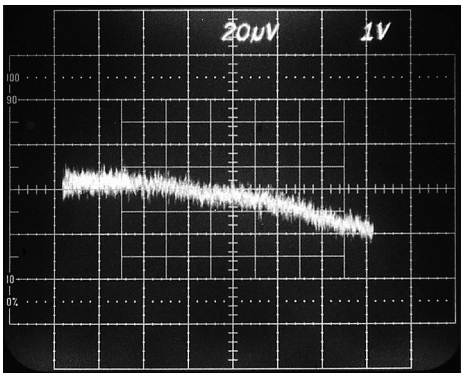

Figure 28. AD623 Gain Nonlinearity. G = –10, 50 ppm/Div

Figure 29 shows the small signal pulse response of the AD623.

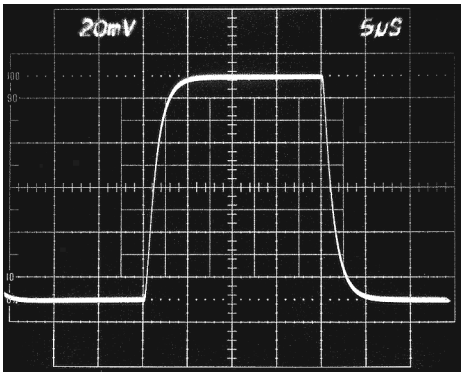

Figure 29. AD623 Small Signal Pulse Response. G = 10, R_L = 10 kΩ, C_L = 100 pF.

Figure 30 is a simplified schematic of the AD627. The AD627 is a true "instrumentation amplifier" built using two feedback loops. Its general properties are similar to those of the classic "two op-amp" instrumentation amplifier configuration, and can be regarded as such, but internally the details are somewhat different. The AD627 uses a modified "current feedback" scheme which, coupled with interstage feedforward frequency compensation, results in a much better CMRR (Common-Mode Rejection Ratio) at frequencies above dc (notably the line frequency of 50 Hz–60 Hz) than might otherwise be expected of a low power instrumentation amplifier.

As shown by Figure 30, A1 completes a feedback loop which, in conjunction with V1 and R5, forces a constant collector current in Q1. Assume that the gain-setting resistor (R_G) is not present for the moment. Resistors R2 and R1 complete the loop and force the output of A1 to be equal to the voltage on the inverting terminal with a gain of (almost exactly) 1.25. A nearly identical feedback loop completed by A2 forces a current in Q2, which is substantially identical to that in Q1, and A2 also provides the output voltage. When both loops are balanced, the gain from the noninverting terminal to V_{OUT} is equal to 5, whereas the gain from the output of A1 to V_{OUT} is equal to –4. The inverting terminal gain of A1, (1.25) times the gain of A2, (–4) makes the gain from the inverting and noninverting terminals equal.

The differential mode gain is equal to 1 + R4/R3, nominally five, and is factory trimmed to 0.01% final accuracy (AD627B typ). Adding an external gain setting resistor (R_G) increases the gain by an amount equal to (R4 + R1)/R_G. The output voltage of the AD627 is given by the following equation.

$$V_{OUT} = [V_{IN}(+) - V_{IN}(-)] \times (5 + 200\ k\Omega/R_G) + V_{REF}$$

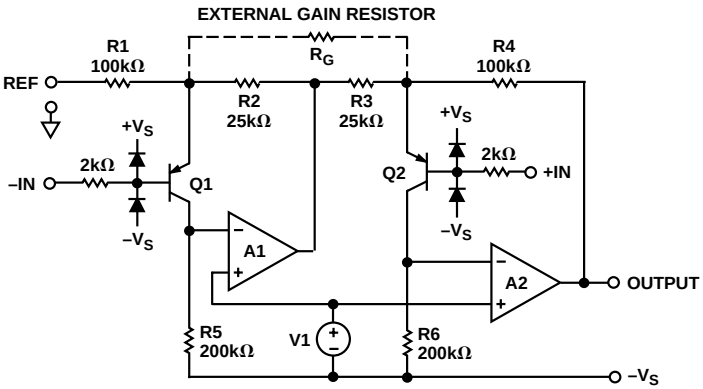

Figure 30. AD627 Simplified Schematic

Laser trims are performed on resistors R1 through R4 to ensure that their values are as close as possible to the absolute values in the gain equation. This ensures low gain error and high common-mode rejection at all practical gains.

Figure 31 shows the AD627's CMR vs. frequency.

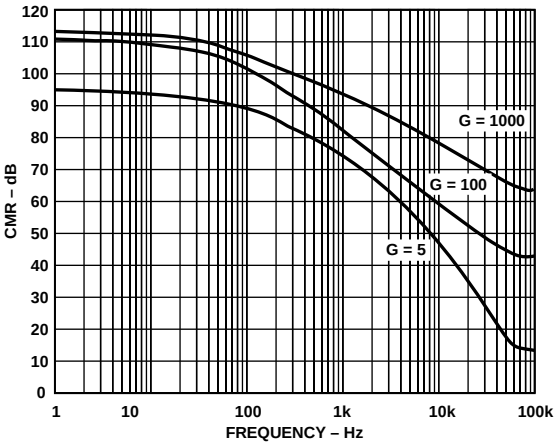

Figure 31. AD627 CMR vs. Frequency

Figures 32 and 33 show the AD627's gain vs. frequency and gain nonlinearity.

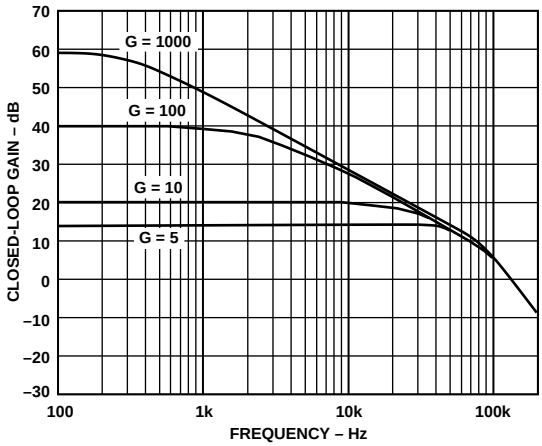

Figure 32. AD627 Closed-Loop Gain vs. Frequency

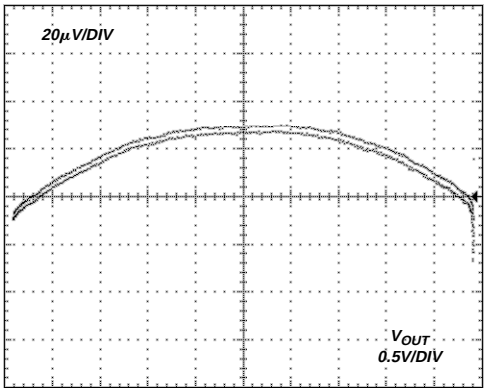

Figure 33. AD627 Gain Nonlinearity. $V_S = \pm 2.5$ V, G = 5

The AD627 also has excellent dynamic response, as shown by Figure 34.

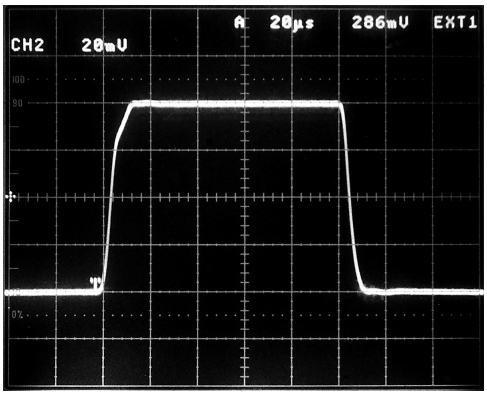

Figure 34. The Small Signal Pulse Response of the AD627. $V_S = \pm 5$ V, G = +10, R_L = 20 kΩ, C_L = 50 pF

Difference (Subtractor) Amplifier Products

The **AMP03** is a monolithic unity-gain, 3 MHz differential amplifier. Incorporating a matched thin-film resistor network, the AMP03 features stable operation over temperature without requiring expensive external matched components. The AMP03 is a basic analog building block for differential amplifier and instrumentation applications (Figure 35).

The differential amplifier topology of the AMP03 serves both to amplify the difference between two signals and to provide extremely high rejection of the common-mode input voltage. With a typical common-mode rejection of 100 dB, the AMP03 solves common problems encountered in instrumentation design. It is ideal for performing either the addition or subtraction of two input signals without using expensive externally-matched precision resistors. Due to its high CMR over frequency, the AMP03 is an ideal general-purpose amplifier for data acquisition systems that must operate in a noisy environment. Figures 36 and 37 show the AMP03's CMR and closed-loop gain vs. frequency.

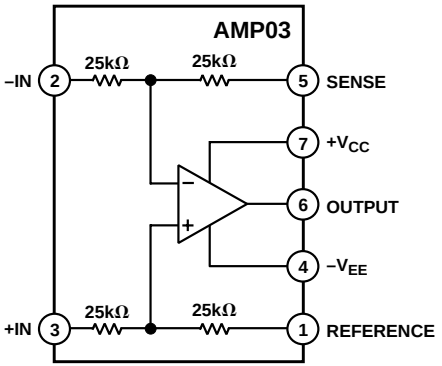

Figure 35. AMP03 Functional Block Diagram

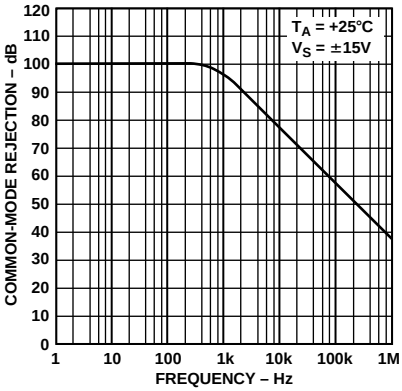

Figure 36. AMP03 CMR vs. Frequency

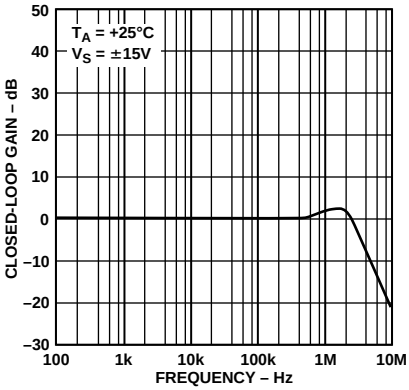

Figure 37. AMP03 Closed-Loop Gain vs. Frequency

Figure 38 shows the small signal pulse response of the AMP03.

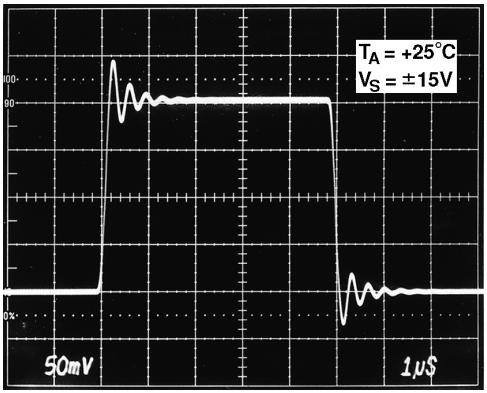

Figure 38. AMP03 Small Signal Pulse Response

The **AD626** is a single or dual supply differential amplifier consisting of a precision balanced attenuator, a very low drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages (much greater than the supply voltage) without the use of any other active components.

Figure 39 shows the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to dual resistive attenuators R1 through R4 whose purpose is to reduce the peak common-mode voltage at the input to the preamplifier—a feedback stage based on the very low drift op-amp A1. This allows the differential input voltage to be accurately amplified in the presence of large common-mode voltages—six times greater than that which can be tolerated by the actual input to A1. As a result, the input common-mode range extends to six times the quantity (V_S – 1 V). The overall common-mode error is minimized by precise laser-trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio of at least 10,000:1 (80 dB). The output of A1 is connected to the input of A2 via a 100 kΩ (R12) resistor to facilitate the low-pass filtering of the signal of interest. The AD626 is easily configured for gains of 10 or 100. For a gain of 10, Pin 7 is simply left unconnected; similarly, for a gain of 100, Pin 7 is grounded. Gains between 10 and 100 are easily set by connecting a resistor between Pin 7 and Analog GND. Because the on-chip resistors have an absolute tolerance of ±20% (although they are ratio matched to within 0.1%), at least a 20% adjustment range must be provided. The nominal value for this gain setting resistor is equal to:

$$R = \left(\frac{50,000\,\Omega}{GAIN - 10}\right) - 555\,\Omega$$

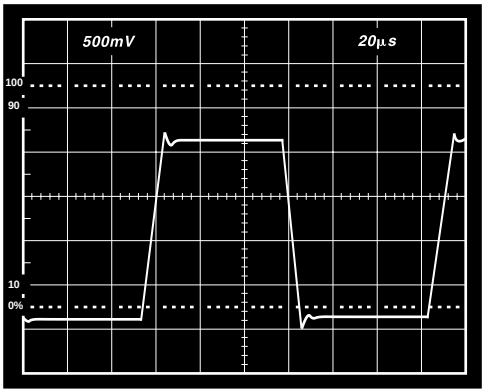

Figure 40. The Large Signal Pulse Response of the AD626. G = 10

Figure 40 shows the large signal pulse response of the AD626.

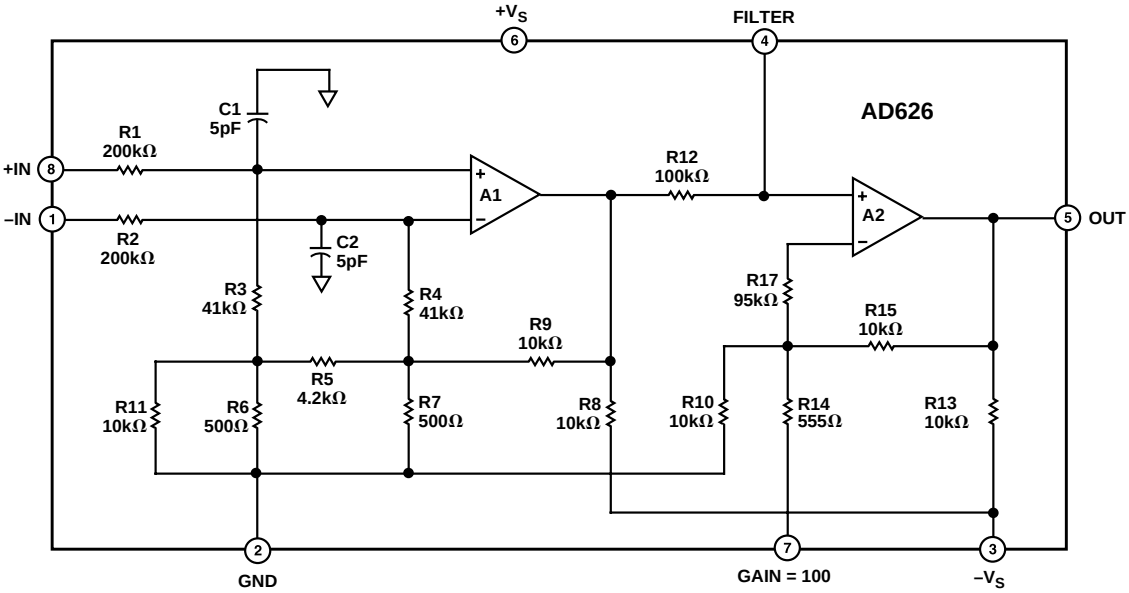

Figure 39. AD626 Simplified Schematic

The **AD629** is a unity gain difference amplifier designed for applications that require the measurement of signals with common-mode input voltages of up to ±270 V. The AD629 has excellent ac and dc specifications that keep errors low when measuring small difference voltages over a wide temperature range. Additionally, the AD629 keeps errors to a minimum by providing excellent CMR in the presence of high common-mode input voltages. Finally, it can operate from a wide power supply range of ±2.5 V to ±18 V.

The AD629 can replace costly isolation amplifiers in applications that do not require galvanic isolation. Figure 41 is the connection diagram of the AD629. Figure 42 shows the AD629's CMR vs. Frequency.

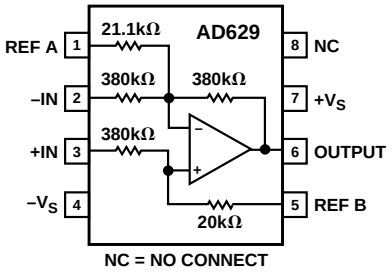

Figure 41. AD629 Connection Diagram

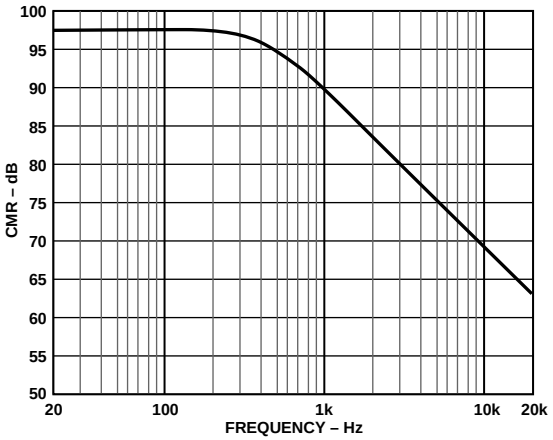

Figure 42. Common-Mode Rejection vs. Frequency

Video Speed In-Amp Products

The **AD830** is a wideband, differencing amplifier designed for general purpose signal processing from dc to 10 MHz (Figure 43). High impedance inputs ease interfacing to finite source impedances and thus preserve its excellent common-mode rejection. In many respects, such as high frequency common-mode rejection, it offers significant improvements over discrete difference amplifier designs.

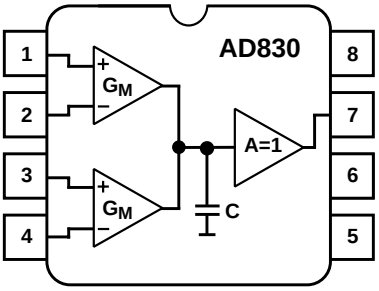

Figure 43. AD830 Connection Diagram

The AD830 uses an active feedback topology to provide inherent advantages in the handling of differential signals, differing system commons, level-shifting and low distortion, high frequency amplification.

The AD830's topology, reduced to its elemental form, is shown in Figure 44. The key feature of this topology is the use of two identical voltage-to-current converters, G_M, that make up the input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage-to-current converters possess fully differential inputs, high linearity, high input impedance and wide voltage range operation.

The two G_M stage current outputs I_X and I_Y, sum together at a high impedance node that is characterized by an equivalent resistance and capacitance connected to an "ac common." A unity voltage gain stage follows the high impedance node, to provide buffering from loads.

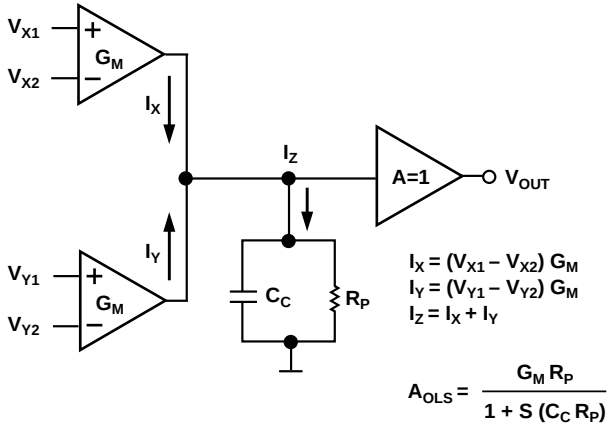

Figure 44. Topology Diagram

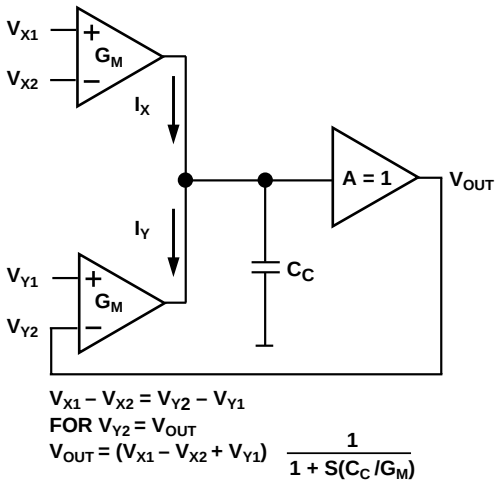

Figure 45. Closed-Loop Connection

Precise amplification is accomplished through closed-loop operation of this topology. Voltage feedback is implemented via the Y G_M stage in which the output is connected to the –Y input for negative feedback as shown in Figure 45. An input signal is applied across the X G_M stage, either differentially or single-ended, which produces a current that is summed at the high impedance node with the output current from the Y G_M stage.

Negative feedback nulls this sum to a small error current necessary to develop the output voltage at the high impedance node. The error current is usually negligible, so the null condition essentially forces the Y G_M output stage current to exactly equal the X G_M output current.

Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input. It is important to note that the bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830.

Figures 46 and 47 show the AD830's CMR vs. frequency and normalized gain vs. frequency.

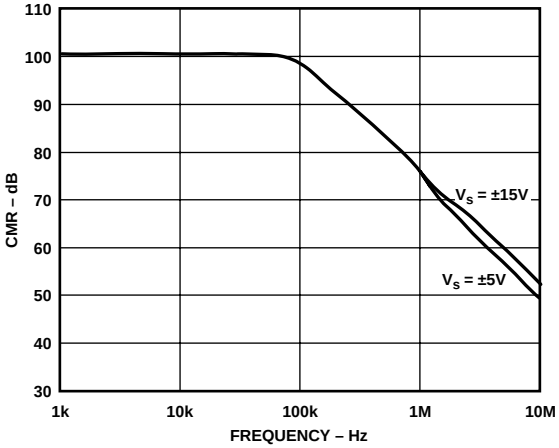

Figure 46. AD830 CMR vs. Frequency

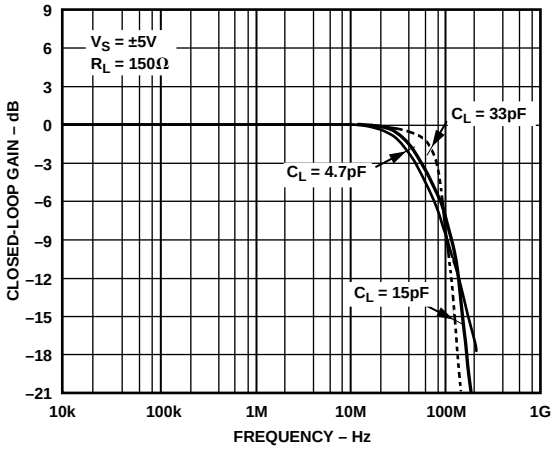

Figure 47. AD830 Closed-Loop Gain vs. Frequency

For details concerning the entire line of monolithic in-amps produced by Analog Devices, refer to Appendix B.