PHAST-1 Device
SONET STS-1 Overhead Terminator
TXC-06101

DATA SHEET

FEATURES

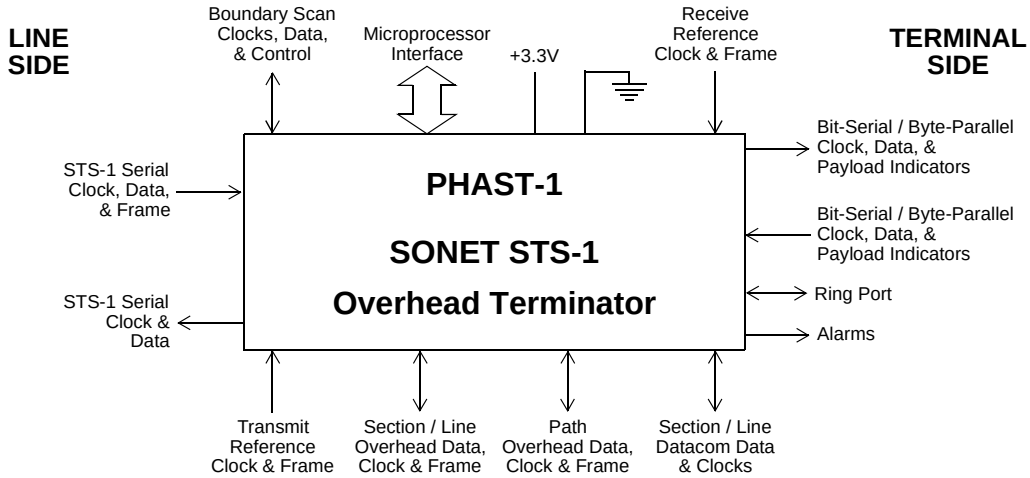
- Provides SONET interface to any type of payload
- Programmable STS-1 or STS-N modes
- Receive bit-serial STS-1 signal input to the Line Side using external reference frame pulse for STS-N applications
- Transmit bit-serial STS-1 signal output from the Line Side using external reference frame pulse for outgoing phase synchronization
- Programmable: full STS-1 or SPE-only I/O on the Terminal Side
- 51.84 Mbit/s bit-serial, or 6.48/19.44 Mbyte/s byte-parallel I/O on the Terminal Side
- Optional AIS communication with peer PHAST-1, SOT-1, SOT-1E, or SOT-3 devices
- Interfaces to microprocessors with hierarchical scan and optional hardware interrupt on alarms
- SONET alarm processing and performance monitoring
- Meets ANSI and Bellcore standards:
  - T1.105-1995
  - GR-253-CORE
  - TR-NWT-000496
  - GR-1400-CORE
  - GR-499
  - GR-1230
- Ring port for USHR/P support
- Boundary Scan Capability (IEEE 1149.1)
- Single + 3.3 volt ± 5% power supply
- 144-pin low profile plastic quad flat package

DESCRIPTION

The PHAST-1 SONET STS-1 Overhead Terminator performs Section, Line and Path Overhead processing for STS-1 SONET signals. This versatile device can be used anywhere in a SONET network where STS-1 signals are in use, e.g., repeaters, and Line or Path termination points. Interfaces are provided for both Section and Line Orderwire and Datacom channels. Further, control bits in the Memory Map enable the PHAST-1 to perform loopback and serial or parallel input/output. Line Side and Terminal Side clock rates can differ. The Receive and Transmit Pointers are recalculated as necessary to compensate for clock differences. All overhead bytes are stored in on-chip RAM. New overhead bytes can be substituted from RAM to either the Terminal or Line Side, depending on the application. The PHAST-1 also provides alarm detection and AIS generation, as well as software and hardware interrupt in the event of errors.

APPLICATIONS

- SONET W-DCS/B-DCS
- SONET terminal or add/drop multiplexers
- High-speed data communication
- Payload extraction, introduction into STS-1
- STS-N multiplexer
- SONET test sets



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TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

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SONET TUTORIAL

A primary goal in developing the SONET (Synchronous Optical NETwork) format was to define a synchronous, optical hierarchy with sufficient flexibility to carry many different payloads. This has been accomplished by defining a basic signal of 51.84 Mbit/s and a byte-interleaved multiplex scheme that results in a family of standard rates and formats defined at a rate of N times 51.84 Mbit/s, where N is an integer. Since some signals that must be transported have speeds greater than the basic rate, a technique of linking several basic rate signals together to form a transport signal of varying capacity has also been defined. There are three major differences between the SONET Hierarchy and the North American Digital Hierarchy (NADH)[1]:

1. SONET is synchronous. All SONET tributaries in a SONET network must be traceable to one or more Stratum 1 synchronization sources.
   NADH is asynchronous. The tributaries need not be synchronized.

2. SONET is a harmonic multiplexing structure. All higher rate SONET signals are integer multiples of a base rate. Lower order SONET tributaries are byte-interleaved to form the higher order SONET signal.
   NADH is hierarchical. Higher order multiplexing is accomplished with bit stuffing to accommodate speed differences in lower order tributaries.

3. SONET overhead (Framing, Performance Monitoring, Alarms, etc.) and payload are distinct entities. In a SONET signal the payload bits do not occupy a fixed position in relation to the transport overhead bits. A pointer mechanism is used to identify the start of the payload.
   NADH overhead bits and payload bits have a fixed, unvarying relationship to each other.

The Basic modular signal (at 51.84 Mbit/s) is called the Synchronous Transport Signal level One (STS-1). The optical counterpart is the Optical Carrier level One (OC-1), which is the result of direct optical conversion of the STS-1 signal. Higher level signals are denoted by STS-N and OC-N, where N is an Integer. At present the standardized values of N are: 1, 3, 12, 24, 48 and 192. These values provide standardized multiplexing rates for SONET systems at 51.84 Mbit/s, 155.52 Mbit/s, 622.08 Mbit/s, 1.24416 Gbit/s, 2.48832 Gbit/s and 9.95328 Gbit/s, respectively.

FORMATS

There are four basic formats upon which the SONET Hierarchy is built.

STS-1 Structure

The basic SONET format is the 51.84 Mbit/s signal designated STS-1. It consists of 810 eight-bit bytes arranged in a matrix of nine rows each of which has 90 columns as shown in Figure 1. This nine by 90 arrangement is referred to as a SONET Frame. It repeats every 125 microseconds. The first three columns consist of the Transport Overhead (TOH). The remaining 87 columns are referred to as the Synchronous Payload Envelope (SPE). It is this portion of a SONET signal that is allowed to "float." Within the TOH is a pointer that identifies the starting position of the SPE with respect to the TOH Bytes in the Frame. The first column of the SPE is the Path Overhead (POH). The other 86 columns contain the actual payload information whose capacity is approximately 50 Mbit/s.

1. The North American Digital Hierarchy is described in ANSI standard T1.107. The ITU-T term "PDH" (Plesiochronous Digital Hierarchy) is used to refer generically to an asynchronous multiplexing structure.

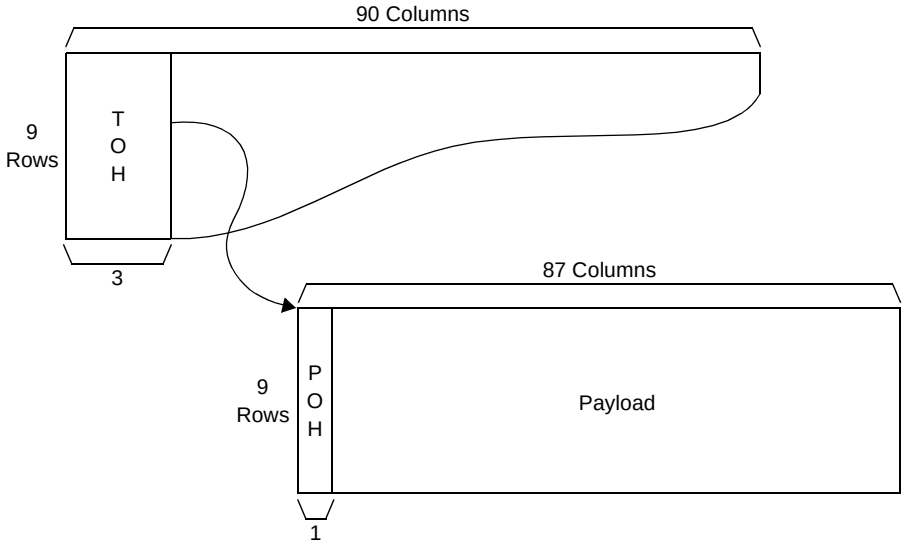


Figure 1. STS-1 Format

STS-N Structure

STS-N formats are higher order multiplex structures which allow the transportation of N number of 50 Mbit/s payloads (e.g., STS-3 transports three 50 Mbit/s payloads). As shown in Figure 2, the Frame consists of nine rows and N × 90 columns. The TOH is N × 3 columns wide. There are N number of nine by 87 SPEs, each of which contains one column of POH. The TOH contains N number of pointers: one for each of the SPEs.

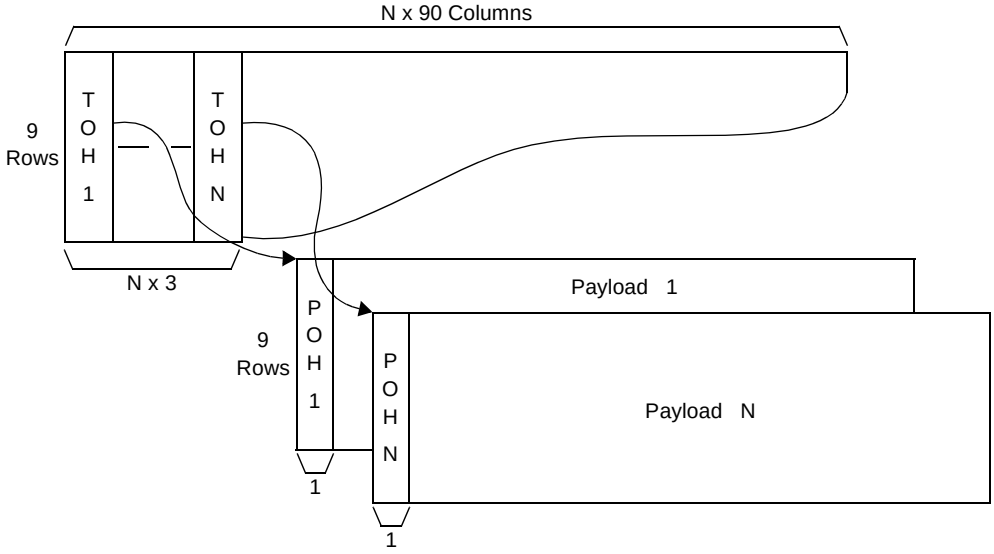


Figure 2. STS-N Format

STS-Nc Structure

As mentioned earlier, SONET contains a mechanism by which payloads that are larger than ≈ 50 Mbit/s can be carried. This mechanism is called Concatenation and is indicated by the designation Nc. STS-Nc formats are higher order structures which allow the transportation of a single payload whose bandwidth is approximately N × 50 Mbit/s (e.g., STS-3c transports a single 149.76 Mbit/s payload).The STS-Nc format is shown in Figure 3. As with the STS-N format, the Frame consists of nine rows and N × 90 columns. The TOH is N × 3 columns wide. There is a single SPE which is nine rows by N × 87 columns. The first SPE column is used for POH. The TOH contains one pointer which identifies the start of the SPE in the Frame.

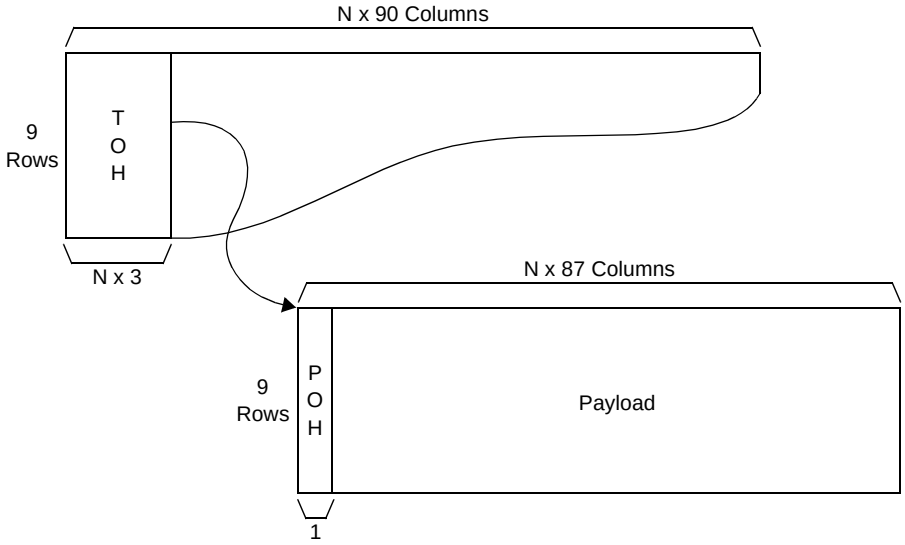


Figure 3. STS-Nc Format

Virtual Tributary Structures

The Virtual Tributary (VT) is a structure designed for transport and switching of sub-STS-1 payloads (payloads less than DS3). As shown in Figure 4, it contains a VT Pointer, which indicates the start of the VT SPE. The VT SPE is composed of VT POH and Tributary Data (Payload). The VT Pointer provides for flexible and dynamic alignment of the VT SPE within the VT, independent of other VTs in the STS-1 SPE.

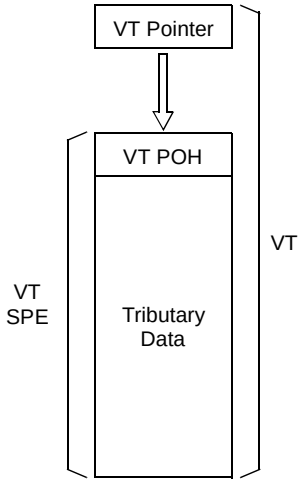


Figure 4. VTn Format

There are four sizes of VT: the VT1.5 (≈ 1.7 Mbit/s), the VT2 (≈ 2.3 Mbit/s), the VT3 (≈ 3.5 Mbit/s) and the VT6 (≈ 6.9 Mbit/s). These are shown in Figure 5. In the nine-row format of the STS-1 SPE they occupy three columns, four columns, six columns and twelve columns, respectively. VTs may only be carried in an STS-1 SPE. STS-Nc SPEs cannot be subrated into VTs. For example, to carry 84 DS1s in SONET an STS-3 format must be used with each STS-1 SPE organized as 28 VT1.5s.

Four consecutive 125-microseconds frames of the STS-1 SPE are organized into a 500-microseconds Superframe, the phase of which is indicated by a Multiframe Indicator Byte (H4) in the STS-1 POH. This defines a 500-microseconds structure for each of the VTs, called the VT Superframe, which is shown in Figure 6. The VT Superframe contains the VT Pointer and the VT SPE. The VT Pointer occupies four bytes designated V1, V2, V3 and V4 and the remaining bytes define the VT SPE, the capacity of which is different for each VT type. The placement of the V1 through V4 Bytes is such that they will appear in Byte 1 (shown in Figure 5) of the VT regardless of the VT size. Since the PHAST-1 does not process VTs there will be no further discussion of VT characteristics.

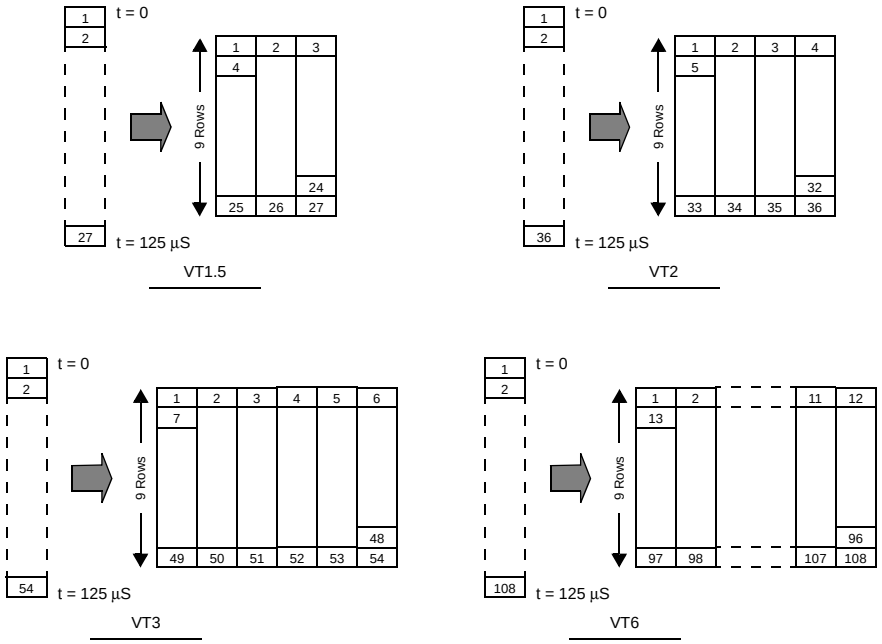


Figure 5. VT Sizes

OVERHEAD

The overhead and transport functions in SONET have been broken into layers to promote understanding and structure. In order of increasing complexity the layers are: Physical Medium, Section, Line and Path. When viewed with a bottom-up approach, each layer builds upon the services provided by the lower layer. The Physical Medium Layer provides transmission at a standard bit rate. The Section layer provides framing, scrambling, and Section maintenance for the bits being transmitted. The Line layer provides Line maintenance and protection as well as multiplexing of the STS SPEs. The Path layer provides the payload mapping function and Path maintenance. Note than all layers can be implemented in a single piece of equipment or they can be broken into multiple pieces of equipment.

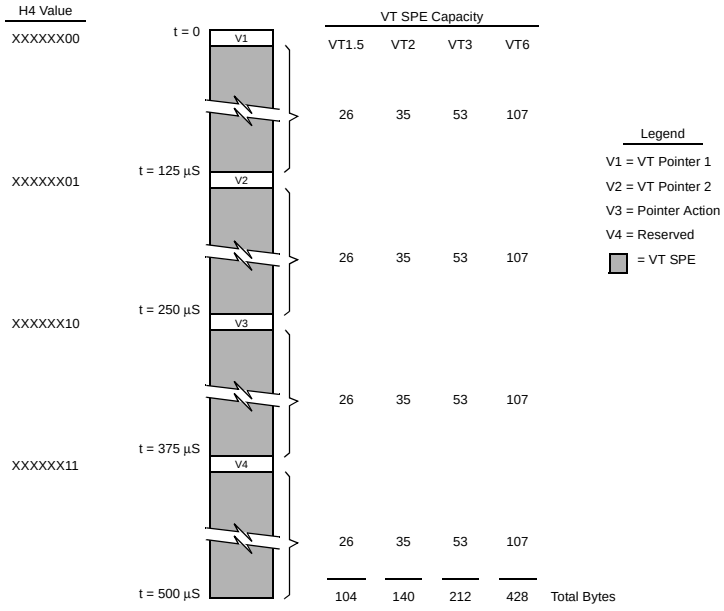


Figure 6. VT Superframe

Physical Medium Layer

The Physical Medium Layer deals with transport of the bits across the transmission medium. No overhead is associated with this layer. Its main function is the conversion between signals internal to a Network Element (NE) and signals suitable for transmission. Issues dealt with at this layer include pulse shape, power levels, and (for optical equipment) wavelength. Electro-optical units communicate at this level.

Section Layer

The Section Layer deals with the reliable transport of an STS-N frame across the physical medium. Functions within this layer include framing, scrambling, error monitoring, data communications, and a local orderwire. Section and Physical Medium Layers can be utilized in some equipment without any higher order layers. A regenerator would operate in this manner.

Line Layer

The Line Layer deals with the reliable transport of Path Layer payload and its overhead across the Section and Physical Medium Layers. Overhead added here is accessed at points where SPEs are multiplexed together. The functions of this layer are to provide synchronization and multiplexing for the Path Layer, as well as error monitoring, data communications, orderwire, and protection signaling for Line protection switching. An example of equipment that communicates at this level is an OC-M to OC-N multiplexer *where*: M < N.

Path Layer

The Path Layer deals with the reliable transport of services over the Line, Section and Physical Medium Layers. Examples of such services are DS1s, DS3s and ATM signals. The main function of this layer is to map the services into the format required by the Line Layer. In addition, this layer provides error monitoring and connectivity checks. The overhead defined for this layer is read, interpreted, and modified by equipment that creates or disassembles the SONET payload for a given service. POH may be monitored but not modified by Line processing equipment. There is an exception to this last statement. Line processing elements that have implemented Tandem Connection Maintenance (see ANSI T1.105.05) may modify certain Path Layer bytes. However, the original Path Layer information must be restored at the termination point of the Tandem Connection function. An example of equipment that communicates at the Path level is a DS3 to STS-1 mapping circuit.

Overhead Termination

Any NE that originates or terminates an overhead layer is considered to be a terminating entity for that layer. This defines three types of NEs:

1. Section Terminating Equipment (STE)
2. Line Terminating Equipment (LTE)
3. Path Terminating Equipment (PTE)

Peer communications occur between pieces of equipment that terminate a particular layer. Examples of STE, LTE, and PTE Equipment and the layers processed by each entity are shown in Figure 7. There are four multiplexers and two regenerators (repeaters) in this example. The two multiplexers on the left and the one on the right are multiplexing and de-multiplexing DS3s into and out of a SONET signal. The multiplexer in the middle represents a higher order unit which is multiplexing and de-multiplexing lower order SONET signals to and from a higher order signal. Since the Physical Medium Layer does not have any overhead associated with it, it will not be discussed. By definition, all SONET NEs are Section Terminating and a regenerator is only STE. There are five Section Layer peer communication links. There are three Line Layer peer communication links: one from each of the leftmost multiplexers to the middle multiplexer, and one between the middle multiplexer and the multiplexer on the right. Finally, there are two Path Layer peer communication links. These exist between the multiplexers on the left and the multiplexer on the right.

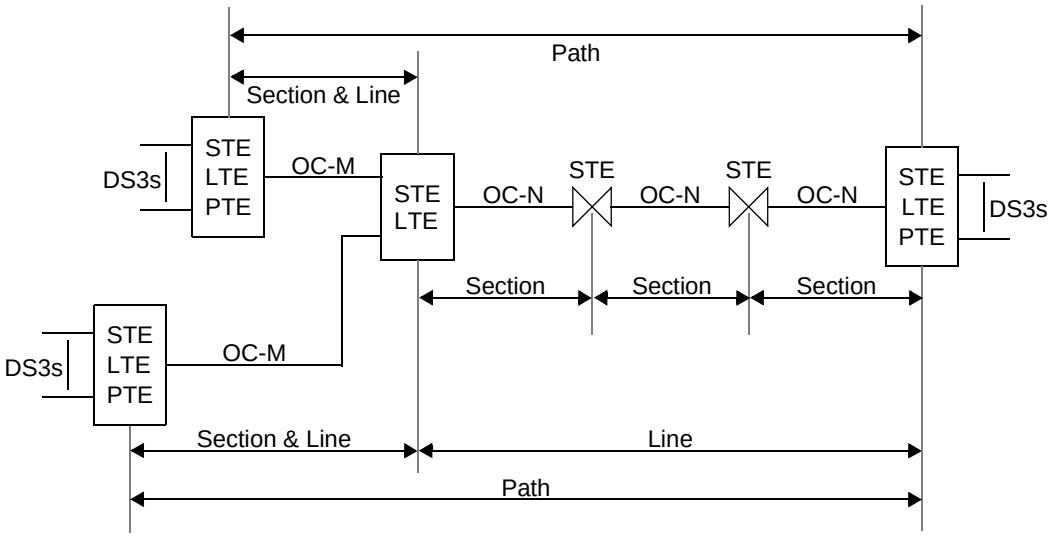


Figure 7. Overhead Utilization

Overhead Locations

The functions of the Section and Line Layers have been combined into a structure of 27 bytes called Transport Overhead (TOH) which occupies the first three columns of an STS-1 Frame. The first three rows are Section Overhead (SOH). The last six rows are Line Overhead (LOH). This is shown in Figure 8. In STS-N and Nc frames there are 3 × N TOH columns. Figures 9 and 10 represent STS-N and Nc formats using STS-3 and 3c as an example. The byte-interleaved characteristic of SONET can be seen in these figures. Some of the transport overhead fields in STS-1 numbers two through N are the same as for STS-1 number one and some are not. In the STS-3 Format there are three H1 and H2 Bytes. Each H1, H2 combination is a pointer for one of the three payloads that is being transported. The STS-3c format is carrying one ≈ 150 Mbit/s payload. There is only one pointer. The H1 and H2 bytes in the STS-1 number one position are the pointer. The two remaining H1 and H2 byte pairs in STS-1 positions two and three are the Concatenation Indicators.

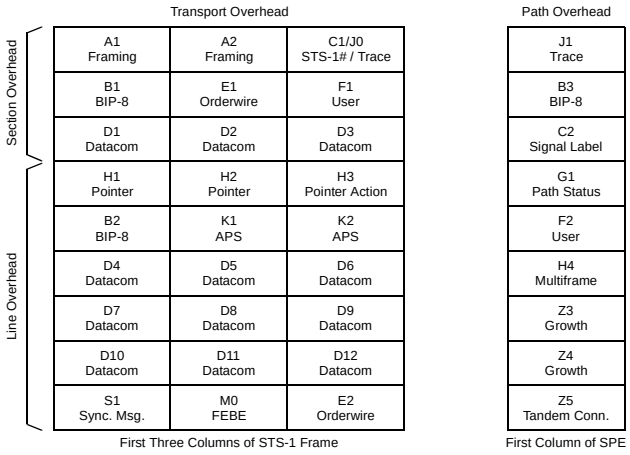


Figure 8. STS-1 Overhead

The Path Layer functions are assigned to the nine bytes occupying the first column of the STS SPE. The distinction between TOH and POH is made so that transmission equipment can be specified without regard to the information structure that is being transported. The STS-1 and STS-3c formats have only one POH field. In the STS-3 format there are three POH fields, one for each payload. The shaded diagonals represent Pointer and POH bytes associated with STS-1 numbers two and three.

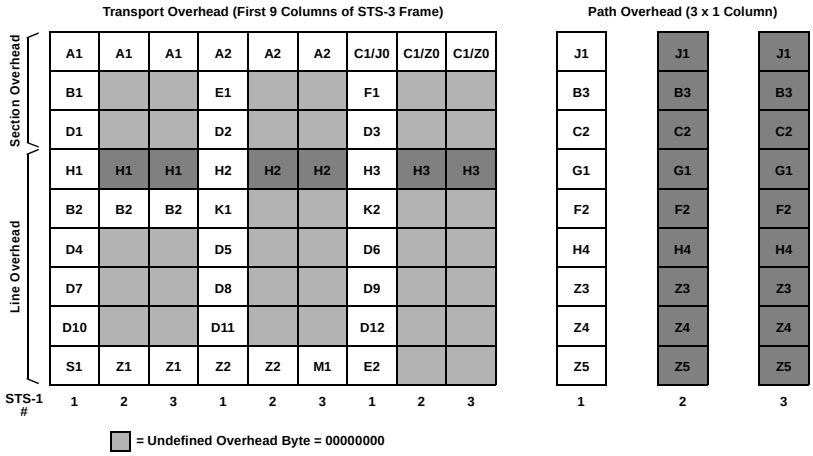


Figure 9. STS-3 Overhead

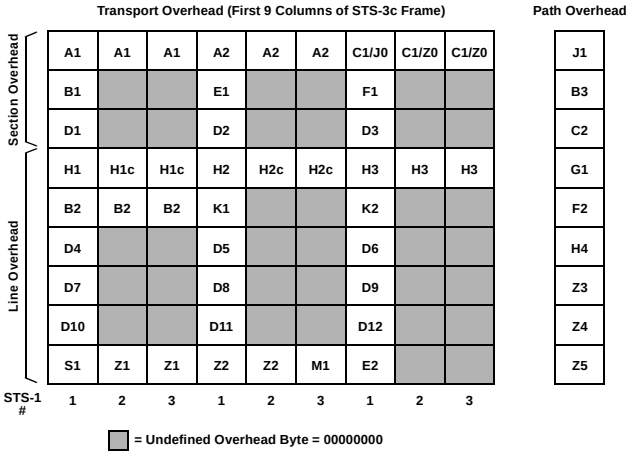


Figure 10. STS-3c Overhead

Section Overhead Definitions - SOH

The definitions for the Section Overhead Bytes are given below.

A1, A2: Framing - Two bytes are allocated in each STS-1 for Framing. The Pattern is A1 = F6[H] and A2 = 28[H]. These bytes are provided in all STS-1 portions of an STS-N/Nc signal.

C1: STS-1 I.D. - In earlier editions of the SONET standard, one byte labeled C1 in each STS-1 was allocated for an STS-1 identification function. These bytes are no longer used for this purpose. Instead, this overhead is currently allocated for Section Trace and Section Growth (defined below). However, to ensure interworking with older equipment, these bytes must be capable of transmitting and receiving the STS-1 Identification Codes. When used in this manner the following definition will apply. The C1 byte in Each STS-1 shall be set to a binary number corresponding to its order of appearance in the byte-interleaved STS-N frame where 01[H] is the number for the first STS-1 appearing in the frame. The C1 Byte is defined for all STS-1s in an STS-N/Nc signal.

J0: Section Trace - One byte is allocated to be used for a Section Trace function. This byte is defined only for STS-1 number one in an STS-N/Nc signal. J0 (formerly C1 of STS-1 number one) is used to repetitively transmit a one-byte fixed length string so that a receiving terminal can verify its continued connection to the intended transmitter. Any value in the range of 00[H] through FF[H] may be placed in this byte. When the Section Trace function is not supported or if no value has been assigned then 01[H] shall be transmitted.

Z0: Section Growth - One byte is defined in each STS-1 for future growth, except for STS-1 number one (defined as J0). For interworking with older equipment, the Z0 bytes shall be capable of being set consistent with the C1 definition described above.

B1: Section BIP-8 - One byte is allocated for a Section Error Monitoring function. This function is a bit-interleaved parity 8 code using even parity. The Section BIP-8 is calculated over all bits of the previous STS-N/Nc frame after scrambling. The computed BIP-8 is placed in the B1 Byte before scrambling. This byte is defined only for STS-1 number one of an STS-N/Nc signal.

E1: Orderwire - One byte is allocated to be used as a Section Orderwire. This is a local orderwire channel reserved for voice communications between STEs, hubs, and remote NEs. It is only defined for STS-1 number one.

F1: Section User Channel - One byte is set aside for the user's purposes. This byte is passed from Section to Section within a transmission system and is readable, writable, or both at each STE in that system. The use of this function is optional. The F1 Byte is defined only for STS 1 number one in an STS N/Nc signal.

D1-D3: Section Datacom Channel - Three bytes are allocated for a Section Data Communications Channel and are considered as a single 192 kbit/s message-based channel between STEs. The messaging protocols used are defined in ANSI T1.105.04. These bytes are defined only for STS-1 number one in an STS-N/Nc signal.

Line Overhead Definitions - LOH

The definitions for the Line Overhead Bytes are given below.

H1, H2: Pointer - Two bytes are allocated to a pointer that indicates the offset in bytes between the pointer and the first byte of the STS SPE. It allows alignment of the STS-1 TOHs in an STS-N/Nc signal and performance of frequency justification. In an STS-Nc signal the actual pointer is in the first set of H1 and H2 bytes. H1 and H2 bytes occupying STS-1 positions two through N carry a Concatenation Indicator, *where:* H1c = 93[H] and H2c = FF[H]. These bytes are required in all STS-1 portions of an STS-N/Nc signal.

H3: Pointer Action - The Pointer Action Byte is allocated for frequency justification purposes. Depending on the pointer value, this byte is used to adjust the fill of input buffers. In the event of a negative justification, it carries valid information. This byte is required in each STS-1 portion of an STS-N/Nc signal.

B2: Line BIP-8 - One byte is allocated in each STS-1 for a Line Error Monitoring function. This function is a bit-interleaved parity 8 code using even parity. The Line BIP-8 is calculated over all bits of the Line Overhead and STS SPE of the previous frame before scrambling. The computed BIP-8 is placed in the B2 Byte before scrambling. This byte is defined for all STS-1s of an STS-N/Nc signal. The N B2 Bytes in an STS-N/Nc are intended to form a single error monitoring function capable of measuring error rate up to 10^{-3} independent of the value of N. It can be thought of as either: (1) N BIP-8 functions each processing $^{1}/_{N}$ of the signal or (2) a single BIP-(N×8) processing all of the information. The errors accumulated are to be accumulated into a single error count.

K1, K2: APS Channel - Two bytes are allocated for Automatic Protection Switching (APS) signaling between LTEs. The signaling protocols used are defined in ANSI T1.105.01. These bytes are defined only for STS-1 number one in an STS-N/Nc signal.

D4-D12: Line Datacom Channel - Nine bytes are allocated for a Line Data Communications Channel and are considered as a single 576 kbit/s message-based channel between LTEs. The messaging protocols used are defined in ANSI T1.105.04. These bytes are defined only for STS-1 number one in an STS-N/Nc signal.

S1: Synchronization Messaging - One byte is allocated for transporting synchronization status messages. Currently, only Bits 5 through 8 are defined. Bits 1 through 4 are reserved for future use. This byte is defined only in STS-1 number one in an STS-N/Nc signal.

M0: STS-1 Line FEBE - In a STS-1 signal one byte is allocated for a Line Far End Block Error (FEBE) function. Currently only Bits 5 through 8 are used. These bits are used to convey the count of errors detected by the B2 Byte. This count has nine legal values, i.e., zero through eight. The remaining seven values are interpreted as zero errors. Bits 1 through 4 are reserved for future use.

M1: STS-N/Nc Line FEBE - In a signal at or above the STS-3/3c level, one byte is allocated for a Line Far End Block Error (FEBE) function. The M1 Byte is located in the third STS-1 in an STS-N/Nc signal. The entire byte is used to convey a count of errors detected by B2 Bytes. This count has (8 × N) + 1 legal values i.e., zero through (8 × N) errors. For rates below STS-48/48c, the remaining possible 255-(8 × N) values are interpreted as zero errors. At rates at and above STS-48/48c, if greater than 255 errors are detected the Line FEBE shall relay a value of 255 errors.

Z1: Growth - In a signal at or above the STS-3/3c level and less than the STS-192/192c rate, one byte is reserved in STS-1 numbers two through N of the STS-N/Nc signal for future growth. At rates greater than or equal to STS-192/192c, Z1 is only defined for STS-1 numbers two through 48.

Z2: Growth - In a SONET signal at or above the STS-3/3c level and at or less than STS-192/192c, one byte is reserved in all STS-1s except for STS-1 number three of the STS-N/Nc signal for future growth. At rates greater than or equal to STS-192/192c, Z2 is only defined for STS-1 numbers one, two, and four through 48.

E2: Orderwire - One byte is allocated to be used as a Line Orderwire. This is an express orderwire channel reserved for voice communications between LTEs. It is only defined for STS-1 number one.

Path Overhead Definitions - POH

Path Overhead is assigned to a payload by a source device (DS3 mapping circuit, DS1 to STS-1 mux, etc.) and remains with the payload until demultiplexed by the sink device. Intermediate LTEs may be required to monitor these bytes. POH functions are divided into four classifications:

Class A Payload Independent Functions - These functions have a standard format and coding and are required for all PTEs.

Class B Mapping Dependent Functions - These functions have a standard format and coding that are specific to the type of payload. They are needed for more than one type of payload but not necessarily all payloads. These functions are processed by the appropriate PTEs.

Class C Application Specific Functions - The format and coding for these functions may not be defined in the SONET Standards. These functions are processed by the appropriate PTEs.

Class D Undefined Overhead functions - These overhead bytes are reserved for future use.

The definitions for the Path Overhead Bytes are given below.

J1: Path Trace; Class A - One byte is used to repetitively transmit a 64-byte fixed length string so that a sink device can verify its continued connection to the intended source device. The content of the message is not constrained by the SONET Standards. However, it is suggested that a message consisting of eight-bit ASCII characters, padded with NULL Characters, and terminated with CR and LF (total length 64 bytes) would be appropriate. If no message is designated then 00[H] is to be transmitted.

B3: Path BIP-8; Class A - One byte is allocated for a Path Error Monitoring function. This function is a bit interleaved parity 8 code using even parity. The Path BIP-8 is calculated over all bits of the previous STS SPE before scrambling. The computed BIP-8 is placed in the B3 Byte before scrambling.

C2: Path Signal Label; Class A/B - One byte is allocated to identify the construction and content of the SPE and for a Path Payload Defect Indicator (PDI-P). The Signal Label portion is a class A function. PDI-P is class B.

G1: Path Status; Class A - One byte is allocated to convey back to the Source PTE the Sink PTE status and performance. Bits 1 through 4 are a Path FEBE. These bits are used to convey the count of errors detected by the B3 Byte. This count has nine legal values i.e., zero through eight. The remaining seven values are interpreted as zero errors. Bits 5, 6 and 7 are used for a Path Remote Defect Indication (RDI-P). Bit 8 is reserved for future use.

F2: Path User Channel; Class C - One byte is allocated for user communications purposes between PTEs.

H4: Multiframe Indicator; Class B - This byte provides a generalized multiframe indicator for payloads. Currently, it is only used with VT structured payloads.

Z3, Z4: Growth; Class D - Two bytes are reserved for future use.

Z5: Tandem Connection Maintenance / Path Data Channel; Class C - One byte is allocated to support Tandem Connection Maintenance (TCM) and a Path Data Channel. Bits 1 through four are reserved for TCM functions. Bits 5 through 8 form a 32 kbit/s data channel that uses the LAPD protocol. The Path Data channel is used in TCM applications and is also available for communications between PTEs. However, TCM messages have priority. Since TCM terminating entities are not required to perform store and forward or Layer 2 termination for non-TCM messages, some or all of the preempted PTE to PTE messages may be lost and require retransmission.

POINTERS

Pointers are defined in SONET at the STS-N and VT Levels. The STS-1 Payload Pointer provides a mechanism to allow the flexible and dynamic alignment of the STS-1 SPE within the SONET Transport Frame. Dynamic alignment means that the STS-1 SPE is allowed to float within the Transport frame. Thus the pointer is able to accommodate differences not only in the phases of the STS-1 SPE and the TOH, but in the frame rates as well. As is shown in Figure 11, the STS-1 SPE will usually start in one frame and end in the following frame.

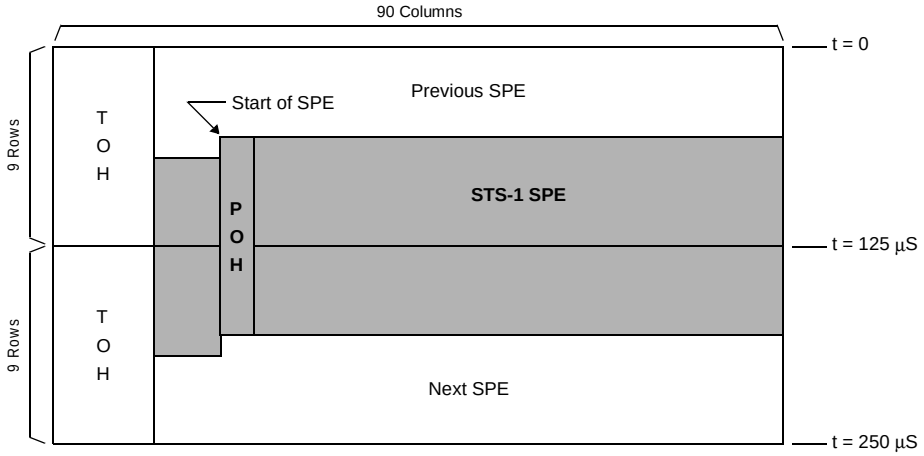


Figure 11. STS-1 Frame

The Pointer Bytes (H1 and H2) can be viewed as one 16-bit word as shown below. The last ten bits (7-16) of the Pointer Word carry the pointer value. This value is a binary number with a range of 0 to 782 that indicates the offset between the Pointer Bytes and the first byte of the SPE (J1). The TOH Bytes are not counted in the offset. For example, a value of "0" indicates that the SPE starts in the byte position immediately following the H3 Byte. The last column of this row is indicated by a pointer value of "86". A value of "87" specifies that the SPE starts at the byte position immediately following the K2 Byte. A value of "522" would position the start of the SPE in the byte position immediately following the C1/J0 Byte. The two S bits are not used in STS-1 Pointers and are set to "00".

H1 Byte								H2 Byte							
MSB							LSB	MSB							LSB
N	N	N	N	S	S	I	D	I	D	I	D	I	D	I	D
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Frequency Justification

If there is a frequency offset between the frame rate of the TOH and that of the STS-1 SPE, then the pointer value will be incremented or decremented, as needed, accompanied by a corresponding positive or negative stuff byte. Consecutive pointer operations must be separated by at least three frames in which the pointer value remains constant.

If the frame rate of the SPE is too slow with respect to the TOH, then the alignment of the envelope is periodically slipped back in time and the pointer is incremented by one. This is shown in Figure 12. The operation is indicated by inverting Bits 7, 9, 11, 13 and 15 (I Bits) of the Pointer Word. A positive stuff byte appears immediately after the H3 Byte in the frame containing the inverted I Bits. Subsequent pointers contain the new offset.

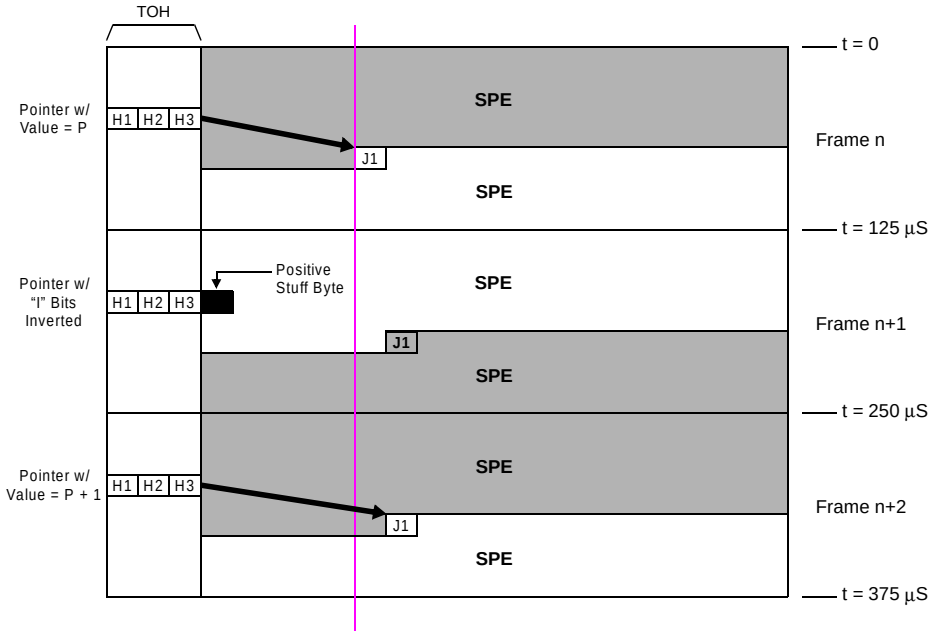


Figure 12. Positive Pointer Justifications

If the frame rate of the SPE is too fast with respect to the TOH, then the alignment of the envelope is periodically advanced in time and the pointer is decremented by one. This operation is indicated by inverting Bits 8, 10, 12, 14 and 16 (D Bits) of the Pointer Word. A negative stuff byte appears in the H3 Byte Position in the frame containing the inverted D Bits. Subsequent pointers contain the new offset. This is shown in Figure 13.

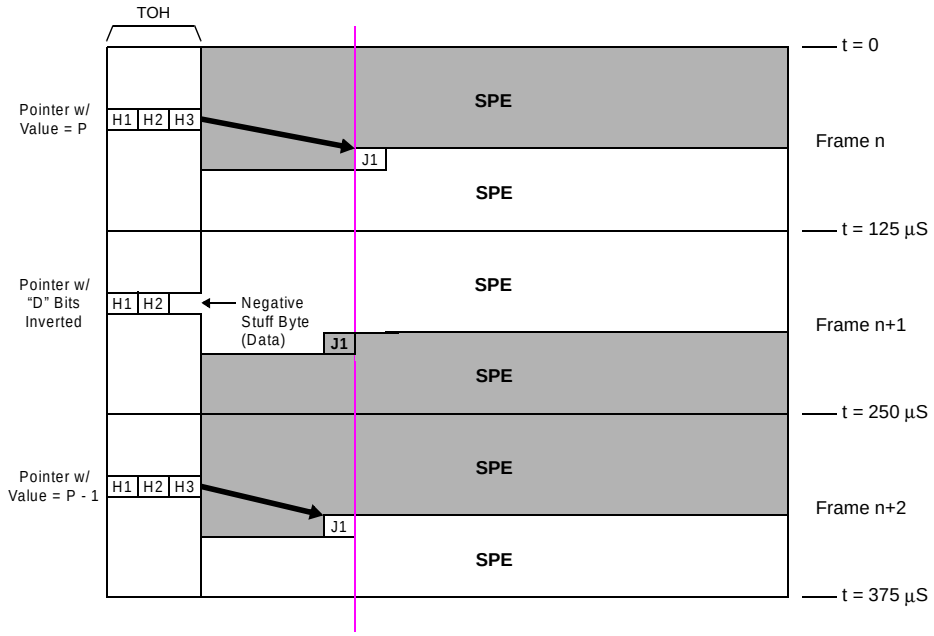


Figure 13. Negative Pointer Justifications

New Data Flag

Bits 1 through 4 (N Bits) of the Pointer Word carry a New Data Flag (NDF). This is a mechanism that allows an arbitrary change of the value of the pointer if that change is due to a change in payload. Normal operation is indicated by a "0110" code in the N Bits. NDF is indicated by inversion of the N Bits to "1001". The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

Concatenation

A concatenation indication contained in the Pointer Word is used to show that the STS-1 is part of an STS-Nc. The operations indicated in the pointer word of the first STS-1 within the STS-Nc apply to all STS-1s within the group. The pointer value must be multiplied by N to obtain the byte offset into the STS-Nc envelope capacity. Positive and negative justifications are performed as N byte multiples. In the remaining pointer words in the group the I and D Bits are set to all "1"s. The N Bits are set to "1001" and the S Bits are set to "00". The PHAST-1 does not support concatenation but does provide a status bit indicating that a concatenation indication has been received in the H1 and H2 Bytes.

BLOCK DIAGRAM

The Block Diagram for the PHAST-1 is shown in Figure 14.

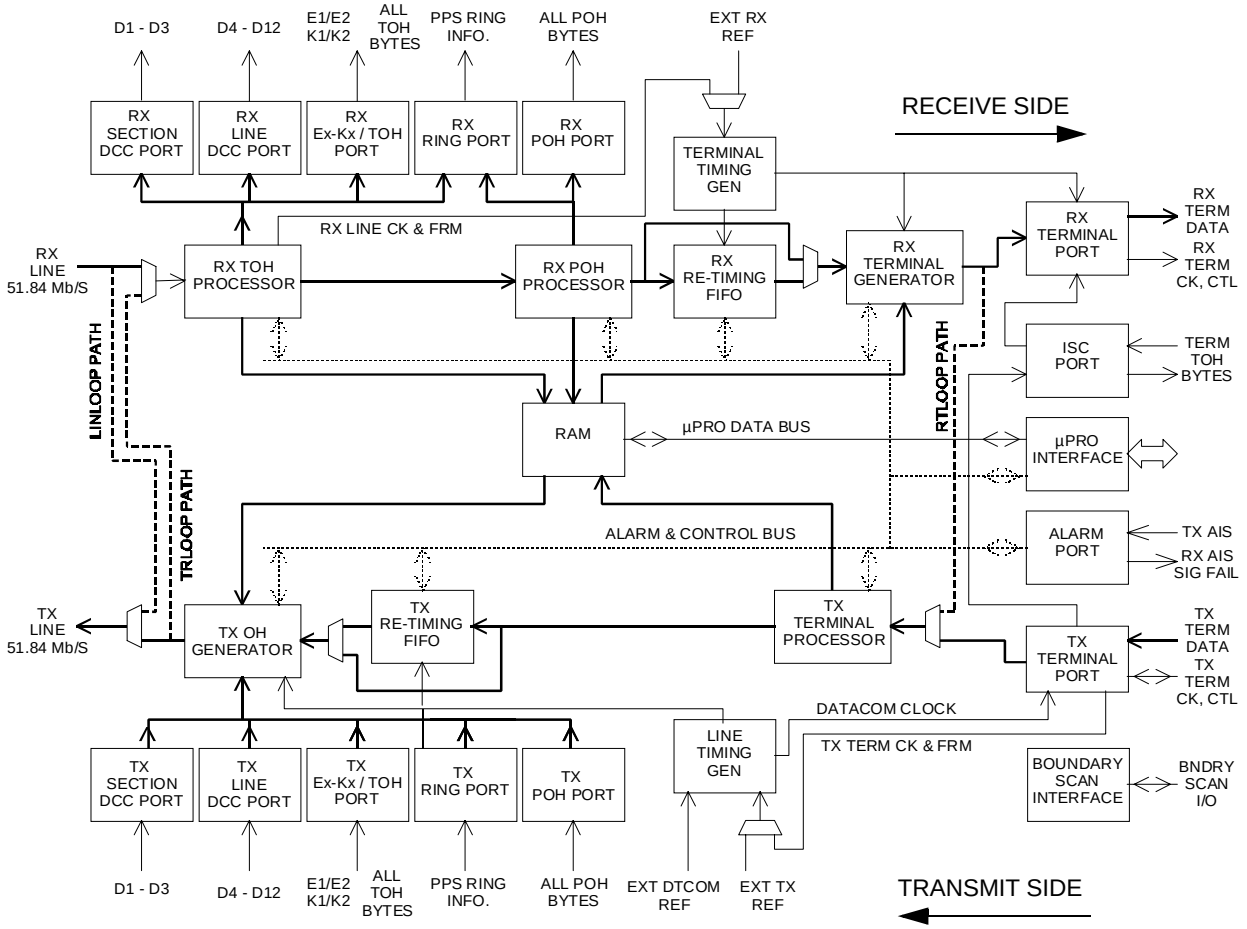


Figure 14. PHAST-1 TXC-06101 Block Diagram

RECEIVE SIDE

The Multiplexer at the Receive Line Input selects either the Line Side Input or the looped signal from the Transmit Line Output. The selected signal is applied to the Rx TOH Processor. The Rx TOH Processor Block is responsible for Framing, De-scrambling, Overhead Distribution and Overhead Processing. All Section and Line Overhead Bytes are stored in RAM and may be read through the µPro[1] Interface. The Section and Line DCC Bytes are output at the Rx Section and Line DCC Ports as serial Bit streams suitable for interfacing to HDLC Controllers. The E_X-K_X/TOH Port has two modes of operation. In the First Mode it outputs the E1, E2, K1 and K2 Bytes in a manner that allows the E1 and E2 Bytes to be directly interfaced to CODECS. The other mode of operation allows external access to all of the Received TOH Bytes. Overhead Processing consists of J0 Processing, Error Accumulation (B1, B2, FEBE-L), Debouncing of selected TOH Bytes, Pointer Tracking and Alarm Detection. Section and Line Level Alarms are reported to the µPro Interface. AIS-L and Signal Fail conditions are output at the Alarm Port.

1. Throughout this document "µPro" is used as a space-saving alias for "microprocessor".

The Rx POH Processor Distributes and Processes the POH Bytes. All bytes are stored in RAM and available at the Rx POH Port. Selected POH Bytes are debounced. B3 and FEBE-P error counts are accumulated. Path Level Alarms are reported to the µPro Interface. AIS-P conditions are output at the Alarm Port.

The Rx Ring Port is for use with a mated PHAST-1 in PPS Ring Operations. The information output consists of FEBE (Line and Path) values and Send RDI (Line and Path) indications.

The Terminal Timing Generator and Rx Re-timing FIFO are used to justify the STS-1 SPE to a Rx Reference Frequency. In certain modes of operation the Re-timing Function can be bypassed. The Reference Frequency may be derived from the Rx Line or from an External Reference Source. The Rx Re-timing FIFO Block performs Frequency Justification and Pointer Re-calculation.

The Rx Terminal Generator and Rx Terminal Port create and format the received Signal appearing at the Rx Terminal Port outputs. The Section and Line Overhead Bytes (not applicable in SPE-only Mode) appearing at the output may be taken from RAM, generated internally, or input at the ISC Port. The POH bytes are taken from RAM or internally generated. The Rx Terminal Generator generates the required bytes and performs Alarm Insertion.

TRANSMIT SIDE

The data to be transmitted enters the PHAST-1 at the Tx Terminal Port. The Tx Terminal Clock and Control Signals are generated and output by the PHAST-1 in Datacom Mode and are inputs for all other modes. The TOH bytes (not applicable in SPE-only Mode) are extracted and output at the ISC Port.

The Multiplexer at the input to the Tx Terminal Processor selects either the Tx Terminal Port Data or the looped signal from the Rx Terminal Generator. The Tx Terminal Processor performs Frame Delineation, Pointer Tracking, stores all TOH (if present) and POH Bytes in RAM, accumulates B1, B2 and B3 errors, and detects Terminal Side Alarms. The payload portion of the STS-1 SPE is forwarded to the Tx Re-Timing FIFO.

The Line Timing Generator and Tx Re-timing FIFO are used to justify the STS-1 SPE to a Tx Reference Frequency. In certain modes of operation the Re-timing Function can be bypassed. The Reference Frequency may be derived from the Tx Terminal or from an External Reference Source. The Tx Re-timing FIFO performs Frequency Justification and Pointer Recalculation.

The Tx OH Generator is responsible for Section, Line and Path Overhead Byte Assembly, TOH and POH Level Alarm Insertion, and scrambling. The POH bytes may be selected from RAM or input at the Tx POH Port. Alarms are generated as a result of Rx Side anomalies, Terminal Side conditions, Alarm Port Input, Tx Ring Port Input or upon command from the µPro Interface. The TOH Bytes are either internally generated, taken from RAM, or input externally. The external sources for the TOH Bytes are the Tx E_X-K_x/TOH Port, the Tx Line DCC Port, or the Tx Section DCC Port. Alarms are generated as a result of Rx Side anomalies, Terminal Side conditions, Alarm Port Input, Tx Ring Port Input or upon command from the µPro Interface. The Tx Line Output consists of either the Tx OH Generator Output or the looped Received Line Signal.

PIN DIAGRAMS

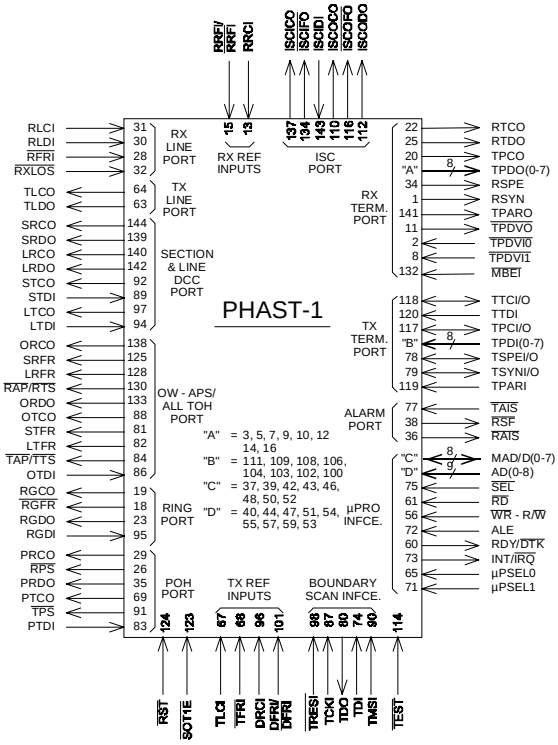


Figure 15. PHAST-1 TXC-06101 Functional Pin Diagram

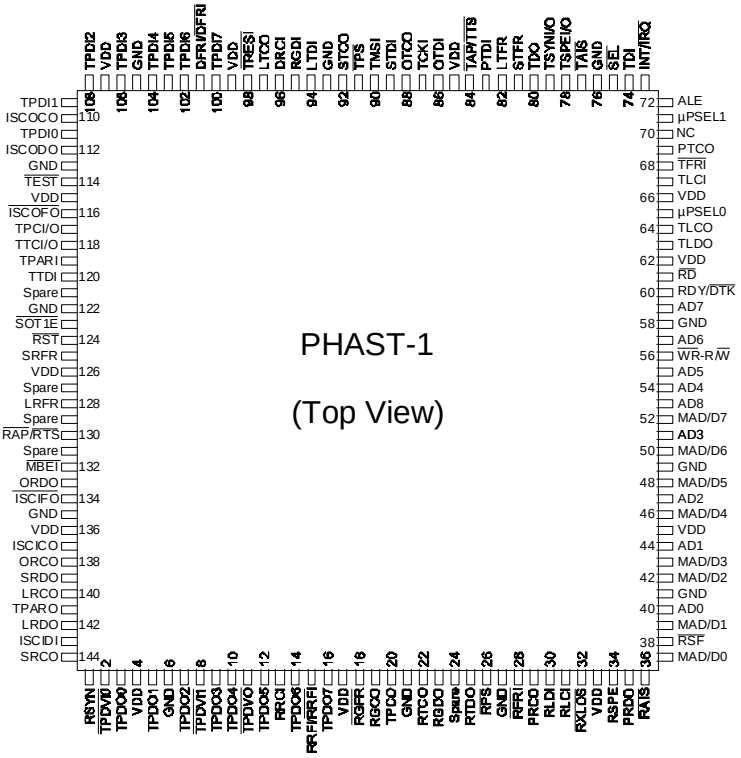


Figure 16. PHAST-1 TXC-06101 Actual Pin Diagram

PIN DESCRIPTIONS

Power Supply, Ground and Spare Pins

Pin Name	Pin No.*	I/O/P(T)	Type	Name/Function
VDD	4, 17, 33, 45, 62, 66, 85, 99, 107, 115, 126, 136	P		+3.3 V ± 5% Supply Voltage, V_{DD}
GND	6, 21, 27, 41, 49, 58, 76, 93, 105, 113, 122, 135	P		V_{SS} or Ground - 0 V reference
SPARE	24, 121, 127, 129, 131	_		**Spare Pins**: Do not connect to Power, Ground, any circuit conductor or any other pin. Connection of this pin may impair performance or cause damage.

*Note: I =Input; O = Output; P = Power; (T) = Tri-state

Reference Inputs

Pin Name	Pin No.	I/O/P(T)	Type**	Name/Function
RRCI	13	I	CMOSp	**Receive Reference Clock Input:** 51.84/19.44/6.48 Mbit/s clock optionally used for Receive Side re-timing. This input is enabled if control bit RCLK = "1" in CR10 (see Memory Map section).
RRFI/$\overline{\text{RRFI}}$	15	I	CMOSp	**Receive Reference Frame Input:** Optional pulse used to define the Receive Terminal start of frame. When RRCI is 51.84 Mbit/s, it is active Low. Otherwise it is active High.
TLCI	67	I	CMOS	**Transmit Line Clock Input:** 51.84 Mbit/s clock. Depending on the operating mode it may be used for Transmit Side re-timing.
$\overline{\text{TFRI}}$	68	I	CMOSp	**Transmit Frame Reference Input:** Optional active Low frame pulse. Depending on the operating modes it may be used to define the Transmit Line start of frame.
DRCI	96	I	CMOSp	**Datacom Reference Clock Input:** 51.84/19.44/6.48 Mbit/s clock used in Datacom Mode to generate TTCI/O or TPCI/O. This is a required input for Datacom Mode.
DFRI/$\overline{\text{DFRI}}$	101	I	CMOSp	**Datacom Reference Frame Input:** Optional 8 kbit/s pulse used in Datacom Mode to define the Transmit Terminal start of frame. When in serial Datacom mode this pin is active Low, otherwise it is active High. When H4INT = "1", then either the pulse repetition rate must be 2 kbit/s or the pin is not used.

**Note: See the Input, Output and I/O Parameters section for Type descriptions.

Receive Line Side Interface

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
$\overline{\text{RFRI}}$	28	I	CMOSp	**Receive Line Frame In:** Optional, active Low frame pulse that occurs during the C1 Byte, Bit 7 time. When used, it reduces the SEF/OOF exit time from two frames to one frame. This input is only enabled if STS1 = "0". It is clocked in on the Rising Edge of RLCI.
RLDI	30	I	CMOS	**Receive Line Data Input:** Incoming, serial STS-1 data which is clocked in on the Rising Edge of RLCI.
RLCI	31	I	CMOS	**Receive Line Clock Input:** Incoming 51.84 Mbit/s Clock.
$\overline{\text{RXLOS}}$	32	I	TTLp	**Receive Loss Of Signal:** Active Low, external, LOS indicator. This input is combined with the internal LOS detectors to produce the RLOS status indicator. The minimum Low time is 20 ns.

Transmit Line Side Interface

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
TLDO	63	O	CT8	**Transmit Line Data Output:** Outgoing, serial STS-1 Data which is clocked out on the Falling Edge of TLCO.
TLCO	64	O	CT8	**Transmit Line Clock Output:** Outgoing 51.84 Mbit/s Clock. When TCLK = "0", it is derived from TTCI/O, DRCI, or TLCI, depending on mode. When TCLK = "1", it is derived from TLCI.

Terminal Side Interface

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
RTCO	22	O	CT8	**Receive Terminal Clock Output:** Serial, 51.84 Mbit/s terminal clock. Depending on the operating modes, RTCO may be derived from either RLCI or RRCI.
RTDO	25	O	CT8	**Receive Terminal Data Output:** Serial, 51.84 Mbit/s data. Data is clocked out on the Falling Edges of RTCO.

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
TPCO	20	O	CT4	**Terminal Parallel Clock Output:** Parallel, 6.48 Mbit/s or 19.44 Mbit/s, Rx Terminal clock. Depending on the operating modes, TPCO at 6.48 Mbit/s may be derived from either RLCI or RRCI. TPCO at 19.44 Mbit/s must be derived from RRCI. When INVPCK = "1", TPCO is inverted. In SONET Modes and 19.44 Mbyte/s Datacom Mode, it is continuous. In 6.48 Mbyte/s Datacom Mode TPCO is: 1. continuous if DISPCKG = "1" 2. gapped during the TOH Byte times when DISPCKG = "0" and ENDCMPOH = "1" 3. gapped during TOH and POH Byte times if DISPCKG = "0" and ENDCMPOH = "0".
TPDO(0-7)	3 5 7 9 10 12 14 16	O(T)	CT4	**Terminal Parallel Data Output:** Parallel, 6.48 Mbyte/s or 19.44 Mbyte/s, Rx Terminal data. TPDO0 is the least significant bit of the SONET Byte. When INVPCK = "0", information is clocked out on the Falling Edges of TPCO. When INVPCK = "1" information is clocked out on the Rising Edges.
RSPE	34	O(T)	CT8	**Receive Terminal SPE Indication:** In SPE-only Mode this is the active Low gapping signal. In Both SONET and Datacom Modes it is Low during the TOH Byte times. In SONET Mode it is High during the SPE Byte times. In Datacom Modes this is: 1. High during the SPE Byte times if ENDCMPOH = "1" 2. Low during the POH Byte times and High during the Payload Byte times if ENDCMPOH = "0" RSPE is clocked out on the Falling Edges of RTCO. When INVPCK = "0", it is clocked out on the Falling Edges of TPCO. When INVPCK = "1" RSPE is clocked out on the Rising Edges of TPCO.
RSYN	1	O(T)	CT8	**Receive Terminal Sync Pulse:** In SONET and Datacom Modes this is High during the C1, J1, and, optionally, V1 Byte times. In SPE-only Mode this is High during the J1 Byte time and, optionally, during the V1 Byte time. RSYN is clocked out on the Falling Edges of RTCO. When INVPCK = "0", RSYN is clocked out on the Falling Edges of TPCO. When INVPCK = "1" it is clocked out on the Rising Edges of TPCO.

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
TPARO	141	O(T)	CT4	**Terminal Parity Output:** Odd parity over TPDO(0-7), RSPE and RSYN when C1J1EN = "1" or in Datacom mode. When C1J1EN = "0", it is generated over TPDO(0-7).
$\overline{\text{TPDVO}}$	11	O	CT4	**Terminal Parallel Data Valid Output:** Active Low Signal that indicates that TPDO(0-7), RSPE, RSYN and TPARO are driving the parallel bus. In 6.48 Mbyte/s applications it will always be Low. When the bus is operating at 19.44 Mbyte/s the settings of ENFSTUA, ENLSTUA, MBSEL0 and MBSEL1 will determine when this pin is active.
$\overline{\text{TPDVI0}}$	2	I	TTLp	**Terminal Parallel Data Valid Input x:** Active Low signals that are used for Bus Collision protection and alarms. They are connected to the $\overline{\text{TPDVO}}$ outputs of other devices. A priority scheme can be implemented by: 1. Providing no inputs to the first Device 2. Providing 1 input to the second Device 3. Providing 2 inputs to the third Device.
$\overline{\text{TPDVI1}}$	8	I	TTLp	
$\overline{\text{MBEI}}$	132	I	TTLp	**Multiplex Bus Enable Input:** Active Low signal that enables 19.44 Mbtye/s bus operation.
TTCI/O	118	I/O	CMOS/ CT8	**Transmit Terminal Clock Input/Output:** Serial, 51.84 Mbit/s terminal clock. In SONET and SPE-only Modes it is an Input. In Datacom Mode it is an Output derived from DRCI. Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin $\overline{\text{RST}}$ to ensure correct operation.
TTDI	120	I	CMOS	**Transmit Terminal Data Input:** Serial, 51.84 Mbit/s data. Data is clocked in on the Rising Edges of TTCI/O.
TPCI/O	117	I/O	TTL/ CT4	**Terminal Parallel Clock Input/Output:** Parallel, 6.48 or 19.44 Mbit/s, Tx Terminal clock. In SONET Modes it is an Input. In Datacom Modes it is an Output derived from DRCI and will be inverted if INVPCK = "1". In 19.44 Mbyte/s Datacom Mode it is continuous. In 6.48 Mbyte/s Datacom Mode it is: 1. continuous if DISPCKG = "1" 2. gapped during the TOH Byte times when DISPCKG = "0" and ENDCMPOH = "1" 3. gapped during the TOH and POH Byte times if DISPCKG = "0" and ENDCMPOH = "0". Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin $\overline{\text{RST}}$ to ensure correct operation.

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
TPDI(0-7)	111 109 108 106 104 103 102 100	I	TTL	**Terminal Parallel Data Input:** Parallel 6.48 Mbyte/s or 19.44 Mbyte/s data. In SONET Modes, data is clocked in on the Rising Edges of TPCI/O when INVPCK = "0", and on the Falling Edges when INVPCK = "1". In Datacom Modes data is sampled on: 1. the Falling Edge of TPCI/O when INVPCK = "0" 2. the Rising Edge of TPCI/O when INVPCK = "1"
TSPEI/O	78	I/O	CMOS/ CT8	**Transmit Terminal SPE Input/Output:** In SONET Modes this is an input which is High during the SPE Byte times. In SPE-only Mode this is an Input which is the active Low gapping signal. In Datacom Modes TSPEI/O is an output that is Low during the TOH Byte times and: 1. High during the SPE Byte times if ENDCMPOH = "1" 2. Low during the POH Byte times and High during the Payload Byte times if ENDCMPOH = "0" In Serial SONET and SPE-only Modes TSPEI/O is sampled on the Rising Edge of TTCI/O. In Parallel SONET mode it is sampled on the Rising Edge of TPCI/O if INVPCK = "0", or the Falling Edge if INVPCK = "1". In Serial Datacom Mode TSPEI/O is clocked out on the Falling Edge of TTCI/O. In Parallel Datacom Mode, TSPEI/O is clocked out on the Falling Edges of TPCI/O when INVPCK = "0" or the Rising Edges of TPCI/O when INVPCK = "1". Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin $\overline{\text{RST}}$ to ensure correct operation.

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
TSYNI/O	79	I/O	CMOS/ CT8	**Transmit Terminal Sync Pulse:** In SONET Mode this is an input which is High during the C1, J1, and, optionally, V1,1 Byte times. In Datacom Mode TSYNI/O is an output which is High during the C1, J1, and, optionally, V1,1 Byte times. In SPE-only Mode this is an input which is High during the J1 Byte time and, optionally V1 Byte time. In Serial SONET and SPE-only Modes TSYNI/O is sampled on the Rising Edge of TTCI/O. In Parallel SONET mode it is sampled on the Rising Edge of TPCI/O if INVPCK = "0", or the Falling Edge if INVPCK = "1". In Serial Datacom Mode TSYNI/O is clocked out on the Falling Edge of TTCI/O. In Parallel Datacom Mode, TSYNI/O is clocked out on the Falling Edges of TPCI/O when INVPCK = "0" or the Rising Edges of TPCI/O when INVPCK = "1". Since it is possible for the device to power up with this pin as an output, a reset should be performed via pin $\overline{\text{RST}}$ to ensure correct operation
TPARI	119	I	TTLp	**Terminal Parity Input:** Odd parity checked over TPDI(0-7), TSPEI/O and TSYNI/O when C1J1EN = "1". When C1J1EN = "0" or in Datacom Mode parity is checked only over TPDI(0-7). It is clocked in on the same edge as TPDI(0-7).

TOH Port

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
ORCO	138	O	CT4	**Receive TOH Port Clock Output:** Rx TOH Port output clock. When OA = "1" the rate is 576 kbit/s. When OA = "0" the rate is 1.728 Mbit/s.
ORDO	133	O	CT4	**Receive Order Wire and APS/TOH Byte Output:** Rx TOH Port data. The information is clocked out on the Rising Edges of ORCO.
SRFR	125	O	CT4	**Receive Section Order Wire Framing Pulse:** Receive frame pulse for Section Order Wire CODEC/filter. SRFR is clocked out on the Rising Edge of ORCO.
LRFR	128	O	CT4	**Receive Line Order Wire Framing Pulse:** Receive frame pulse for Line Order Wire CODEC/filter. LRFR is clocked out on the Rising Edge of ORCO.

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
$\overline{\text{RAP}}$/$\overline{\text{RTS}}$	130	O	CT4	**Receive APS/TOH Framing Pulse:** Active Low receive framing Pulse. When OA = "1" this signal occurs one clock cycle after the LSB of the K2 Byte in OTDO. When OA = "0" it occurs one clock cycle before the MSB of the A1 Byte. $\overline{\text{RAP}}$/$\overline{\text{RTS}}$ is clocked out on the Rising Edge of ORCO.
OTCO	88	O	CT4	**Transmit TOH Port Clock Output:** Output Tx TOH Port clock which is used for sourcing data into the PHAST-1. When OA = "1" the rate is 576 kbit/s. When OA = "0" the rate is 1.728 Mbit/s.
OTDI	86	I	TTLp	**Transmit Order Wire and APS/TOH Byte Input:** Tx TOH Port data. The information is clocked in on the Falling Edges of OTCO.
STFR	81	O	CT4	**Transmit Section Order Wire Framing Pulse:** Transmit frame pulse for Section Order Wire CODEC/filter. STFR is clocked out on the Rising Edge of OTCO.
LTFR	82	O	CT4	**Transmit Line Order Wire Framing Pulse:** Transmit frame pulse for Line Order Wire CODEC/filter. LTFR is clocked out on the Rising Edge of OTCO.
$\overline{\text{TAP}}$/$\overline{\text{TTS}}$	84	O	CT4	**Transmit APS/TOH Framing Pulse:** Active Low transmit framing Pulse. When OA = "1" this signal occurs one clock cycle before the MSB of the K1 Byte is expected on OTDI. When OA = "0" it occurs one clock cycle before the MSB of the A1 Byte is expected on OTDI. $\overline{\text{TAP}}$/$\overline{\text{TTS}}$ is clocked out on the Falling Edge of OTCO.

POH Port

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
PRCO	29	O	CT4	**Receive POH Clock Output:** ≈ 576 kbit/s clock, derived from RLCI, which is used for clocking out the POH Bytes from the PHAST-1. Clock frequency and duty cycle vary with Pointer Movements.
PRDO	35	O	CT4	**Receive POH Data Output:** POH Port Output data. The POH Bytes are clocked out on the Rising Edges of PRCO.
$\overline{\text{RPS}}$	26	O	CT4	**Receive POH Framing Pulse:** Active Low receive framing Pulse occurring one clock cycle before the MSB of the J1 Byte. $\overline{\text{RPS}}$ is clocked out on the Rising Edge of PRCO.

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
PTCO	69	O	CT4	**Transmit POH Clock Output:** ≈ 576 kbit/s clock, synchronous to TLCO, which is used for sourcing the POH Bytes into the PHAST-1. Clock frequency and duty cycle vary with Pointer Movements.
PTDI	83	I	TTLp	**Transmit POH Data Input:** POH Port input data. The POH Bytes are clocked in on the Rising Edges of PTCO.
$\overline{\text{TPS}}$	91	O	CT4	**Transmit POH Framing Pulse:** Active Low transmit framing Pulse occurring one and a half clock cycles before the MSB of the J1 Byte is sampled on PTDI. $\overline{\text{TPS}}$ is clocked out on the Falling Edge of PTCO.

ISC Port

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
ISCICO	137	O	CT4	**Input ISC Port Clock Output:** Gapped clock with an average frequency of 1.408 Mbit/s, derived from Rx Terminal Clock, which is used for clocking in the ISC Bytes to the PHAST-1.
ISCIDI	143	I	TTLp	**Input ISC Port Data Input:** ISC Port input data. The ISC Bytes are clocked in on the Rising Edges of ISCICO.
$\overline{\text{ISCIFO}}$	134	O	CT4	**Input ISC Port Framing Pulse Output:** Active Low framing Pulse occurring one and a half clock cycles before the MSB of the C1 Byte is sampled on ISCIDI. $\overline{\text{ISCIFO}}$ is clocked out on the Falling Edge of ISCICO.
ISCOCO	110	O	CT4	**Output ISC Port Clock Output:** Gapped clock with an average frequency of 1.408 Mbit/s, derived from the Tx Terminal Clock, which is used for clocking out the ISC Bytes from the PHAST-1.
ISCODO	112	O	CT4	**Output ISC Port Data Output:** ISC Port output data. The ISC Bytes are clocked out on the Rising Edges of ISCOCO.
$\overline{\text{ISCOFO}}$	116	O	CT4	**Output ISC Port Framing Pulse Output:** Active Low framing Pulse occurring one clock cycle before the MSB of the C1 Byte is output on ISCODO. $\overline{\text{ISCOFO}}$ is clocked out on the Rising Edge of ISCOCO.

Ring Port

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
RGCO	19	O	CT4	**Ring Port Clock Output:** Gapped, 648 kbit/s Clock derived from Rx Terminal Clock, which is used to output Ring Port Data and Frame.
$\overline{\text{RGFR}}$	18	O	CT4	**Ring Port Frame:** Active Low framing Pulse occurring immediately after the framing sequence is output on RGDO. $\overline{\text{RGFR}}$ is clocked out on the Rising Edge of RGCO.
RGDO	23	O	CT4	**Ring Port Data Output:** Ring Port Output Data. RGDO is clocked out on the Rising Edge of RGCO.
RGDI	95	I	TTLp	**Ring Port Data Input:** Ring Port Input Data. The Ring Port data input is self clocking.

Section and Line Data Communications Port

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
SRCO	144	O	CT4	**Receive Section DCC Clock Output:** 192 kbit/s Clock, derived from RLCI, which is used for clocking out Section DCC information.
SRDO	139	O	CT4	**Receive Section DCC Data Output:** Serial 192 kbit/s output for D1-D3 Bytes. Data is clocked out on the Falling Edges of SRCO.
LRCO	140	O	CT4	**Receive Line DCC Clock Output:** 576 kbit/s Clock, derived from RLCI, which is used for clocking out Line DCC information.
LRDO	142	O	CT4	**Receive Line DCC Data Output:** Serial 576 kbit/s output for D4-D12 Bytes. Data is clocked out on the Falling Edges of LRCO.
STCO	92	O	CT4	**Transmit Section DCC Clock Output:** 192 kbit/s Clock, derived from TLCO, which is used for sourcing the Section DCC information into the PHAST-1.
STDI	89	I	TTLp	**Transmit Section DCC Data Input:** Serial 192 kbit/s input for D1-D3 Bytes. Data is clocked in on the Rising Edges of STCO.
LTCO	97	O	CT4	**Transmit Line DCC Clock Output:** 576 kbit/s Clock, derived from TLCO, which is used for sourcing Line DCC information into the PHAST-1.
LTDI	94	I	TTLp	**Transmit Line DCC Data Input:** Serial 576 kbit/s input for D4-D12 Bytes. Data is clocked in on the Rising Edges of LTCO.

Microprocessor Interface

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
µPSEL0	65	I	TTLp	**µPro Interface Select:** Selects the µPro Interface type as shown below: µPSEL1 µPSEL0 Interface Type Low Low Motorola Low High Intel High Low Undefined - DO NOT USE High High Multiplexed Address/Data
µPSEL1	71			
MAD0	37	I/O	TTL/ CT8	**Multiplexed Address and Data Bus:** Multiplexed Interface. Pin 53 (AD8) is used for the most significant bit (MSB) of the address input.
D0				
MAD1	39			
D1				
MAD2	42			
D2				
MAD3	43			
D3				
MAD4	46			**Data Bus:** Intel and Motorola Interfaces
D4				
MAD5	48			
D5				
MAD6	50			
D6				
MAD7	52			
D7				
AD(0-7)	40 44 47 51 54 55 57 59	I	TTLp	**Address Bus:** Intel and Motorola Interfaces. Multiplexed Interface uses AD8 for MSB of address.
AD8	53	I	TTL	
$\overline{\text{SEL}}$	75	I	TTLp	**Device Select:** All Interfaces. Active Low signal that allows reading or writing to the PHAST-1.

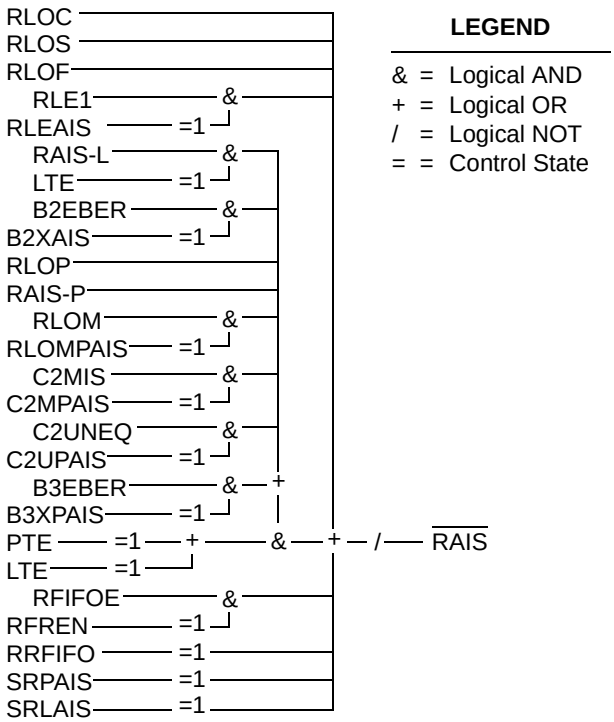
Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
$\overline{RD}$	61	I	TTLp	**Read Input:** Multiplexed and Intel Interfaces. A Low enables Read.
$\overline{WR}$	56	I	TTLp	**Write Input:** Multiplexed and Intel Interfaces A Low enables Write.
R/$\overline{W}$				**Read/Write Input:** Motorola Interface. A High enables Read and a Low enables Write.
RDY	60	O(T)	CT8	**Ready Output:** Multiplexed and Intel Interfaces. A High indicates the data transfer may take place. A Low indicates that wait states are required.
$\overline{DTK}$				**Data Acknowledge Output:** Motorola Interface. A Low during Read indicates that data is valid. A Low during Write indicates that data is accepted.
INT	73	O	CT4	**Interrupt Output:** Multiplexed and Intel Interfaces. A High indicates an Interrupt Request to the µPro.
$\overline{IRQ}$				**Interrupt Request Output:** Motorola Interface. A Low indicates an Interrupt Request to the µPro.
ALE	72	I	TTLp	**Address Latch Enable:** Multiplexed Interface. Falling Edge latches address information.

Boundary Scan Interface

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
$\overline{TRESI}$	98	I	TTLp	**Test Reset Input:** A Low will cause an asynchronous reset of the Boundary Scan Test Controller. For normal operation this pin should be tied Low. If a reset pulse is applied to this pin to initiate boundary scan it should be low for a minimum of 20 ns.
TCKI	87	I	TTLp	**Test Clock Input:** Boundary Scan Clock Input
TDO	80	O(T)	CT4	**Test Data Output:** Serial, Boundary Scan Data Output. Information is clocked out on the Falling Edge of TCKI.
TDI	74	I	TTLp	**Test Data Input:** Serial, Boundary Scan Data Input. Information is clocked in on the Rising Edge of TCKI.
TMSI	90	I	TTLp	**Test Mode Select Input:** This signal is used to control test operations. It is sampled on the Rising Edge of TCKI.

Alarm Port

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
$\overline{RSF}$	38	O	CT4	**Receive Signal Fail:** Active Low signal indicating that RLOC, RLOS or RLOF has been detected.

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
$\overline{\text{RAIS}}$	36	O	CT4	**Receive Alarm Indication Signal:** Active Low signal indicating that a received AIS condition has been detected. 
$\overline{\text{TAIS}}$	77	I	TTLp	**Transmit Alarm Indication Signal:** Active Low signal that causes AIS to be introduced into the Tx Line.

Miscellaneous Pins

Pin Name	Pin No.	I/O/P(T)	Type	Name/Function
$\overline{\text{RST}}$	124	I	TTL	**Reset:** Hardware Reset. $\overline{\text{RST}}$ is a negative pulse with a minimum pulse width of 20 ns. It must be used after power is applied and the clocks are stable.
$\overline{\text{TEST}}$	114	I	TTLp	**Test Enable:** An Active Low signal that invokes a TXC Test Mode. If both $\overline{\text{RST}}$ and $\overline{\text{TEST}}$ are Low all Output and Bidirectional (I/O) pins assume the tri-state condition.
$\overline{\text{SOT1E}}$	123	I	CMOSp	**Device Enable Pin:** Must be tied Low for Boundary Scan, RDY/$\overline{\text{DTK}}$ (pin 60) and normal features to function properly.
NC	70	O		**No Connect:** To be left open - Do not make any connection to this pin. This pin is used for manufacturing tests.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply Voltage	V_{DD}	-0.3	3.9	V	Note 1
Input Voltage	V_{IN}	-0.3	5.5	V	Note 1
Storage Temperature	T_S	-55	150	^oC	Note 1
Ambient operating temperature range	T_A	-40	85	^oC	0 ft/min linear airflow
Component temperature x time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance - junction to ambient	θ_{JA}			45	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.15	3.30	3.45	V
Supply Current	I_{DD}		75	100	mA
Power Dissipation	P_{DD}		250	345	mW

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.25	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current			10	µA	V_{DD} = 3.45V (Note 1)
Input Capacitance			5.0	pF	

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		5.25	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current			100	µA	V_{DD} = 3.45V (Notes 5, 7)
Input Capacitance			5.0	pF	

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 x V_{DD}		5.25	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.3 x V_{DD}	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current			10	µA	V_{DD} = 3.45V (Note 1)
Input Capacitance			5.0	pF	

INPUT PARAMETERS FOR CMOSp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 x V_{DD}		5.25	V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.3 x V_{DD}	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current			100	µA	V_{DD} = 3.45V (Notes 5, 7)
Input Capacitance			5.0	pF	

OUTPUT PARAMETERS FOR CT4

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 3.15, I_{OH} = -4.0 (Note 2)
V_{OL}		0.2	0.4	V	V_{DD} = 3.15, I_{OH} = 4.0 (Note 3)
I_{OL}			4.0	mA	Note 4
I_{OH}			-4.0	mA	Note 4
Tri-state leakage current		±10	-500	µA	V_{DD} = 3.45V, V_{IL} = 0 Note 8
Output Capacitance			5.0	pF	

OUTPUT PARAMETERS FOR CT8

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 3.15, I_{OH} = -8.0 (Note 2)
V_{OL}		0.2	0.4	V	V_{DD} = 3.15, I_{OH} = 8.0 (Note 3)
I_{OL}			8.0	mA	Note 4
I_{OH}			-8.0	mA	Note 4
Tri-state leakage current		±10	-500	µA	V_{DD} = 3.45V, V_{IL} = 0 Note 8
Output Capacitance			5.0	pF	

Notes:
1. V_{IH} = 5.25 V
2. V_{DD} = 3.15 V, I_{OH} = Max at rated current (4 or 8 mA)
3. V_{DD} = 3.15 V, I_{OL} = Max at rated current (4 or 8 mA)
4. V_{DD} = 3.15 V
5. V_{DD} = 3.45 V, Input = 0 V
6. Both CT outputs are CMOS and TTL compatible
7. Suffix p on Input Pin Type indicates that it is equipped with a pull-up feature
8. Leakage current is from V_{DD} and is most pronounced at -40 ^{o}C

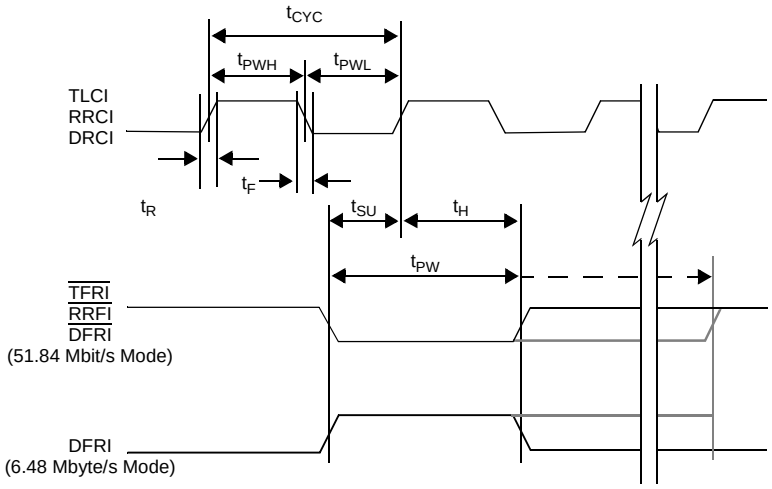
TIMING CHARACTERISTICS

This section presents the detailed timing characteristics for the PHAST-1. All output times are measured with a load capacitance of 25 pF, unless otherwise indicated. Timing parameters are measured at:

1. TTL Inputs - V_{IL} = 0 V, V_{IH} = 3.0 V, and Input Transitions = 1.4 V
2. TTL Outputs - 1.4 V
3. CMOS Inputs - V_{IL} = 0 V, V_{IH} = V_{DD}, and Input Transitions = (V_{DD} /2) V
4. CMOS Outputs - [(V_{OH} + V_{OL}) / 2] V

TIMING GENERATORS

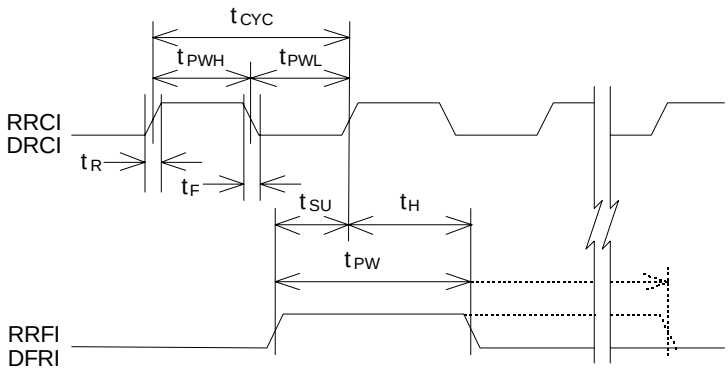
Figures 17, 18 and 19 show the timing requirements for both the Terminal Timing Generator and the Line Timing Generator. The Timing Generators synchronize to the first Rising Edge of the clock following the active Level of the Frame Reference.



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TLCI/RRCI/DRCI Period	t_{CYC}	19.25	19.29	19.33	ns	
TLCI/RRCI/DRCI Fall Time (90% - 10%)	t_F			4.0	ns	
$\overline{TFRI}$/$\overline{RRFI}$/$\overline{DFRI}$ Hold Time after ↑ TLCI/RRCI/DRCI	t_H	2.0			ns	
$\overline{TFRI}$/$\overline{RRFI}$/DFRI Pulse Width	t_{PW}	0.9	1.0	8.1	x t_{CYC}	
TLCI/RRCI/DRCI High Time	t_{PWH}	45	50	55	% t_{CYC}	
TLCI/RRCI/DRCI Low Time	t_{PWL}	45	50	55	% t_{CYC}	
TLCI/RRCI/DRCI Rise Time (10% - 90%)	t_R			4.0	ns	
$\overline{TFRI}$/$\overline{RRFI}$/$\overline{DFRI}$ Setup Time to ↑ TLCI/RRCI/DRCI	t_{SU}	4.0			ns	

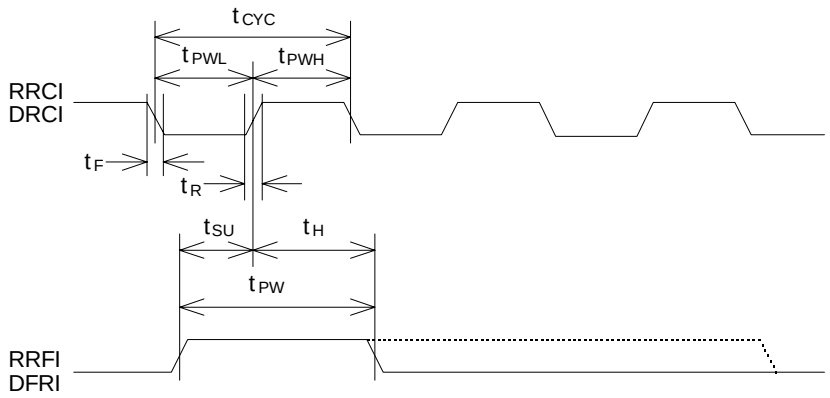
Figure 17. TTG and LTG 51.84 Mbit/s Input Timing

Figure 18. TTG and LTG 6.48 Mbyte/s Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
RRCI/DRCI Period	t_{CYC}	154.0	154.3	154.6	ns	
RRCI/DRCI Fall Time (90% - 10%)	t_F			6.0	ns	
RRFI/DFRI Hold Time after ↑ RRCI/DRCI	t_H	3.0			ns	
RRFI/DFRI Pulse Width	t_{PW}	0.9	1.0	8.1	x t_{CYC}	
RRCI/DRCI High Time	t_{PWH}	45	50	55	% t_{CYC}	
RRCI/DRCI Low Time	t_{PWL}	45	50	55	% t_{CYC}	
RRCI/DRCI Rise Time (10% - 90%)	t_R			6.0	ns	
RRFI/DFRI Setup Time to ↑ RRCI/DRCI	t_{SU}	7.0			ns	

Figure 19. TTG and LTG 19.44 Mbyte/s Input Timing



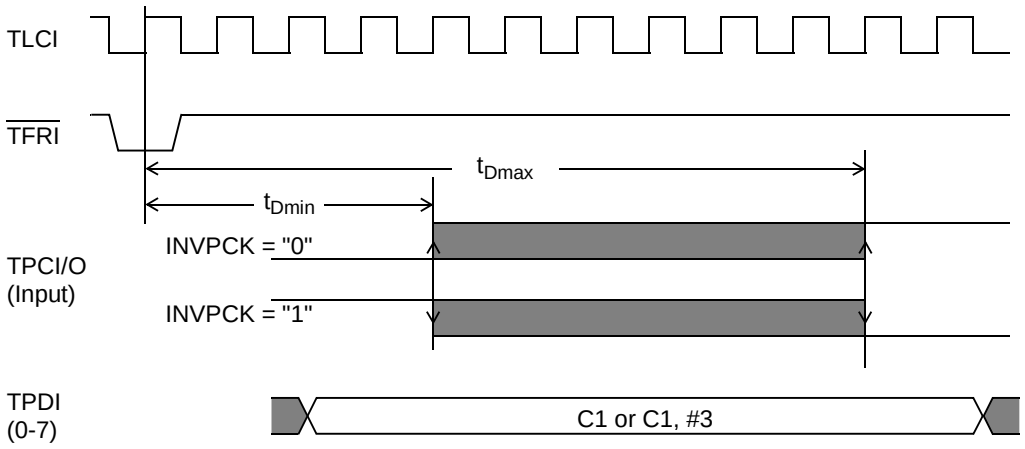
Parameter	Symbol	Min	Typ	Max	Unit	Notes
RRCI/DRCI Period	t_{CYC}	50.0	51.44		ns	
RRCI/DRCI Fall Time (90% - 10%)	t_F			6.0	ns	
RRFI/DFRI Hold Time after ↑ RRCI/DRCI	t_H	3.0			ns	
RRFI/DFRI Pulse Width	t_{PW}	0.9	1.0	3.1	x t_{CYC}	
RRCI/DRCI High Time	t_{PWH}	45	50	55	% t_{CYC}	
RRCI/DRCI Low Time	t_{PWL}	45	50	55	% t_{CYC}	
RRCI/DRCI Rise Time (10% - 90%)	t_R			6.0	ns	
RRFI/DFRI Setup Time to ↑ RRCI/DRCI	t_{SU}	7.0			ns	

TERMINAL TIMING IN PARALLEL MODES

When the PHAST-1 is operating in modes where TCLK is set to "0" and when the Tx terminal port is in a configuration which does not have a 51.84 MHz clock, then TLCI and $\overline{\text{TFRI}}$ must be supplied as follows:

1. TLCI and TPCI/O derived from the same source
2. the phase relationship shown in Figure 20 must be maintained.

Please refer to the Line Timing Generator subsection at the beginning of the Operation section.



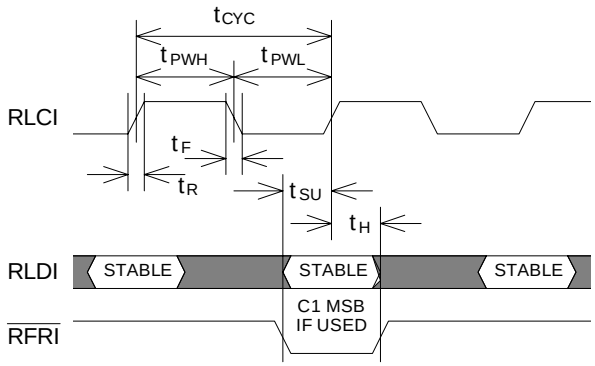
Parameter	Symbol	Unit	Notes
Minimum delay from ↑ TLCI that clocks in $\overline{\text{TFRI}}$ to the active edge of TPCI/O that clocks in the C1 Byte	t_{Dmin}	4 TLCI Clock Periods	1, 2, 3
Maximum delay from ↑ TLCI that clocks in $\overline{\text{TFRI}}$ to the active edge of TPCI/O that clocks in the C1 Byte	t_{Dmax}	10 TLCI Clock Periods	

Notes:
1. If TPCI/0 is 6.48 Mbit/s then TPDI(0-7) Data must be the C1 Byte.
2. If TPCI/0 is 19.44 Mbit/s then TPDI(0-7) Data must be the third C1 Byte.
3. Cross-hatched periods in waveform diagrams represent "Don't Care" inputs or indeterminate outputs.

Figure 20. Frame Phase Margin - Tx Re-Timing Disabled

LINE SIDE TIMING

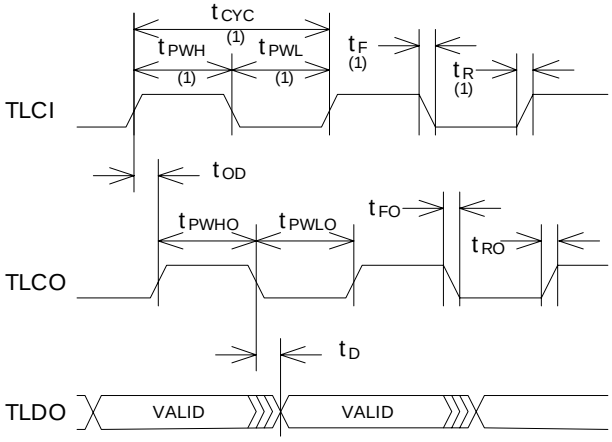
Figures 21 and 22 detail the timing for the Receive and Transmit Line Inputs and Outputs, respectively.



Parameter	Symbol	Min	Typ	Max	Unit	Notes
RLCI Clock Period	t_{CYC}	19.25	19.29	19.33	ns	
RLCI Fall Time (90% - 10%)	t_F			4.0	ns	
RLDI, $\overline{RFRI}$ Hold Time after ↑ RLCI	t_H	2.0			ns	
RLCI High Time	t_{PWH}	45	50	55	% t_{CYC}	
RLCI Low Time	t_{PWL}	45	50	55	% t_{CYC}	
RLCI Rise Time (10% - 90%)	t_R			4.0	ns	
RLDI, $\overline{RFRI}$ Setup Time to ↑ RLCI	t_{SU}	4.0			ns	

Figure 21. Receive Line Input Timing

Figure 22. Transmit Line Output Timing

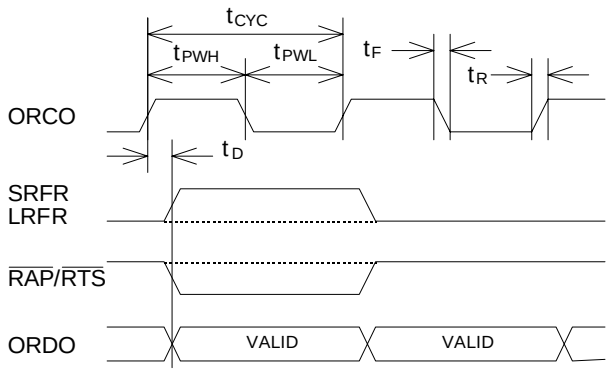


Parameter	Symbol	Min	Typ	Max	Unit	Notes
TLDO Delay after ↓ TLCO	t_D	-1.0	0.0	3.0	ns	
TLCO Output Fall Time (90% - 10%)	t_{FO}			1.7	ns	2
↑ TLCO Delay after ↑ TLCI	t_{OD}	6.0	15	24	ns	
TLCO High Time	t_{PWHO}	40	50	60	% t_{CYC}	
TLCO Low Time	t_{PWLO}	40	50	60	% t_{CYC}	
TLCO Output Rise Time (10% - 90%)	t_{RO}			1.5	ns	2

Notes:
1. See LTG Timing Characteristics (Figure 17).
2. With 25 pF load

ORDER WIRE-APS / TOH PORT TIMING

The output timing characteristics of the Order Wire-APS (OW/APS) / Port are shown in Figures 23 and 24.

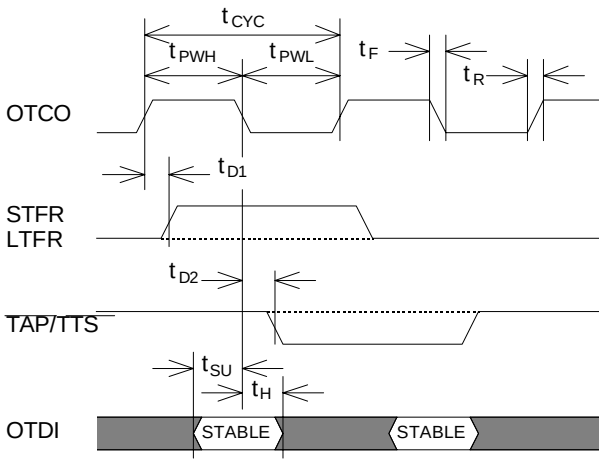


Parameter	Symbol	Min	Typ	Max	Unit	Notes
ORCO Clock Period - OW/APS Mode	t_{CYC}	1732	1736	1740	ns	
ORCO Clock Period - All TOH Mode		576.0	578.7	581.4		
SRFR, LRFR, $\overline{RAP}$/$\overline{RTS}$ or ORDO Delay after ↑ ORCO	t_D	-5.0		5.0	ns	
ORCO Fall Time (90% - 10%)	t_F			2.5	ns	1
ORCO High Time	t_{PWH}	40	50	60	% t_{CYC}	
ORCO Low Time	t_{PWL}	40	50	60	% t_{CYC}	
ORCO Rise Time (10% - 90%)	t_R			2.0	ns	1

Note 1: With 25 pF Load

Figure 23. Rx OW-APS / TOH Port Output Timing

Figure 24. Tx OW-APS / TOH Port Input Timing



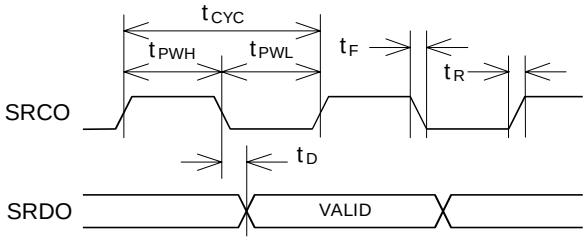
Parameter	Symbol	Min	Typ	Max	Unit	Notes
OTCO Clock Period - OW/APS Mode	t_{CYC}	1732	1736	1740	ns	
OTCO Clock Period - All TOH Mode		576.0	578.7	581.4		
STFR, LTFR Delay after ↑ OTCO	t_{D1}	-5.0		5.0	ns	
$\overline{TAP}/\overline{TTS}$ Delay after ↓ OTCO	t_{D2}	-5.0		5.0	ns	
OTCO Fall Time (90% - 10%)	t_F			2.5	ns	1
OTDI Hold Time after ↓ OTCO	t_H	0.0			ns	
OTCO High Time	t_{PWH}	40	50	60	% t_{CYC}	
OTCO Low Time	t_{PWL}	40	50	60	% t_{CYC}	
OTCO Rise Time (10% - 90%)	t_R			2.0	ns	1
OTDI Setup Time to ↓ OTCO	t_{SU}	10			ns	

Note 1: With 25 pF Load

SECTION AND LINE DCC PORT TIMING

The output timing for the Section and Line DCC Ports are shown in Figures 25 and 26. Figures 27 and 28 depict the input timing.

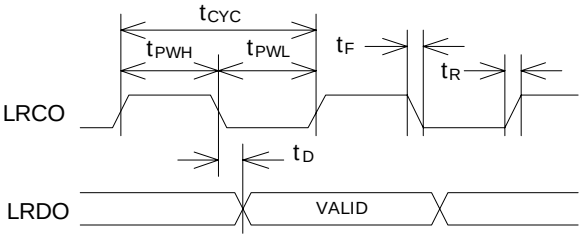
Figure 25. Rx Section DCC Port Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
SRCO Clock Period	t_{CYC}	5.20	5.21	5.22	µs	
SRDO Delay after ↓ SRCO	t_D	-5.0	0.0	5.0	ns	
SRCO Fall Time (90% - 10%)	t_F			2.5	ns	1
SRCO High Time	t_{PWH}	40	50	60	% t_{CYC}	
SRCO Low Time	t_{PWL}	40	50	60	% t_{CYC}	
SRCO Rise Time (10% - 90%)	t_R			2.0	ns	1

Note 1: With 25 pF Load

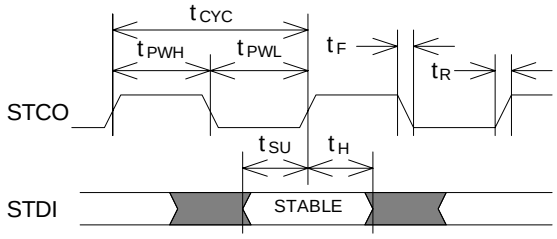
Figure 26. Rx Line DCC Port Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
LRCO Clock Period	t_{CYC}	1732	1736	1740	ns	
LRDO Delay after ↓ LRCO	t_D	-5.0	0.0	5.0	ns	
LRCO Fall Time (90% - 10%)	t_F			2.5	ns	1
LRCO High Time	t_{PWH}	40	50	60	% t_{CYC}	
LRCO Low Time	t_{PWL}	40	50	60	% t_{CYC}	
LRCO Rise Time (10% - 90%)	t_R			2.0	ns	1

Note 1: With 25 pF Load

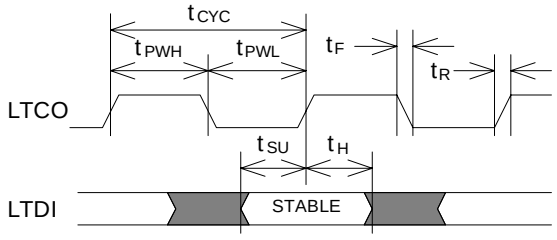
Figure 27. Tx Section DCC Port Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
STCO Clock Period	t_{CYC}	5.20	5.21	5.22	µs	
STCO Fall Time (90% - 10%)	t_F			2.5	ns	1
STDI Hold Time after ↑ STCO	t_H	0.0			ns	
STCO High Time	t_{PWH}	40	50	60	% t_{CYC}	
STCO Low Time	t_{PWL}	40	50	60	% t_{CYC}	
STCO Rise Time (10% - 90%)	t_R			2.0	ns	1
STDI Setup Time to ↑ STCO	t_{SU}	7.0			ns	

Note 1: With 25 pF Load

Figure 28. Tx Line DCC Port Input Timing

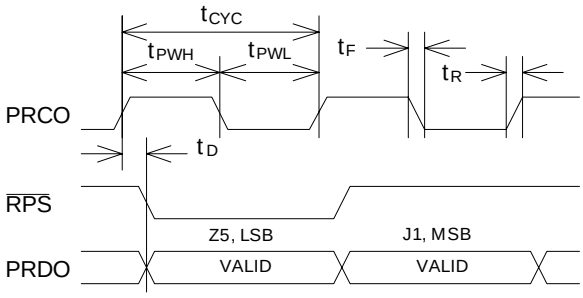


Parameter	Symbol	Min	Typ	Max	Unit	Notes
LTCO Clock Period	t_{CYC}	1732	1736	1740	ns	
LTCO Fall Time (90% - 10%)	t_F			2.5	ns	1
LTDI Hold Time after ↑ LTCO	t_H	0.0			ns	
LTCO High Time	t_{PWH}	40	50	60	% t_{CYC}	
LTCO Low Time	t_{PWL}	40	50	60	% t_{CYC}	
LTCO Rise Time (10% - 90%)	t_R			2.0	ns	1
LTDI Setup Time to ↑ LTCO	t_{SU}	7.0			ns	

Note 1: With 25 pF Load

POH PORT TIMING

The output timing characteristics of the POH Port are shown in Figure 29. Figure 30 depicts the input timing.

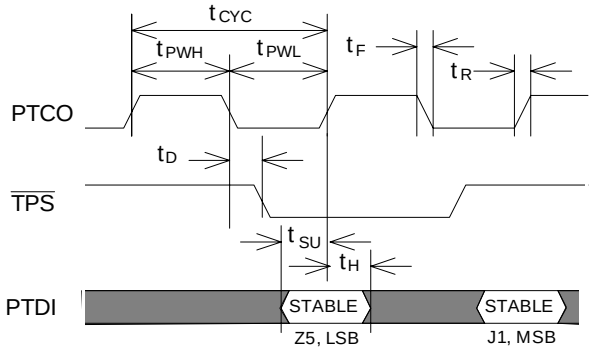


Parameter	Symbol	Min	Typ	Max	Unit	Notes
PRCO Clock Period	t_{CYC}		1697		ns	
$\overline{RPS}$ or PRDO Delay after ↑ PRCO	t_D	-5.0	0	5.0	ns	
PRCO Fall Time (90% - 10%)	t_F			2.5	ns	1
PRCO High Time	t_{PWH}	761	926		ns	
PRCO Low Time	t_{PWL}	761	771		ns	
PRCO Rise Time (10% - 90%)	t_R			2.0	ns	1

Note 1: With 25 pF Load

Figure 29. Rx POH Port Output Timing

Figure 30. Tx POH Port Input Timing

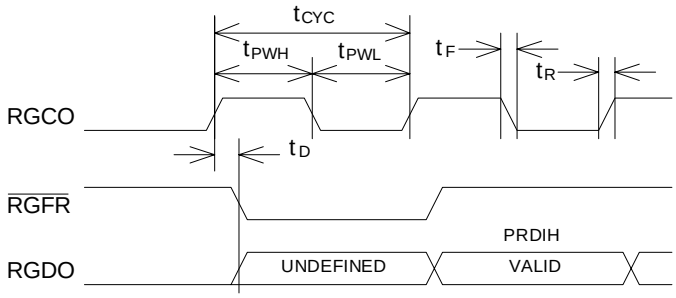


Parameter	Symbol	Min	Typ	Max	Unit	Notes
PTCO Clock Period	t_{CYC}		1697		ns	
$\overline{TPS}$ Delay after ↓ PTCO	t_D	-5.0		5.0	ns	
PTCO Fall Time (90% - 10%)	t_F			2.5	ns	1
PTDI Hold Time after ↑ PTCO	t_H	0.0			ns	
PTCO High Time	t_{PWH}	761	926		ns	
PTCO Low Time	t_{PWL}	761	771		ns	
PTCO Rise Time (10% - 90%)	t_R			2.0	ns	1
PTDI Setup Time to ↑ PTCO	t_{SU}	7.0			ns	

Note 1: With 25 pF Load

RING PORT TIMING

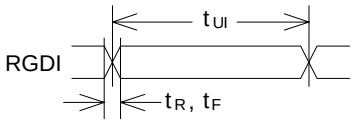
The output timing characteristics of the Ring Port are shown in Figure 31. Figure 32 depicts the input timing.



Parameter	Symbol	Min	Typ	Max	Unit	Notes
RGCO Clock Period	t_{CYC}	1536	1543	1550	ns	1
$\overline{\text{RGFR}}$ or RGDO Delay after ↑ RGCO	t_D	-5.0		5.0	ns	
RGCO Fall Time (90% - 10%)	t_F			2.5	ns	2
RGCO High Time	t_{PWH}	750	771		ns	1
RGCO Low Time	t_{PWL}	750	771		ns	1
RGCO Rise Time (10% - 90%)	t_R			2.0	ns	2

Notes:
1. Clock is gapped and remains Low during the first bit time of each Row and for the entire first Row of the Frame.
2. With 25 pF Load

Figure 31. Rx Ring Port Output Timing



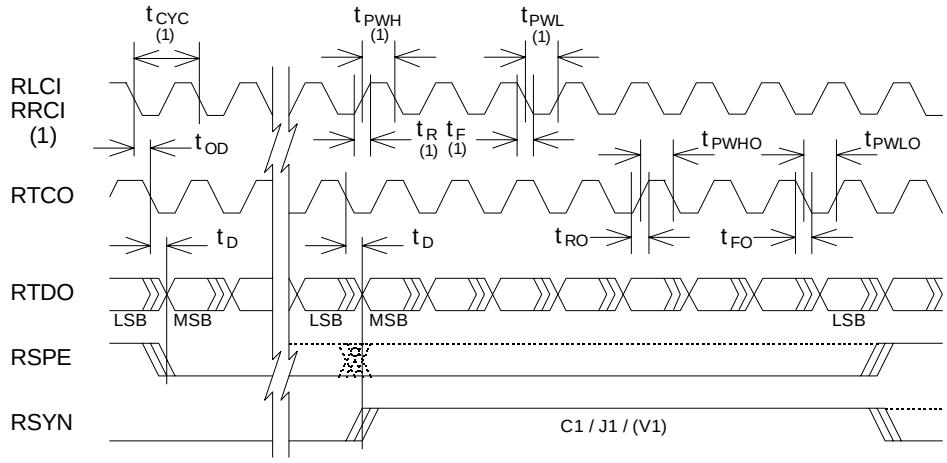
Parameter	Symbol	Min	Typ	Max	Unit	Notes
RGDI Fall Time (90% - 10%)	t_F			6.0	ns	
RGDI Rise Time (10% - 90%)	t_R			6.0	ns	
RGDI Bit Time	t_{UI}	1506	1543	1580	ns	

Figure 32. Tx Ring Port Input Timing

TERMINAL SIDE TIMING

The Tx and Rx Terminal Port Timing is shown in Figures 33-42.

Figures 33 through 36 show the output timing for the Rx Terminal Port. Figure 36 depicts the outputs when the PHAST-1 is configured for the first third of the Bus.

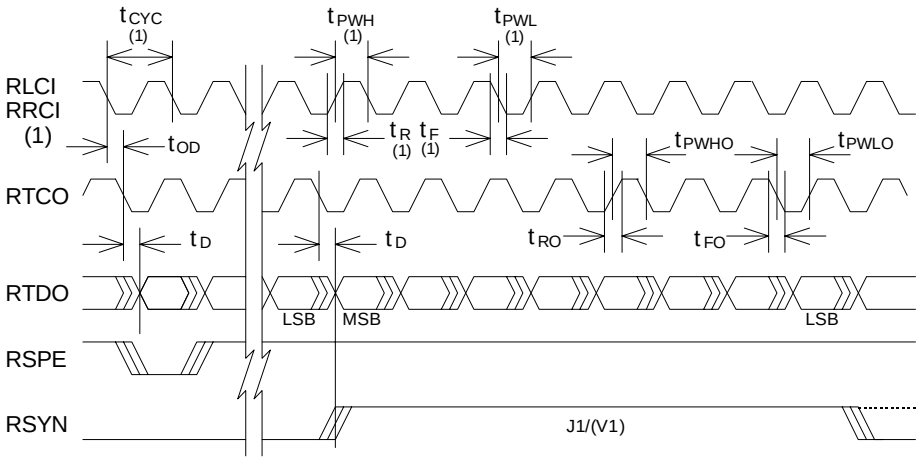


Parameter	Symbol	Min	Typ	Max	Unit	Notes
RTDO, RSPE or RSYN Delay after ↓ RTCO	t_D	-1.0	0.0	3.5	ns	
RTCO Output Fall Time (90% - 10%)	t_{FO}			1.7	ns	2
↓ RTCO Output Delay after ↓ RLCI/RRCI	t_{OD}	6.0	15	24	ns	
RTCO Output Rise Time (10% - 90%)	t_{RO}			1.5	ns	2
RTCO High Time	t_{PWHO}	40	50	60	% t_{CYC}	
RTCO Low Time	t_{PWLO}	40	50	60	% t_{CYC}	

Notes:
1. See TTG or Rx Line Timing Characteristics (Figures 17 or 21).
2. With 25 pF Load

Figure 33. SONET and Datacom Serial Output Timing

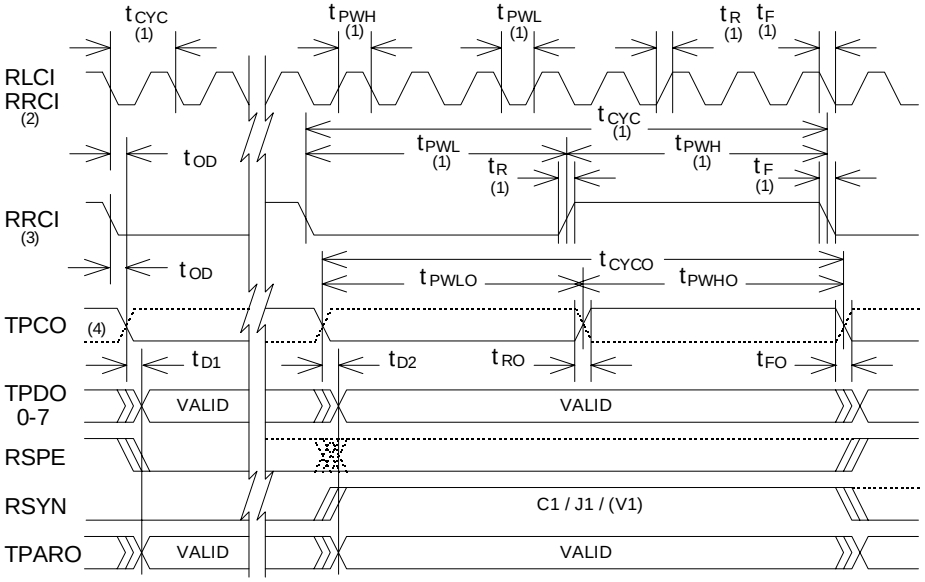
Figure 34. SPE-Only Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
RTDO, RSPE or RSYN Delay after ↓ RTCO	t_D	-1.0	0	3.5	ns	
RTCO Output Fall Time (90% - 10%)	t_{FO}			1.7	ns	2
↓ RTCO Output Delay after ↓ RLCI/RRCI	t_{OD}	6.0	15	24	ns	
RTCO Output Rise Time (10% - 90%)	t_{RO}			1.5	ns	2
RTCO High Time	t_{PWHO}	40	50	60	% t_{CYC}	
RTCO Low Time	t_{PWLO}	40	50	60	% t_{CYC}	

Notes:
1. See TTG or Rx Line Timing Characteristics (Figures 17 or 21).
2. With 25 pF Load

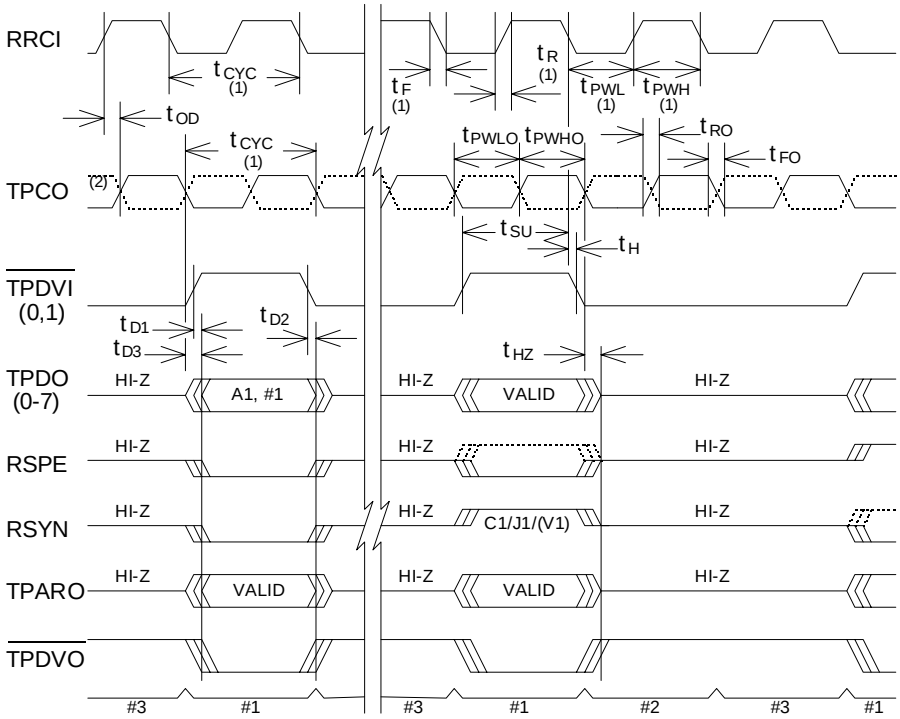
Figure 35. 6.48 Mbyte/s Parallel Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TPCO Clock Period (from RLCI/RRCI)	t_{CYCO}		8		x t_{CYC}	2
TPCO Clock Period (from RRCI)			1		x t_{CYC}	3
RSPE, RSYN or TPARO Delay after ↓ TPCO	t_{D1}	-5.0	0.0	5.0	ns	6
TPDO(0-7) Delay after ↓ TPCO	t_{D2}	-5.0	0.0	5.0	ns	6
TPCO Output Fall Time (90% - 10%)	t_{FO}			2.5	ns	7
↓ TPCO Output Delay after ↓ RLCI	t_{OD}	6.0	15	24	ns	6
↓ TPCO Output Delay after ↓ RRCI		6.0	15	24		2,6
↓ TPCO Output Delay after ↓ RRCI		6.0	15	24		3,6
TPCO Output Rise Time (10% - 90%)	t_{RO}			2.0	ns	7
TPCO High Time	t_{PWHO}	40	50	60	% t_{CYCO}	5
TPCO Low Time	t_{PWLO}	40	50	60	% t_{CYCO}	5

Notes:
1. See TTG or Rx Line Characteristics (Figures 17, 18 or 21).
2. RRCI when RETSEL = "1"
3. RRCI when RETSEL = "0"
4. TPCO inverted (dotted line) when INVPCK = "1"
5. In Datacom Mode TPCO may be gapped.
6. ↑ TPCO when INVPCK = "1"
7. With 25 pF Load

Figure 36. 19.44 Mbyte/s Parallel Output Timing



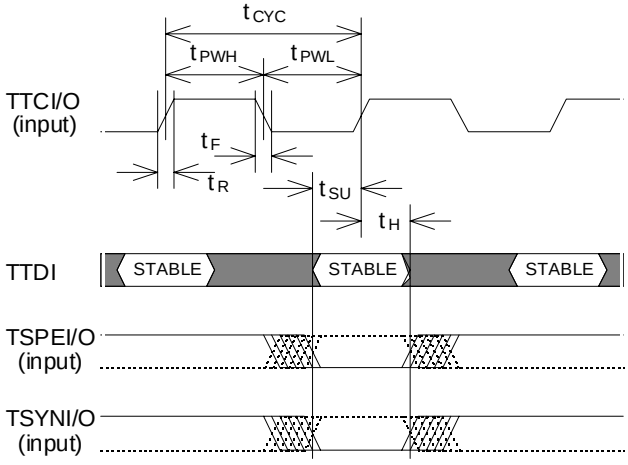
Parameter	Symbol	Min	Typ	Max	Unit	Notes
TPDO(0-7), RSPE, RSYN, TPARO (active) Delay after ↑ TPDVI(0,1)	t_{D1}	4.0	10	15	ns	
TPDO(0-7), RSPE, RSYN, TPARO (HI-Z) Delay after ↓ TPDVI(0,1)	t_{D2}	1.0	3.0	10	ns	
TPDO(0-7), RSPE, RSYN, TPARO or TPDVO Delay after ↓ TPCO	t_{D3}	-2.0		5.0	ns	3
TPCO Output Fall Time (90% - 10%)	t_{FO}			2.5	ns	4
TPDVI(0,1) Hold Time after ↓ RRCI for RBUSCOL declaration	t_{H}	6.0			ns	
TPDO, RSPE, RSYN, TPARO (HI-Z) Delay After ↓ TPCO	t_{HZ}	-2.0	0.0	5.0	ns	3
↑ TPCO Output Delay After ↑ RRCI	t_{OD}	6.0	15	24	ns	5
TPCO Output Rise Time (10% - 90%)	t_{RO}			2.0	ns	4
TPDVI(0,1) Setup Time to ↓ RRCI for RBUSCOL declaration	t_{SU}	10			ns	
TPCO High Time	t_{PWHO}	40	50	60	% t_{CYC}	
TPCO Low Time	t_{PWLO}	40	50	60	% t_{CYC}	

See Notes on next page

Notes:
1. See TTG Characteristics (Figure 19).
2. TPCO inverted (dotted line) when INVPCK = "1"
3. ↑ TPCO when INVPCK = "1"
4. With 25 pF Load
5. Delay is from ↑ RRCI to ↓ TPCO when INVPCK = "1"

Tx Terminal Port Timing

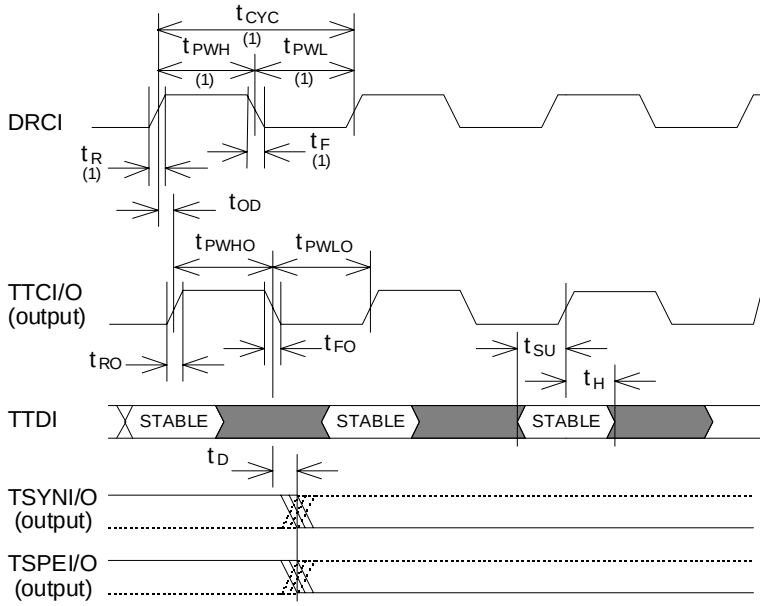
Figure 37 through 42 show the input timing for the Tx Terminal Port. Figure 42 depicts the inputs when the PHAST-1 is configured for the first third of the Bus.



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TTCI/O Clock Period	t_{CYC}	19.25	19.29	19.33	ns	
TTCI/O Fall Time (90% - 10%)	t_F			4.0	ns	
TTDI, TSPEI/O, or TSYNI/O Hold Time after ↑ TTCI/O	t_H	2.0			ns	
TTCI/O High Time	t_{PWH}	45	50	55	% t_{CYC}	
TTCI/O Low Time	t_{PWL}	45	50	55	% t_{CYC}	
TTCI/O Rise Time (10% - 90%)	t_R			4.0	ns	
TTDI, TSPEI/O, or TSYNI/O Setup Time to ↑ TTCI/O	t_{SU}	4.0			ns	

Figure 37. Serial SONET and SPE-Only Input Timing

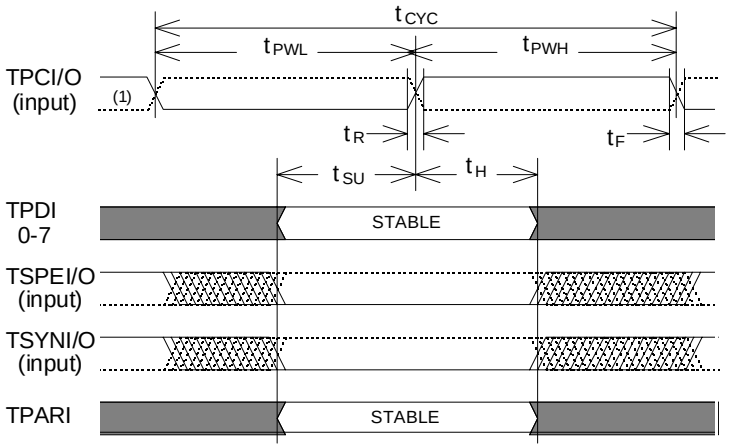
Figure 38. Serial Datacom Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSYNI/O or TSPEI/O Delay after ↓ TTCI/O	t_D	-1.0		3.0	ns	
TTCI/O Fall Time (90% - 10%)	t_{FO}			1.7	ns	2
TTDI Hold Time after ↑ TTCI/O	t_H	0.0			ns	
↑ TTCI/O Output Delay after ↑ DRCI	t_{OD}	6.0	15	24	ns	
TTCI/O High Time	t_{PWHO}	40	50	60	% t_{CYC}	
TTCI/O Low Time	t_{PWLO}	40	50	60	% t_{CYC}	
TTCI/O Rise Time (10% - 90%)	t_{RO}			1.5	ns	2
TTDI Setup Time to ↑ TTCI/O	t_{SU}	10			ns	

Notes:
1. See LTG Timing Characteristics (Figure 17).
2. With 25 pF Load.

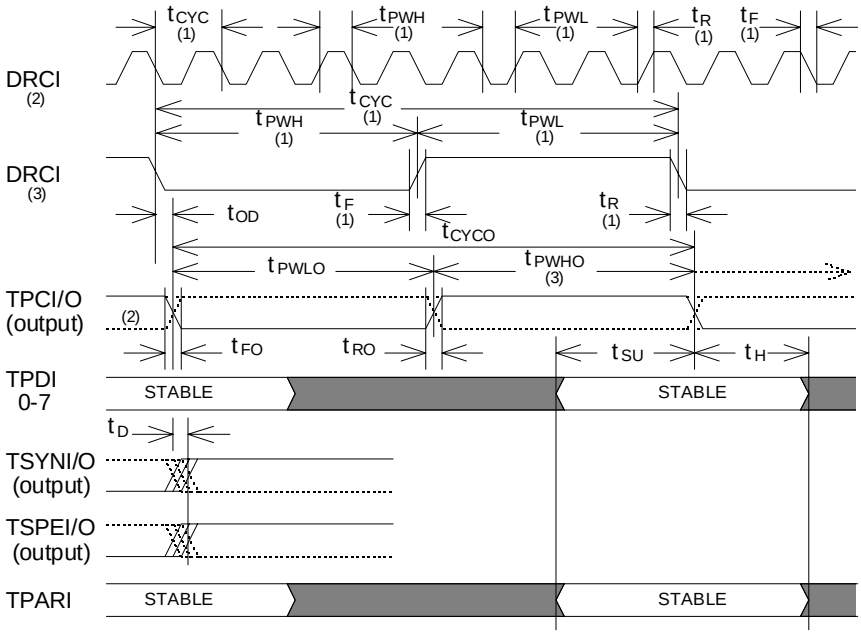
Figure 39. 6.48 Mbyte/s Parallel SONET Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TPCI/O Clock Period	t_{CYC}	154.0	154.3	154.6	ns	
TPCI/O Fall Time (90% - 10%)	t_F			6.0	ns	
TPDI(0-7), TSPEI/O, TSYNI/O or TPARI Hold Time after ↑ TPCI/O	t_H	3.0			ns	1
TPCI/O High Time	t_{PWH}	45	50	55	% t_{CYC}	
TPCI/O Low Time	t_{PWL}	45	50	55	% t_{CYC}	
TPCI/O Rise Time (10% - 90%)	t_R			6.0	ns	
TTDI, TSPEI/O, TSYNI/O or TPARI Setup Time to ↑ TPCI/O	t_{SU}	7.0			ns	1

Note 1: Sampling occurs on Falling Edge of TPCI/O (dotted line) when INVPCK = "1".

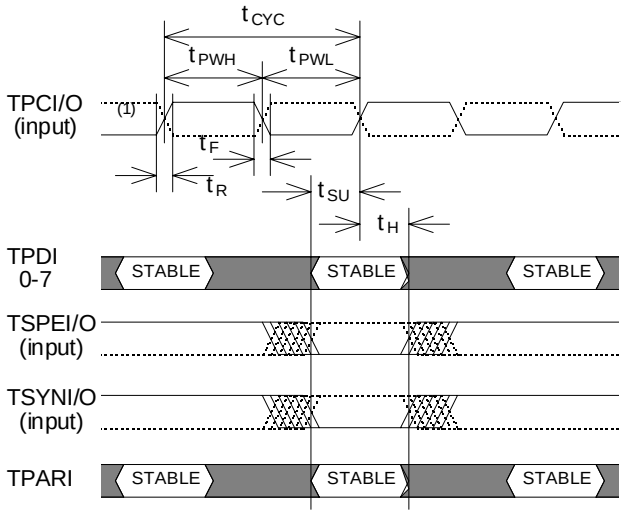
Figure 40. 6.48 Mbyte/s Parallel Datacom Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TPCI/O Clock Period (Generated by DRCI)	t_{CYCO}		8		x t_{CYC}	2
TPCI/O Clock Period (Generated by DRCI)			1			3
TSYNI/O or TSPEI/O Delay after ↓TPCI/O	t_D	-5.0	0.0	5.0	ns	6
TPCI/O Fall Time (90% - 10%)	t_{FO}			2.5	ns	7
TPDI, TPARI Hold Time after ↓ TPCI/O	t_H	0.0			ns	6
↓ TPCI/O Output Delay after ↓ DRCI	t_{OD}	6.0	15	24	ns	2, 6
↓ TPCI/O Output Delay after ↓ DRCI		6.0	15	24		3, 6
TPCI/O High Time	t_{PWHO}	40	50	60	% t_{CYCO}	5
TPCI/O Low Time	t_{PWLO}	40	50	60	% t_{CYCO}	
TPCI/O Rise Time (10% - 90%)	t_{RO}			2.0	ns	7
TPDI, TPARI Setup Time to ↓ TPCI/O	t_{SU}	20			ns	6

Notes:
1. See TTG and LTG Timing Characteristics (Figures 17 and 18).
2. DRCI when DETSEL = "1"
3. DRCI when DETSEL = "0"
4. TPCI/O inverted (dotted line) when INVPCK = "1".
5. TPCI/O can be gapped during TOH and POH Times.
6. ↑ TPCI/O when INVPCK = "1"
7. With 25 pF Load

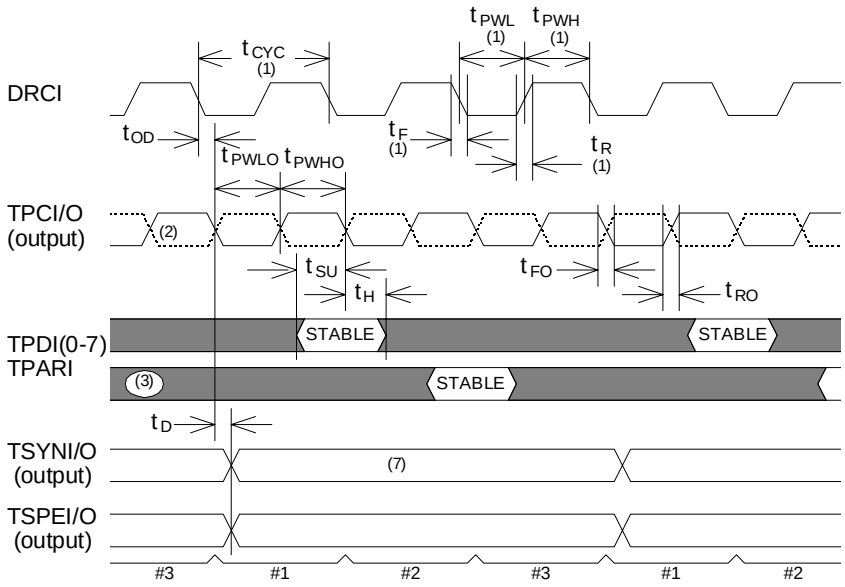
Figure 41. 19.44 Mbyte/s Parallel SONET Input Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
TPCI/O Clock Period	t_{CYC}	50	51.44		ns	
TPCI/O Fall Time (90% - 10%)	t_F			6.0	ns	2
TPDI(0-7), TSPEI/O, TSYNI/O or TPARI Hold Time after ↑ TPCI/O	t_H	3.0			ns	1
TPCI/O High Time	t_{PWH}	40	50	60	% t_{CYC}	
TPCI/O Low Time	t_{PWL}	40	50	60	% t_{CYC}	
TPCI/O Rise Time (10% - 90%)	t_R			6.0	ns	2
TPDI(0-7), TSPEI/O, TSYNI/O or TPARI Setup Time to ↑ TPCI/O	t_{SU}	7.0			ns	1

Notes:
1. Sampling occurs on Falling Edge of TPCI/O (dotted line) when INVPCK = "1".
2. With 25 pF Load

Figure 42. 19.44 Mbyte/s Parallel Datacom Input Timing



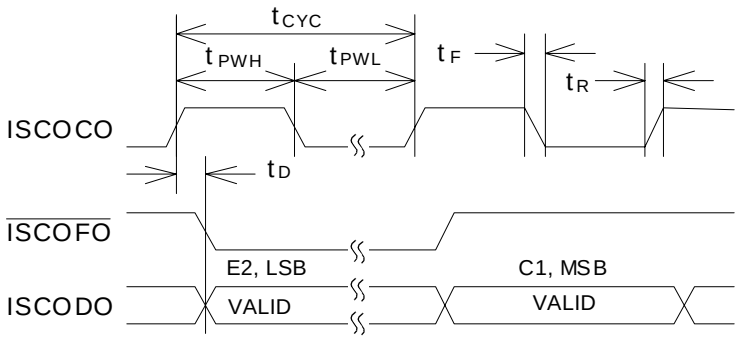
Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSYNI/O or TSPEI/O (valid) Delay after ↓ TPCI/O	t_D	-2.0	0.0	5.0	ns	4
TPCI/O Fall Time (90% - 10%)	t_{FO}			2.5	ns	6
TPDI(0-7) Hold Time after ↓ TPCI/O	t_H	0.0			ns	4, 5
↓ TPCI/O Output Delay after ↓ DRCI	t_{OD}	6.0	15	24	ns	4
TPCI/O High Time	t_{PWHO}	40	50	60	% t_{CYC}	
TPCI/O Low Time	t_{PWLO}	40	50	60	% t_{CYC}	
TPCI/O Rise Time (10% - 90%)	t_{RO}			2.0	ns	6
TPDI(0-7) Setup Time to ↓ TPCI/O	t_{SU}	20			ns	4, 5

Notes:
1. See LTG Timing Characteristics (Figure 19).
2. TPCI/O inverted (dotted line) when INVPCK = "1"
3. TDDLY = "1"
4. ↑ of TPCI/O when INVPCK = "1".
5. When TDDLY = "1", Data is sampled one TPCI/O Period later.
6. With 25 pF Load
7. TSYNI/O is High during all three slots of C1 time.

ISC PORT TIMING

The output timing characteristics of the ISC Port are shown in Figure 43. Figure 44 depicts the input timing.

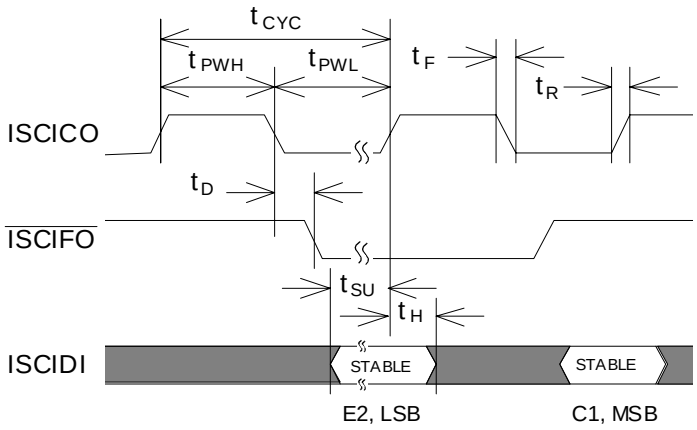
Figure 43. ISC Port Output Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
ISCOCO Clock Period	t_{CYC}		579		ns	1
$\overline{\text{ISCOFO}}$ or ISCODO Delay after ↑ ISCOCO	t_D	-5.0		5.0	ns	
ISCOCO Fall Time (90% - 10%)	t_F			2.5	ns	2
ISCOCO High Time	t_{PWH}	145			ns	1
ISCOCO Low Time	t_{PWL}	145			ns	1
ISCOCO Rise Time (10% - 90%)	t_R			2.0	ns	2

Notes:
1. t_{CYC}, t_{PWH} and t_{PWL} will vary during pointer movements.
2. With 25 pF Load

Figure 44. ISC Port Input Timing



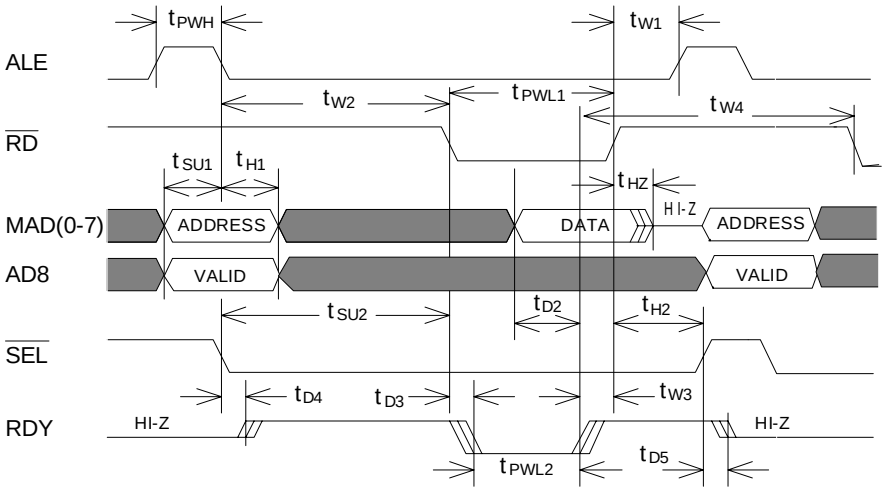
Parameter	Symbol	Min	Typ	Max	Unit	Notes
ISCICO Clock Period	t_{CYC}		579		ns	1
$\overline{\text{ISCIFO}}$ Delay after ↓ ISCICO	t_D	-5.0		5.0	ns	
ISCICO Fall Time (90% - 10%)	t_F			2.5	ns	2
ISCIDI Hold Time after ↑ ISCICO	t_H	0.0			ns	
ISCICO High Time	t_{PWH}	145			ns	1
ISCICO Low Time	t_{PWL}	145			ns	1
ISCICO Rise Time (10% - 90%)	t_R			2.0	ns	2
ISCIDI Setup Time to ↑ ISCICO	t_{SU}	10			ns	

Notes:
1. t_{CYC}, t_{PWH} and t_{PWL} will vary during pointer movements and when gaps occur following E2 and D3 bytes.
2. With 25 pF Load.

MICROPROCESSOR INTERFACE TIMING

Figures 45 through 50 present the µPro Interface timing requirements.

Figure 45. Intel Multiplexed Read Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
MAD(0-7) Data Valid Delay to ↑ RDY	t_{D2}	0.0	20		ns	1
↓ RDY Delay after ↓ $\overline{RD}$	t_{D3}	2.0		15	ns	1
RDY (Active) Delay after ↓ $\overline{SEL}$	t_{D4}			10	ns	
RDY (HI-Z) Delay after ↑ $\overline{SEL}$	t_{D5}			9.0	ns	
MAD(0-7)/AD8 Address Hold Time after ↓ ALE	t_{H1}	3.0			ns	
↑ $\overline{SEL}$ Hold Time after ↑ $\overline{RD}$	t_{H2}	0.0			ns	
MAD(0-7) (HI-Z) Delay after ↑ $\overline{RD}$	t_{HZ}	2.0		7.0	ns	1
ALE High Time	t_{PWH}	20			ns	
$\overline{RD}$ Low Time	t_{PWL1}	40			ns	2
RDY Low Time	t_{PWL2}	0.0		1220	ns	1, 4, 5, 6
MAD(0-7)/AD8 Address Setup Time to ↓ ALE	t_{SU1}	7.0			ns	
↓ $\overline{SEL}$ Setup Time to ↓ $\overline{RD}$	t_{SU2}	0.0			ns	
↑ ALE Wait Time after ↑ $\overline{RD}$	t_{W1}	0.0			ns	
↓ $\overline{RD}$ Wait Time after ↓ ALE	t_{W2}	0.0			ns	
↑ $\overline{RD}$ Wait Time after ↑ RDY	t_{W3}	0.0			ns	
↓ $\overline{WR}$ or ↓ $\overline{RD}$ Wait Time after ↑ RDY	t_{W4}	325			ns	3, 5, 6

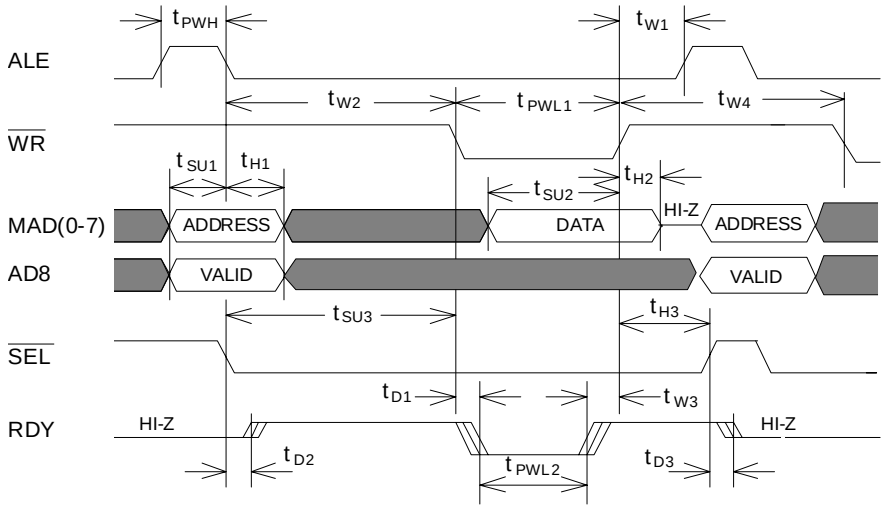
See Notes on next page

Notes:

1. With 75 pF Load.
2. Or time RDY is Low - whichever is greater.
3. t_{W4} = 325 ns[5] from ↑ RDY of two-byte read* to ↓ $\overline{RD}$ of next read of a different address
   10 ns from ↑ RDY of any other case of read to ↓ $\overline{WR}$ or ↓ $\overline{RD}$.
4. 600 ns[5] + max of: (0 ns), or
   (65 ns) - (time since ↑ RDY of last two-byte read* to same address), or
   (310 ns) - (time since ↑ $\overline{WR}$ of last one-byte write to same address), or
   (620 ns) - (time since ↑ $\overline{WR}$ of last two-byte write* to same address).
5. Increase time by 200 ns for SPE mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.
6. All references to edges of $\overline{RD}$ or $\overline{WR}$ for access times or wait times between accesses are understood to be with pin $\overline{SEL}$ Low, which selects this device.

* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

Figure 46. Intel Multiplexed Write Timing



Parameter	Symbol	Min	Typ	Max	Unit	Notes
↓ RDY Delay after ↓ $\overline{WR}$	t_{D1}	2.0		15	ns	1
RDY (Active) Delay after ↓ $\overline{SEL}$	t_{D2}			10	ns	
RDY (HI-Z) Delay after ↑ $\overline{SEL}$	t_{D3}			9.0	ns	
MAD(0-7)/AD8 Address Hold Time after ↓ ALE	t_{H1}	3.0			ns	
MAD(0-7) Data Hold Time after ↑ $\overline{WR}$	t_{H2}	3.0			ns	
↑ $\overline{SEL}$ Hold Time after ↑ $\overline{WR}$	t_{H3}	0.0			ns	
ALE High Time	t_{PWH}	20			ns	
$\overline{WR}$ Low Time	t_{PWL1}	20			ns	2
RDY Low Time	t_{PWL2}	0.0		900	ns	1, 4, 5, 6

Continued on next page

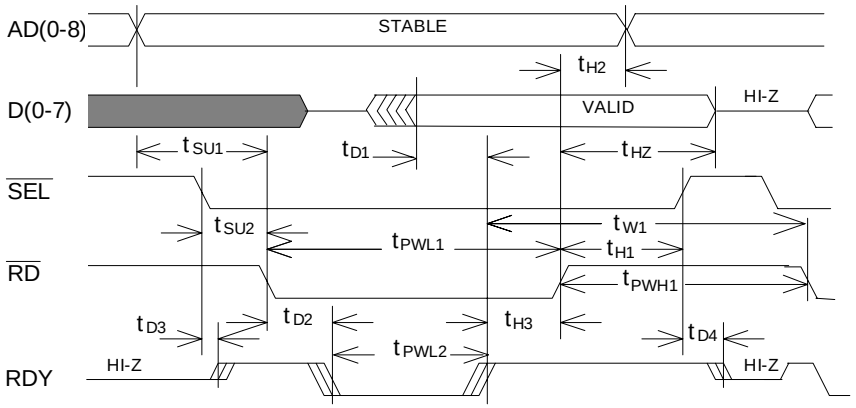
Parameter	Symbol	Min	Typ	Max	Unit	Notes
MAD(0-7)/AD8 Address Setup Time to ↓ ALE	t_{SU1}	7.0			ns	
MAD(0-7) Data Setup Time to ↑ $\overline{WR}$	t_{SU2}	10			ns	
↓ $\overline{SEL}$ Setup Time to ↓ $\overline{WR}$	t_{SU3}	0.0			ns	
↑ ALE Wait Time after ↑ $\overline{WR}$	t_{W1}	0.0			ns	
↓ $\overline{WR}$ Wait Time after ↓ ALE	t_{W2}	0.0			ns	
↑ $\overline{WR}$ Wait Time after ↑ RDY	t_{W3}	0.0			ns	
↓ $\overline{WR}$ or ↓ $\overline{RD}$ Wait Time after ↑ $\overline{WR}$	t_{W4}	900			ns	3, 5, 6

Notes:

1. With 75 pF Load.
2. Or time RDY is Low - whichever is greater.
3. t_{W4} = 600 ns[5] from ↑ $\overline{WR}$ of one-byte write to ↓ $\overline{RD}$ of next read of a different address
   900 ns[5] from ↑ $\overline{WR}$ of two-byte write* to ↓ $\overline{RD}$ of next read of a different address
   10 ns from ↑ $\overline{WR}$ of any other case of write to ↓ $\overline{WR}$ or ↓ $\overline{RD}$.
4. Max of: (0 ns), or
   (350 ns)[5] - (time since ↑ $\overline{RDY}$ of last two-byte read* to same address), or
   (900 ns)[5] - (time since ↑ $\overline{WR}$ of last two-byte write* to any address), or
   (600 ns)[5] - (time since ↑ $\overline{WR}$ of last one-byte write to any address).
5. Increase time by 200 ns for $\overline{SPE}$ mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.
6. All references to edges of $\overline{RD}$ or $\overline{WR}$ for access times or wait times between accesses are understood to be with the $\overline{SEL}$ pin Low, which selects this device.

* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

Figure 47. Intel Read Timing

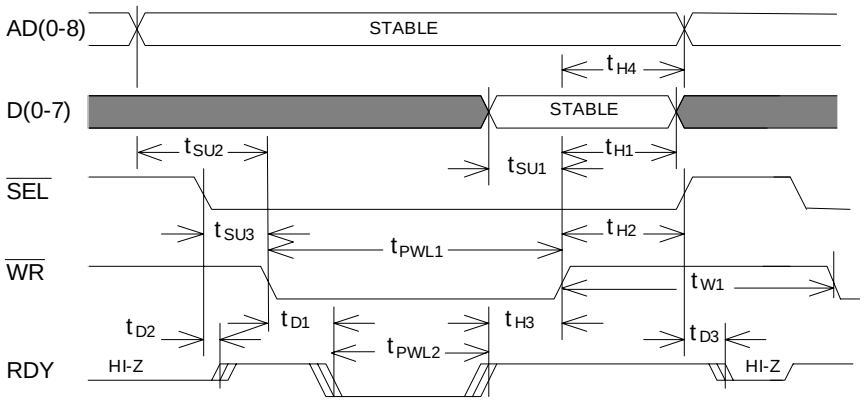


Parameter	Symbol	Min	Typ	Max	Unit	Notes
↑ RDY Delay after D(0-7) (Data Valid)	t_{D1}	0.0	20		ns	1
↓ RDY Delay after ↓ $\overline{RD}$	t_{D2}	2.0		15	ns	1
RDY (Active) Delay after ↓ $\overline{SEL}$	t_{D3}			10	ns	
RDY (HI-Z) Delay after ↑ $\overline{SEL}$	t_{D4}			9.0	ns	
D(0-7) (HI-Z) Delay after ↑ $\overline{RD}$	t_{HZ}	2.0		7.0	ns	1
$\overline{SEL}$ Low Hold Time after ↑ $\overline{RD}$	t_{H1}	0.0			ns	
AD(0-8) Address Hold Time after ↑ $\overline{RD}$	t_{H2}	0.0			ns	
$\overline{RD}$ Low Hold Time after ↑ RDY	t_{H3}	0.0			ns	
$\overline{RD}$ Low Time	t_{PWL1}	40			ns	2
$\overline{RD}$ High Time	t_{PWH1}	10			ns	
↓ $\overline{WR}$ or ↓ $\overline{RD}$ Wait Time after ↑ RDY	t_{W1}	325			ns	3, 5, 6
RDY Low Time	t_{PWL2}	0.0		1220	ns	1, 4, 5, 6
AD(0-8) Address Setup Time to ↓ $\overline{RD}$	t_{SU1}	0.0			ns	
↓ $\overline{SEL}$ Setup Time to ↓ $\overline{RD}$	t_{SU2}	0.0			ns	

Notes:
1. With 75 pF Load.
2. Or time RDY is Low - whichever is greater.
3. t_{W1} = 325 ns[5] from ↑ RDY of two-byte read* to ↓ $\overline{RD}$ of next read of a different address
   10 ns from ↑ RDY of any other case of read to ↓ $\overline{WR}$ or ↓ $\overline{RD}$.
4. 600 ns[5] + max of: (0 ns), or
   (65 ns) - (time since ↑ RDY of last two-byte read* to same address), or
   (310 ns) - (time since ↑ $\overline{WR}$ of last one-byte write to same address), or
   (620 ns) - (time since ↑ $\overline{WR}$ of last two-byte write* to same address).
5. Increase time by 200 ns for SPE mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.
6. All references to edges of $\overline{RD}$ or $\overline{WR}$ for access times or wait times between accesses are understood to be with the $\overline{SEL}$ pin Low, which selects this device.

* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

Figure 48. Intel Write Timing

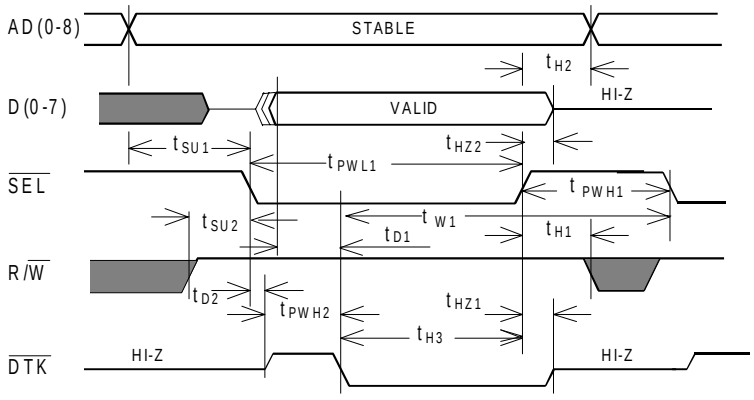


Parameter	Symbol	Min	Typ	Max	Unit	Notes
AD(0-8) Address Hold Time after ↑ $\overline{WR}$	t_{H4}	3.0			ns	
↓ RDY Delay after ↓ $\overline{WR}$	t_{D1}	2.0		15	ns	1
RDY (Active) Delay after ↓ $\overline{SEL}$	t_{D2}			10	ns	
RDY (HI-Z) Delay after ↑ $\overline{SEL}$	t_{D3}			9.0	ns	
D(0-7) Data Hold Time after ↑ $\overline{WR}$	t_{H1}	3.0			ns	
↑ $\overline{SEL}$ Hold Time after ↑ $\overline{WR}$	t_{H2}	0.0			ns	
↑ $\overline{WR}$ Hold Time after ↑ RDY	t_{H3}	0.0			ns	
$\overline{WR}$ Low Time	t_{PWL1}	20			ns	2
↓ $\overline{WR}$ or ↓ $\overline{RD}$ Wait Time after ↑ $\overline{WR}$	t_{W1}	900			ns	3, 5, 6
RDY Low Time	t_{PWL2}	0.0		900	ns	1, 4, 5, 6
D(0-7) Data Setup Time to ↑ $\overline{WR}$	t_{SU1}	10			ns	
AD(0-8) Address Setup Time to ↓ $\overline{WR}$	t_{SU2}	0.0			ns	
↓ $\overline{SEL}$ Setup Time to ↓ $\overline{WR}$	t_{SU3}	0.0			ns	

Notes:
1. With 75 pF Load.
2. Or time RDY is Low - whichever is greater.
3. t_{W1} = 600 ns[5] from ↑ $\overline{WR}$ of one-byte write to ↓ $\overline{RD}$ of next read of a different address
   900 ns[5] from ↑ $\overline{WR}$ of two-byte write* to ↓ $\overline{RD}$ of next read of a different address
   10 ns from ↑ $\overline{WR}$ of any other case of write to ↓ $\overline{WR}$ or ↓ $\overline{RD}$.
4. Max of: (0 ns), or
   (350 ns)[5] - (time since ↑ RDY of last two-byte read* to same address), or
   (900 ns)[5] - (time since ↑ $\overline{WR}$ of last two-byte write* to any address), or
   (600 ns)[5] - (time since ↑ $\overline{WR}$ of last one-byte write to any address).
5. Increase time by 200 ns for SPE mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.
6. All references to edges of $\overline{RD}$ or $\overline{WR}$ for access times or wait times between accesses are understood to be with the $\overline{SEL}$ pin Low, which selects this device.

* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

Figure 49. Motorola Read Timing

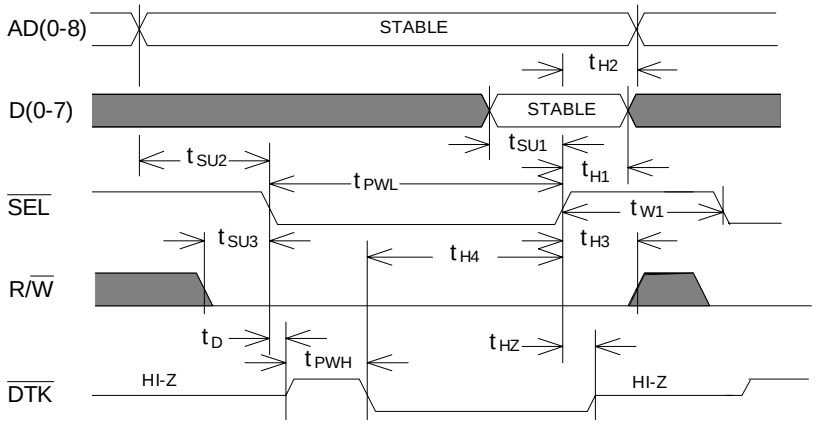


Parameter	Symbol	Min	Typ	Max	Unit	Notes
↓ $\overline{DTK}$ Delay after D(0-7) (Data Valid)	t_{D1}	0.0	20		ns	1
↑ $\overline{DTK}$ Delay after ↓ $\overline{SEL}$	t_{D2}	2.0		15	ns	1
R/$\overline{W}$ Hold Time after ↑ $\overline{SEL}$	t_{H1}	3.0			ns	
AD(0-8) Address Hold Time after ↑ $\overline{SEL}$	t_{H2}	3.0			ns	
↑ $\overline{SEL}$ Hold Time after ↓ $\overline{DTK}$	t_{H3}	0.0			ns	
$\overline{DTK}$ (HI-Z) Hold Time after ↑ $\overline{SEL}$	t_{HZ1}	2.0		9.0	ns	1
D(0-7) Data Hi-Z Delay after ↑ $\overline{SEL}$	t_{HZ2}	2.0		7.0	ns	1
$\overline{SEL}$ High Time	t_{PWH1}	10			ns	
$\overline{SEL}$ Low Time	t_{PWL1}	40			ns	2
$\overline{DTK}$ High Time	t_{PWH2}	0.0		1220	ns	1, 4, 5
↓ $\overline{SEL}$ Wait Time after ↓ $\overline{DTK}$	t_{W1}	325			ns	3, 5
AD(0-8) Address Setup Time to ↓ $\overline{SEL}$	t_{SU1}	0.0			ns	
↑ R/$\overline{W}$ Setup Time to ↓ $\overline{SEL}$	t_{SU2}	5.0			ns	

Notes:
1. With 75 pF Load.
2. Or time $\overline{DTK}$ is High - whichever is greater.
3. tW1 = 325 ns[5] from ↓ $\overline{DTK}$ of two-byte read* to ↓ $\overline{SEL}$ of next read of a different address
   10 ns from ↓ $\overline{DTK}$ of any other case of read to ↓ $\overline{SEL}$.
4. 600 ns[5] + max of: (0 ns), or
   (65 ns) - (time since ↓ $\overline{DTK}$ of last two-byte read* to same address), or
   (310 ns) - (time since ↑ $\overline{SEL}$ of last one-byte write to same address), or
   (620 ns) - (time since ↑ $\overline{SEL}$ of last two-byte write* to same address).
5. Increase time by 200 ns for SPE mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.

* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

Figure 50. Motorola Write Timing

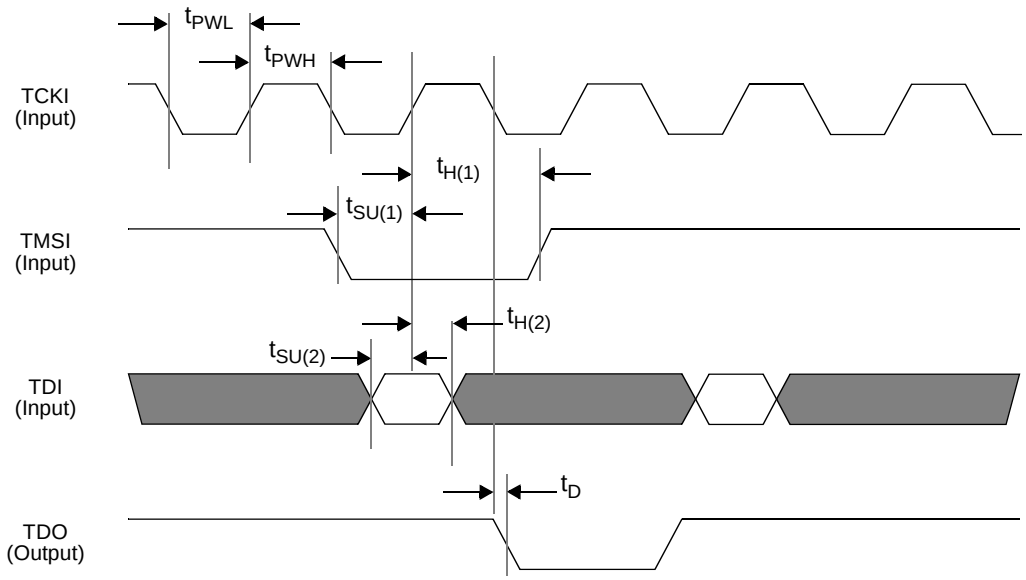


Parameter	Symbol	Min	Typ	Max	Unit	Notes
↑ $\overline{\text{DTK}}$ Delay after ↓ $\overline{\text{SEL}}$	t_D	2.0		15	ns	
$\overline{\text{DTK}}$ (HI-Z) Delay after ↑ $\overline{\text{SEL}}$	t_{HZ}			9.0	ns	
D(0-7) Data Hold Time after ↑ $\overline{\text{SEL}}$	t_{H1}	3.0			ns	
AD(0-8) Address Hold Time after ↑ $\overline{\text{SEL}}$	t_{H2}	3.0			ns	
R/$\overline{\text{W}}$ Hold Time after ↑ $\overline{\text{SEL}}$	t_{H3}	3.0			ns	
↑ $\overline{\text{SEL}}$ Hold Time after ↓ $\overline{\text{DTK}}$	t_{H4}	0.0			ns	
$\overline{\text{DTK}}$ High Time	t_{PWH}	0.0		900	ns	1, 4, 5
$\overline{\text{SEL}}$ Low Time	t_{PWL}	20			ns	2
↓ $\overline{\text{SEL}}$ Wait Time after ↑ $\overline{\text{SEL}}$	t_{W1}	900			ns	3, 5
D(0-7) Data Setup Time to ↑ $\overline{\text{SEL}}$	t_{SU1}	10			ns	
AD(0-8) Address Setup Time to ↓ $\overline{\text{SEL}}$	t_{SU2}	0.0			ns	
↓ R/$\overline{\text{W}}$ Setup Time to ↓ $\overline{\text{SEL}}$	t_{SU3}	5.0			ns	

Notes:
1. With 75 pF Load.
2. Or time DTK is High - whichever is greater.
3. t_{W1} = 600 ns[5] from ↑ $\overline{\text{SEL}}$ of one-byte write to ↓ $\overline{\text{SEL}}$ of next read of a different address
   900 ns[5] from ↑ $\overline{\text{SEL}}$ of two-byte write* to ↓ $\overline{\text{SEL}}$ of next read of a different address
   10 ns from ↑ $\overline{\text{SEL}}$ of any other case of write to ↓ $\overline{\text{SEL}}$.
4. Max of: (0 ns), or
   (350 ns)[5] - (time since ↓ $\overline{\text{DTK}}$ of last two-byte read* to same address), or
   (900 ns)[5] - (time since ↑ $\overline{\text{SEL}}$ of last two-byte write* to any address), or
   (600 ns)[5] - (time since ↑ $\overline{\text{SEL}}$ of last one-byte write to any address).
5. Increase time by 200 ns for SPE mode with evenly spaced gaps, or by 775 ns if gaps are grouped together in a row.

* Two-byte read/write is a read or write of the low byte of a 16-bit counter when CNT16EN = "1".

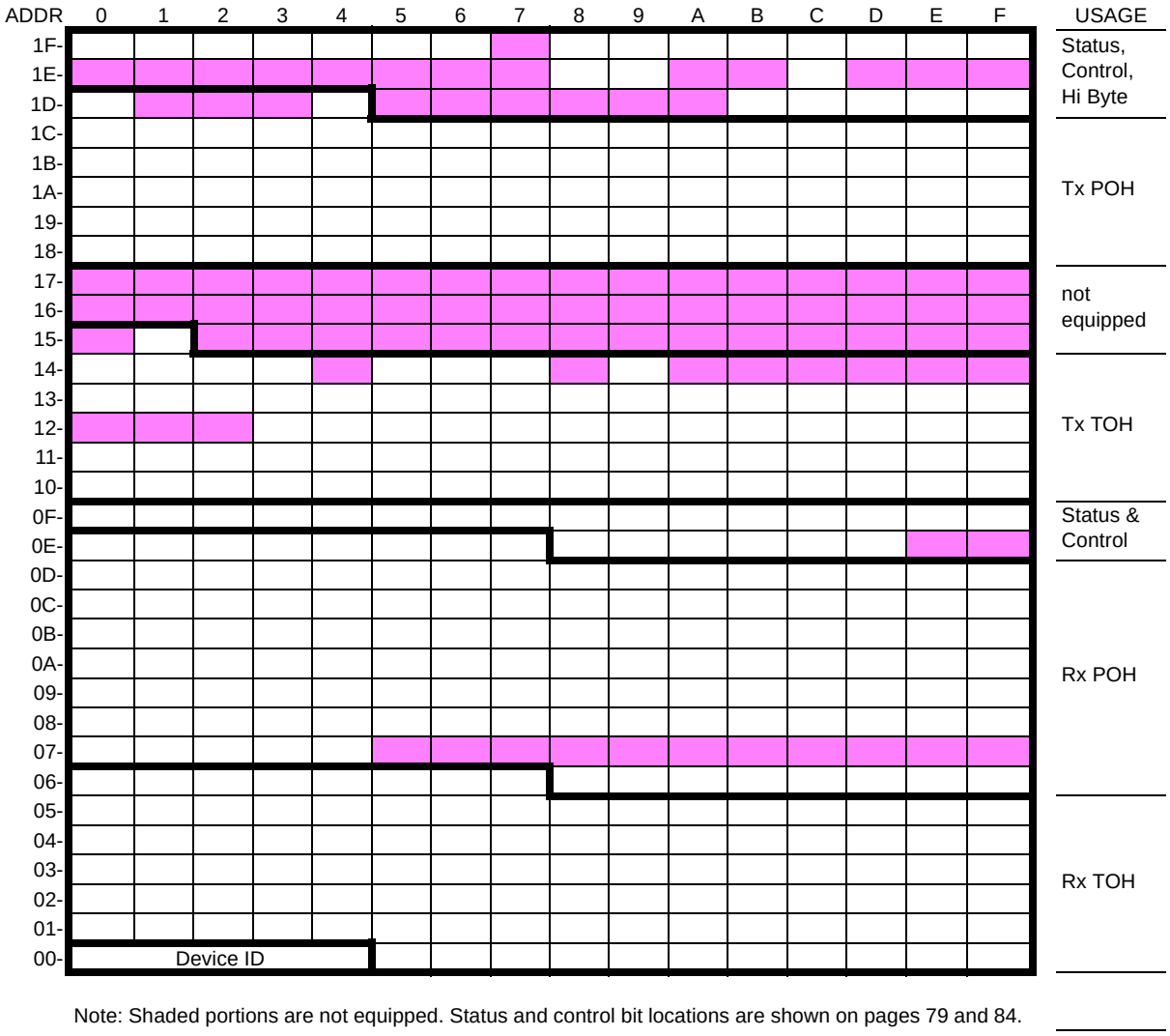
Figure 51. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCKI Clock High Time	t_{PWH}	50		ns
TCKI Clock Low Time	t_{PWL}	50		ns
TMSI Setup Time to TCKI↑	$t_{SU(1)}$	3.0	-	ns
TMSI Hold Time after TCKI↑	$t_{H(1)}$	2.0	-	ns
TDI Setup Time to TCKI↑	$t_{SU(2)}$	3.0	-	ns
TDI Hold Time after TCKI↑	$t_{H(2)}$	2.0	-	ns
TDO Delay after TCKI↓	t_D	-	7.0	ns

MEMORY MAP

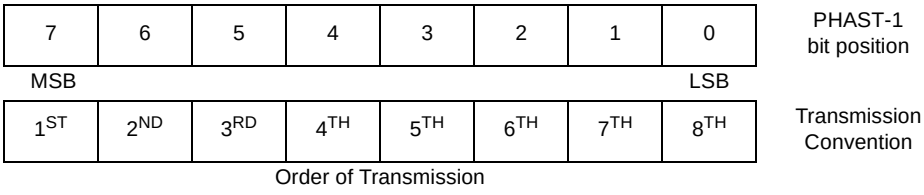
The overall Memory Map is shown in Figure 52. All register (byte location) addresses are shown in Hex as xyz[H]. The row positions represent the least significant address character (z). Detailed descriptions of the used byte locations are provided in the following sections.



Note: Shaded portions are not equipped. Status and control bit locations are shown on pages 79 and 84.

Figure 52. Overall Memory Map

The relationship between the bits of a Transmission Byte, e.g., C1, and the corresponding bits of a PHAST-1 memory map byte location is shown below.



DEVICE IDENTIFICATION - Read Only

Address [H]	Status Bits	Control Bits	Description
000 - 004			**ID 0**: all "0" **ID 1**: all "0" **ID 2**: all "0" **ID 3**: all "0" **ID 4**: all "0"

Note: Device identification is not encoded in the Device Identification byte locations.

RX TOH BYTES - Read/Write

Address [H]	Status Bits	Control Bits	Description
005 - 007		OA	**Rx Line D1-D3**: Section DCC Bytes - The D1-D3 Bytes are also output as a single 192 kbit/s channel at the Rx Section DCC Port. These bytes are also optionally available at the Rx OA/TOH Port. 005[H] = D1 and 007[H] = D3.
008 - 010		OA	**Rx Line D4-D12**: Line DCC Bytes - The D4-D12 Bytes are also output as a single 576 kbit/s channel at the Rx Line DCC Port. These bytes are also optionally available at the Rx OA/TOH Port. 008[H] = D4 and 010[H] = D12
011 and 012	RNPTR RLOP RAIS-P RCPTR	OA	**Rx Line H1 and H2**: Pointer Bytes - The H1 and H2 bytes are processed internally. These bytes are also optionally available at the Rx OA/TOH Port.
013		OA	**Rx Line H3**: Pointer Action Byte - This byte is also optionally available at the Rx OA/TOH Port.
014		STS1 OA	**Rx Line B1**: Section Parity Byte - If STS1 = "1", this byte contains BIP-8 Parity which is even parity over all bytes in the frame. If STS1 = "0", this Byte contains Parity Error Information *where*: any "1"s indicate a BIP-8 Error in that Bit Position. Parity Errors are accumulated by the Rx B1 Error Counter. This byte is also optionally available at the Rx OA/TOH Port.
015		OA	**Rx Line B2**: Line BIP-8 Parity Byte - The Parity Calculation is even parity over all bytes in the frame except the 9 Section Overhead Bytes. Parity Errors are accumulated by the Rx B2 Error Counter. Additional processing is performed to develop an Excess B2 BER Alarm. This byte is also optionally available at the Rx OA/TOH Port.
016 and 017	RFE RSEF RLOF	OA	**Rx Line A1 and A2**: Framing Bytes - The expected pattern is F6[H] and 28[H] in the A1 and A2 Bytes, respectively. These bytes are also optionally available at the Rx OA/TOH Port.
018	RLE1	RE2A	**Rx Line E1**: Section Order Wire Byte - This byte can be optionally used for AIS communication between PHAST-1s and/or SOT-1s/SOT-1Es and is also available at the Rx OA/TOH Port.
019			**Rx Line E2**: Line Order Wire Byte - This byte is also available at the Rx OA/TOH Port.

Address [H]	Status Bits	Control Bits	Description
01A		OA	**Rx Line Z1**: 1ST Growth Byte - This byte is debounced and stored in Location 05A[H]. This Byte is also optionally available at the Rx OA/TOH Port.
01B		OA	**Rx Line Z2**: 2ND Growth Byte - This byte is debounced and stored in Location 05B[H]. Bits 5-8 (Transmission Convention) are interpreted as FEBE-L Information and Errors are accumulated by the FEBE-L Counter. This byte is also optionally available at the Rx OA/TOH Port.
01C	J0MIS	J0EN0 J0EN1 OA	**Rx Line C1**: STS-1 Number/J0 - This byte is debounced and stored in Location 05C[H]. If J0EN(1,0) = "00", no further Processing is performed. If J0EN(1,0) = "01", the received value is also compared to value in Location 067[H]. If J0EN1 = "1", the J0 message is internally stored and accessible through Locations 080[H] - 0BF[H]. This byte is also optionally available at the Rx OA/TOH Port.
01D		OA	**Rx Line F1**: Section User Byte - This byte is debounced and stored in Location 05D[H] and is also optionally available at the Rx OA/TOH Port.
01E and 01F	RAPS RAIS-L RRDI-L		**Rx Line K1 and K2**: APS Bytes - These bytes are debounced and stored in Locations 05E[H] and 05F[H], respectively. They are monitored for APS Channel Failure. K2 Byte, Bits 6-8 (Transmission Convention) are monitored for AIS-L and RDI-L Alarms. These bytes are also available at the Rx OA/TOH Port.
020 and 021			Internal Use - Do Not Access
022	LPJOF	RXRTM SPE RCLK RRAIS SRLAIS SRPAIS RSWRES	**Local PJ Count**: count of all Positive and Negative Pointer Justifications that are created when Rx Re-timing is enabled. This is an 8-Bit, Clear on Read, Saturating Counter. Counting is inhibited upon declaration of RLOC, RLOS, RLOF or RAIS-L, or if AIS-L or AIS-P is inserted at the Rx Terminal Port.
023 and 024			**Reserved**: Reserved for future use
025 - 027		Pin $\overline{\text{MBEI}}$ SPE RRSD TTOHEN	**Rx Insert D1-D3**: 1. bytes, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled 2. bytes received at Input ISC Port if ISC Port Option is enabled; 025[H] = D1 and 027[H] = D3.
028 - 030		Pin $\overline{\text{MBEI}}$ SPE RRLD TTOHEN	**Rx Insert D4-D12**: 1. bytes, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled 2. bytes received at Input ISC Port if ISC Port Option is enabled; 028[H] = D4 and 030[H] = D12
031 and 032		Pin $\overline{\text{MBEI}}$ SPE RRPTR	**Rx Insert H1 and H2**: bytes to be multiplexed into Rx Terminal Port Data if insertion option is enabled. **WARNING**: This is for test purposes only. The Payload does not track the pointer value written in these locations.

Address [H]	Status Bits	Control Bits	Description
033		Pin $\overline{\text{MBEI}}$ SPE RCLK RXRTM	**Rx Insert H3**: Rx Terminal Port Data H3 Byte value when Rx Re-timing is enabled and a Pointer Decrement is not performed.
034		Pin $\overline{\text{MBEI}}$ SPE RRB1 TTOHEN	**Rx Insert B1**: 1. internally generated B1 value multiplexed into Rx Terminal Port Data if insertion option is enabled. The Parity Calculation is even parity over all bytes in the frame. 2. byte received at Input ISC Port if ISC Port Option is enabled.
035		Pin $\overline{\text{MBEI}}$ SPE RRB2 TTOHEN	**Rx Insert B2**: 1. internally generated B2 value multiplexed into Rx Terminal Port Data if insertion option is enabled. The Parity Calculation is even parity over all bytes in the frame except the 9 Section Overhead Bytes. 2. byte received at Input ISC Port if ISC Port Option is enabled.
036 and 037		Pin $\overline{\text{MBEI}}$ SPE RRFRM	**Rx Insert A1 and A2**: internally generated A1 and A2 values multiplexed into Rx Terminal Port Data.
038		Pin $\overline{\text{MBEI}}$ SPE RRE1 TTOHEN RA2E	**Rx Insert E1**: 1. byte, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled. 2. byte received at Input ISC Port if ISC Port Option is enabled. This byte can be used for AIS communication between SOT-1s, SOT-1Es and/or PHAST-1s.
039		Pin $\overline{\text{MBEI}}$ SPE RRE2 TTOHEN	**Rx Insert E2**: 1. byte, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled. 2. byte received at Input ISC Port if ISC Port Option is enabled.
03A		Pin $\overline{\text{MBEI}}$ SPE RRZ1 TTOHEN	**Rx Insert Z1**: 1. byte, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled. 2. byte received at Input ISC Port if ISC Port Option is enabled.
03B		Pin $\overline{\text{MBEI}}$ SPE RRZ2 TTOHEN	**Rx Insert Z2**: 1. byte, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled. 2. byte received at Input ISC Port if ISC Port Option is enabled.
03C		Pin $\overline{\text{MBEI}}$ SPE RRC1 TTOHEN	**Rx Insert C1**: 1. byte, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled. 2. byte received at Input ISC Port if ISC Port Option is enabled.
03D		Pin $\overline{\text{MBEI}}$ SPE RRF1 TTOHEN	**Rx Insert F1**: 1. byte, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled. 2. byte received at Input ISC Port if ISC Port Option is enabled.
03E and 03F		Pin $\overline{\text{MBEI}}$ SPE RRAPS TTOHEN	**Rx Insert K1 and K2**: 1. bytes, written by µPro, to be multiplexed into Rx Terminal Port Data if insertion option is enabled 2. bytes received at Input ISC Port if ISC Port Option is enabled

Address [H]	Status Bits	Control Bits	Description
040	RLFEBEOF	RSWRES CNT16EN DISRLAL	**FEBE-L Count**: count of FEBE-L Errors that are incoming on the Rx Line. This is an 8 or 16-Bit, Clear on Read, Saturating Counter. In 8-Bit Mode the total counter value is available at this location. In 16-Bit Mode this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16-Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, or RAIS-L or by DISRLAL.
041 - 043			Internal Use - Do Not Access
044	RPJOF	RSWRES	**Rx PJ Count**: count of all Positive and Negative Pointer Justifications that are incoming on the Rx Line. This is an 8-Bit, Clear on Read, Saturating Counter. Counting is inhibited upon declaration of RLOC, RLOS, RLOF or RAIS-L.
045	RPMOVOF	RSWRES	**Rx Inc Count/Dec Count**: two - 4-Bit Counters. Bits 7-4 accumulate Pointer Increments incoming on the Rx Line. Bits 3-0 accumulate Pointer Decrements incoming on the Rx Line. Both Counters are Saturating and Clear on Read. Counting is inhibited upon declaration of RLOC, RLOS, RLOF or RAIS-L.
046	RB1COF	RSWRES CNT16EN DISRLAL	**Rx B1 Error Count**: count of B1 Errors that are incoming on the Rx Line. This is an 8 or 16-Bit, Clear on Read, Saturating Counter. In 8-Bit Mode the total counter value is available at this location. In 16-Bit Mode this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16-Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS or RLOF or by DISRLAL.
047	RB2COF	RSWRES CNT16EN DISRLAL	**Rx B2 Error Count**: count of B2 Errors that are incoming on the Rx Line. This is an 8 or 16-Bit, Clear on Read, Saturating Counter. In 8-Bit Mode the total counter value is available at this location. In 16-Bit Mode this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16-Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF or RAIS-L or by DISRLAL.
048			Internal Use - Do Not Access
049			**Rx B1 Error Mask**: the contents of this location are exclusive-OR gated, bit by bit, with the B1 Byte output at the Rx Terminal Port.
04A - 04F			**Frm-1 (Z1, Z2, C1, F1, K1, K2)**: respective bytes received in the previous frame *where*: 04A[H] = Frm-1 Z1 and 04F[H] = Frm-1 K2.
050			Internal Use - Do Not Access
051			**Rx B2 Error Mask**: the contents of this location are exclusive-OR gated, bit by bit, with the B2 Byte output at the Rx Terminal Port.
052 - 057			**Frm-2 (Z1, Z2, C1, F1, K1, K2)**: respective bytes received two frames earlier *where*; 052[H] = Frm-2 Z1 and 057[H] = Frm-2 K2.

Address [H]	Status Bits	Control Bits	Description
058 and 059			Internal Use - Do Not Access
05A - 05F	RTNEW		**Debounced (Z1, Z2, C1, F1, K1, K2)**: respective debounced bytes *where*: 05A[H] = Debounced Z1 and 05F[H] = Debounced K2. Any byte that is received with a New Value, and that New Value is constant for three consecutive frames, will cause the New Value to be written to these locations. The algorithm is illustrated below *where*: F and F+n = Frame Numbers in an arbitrary sequence of consecutive frames N = a Z1, Z2, C1, F1, K1, or K2 Byte Location X, Y and Z = Received Values of the N Byte Rx Frame Number Parameter F F+1 F+2 F+3 F+4 F+5 Rx Line N X Y X Z Z Z Frm-1 N X X Y X Z Z Frm-2 N X X X Y X Z Debnce. N X X X X X Z RTNEW 0 0 0 0 0 1
060	B2EBER	B2MULT0 B2MULT1 B2MULT2	**Block Size (B2M)**: See Table 9 for B2EBER Parameter settings. Bits 4-7 are not used.
061			**B2WIN**: see Table 9 for B2EBER Parameter settings.
062			**B2CCV/B2SCV**: Bits 0-3 are the B2CCV Parameter. Bits 4-7 are the B2SCV Parameter. See Table 9 for B2EBER Parameter settings.
063			**B2 Set**: see Table 9 for B2EBER Parameter settings.
064			**B2 Clear**: see Table 9 for B2EBER Parameter settings.
065 and 066			Internal Use - Do Not Access
067			**J0 Expect**: value with which Rx Line C1 Location is compared for Single Byte J0 Processing.

RX POH BYTES - Read/Write

Address [H]	Status Bits	Control Bits	Description
068	B3EBER	B3MULT0 B3MULT1 B3MULT2	**Block Size (B3M)**: See Table 15 for B3EBER Parameter settings. Bits 4-7 are not used.
069			**B3WIN**: see Table 15 for B3EBER Parameter settings.

Address [H]	Status Bits	Control Bits	Description
06A			**B3CCV/B3SCV**: Bits 0-3 are the B3CCV Parameter. Bits 4-7 are the B3SCV Parameter. See Table 15 for B3EBER Parameter settings.
06B			**B3 Set**: see Table 15 for B3EBER Parameter settings.
06C			**B3 Clear**: see Table 15 for B3EBER Parameter settings.
06D and 06E			Internal Use - Do Not Access
06F			**Reserved**: Reserved for future use
070 - 072			Internal Use - Do Not Access
073 and 074			**Reserved**: Reserved for future use
075 - 07F			NOT EQUIPPED
080 - 0BF		J0RWEN J0EN0 J0EN1 J0SYNC	**Rx Line J0/J1**: Line or Path Trace Bytes - Multiple byte J0 messages and the J1 Bytes are accessed at these locations. These locations are only used for J0 Messages if J0EN1 = "1". If J1SYNCEN = "1" or J0EN(1,0) = "11" the byte immediately following an ASCII <CR> and <LF>, of the appropriate message, will be stored in Location 080[H]. The Rx Line J1 Bytes are always output at the Rx Terminal Port. These Bytes are also available at the Rx POH Port.
0C0			**Rx Line B3**: Path BIP-8 Parity Byte - The Parity Calculation is even parity over all SPE Bytes (the 27 TOH Bytes are excluded). Parity Errors are accumulated by the Rx B3 Error Counter. Additional processing is performed to develop an Excess B3 BER Alarm. These Bytes are also available at the Rx POH Port.
0C1	C2MIS C2UNEQ RPDI-P		**Rx Line C2**: Path Signal Label Byte - This byte is debounced and stored in Location 0D1[H]. Additional processing is performed to develop Mismatch, Unequipped, and Path Defect Indications. This byte is also available at the Rx POH Port.
0C2	RRDI-P RRDI-PSD RRDI-PCD RRDI-PPD	PRDISEL	**Rx Line G1**: Path Status Byte - Bits 1-4 (Transmission Convention) are processed for FEBE-P information and the Errors are accumulated by the FEBE-P Counter. Bits 5, 6 and 7, (Transmission Convention) are processed as the RDI-P Alarm, either for Single Bit RDI-P or for Three Bit RDI-P applications. This byte is also available at the Rx POH Port.
0C3			**Rx Line F2**: Path User Channel Byte - This byte is debounced and stored in Location 0D3[H]. This byte is also available at the Rx POH Port.
0C4	RLOM	H4INT	**Rx Line H4**: Multiframe Indicator Byte - Bits 7 and 8 (Transmission Convention) are optionally used to synchronize an internal, 2-Bit, Modulo 4, Rx Multiframe Counter for VT structured payloads. Bits 1-6 (Transmission Convention) are not processed. This byte is also available at the Rx POH Port.

Address [H]	Status Bits	Control Bits	Description
0C5 - 0C7			**Rx Line (Z3, Z4 and Z5)**: 3^{RD}, 4^{TH} and 5^{TH} Growth Bytes - These bytes are debounced and stored in Locations 0D5[H], 0D6[H], and 0D7[H], respectively. These Bytes are also available at the Rx POH Port. OC5[H] = Z3 and 0C7[H] = Z5.
0C8		RPATH H4INT	**Rx Insert B3**: internally generated B3 value multiplexed into Rx Terminal Port Data if insertion option is enabled. The Parity Calculation is even parity over all SPE Bytes (the 27 TOH Bytes are excluded).
0C9		RPATH	**Rx Insert C2**: byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled
0CA		RPATH	**Rx Insert G1**: byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled
0CB		RPATH	**Rx Insert F2**: byte to be multiplexed into Rx Terminal Port Data if insertion option is enabled
0CC			Internal Use - Do Not Access
0CD - 0CF		RPATH	**Rx Insert (Z3, Z4 and Z5)**: bytes to be multiplexed into Rx Terminal Port Data if insertion option is enabled *where*: OCD[H] = Z3 and 0CF[H] = Z5
0D0			**Rx B3 Error Mask**: the contents of this location are exclusive-OR gated, bit by bit, with the B3 Byte output at the Rx Terminal Port.
0D1	RPNEW		**Debounced C2**: the Debounce Algorithm is the same as used for TOH Debouncing (see 05A[H] to 05F[H] above).
0D2	RPFEBEOF	RSWRES CNT16EN	**FEBE-P Count**: count of FEBE-P Errors that are incoming on the Rx Line. This is an 8 or 16-Bit, Clear on Read, Saturating Counter. In 8-Bit Mode, the total counter value is available at this location. In 16-Bit Mode this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16-Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, RAIS-L, RLOP, or RAIS-P.
0D3	RPNEW		**Debounced F2**: the Debounce Algorithm is the same as used for TOH Debouncing (see 05A[H] to 05F[H] above).
0D4	RB3COF	RSWRES CNT16EN	**Rx B3 Error Count**: count of B3 Errors that are incoming on the Rx Line. This is an 8 or 16-Bit, Clear on Read, Saturating Counter. In 8-Bit Mode the total counter value is available at this location. In 16-Bit Mode this location is the Lower Order 8 Bits. The Higher Order 8 Bits are readable in Location 1FF[H]. The Lower Order Byte must be Read first in 16-Bit Mode. Counting is inhibited upon declaration of RLOC, RLOS, RLOF, RAIS-L, RLOP, or RAIS-P.
0D5 - 0D7	RPNEW		**Debounced (Z3, Z4 and Z5)**: *where*: OD5[H] = Z3 and 0D7[H] = Z5. The Debounce Algorithm is the same as used for TOH Debouncing (see 05A[H] to 05F[H] above).
0D8			Internal Use - Do Not Access
0D9			**Frm-1 C2**: C2 Byte received in the previous frame
0DA			Internal Use - Do Not Access

Address [H]	Status Bits	Control Bits	Description
0DB			**Frm-1 F2**: F2 Byte received in the previous frame
0DC			Internal Use - Do Not Access
0DD - 0DF			**Frm-1 (Z3, Z4 and Z5)**: respective bytes received in the previous frame *where*: 0DD[H] = Frm-1 Z3 and 0DF[H] = Frm-1 Z5
0E0			Internal Use - Do Not Access
0E1			**Frm-2 C2**: C2 Byte received two frames earlier
0E2			Internal Use - Do Not Access
0E3			**Frm-2 F2**: F2 Byte received two frames earlier
0E4			**C2 Expect**: value with which Rx Line C2 Location is compared for Signal Label Mismatch
0E5 - 0E7			**Frm-2 (Z3, Z4 and Z5)**: respective bytes received two frames earlier *where*: 0E5[H] = Frm-2 Z3 and 0E7[H] = Frm-2 Z5

STATUS AND CONTROL REGISTERS (0E8[H]-0FF[H]) - Read/Write

Address [H]	Name[1]	Mode[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E8	SR3[3]	R	RLFRI	RFE	B2EBER	B3EBER	RCPTR	C2MIS	C2UNEQ	RLOM
0E9	SR3	R/W	Same as 0E8[H] except does not reset on Read Write "1" to reset individual bits to "0"							
0EA	SR6[3]	R	RRDI-PSD	RRDI-PCD	RRDI-PPD	RPDI-P	J0MIS	Unused		
0EB	SR6[5]	R/W	Same as 0EA[H] except does not reset on Read Write "1" to reset individual bits to "0"							
0EC	SR3	R	Same as 0E8[H] except unlatched values							
0ED	SR6	R	Same as 0EA[H] except unlatched values							
0EE and 0EF			NOT EQUIPPED							
0F0	SR0[3]	R	RLOC	RNPTR	RAIS-P	RAIS-L	RLOP	RLOF	RSEF	RLOS
0F1	SR0[5]	R/W	Same as 0F0[H] except does not reset on Read Write "1" to reset individual bits to "0"							
0F2	SR1[3]	R	INT	RTNEW	RPNEW	RRDI-P	RRDI-L	RAPS	RBUSCOL	HWRST
0F3	SR1[5]	R/W	Same as 0F2[H] except does not reset on Read Write "1" to reset individual bits to "0"							
0F4	SR0	R	Same as 0F0[H] except unlatched values							
0F5	SR1	R	Same as 0F2[H] except unlatched values							
0F6	SR7[4]	R	RB3COF	RB2COF	RB1COF	RPFEBEOF	RLFEBEOF	RPMOVOF	RPJOF	LPJOF
0F7	SR9[4]	R	REG0	REG1	REG3	REG6	REG2	REG4	REG5	REG78
0F8	CR0	R/W	RRSD	RRLD	RRE1	RRE2	RPATH	RRAPS	RRPTR	TRLOOP
0F9	CR1	R/W	RRF1	RRC1	RRZ1	RRZ2	RRAIS	LTE	RRFRM	RRB1
0FA	CR2	R/W	STS1	PARA	HWINE	TRLRDI	ALTOW	TIEN	PIEN	-VE
0FB	CR3	R/W	RRFIEN	RFREN	RRFIFO	SBPE	DISRLAL	CNT16EN	RSWRES	TTOHEN
0FC	CR4	R/W	SRLAIS	B2XAIS	SRPAIS	B3XPAIS	RLOMPAIS	C2MPAIS	C2UPAIS	RLEAIS
0FD	CR5	R/W	DIEN	DATACOM	ENDCMPOH	DISPCKG	INVPCK	MBSEL1	MBSEL0	INVINT
0FE	CR6	R/W	B2FREN	RAMTSTEN	H4INT	J1SYNCEN	S1	S0	C1J1EN	OA
0FF	CR16	R/W	RETSEL	PRDISEL	B2MULT2	B2MULT1	B2MULT0	B3MULT2	B3MULT1	B3MULT0

Notes:

1. SRn = Status Register n, CRn = Control Register n. See following pages for descriptions of the register bits.
2. R = Read Only, R/W = Read/Write
3. Resets to all "0"s when Read; also resets the next higher address register to all “0”s when Read
4. Unlatched values only
5. Write “1” to Clear also resets corresponding bit of next lower address register to “0”.

TX TOH BYTES - Read/Write

Address [H]	Status Bits	Control Bits	Description
100 - 104			**Reserved**: Reserved for future use
105 - 110		Pin $\overline{\text{MBEI}}$ SPE	**Tx Term D1-D12**: information incoming at the Tx Terminal Port *where*: 105[H] = D1 and 110[H] = D12. These bytes are also available at the Output ISC Port.
111 and 112	TNPTR TLOP TAIS-P TCPTR	Pin $\overline{\text{MBEI}}$ SPE C1J1EN	**Tx Term H1 and H2**: information incoming at the Tx Terminal Port. These bytes are optionally internally processed as Pointer Bytes.
113		Pin $\overline{\text{MBEI}}$ SPE	**Tx Term H3**: information incoming at the Tx Terminal Port.
114		Pin $\overline{\text{MBEI}}$ SPE	**Tx Term B1**: information incoming at the Tx Terminal Port. This byte is optionally processed as a B1 Parity Byte with Parity Errors accumulated by the Tx B1 Error Counter. The Parity Calculation is even parity over all bytes in the frame. This byte is also available at the Output ISC Port.
115		Pin $\overline{\text{MBEI}}$ SPE	**Tx Term B2**: information incoming at the Tx Terminal Port. This byte is optionally processed as a B2 Parity Byte with Parity Errors accumulated by the Tx B2 Error Counter. The Parity Calculation is even parity over all bytes in the frame except the 9 Section Overhead Bytes. This byte is also available at the Output ISC Port.
116 and 117	TFE TSEF TLOF	Pin $\overline{\text{MBEI}}$ SPE C1J1EN	**Tx Term A1 and A2**: information incoming at the Tx Terminal Port. These bytes are optionally processed as Framing Bytes.
118	TTE1	Pin $\overline{\text{MBEI}}$ SPE TE2A	**Tx Term E1**: information incoming at the Tx Terminal Port. This byte can be optionally used for AIS communication between PHAST-1s, SOT-1s and/or SOT-1Es and is also available at the Output ISC Port.
119 - 11F	TAIS_L	Pin $\overline{\text{MBEI}}$ SPE	**Tx Term E2, Z1, Z2, C1, F1, K1 and K2**: information incoming at the Tx Terminal Port *where*: 119[H] = E2 and 11F[H] = K2. These bytes are also available at the Output ISC Port.
120 - 122			NOT EQUIPPED
123 and 124			Internal Use - Do Not Access
125 - 127		TRSD TXSDEXT SDCCEN OA	**Tx Insert D1-D3**: Section DCC Bytes - information to be multiplexed into Tx Line Port Data if insertion option is enabled. 125[H] = D1 and 127[H] = D3. These locations may be written by the µPro, or contain information input at the Tx Section DCC Port or optionally at the Tx OA/TOH Port.
128 - 130		TRLD TXLDEXT LDCCEN OA	**Tx Insert D4-D12**: Line DCC Bytes - information to be multiplexed into Tx Line Port Data if insertion option is enabled. 128[H] = D4 and 130[H] = D12. These locations may be written by the µPro, or contain information input at the Tx Section DCC Port or optionally at the Tx OA/TOH Port.

Address [H]	Status Bits	Control Bits	Description
131 and 132			**Reserved**: Reserved for future use
133		C1J1EN TXRTM	**Tx Insert H3**: Pointer Action Byte - Tx Line Port H3 Byte value when Tx Re-timing is enabled and a Pointer Decrement is not performed. This Location can only be accessed by the µPro.
134			Internal Use - Do Not Access
135			Internal Use - Do Not Access
136 and 137		TRFRM TFRMEXT OA	**Tx Insert A1 and A2**: Framing Bytes - information to be multiplexed into Tx Line Port Data if insertion option is enabled. These locations may be written by the µPro, or contain the internally generated values, or optionally contain information input at the Tx OA/TOH Port.
138		TRE1 TXE1EXT	**Tx Insert E1**: Section Order Wire Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx OA/TOH Port.
139		TRE2 TXE2EXT	**Tx Insert E2**: Line Order Wire Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx OA/TOH Port.
13A		TRZ1 TXZ1EXT OA	**Tx Insert Z1**: 1^{ST} Growth Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or optionally contain information input at the Tx OA/TOH Port.
13B		TRZ2 TXZ2EXT OA TLFEBEEN	**Tx Insert Z2**: 2^{ND} Growth Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or optionally contain information input at the Tx OA/TOH Port. If the Line FEBE option is enabled, Bits 5-8 (Transmission Convention) will be overwritten by the FEBE-L Value.
13C		J0EN1 TRC1 TXC1EXT OA	**Tx Insert C1**: C1 Byte/Single Byte J0 - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or optionally contain information input at the Tx OA/TOH Port.
13D		TRF1 TXF1EXT OA	**Tx Insert F1**: Section User Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or optionally contain information input at the Tx OA/TOH Port.
13E and 13F		TRAPS EXAPS TRLRDI	**Tx Insert K1 and K2**: APS Bytes - information to be multiplexed into Tx Line Port Data if insertion option is enabled. These locations may be written by the µPro or contain information input at the Tx OA/TOH Port.
140 - 143			Internal Use - Do Not Access
144			NOT EQUIPPED

Address [H]	Status Bits	Control Bits	Description
145	TPMOVOF	C1J1EN TSWRES	**Tx Inc/Dec Count**: two - 4-Bit Counters. Bits 7-4 = accumulate Pointer Increments incoming at the Tx Terminal Port. Bits 3-0 accumulate Pointer Decrements incoming at the Tx Terminal Port. Both Counters are Saturating and Clear on Read. Counting is inhibited upon declaration of TLOC, TLOS, TLOF, or TAIS-L. or by C1J1EN.
146		TSWRES INHTB1C	**Tx B1 Error Count**: count of B1 Errors that are incoming at the Tx Terminal Port. This is an 8-Bit, Clear on Read, Roll Over Counter. Counting is inhibited upon declaration of TLOC, TLOS, or TLOF, or INHTB1C.
147		TSWRES INHTB2C	**Tx B2 Error Count**: count of B2 Errors that are incoming at the Tx Terminal Port. This is an 8-Bit, Clear on Read, Roll Over Counter. Counting is inhibited upon declaration of TLOC, TLOS, TLOF, or TAIS-L or INHTB2C.
148			NOT EQUIPPED
149		TRERR	**Tx B1 Error Mask**: the contents of this location are 'exclusive-OR gated, bit by bit, with the B1 Byte output at the Tx Line Port.
14A - 150			NOT EQUIPPED
151		TRERR	**Tx B2 Error Mask**: the contents of this location are exclusive-OR gated, bit by bit, with the B2 Byte output at the Tx Line Port.
152 - 17F			NOT EQUIPPED

TX POH BYTES - Read/Write

Address [H]	Status Bits	Control Bits	Description
180 - 1BF		J0RWEN J0EN0 J0EN1 TRC1 TXC1EXT OA TPATH TJ1EXT J1SYNCEN	**Tx Insert J0/J1**: Line or Path Trace Bytes - information to be multiplexed into Tx Line Port Data if insertion option is enabled or external data input at Tx OA/TOH Port, Tx Terminal Port, or Tx POH Port. J0 Processing These locations are only used for J0 Messages if J0EN1 = "1". They may be written by the µPro or optionally contain information input at the Tx OA/TOH Port. If the Tx OA/TOH Port option is enabled and J0EN(1,0) = "11" the byte immediately following an ASCII <CR> and <LF>, will be stored in Location 180[H]. J1 Processing These locations may be written by the µPro or contain information input at either the Tx Terminal Port or the Tx POH Port. If either external option is enabled and J1SYNCEN = "1", the byte immediately following an ASCII <CR> and <LF> will be stored in Location 180[H].
1C0			**Tx Term B3**: information incoming at the Tx Terminal Port. This byte is optionally processed as a B3 Parity Byte with Parity Errors accumulated by the Tx B3 Error Counter. The Parity Calculation is even parity over all SPE Bytes (the 27 TOH Bytes are excluded).

Address [H]	Status Bits	Control Bits	Description
1C1 - 1C7			**Tx Term C2, G1, F2, H4, Z3, Z4 and Z5**: information incoming at the Tx Terminal Port *where*: 1C1[H] = C2 and 1C7[H] = Z5
1C8			Internal Use - Do Not Access
1C9		TPATH TC2EXT	**Tx Insert C2**: Signal Label Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx POH Port.
1CA		TPATH TG1EXT TPFEBEEN TPRDIEN	**Tx Insert G1**: Path Status Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx POH Port. Bits 1-4 and/or Bits 5, 6 and 7 (Transmission Convention) may be overwritten by FEBE-P and/or RDI-P information.
1CB		TPATH TF2EXT	**Tx Insert F2**: Path User Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx POH Port.
1CC		TPATH H4INT TXH4INS	**Tx Insert H4**: Multiframe Indicator Byte - µPro information to be multiplexed into Tx Line Port Data if insertion option is enabled. Bits 7 and 8 (Transmission Convention) may be overwritten by the internal, 2-Bit, Modulo 4, Tx Multiframe Counter.
1CD		TPATH TZ3EXT	**Tx Insert Z3**: 3^{RD} Growth Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx POH Port.
1CE		TPATH TZ4EXT	**Tx Insert Z4**: 4^{TH} Growth Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx POH Port.
1CF		TPATH TZ5EXT	**Tx Insert Z5**: 5^{TH} Growth Byte - information to be multiplexed into Tx Line Port Data if insertion option is enabled. This location may be written by the µPro or contain information input at the Tx POH Port.
1D0		TRERR	**Tx B3 Error Mask**: the contents of this location are exclusive-OR gated, bit by bit, with the B3 Byte output at the Tx Line Port. If the B3 Byte is not calculated internally then the number of generated errors will be doubled.
1D1 - 1D3			NOT EQUIPPED
1D4		TSWRES TPATH	**Tx B3 Error Count**: count of B3 Errors that are incoming at the Tx Terminal Port. This is an 8-Bit, Clear on Read, Roll Over Counter. Counting is inhibited upon declaration of TLOC, TLOS, TLOF, TAIS-L, TAIS-P or TLOP or if TPATH = "1".
1D5 - 1DA			NOT EQUIPPED

STATUS AND CONTROL REGISTERS (1DB[H]-1FF[H]) - Read/Write

Address [H]	Name[1]	Mode[2]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1DB	CR19	R/W	Reserved	Reserved	TPRDISD	TPRDICD	TPRDIPD	B3PRDISD	B3PRDICD	TOHPRDISD
1DC	CR18	R/W	J0RWEN	J0MLRDI	J0MLAIS	J0EN1	J0EN0	TMBSEL1	TMBSEL0	CHPRES
1DD	CR17	R/W	SDCCEN	LDCCEN	STLAIS	TEST1	TEST2	LINLOOP	DISTB2R	TPRDI20
1DE	CR7	R/W	TIDL	IDLSEL	TPFEBEEN	TPRDIEN	C2MPRDI	C2UPRDI	ENFSTUA	ENLSTUA
1DF	CR15	R/W	TXLDEXT	TSWRES	TTEAIS	TLFEBEEN	INHTB1C	INHTB2C	STLRDI	B2ELRDI
1E0 - 1E7			NOT EQUIPPED							
1E8	SR5[3]	R	TBPE	TFE	TCPTR	TTE1	TRCOFA	DRCOFA	LOTR	TFIFOE
1E9	SR5[5]	R/W	Same as 1E8[H] except does not reset on Read Write "1" to reset individual bits to "0"							
1EA and 1EB			NOT EQUIPPED							
1EC	SR5	R	Same as 1E8[H] except unlatched values							
1ED - 1EF			NOT EQUIPPED							
1F0	SR2[3]	R	TLOC	TNPTR	TAIS-P	TAIS-L	TLOP	TLOF	TSEF	TLOS
1F1	SR2[5]	R/W	Same as 1F0[H] except does not reset on Read Write "1" to reset individual bits to "0"							
1F2	SR4[3]	R	RRCOFA	LORR	RFIFOE	RLE1	TAISV	LORG	RGRDI-P	RGRDI-L
1F3	SR4[5]	R/W	Same as 1F2[H] except does not reset on Read Write "1" to reset individual bits to "0"							
1F4	SR2	R	Same as 1F0[H] except unlatched values							
1F5	SR4	R	Same as 1F2[H] except unlatched values							
1F6	SR8[4]	R	Reserved	Reserved	Reserved	TPMOVOF	RPAISC	RLAISC	TPAISC	TLAISC
1F7			NOT EQUIPPED							
1F8	CR8	R/W	TRSD	TRLD	TRE1	TRE2	TPATH	TRAPS	EXAPS	RTLOOP
1F9	CR9	R/W	TRF1	TRC1	TRZ1	TRZ2	TRAIS	PTE	RXRTM	RRB2
1FA	CR10	R/W	SPE	TCLK	RCLK	DISTBPE	TXRTM	DETSEL	INC	DEC
1FB	CR11	R/W	TRFRM	TRERR	STPAIS	RING	RE2A	RA2E	TE2A	TA2E
1FC	CR12	R/W	TFREN	RTFIFO	DISTLAIS	LPAISEN	LPAISSEL	TFRIEN	DFRIEN	TDDLY
1FD	CR13	R/W	TJ1EXT	TC2EXT	TG1EXT	TF2EXT	TXH4INS	TZ3EXT	TZ4EXT	TZ5EXT
1FE	CR14	R/W	TFRMEXT	TXC1EXT	TXE1EXT	TXF1EXT	TXSDEXT	TXZ1EXT	TXZ2EXT	TXE2EXT
1FF	HIBYTE	R/W	Most Significant Byte for 16-Bit Counters							

Notes:
1. SRn = Status Register n, CRn = Control Register n. See following pages for descriptions of the register bits.
2. R = Read Only, R/W = Read/Write
3. Resets to all "0"s when Read; also resets the next higher address register to all “0”s when Read
4. Unlatched values only
5. Write “1” to Clear also resets corresponding bit of next lower address register to “0”.

STATUS REGISTER DESCRIPTIONS

STATUS REGISTER 0

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F0 0F1 0F4	7	RLOC	**Rx Loss of Clock**: 200 - 2000 ns without transitions at RLCI	Any Transition at RLCI	if TRLOOP = "1" Looped Clock is monitored
	6	RNPTR	**Rx New Pointer**: New Pointer due to NDF or receipt of three, consecutive, valid, new pointers	No Exit Conditions - Latched Values are reset by µPro Read of 0F0[H] or Writing "1" to this bit in 0F1[H].	inhibited if RLOC, RLOS, RLOF or RAIS-L is declared 0F4, see Note 2.
	5	RAIS-P	**Rx AIS-P**: 3 consecutive H1 and H2 bytes with all "1"	receipt of NDF and Valid Pointer or three valid, consecutive, stable pointers	inhibited if RLOC, RLOS, RLOF or RAIS-L is declared
	4	RAIS-L	**Rx AIS-L**: K2 Byte bits 6, 7 and 8 = "111" for 5 consecutive frames	K2 Byte bits 6, 7 and 8 ≠ "111" for 5 consecutive frames	inhibited if RLOC, RLOS or RLOF is declared or if DISRLAL = "1"
	3	RLOP	**Rx Loss of Pointer**: 8 consecutive frames of NDF or Invalid Pointer	3 consecutive frames of Valid Pointer or AIS indicator	inhibited if RLOC, RLOS, RLOF or RAIS-L is declared
	2	RLOF	**Rx Loss of Frame**: RSEF persists for 3 ms	1 ms without RSEF	inhibited if RLOC or RLOS is declared
	1	RSEF	**Rx Severely Errored Frame**: RFE Persists for 4 consecutive frames	2 consecutive frames without RFE or STS1 = "0" and $\overline{\text{RFRI}}$ Valid followed by A1 and A2 as expected	inhibited if RLOC or RLOS is declared
	0	RLOS	**Rx Loss of Signal**: STS1 = "1": $\overline{\text{RXLOS}}$ pin Low or 720-1440 Bit Times without transitions at RLDI STS1 = "0": $\overline{\text{RXLOS}}$ pin Low or 6480 - 12960 Bit Times without transitions at RLDI	$\overline{\text{RXLOS}}$ pin High, and any transitions at RLDI	inhibited if RLOC is declared If TRLOOP = "1" Looped Data is monitored See Note 1.

Notes:
1. When Internally generated ($\overline{\text{RXLOS}}$ pin is High), this is a device level alarm. It is not the Physical Layer LOS.
2. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.

STATUS REGISTER 1

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F2 0F3 0F5	7	INT	**Interrupt**: any event that causes a µPro Interrupt	No Exit Conditions - Latched Values are reset by µPro Read of 0F2[H] or Writing "1" to this bit in 0F3[H].	0F5, see Note 2.
	6	RTNEW	**Rx TOH New**: any new debounced value of C1, F1, K1, K2, Z1 or Z2	No Exit Conditions - Latched Values are reset by µPro Read of 0F2[H] or Writing "1" to this bit in 0F3[H].	inhibited if RLOC, RLOS or RLOF is declared or if DISRLAL = "1" 0F5, see Note 2.
	5	RPNEW	**Rx POH New**: any new debounced value of C2, F2, Z3, Z4 or Z5	No Exit Conditions - Latched Values are reset by µPro Read of 0F2[H] or Writing "1" to this bit in 0F3[H].	inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared 0F5, see Note 2.
	4	RRDI-P	**Rx RDI-P**: PRDISEL = "0" and G1, Bits 5-7 = "100" or "111" for 10 consecutive Frames	PRDISEL = "0" and G1, Bits 5-7≠ "100" or "111" for 10 consecutive Frames	note 1 inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared
			PRDISEL = "1" and G1, Bits 5-7 = "100" or "111" for 5 consecutive Frames	PRDISEL = "1" and G1, Bits 5-7≠ "100" or "111" for 5 consecutive Frames	
	3	RRDI-L	**Rx RDI-L**: K2 Byte bits 6, 7 and 8 = "110" for 5 consecutive frames	K2 Byte bits 6, 7 and 8 ≠ "110" for 5 consecutive frames	inhibited if RLOC, RLOS, or RLOF is declared or if DISRLAL = "1"
	2	RAPS	**Rx APS Fail**: 12 frame sliding window that does not contain 3 consecutive, identical pairs of K1 and K2 Bytes	reception of 3 consecutive, identical pairs of K1 and K2 Bytes	inhibited if RLOC, RLOS, or RLOF is declared or if DISRLAL = "1"
	1	RBUSCOL	**Rx Terminal Bus Collision**: $\overline{\text{TPDVO}}$ Low and either $\overline{\text{TPDV0}}$ or $\overline{\text{TPDV1}}$ Low at the clock edge upon which data is output.	$\overline{\text{TPDVO}}$ Low and both $\overline{\text{TPDV0}}$ and $\overline{\text{TPDV1}}$ High at the clock edge upon which data is output.	0F5, see Note 2.
	0	HWRST	**Hardware Reset**: Hardware reset via pin $\overline{\text{RST}}$	No Exit Conditions - Latched Values are reset by µPro Read of 0F2[H] or Writing "1" to this bit in 0F3[H].	0F5, see Note 2.

Notes:
1. This is the alarm that is used to report Single Bit RDI-P. It is retained for backwards compatibility.
2. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.

STATUS REGISTER 2

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F0 1F1 1F4	7	TLOC	**Tx Loss of Clock**: either SPE-only Mode selected or SONET Mode selected and PARA = "0" and 200 - 2000 ns without transitions at TTCI/O	either Datacom Mode selected or any transition at the enabled pin (TTCI/O or TPCI/O).	
			SONET Mode selected and PARA = "1" and 200 - 2000 ns without transitions at TPCI/O		
	6	TNPTR	**Tx New Pointer**: New Pointer due to NDF or receipt of three, consecutive, valid new pointers	No Exit Conditions - Latched Values are reset by µPro Read of 1F0[H] or Writing "1" to this bit in 1F1[H].	inhibited if TLOC, TLOS, TLOF or TAIS-L is declared or if C1J1EN = "1" 1F4, see Note 1.
	5	TAIS-P	**Tx AIS-P**: 3 consecutive H1 and H2 bytes with all "1" at the Tx Terminal Port	receipt of NDF and Valid Pointer or three valid, consecutive, stable pointers	inhibited if TLOC, TLOS, TLOF or TAIS-L is declared or if C1J1EN = "1"
	4	TAIS-L	**Tx AIS-L**: K2 Byte bits 6, 7 and 8 = "111" for 5 consecutive frames at the Tx Terminal Port	K2 Byte bits 6, 7 and 8 ≠ "111" for 5 consecutive frames	inhibited if TLOC, TLOS or TLOF is declared or if DISTLAIS = "1"
	3	TLOP	**Tx Loss of Pointer**: 8 consecutive frames of NDF or Invalid Pointer at the Tx Terminal Port	3 consecutive frames of Valid Pointer or AIS indicator	inhibited if TLOC, TLOS, TLOF or TAIS-L is declared or if C1J1EN = "1"
	2	TLOF	**Tx Loss of Frame**: TSEF persists for 3 ms at the Tx Terminal Port	1 ms without TSEF	inhibited if TLOC or TLOS is declared or if C1J1EN = "1"
	1	TSEF	**Tx Severely Errored Frame**: TFE Persists for 4 consecutive frames at the Tx Terminal Port	2 consecutive frames without TFE	inhibited if TLOC or TLOS is declared or if C1J1EN = "1"

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F0 1F1 1F4 (cont.)	0	TLOS	**Tx Loss of Signal**: SPE-only Mode selected and 2-4 Frames without transitions on TSPEI/O or TSYNI/O	SPE-only Mode selected and any transitions on failed input	inhibited if TLOC is declared
			SONET Mode selected and: 1. If C1J1EN = "0" and PARA = "0", then 6480-12960 bit times without transitions on TTDI 2. If C1J1EN = "0" and PARA = "1", then 810-1620 byte times without transitions on TPDI0 - TPDI7 or 16 or more parity error occurrences in a fixed 90 byte window 3. If C1J1EN = "1" and PARA = "0" then 2-4 Frames without transitions on TSPEI/O or TSYNI/O 4. If C1J1EN = "1" and PARA = "1" then 2-4 Frames without transitions on TSPEI/O or TSYNI/O or 16 or more parity error occurrences in a fixed 90 byte window	SONET Mode selected and: if 1. or 2. then either C1J1EN = "1" or PARA = "0" and any transition on failed inputs or PARA = "1" and no parity error occurrences in a fixed 90 byte window and any transition on failed inputs. if 3. or 4. then either C1J1EN = "0" or PARA = "0" and any transitions on failed inputs or PARA = "1" and no parity error occurrences in a fixed 90 byte window and any transition on failed inputs	
			Datacom Mode selected and 16 parity error occurrences in a fixed 90 byte window.	Datacom Mode Selected and no parity error occurrences in a fixed 90 byte window.	inhibited if DISTBPE = "1"

Note 1: This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.

STATUS REGISTER 3

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0E8 0E9 0EC	7	RLFRI	**Rx Loss of Frame Input**: 8 frames without transitions on $\overline{\text{RFRI}}$	any transitions on $\overline{\text{RFRI}}$ pin	inhibited if RLOC or RLOS is declared or TRLOOP = "1" or STS1 = "1"
	6	RFE	**Rx Frame Error**: one or more A1 or A2 bits in error	one pair of A1 and A2 bytes received without errors	inhibited if RLOC or RLOS is declared
	5	B2EBER	**B2 Excessive BER**: B2 Error Rate exceeds 1 in 10^3	B2 Error Rate less than 1 in 10^3	inhibited if RLOC, RLOS, RLOF or RAIS-L is declared or if DISRLAL = "1" See note 4.

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0E8 0E9 0EC	4	B3EBER	**B3 Excessive BER**: B3 Error Rate exceeds 1 in 10^3	B3 Error Rate less than 1 in 10^3	inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared See note 4.
	3	RCPTR	**Rx Concatenated Pointer**: RLOP declared and NDF Bits = "1001" SS Bits = "00" I Bits = "1" D Bits = "1"	RLOP not declared or concatenation indication not received	inhibited if RLOC, RLOS, RLOF or RAIS-L is declared
	2	C2MIS	**C2 Mismatch**: any of the combinations of Expect C2 Register and 5 consecutive Rx C2 Bytes that are listed below C2 REG.[H] — Rx C2[H] 00 — 01-FD 01 — 00 02 — 00, 03-E0, FC, FD-FF 03 — 00, 02, 04-E0, FC, FD-FF 04 — 00, 02, 03, 05-FB, FD-FF 05 ≤ x ≤ 11 — 00,02-04, 05-11 excluding x, 12-FF 13 — 00, 02-12, 14-FB, FD-FF 14 — 00, 02-13, 15-FB, FD-FF 15 — 00, 02-14, 16-FB, FD-FF 16 ≤ x ≤ E0 — 00, 02-15, 16-E0 excluding x, E1-FF	any of the combinations of Expect C2 Register and 5 consecutive Received C2 Bytes that are not listed as an Enter condition	inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared See notes 1, 2 and 3.
	1	C2UNEQ	**C2 Unequipped**: 5 consecutive Received C2 Bytes = 00[H]	5 consecutive Received C2 Bytes≠ 00[H]	inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared See notes 1 and 2.
	0	RLOM	**Rx Loss of Multiframe**: 2 successive frames in which the Received H4 Value does not match expected sequence, which is described for the exit condition.	2 successive frames in which the value of the second H4 byte is equal to the first H4 value +1, modulo 4	inhibited if RLOC, RLOS, RLOF, RAIS-L, RAIS-P or RLOP is declared or H4INT = "0"

See notes on next page

Notes
1: For Bellcore GR-253-CORE issue 2 compliance, if C2 REG.[H] = 00 also set control bits C2UPRDI and C2MPRDI (bits 3 and 2 in control register 7) to 0. The local microprocessor should also ignore the unequipped and mismatch alarms.
2: When the received C2[H] value is 00 both C2MIS and C2UNEQ alarms are generated. For Bellcore GR-253-CORE issue 2 compliance only, C2UNEQ should be reported by the local microprocessor.
3: When the expected signal label in C2 REG.[H] = 02 or 03, values of received C2[H] from E1 through FB do not generate a C2MIS alarm; they indicate the number of VT's with payload defects (see RPDI-P in Status Register 6).
4: B2EBER and B3EBER thresholds are set as described in the operations section under "Rx B2 processing" and "Rx B3 processing".

STATUS REGISTER 4

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F2 1F3 1F5	7	RRCOFA	**Rx Reference Change of Frame Alignment**: any RRFI/$\overline{\text{RRFI}}$ pulse that varies in frame position from the previous pulse.	No Exit Conditions - Latched Values are reset by µPro Read of 1F2[H] or Writing "1" to this bit in 1F3[H].	1F5, see Note 1.
	6	LORR	**Loss of Rx Reference**: 200 - 2000 ns without transitions at RRCI or RRFIEN = "1" and 8 frames without transitions on RRFI.	Any transitions on the enabled pins.	inhibited if RCLK = "0"
	5	RFIFOE	**Rx FIFO Error**: Receive FIFO Overflow or Underflow when Rx re-timing is enabled as shown below: SPE Mode / RCLK / RXRTM Selected - - Not Selected 1 - Not Selected 0 0	No Exit Conditions - Latched Values are reset by µPro Read of 1F2[H] or Writing "1" to this bit in 1F3[H].	inhibited if SPE = "0", RCLK = "0" and RXRTM = "1" 1F5, see Note 2.
	4	RLE1	**Rx Line E1 Alarm**: 5 or more bits Set to "1" in the Rx Line E1 Byte.	fewer than 5 bits in the Rx Line E1 Byte set to "1".	inhibited if RLOC, RLOS or RLOF is declared or RE2A = "0"
	3	TAISV	**Tx AIS Valid**: pin $\overline{\text{TAIS}}$ at the Low Level.	pin $\overline{\text{TAIS}}$ at the High Level.	
	2	LORG	**Loss of Ring Port**: 250 to 375 µs with no Ring Port Framing Pattern ("1111111110") on RGDI.	Ring Port Frame Pattern detected.	inhibited if LOTR = "1"
	1	RGRDI-P	**Ring Port RDI-P**: PRDIH and/or PRDIL Bits = "1" in Ring Port data on RGDI.	Both PRDIH and PRDIL Bits = "0" in Ring Port data on RGDI.	inhibited if LOTR = "1", LORG = "1" or RING = "0".
	0	RGRDI-L	**Ring Port RDI-L**: Ring Port LRDI Bit = "1" in Ring Port data on RGDI.	LRDI Bit = "0" in Ring Port data on RGDI.	inhibited if LOTR = "1", LORG = "1" or RING = "0".

Notes:
1. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.
2. If Automatic Rx FIFO Reset is enabled (RFREN = "1") this is a short duration event and the µPro may not be able to read the unlatched value.

STATUS REGISTER 5

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1E8 1E9 1EC	7	TBPE	**Tx Bus Parity Error**: any parity error detected at Tx Terminal Input	no parity error detected at Tx Terminal Input	notes 1, 2 1EC, see Note 3.
	6	TFE	**Tx Frame Error**: one or more A1 or A2 bits in error at Tx Terminal Interface	one pair of A1 and A2 bytes received without errors at Tx Terminal Interface	inhibited if TLOC or TLOS is declared or C1J1EN = "1"
	5	TCPTR	**Tx Concatenated Pointer**: TLOP declared and NDF Bits = "1001" SS Bits = "00" I Bits = "1" D Bits = "1"	TLOP not declared or concatenation indication not received	inhibited if TLOC, TLOS, TLOF or TAIS-L is declared or if C1J1EN = "1"
	4	TTE1	**Tx Terminal E1 Alarm**: 5 or more bits Set to "1" in the E1 Byte at the Tx Terminal Port	fewer than 5 bits set to "1" in the E1 Byte at the Tx Terminal Port	inhibited if TLOC, TLOS or TLOF is declared or TE2A = "0"
	3	TRCOFA	**Tx Reference Change of Frame Alignment**: any $\overline{\text{TFRI}}$ pulse that varies in frame position from the previous pulse	No Exit Conditions - Latched Values are reset by µPro Read of 1E8[H] or Writing "1" to this bit in 1E9[H].	1EC, see Note 3.
	2	DRCOFA	**Datacom Reference Change of Frame Alignment**: any DFRI pulse that varies in frame position from the previous pulse	No Exit Conditions - Latched Values are reset by µPro Read of 1E8[H] or Writing "1" to this bit in 1E9[H].	Valid only in Datacom Mode. 1EC, see Note 3.
	1	LOTR	**Loss of Tx Reference**: SPE-only or SONET Modes Selected; TCLK = "1" and either; 200 - 2000 ns without transitions at TLCI or TFRIEN = "1" and 8 frames without transitions on $\overline{\text{TFRI}}$	any transitions on enabled pins listed for Enter conditions	
			Datacom Mode selected; RTLOOP = "0" or TTOHEN = "1" and either; 200 - 2000 ns without transitions at DRCI or DFRIEN = "1" and 8 frames without transitions on DFRI		

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1E8 1E9 1EC (cont.)	0	TFIFOE	**Tx FIFO Error**: Transmit FIFO Overflow or Underflow when Tx re-timing is enabled as shown below ↓ ↓ ↓ ↓ SPE-only Mode 0 0 0 1 Datacom Mode 0 0 1 - C1J1EN 0 1 - - TXRTM 1 - 1 -	No Exit Conditions - Latched Values are reset by µPro Read of 1E8[H] or Writing "1" to this bit in 1E9[H].	inhibited when: ↓ ↓ SPE-only 0 0 Datacom 0 1 C1J1EN 0 - TXRTM 0 0 1EC, see Note 4.

Notes:
1. This alarm is inhibited in all serial modes or if DISTBPE = "1".
2. If SONET Mode is selected and C1J1EN = "1", Parity is checked over TPDI0-TPDI7, TSYNI/0 and TSPEI/O. If C1J1EN = "0" or Datacom Mode is selected, parity is checked over TPDI0-TPDI7.
3. This is a short duration event (« 1 Frame). The µPro may not be able to read the unlatched value.
4. If Automatic Tx FIFO Reset is enabled (TFREN = "1") this is a short duration event and the µPro may not be able to read the unlatched value.

STATUS REGISTER 6

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0EA 0EB 0ED	7	RRDI-PSD	**Rx RDI-P, Signal Defect**: PRDISEL = "0" and G1, Bits 5-7 = "101" for 10 consecutive Frames	PRDISEL = "0" and G1, Bits 5-7 ≠ "101" for 10 consecutive Frames	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared
			PRDISEL = "1" and G1, Bits 5-7 = "101" for 5 consecutive Frames	PRDISEL = "1" and G1, Bits 5-7 ≠ "101" for 5 consecutive Frames	
	6	RRDI-PCD	**Rx RDI-P, Connectivity Defect**: PRDISEL = "0" and G1, Bits 5-7 = "110" for 10 consecutive Frames	PRDISEL = "0" and G1, Bits 5-7 ≠ "110" for 10 consecutive Frames	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared
			PRDISEL = "1" and G1, Bits 5-7 = "110" for 5 consecutive Frames	PRDISEL = "1" and G1, Bits 5-7 ≠ "110" for 5 consecutive Frames	
	5	RRDI-PPD	**Rx RDI-P, Payload Defect**: PRDISEL = "0" and G1, Bits 5-7 = "010" for 10 consecutive Frames	PRDISEL = "0" and G1, Bits 5-7 ≠ "010" for 10 consecutive Frames	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared
			PRDISEL = "1" and G1, Bits 5-7 = "010" for 5 consecutive Frames	PRDISEL = "1" and G1, Bits 5-7 ≠ "010" for 5 consecutive Frames	
	4	RPDI-P	**Rx PDI-P**: Rx C2 Byte equal to any constant value in the range E1[H] through FC[H], inclusive, for 5 consecutive frames	Rx C2 Byte not equal to any constant value in the range E1[H] through FC[H], inclusive, for 5 consecutive frames	Inhibited if RLOC, RLOS, RLOF, RAIS-L, RLOP or RAIS-P is declared See note 1.
	3	J0MIS	**J0 Mismatch**: J0EN(1,0) = "01" and Rx J0 Byte ≠ J0 Expect Register in 5 consecutive Frames	either J0EN(1,0) ≠ "01" or J0EN(1,0) = "01" and Rx J0 Byte = J0 Expect Register in 5 consecutive Frames	inhibited if RLOC, RLOS or RLOF is declared
	2-0	Unused			

Note:
1. See C2MIS in Status Register 3, Bit 2.

STATUS REGISTER 7

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F6	7	RB3COF	**Rx B3 Counter Overflow**: Overflow of Rx B3 Counter	µPro Read of Rx B3 Counter	
	6	RB2COF	**Rx B2 Counter Overflow**: Overflow of Rx B2 Counter	µPro Read of Rx B2 Counter	
	5	RB1COF	**Rx B1 Counter Overflow**: Overflow of Rx B1 Counter	µPro Read of Rx B1 Counter	
	4	RPFEBEOF	**Rx Path FEBE Counter Overflow**: Overflow of Rx FEBE-P Counter	µPro Read of Rx FEBE-P Counter	
	3	RLFEBEOF	**Rx Line FEBE Counter Overflow**: Overflow of Rx FEBE-L Counter	µPro Read of Rx FEBE-L Counter	
	2	RPMOVOF	**Rx Pointer Movement Counters Overflow**: Overflow of either the Rx Pointer Increment or Decrement Counters	µPro Read of the counter which has overflowed	
	1	RPJOF	**Rx Pointer Justification Counter Overflow**: Overflow of the Rx Pointer Justification Counter	µPro Read of the Rx Pointer Justification Counter	
	0	LPJOF	**Local Pointer Justification Counter Overflow**: Overflow of the Local Pointer Justification Counter	µPro Read of the Local Pointer Justification Counter	

STATUS REGISTER 8

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
1F6	7-5	Reserved			
	4	TPMOVOF	**Tx Pointer Movement Counters Overflow**: Overflow of either the Tx Pointer Increment or Decrement Counters	µPro Read of the counter which has overflowed	
	3	RPAISC	**Rx Path AIS Conditions**: Rx Line conditions are such that: 1. AIS-P will be inserted at the Rx Terminal Port if RRAIS = "1" 2. An E1 Alarm will be output at the Rx Terminal Port if RA2E = "1"	No Rx Line conditions exist that would cause an AIS-P or E1 Alarm to be output at the Rx Terminal Port If the functions were enabled.	See RRAIS and RA2E.
	2	RLAISC	**Rx Line AIS Conditions**: Rx Line conditions are such that: 1. AIS-L will be inserted at the Rx Terminal Port if RRAIS = "1" 2. An E1 Alarm will be output at the Rx Terminal Port if RA2E = "1"	No Rx Line conditions exist that would cause an AIS-L or E1 Alarm to be output at the Rx Terminal Port If the functions were enabled.	See RRAIS and RA2E.
	1	TPAISC	**Tx Path AIS Conditions**: Tx Terminal conditions are such that: 1. AIS-P will be inserted on the Tx Line if TRAIS = "1" 2. An E1 Alarm will be output on the Tx Line if TA2E = "1"	No Tx Terminal conditions exist that would cause an AIS-P or E1 Alarm to be output on the Tx Line if the functions were enabled.	See TRAIS and TA2E.
	0	TLAISC	**Tx Line AIS Conditions**: Tx Terminal conditions are such that: 1. AIS-L will be inserted on the Tx Line if TRAIS = "1" 2. An E1 Alarm will be output on the Tx Line if TA2E = "1"	No Tx Terminal conditions exist that would cause an AIS-L or E1 Alarm to be output on the Tx Line if the functions were enabled.	See TRAIS and TA2E.

STATUS REGISTER 9

Address [H]	Bit	Symbol	Conditions		Comments
			Enter	Exit	
0F7	7	REG0	**Register 0 Status Set**: One or more latched bits set to "1" in Status Register 0	All latched Bits = "0" in Status Register 0	0F0[H] 0F1[H]
	6	REG1	**Register 1 Status Set**: One or more latched bits set to "1" in Status Register 1.	All latched Bits = "0" in Status Register 1	0F2[H] 0F3[H]
	5	REG3	**Register 3 Status Set**: One or more latched bits set to "1" in Status Register 3.	All latched Bits = "0" in Status Register 3	0E8[H] 0E9[H]
	4	REG6	**Register 6 Status Set**: One or more latched bits set to "1" in Status Register 6.	All latched Bits = "0" in Status Register 6	0EA[H] 0EB[H]
	3	REG2	**Register 2 Status Set**: One or more latched bits set to "1" in Status Register 2.	All latched Bits = "0" in Status Register 2	1F0[H] 1F1[H]
	2	REG4	**Register 4 Status Set**: One or more latched bits set to "1" in Status Register 4.	All latched Bits = "0" in Status Register 4	1F2[H] 1F3[H]
	1	REG5	**Register 5 Status Set**: One or more latched bits set to "1" in Status Register 5.	All latched Bits = "0" in Status Register 5	1E8[H] 1E9[H]
	0	REG78	**Registers 7 or 8 Status Set**: One or more bits in Status Register 7 or any of Bits 7-4 in Status Register 8 = "1".	All bits in Status Register 7 and all of Bits 7-4 in Status Register 8 = "0".	0F6[H] 1F6[H], Bits 7-4

CONTROL REGISTER DESCRIPTIONS

CONTROL REGISTER 0

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F8	7	RRSD	**Rx Terminal Port Section Datacom:** outgoing Terminal Data contains D1-D3 Bytes from Rx TOH Insert RAM Locations.	outgoing Terminal Data contains D1-D3 Bytes from the Rx Line or ISC Port.	Notes 1, 2
	6	RRLD	**Rx Terminal Port Line Datacom Bytes Control:** outgoing Terminal Data contains D4-D12 Bytes from Rx TOH Insert RAM Locations	outgoing Terminal Data contains D4-D12 Bytes from the Rx Line or ISC Port.	Notes 1, 2
	5	RRE1	**Tx Terminal Port E1 Byte Control:** outgoing Terminal Data contains E1 Byte from Rx TOH Insert RAM Location.	outgoing Terminal Data contains E1 Byte from the Rx Line or ISC Port.	Notes 1, 2, 3
	4	RRE2	**Tx Terminal Port E2 Byte Control:** outgoing Terminal Data contains E2 Byte from Rx TOH Insert RAM Location.	outgoing Terminal Data contains E2 Byte from the Rx Line or ISC Port.	Notes 1, 2
	3	RPATH	**Rx Terminal Port POH Bytes Control:** outgoing Terminal Data contains POH Bytes from Rx TOH Insert RAM Locations.	outgoing Terminal Data contains POH Bytes from the Rx Line.	Note 4 See H4INT.
	2	RRAPS	**Rx Terminal Port APS bytes Control:** outgoing Terminal Data contains K1 and K2 Bytes from Rx TOH Insert RAM Locations.	outgoing Terminal Data contains K1 and K2 Bytes from the Rx Line or ISC Port.	Notes 1, 2
	1	RRPTR	**Rx Terminal Port Pointer Bytes Control:** outgoing Terminal Data contains H1, H2 and H3 Bytes from Rx TOH Insert RAM Locations.	1. Re-timing disabled: outgoing Terminal Data contains H1, H2 and H3 Bytes from the Rx Line 2. Re-timing enabled: H1 and H2 recalculated and H3 from Rx TOH Insert RAM Location	This is for test purposes only. Payload does not track insert location H1 and H2 values.
	0	TRLOOP	**Tx-Rx Loop Back Enable:** Tx Line Output looped back to Rx Line Input	normal operation	See LPAISEN and LPAISSEL.

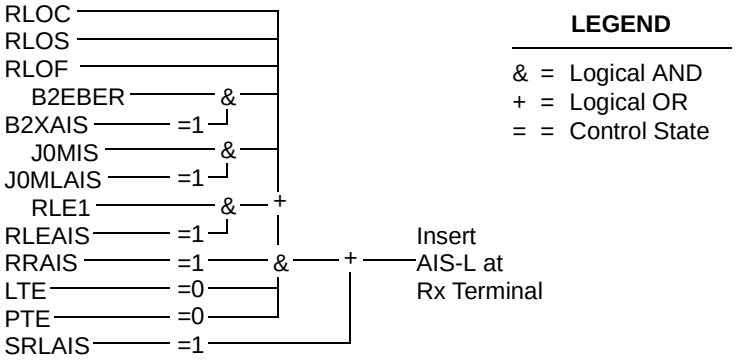
Notes:
1. If SPE-only Mode is selected, this control has no effect and neither condition occurs.
2. If TTOHEN = "1", ISC Port Data will be used when Bit Equal to “0”.
3. This control is only enabled if RA2E = "0".
4. The J1 Bytes are always passed through from the Rx Line. The H4 Byte selection is controlled by H4INT. The Rx POH Insert RAM B3 Location contains the recalculated B3 value. B3 Recalculation is performed and the Insert Location is used if RPATH or H4INT = "1".

CONTROL REGISTER 1

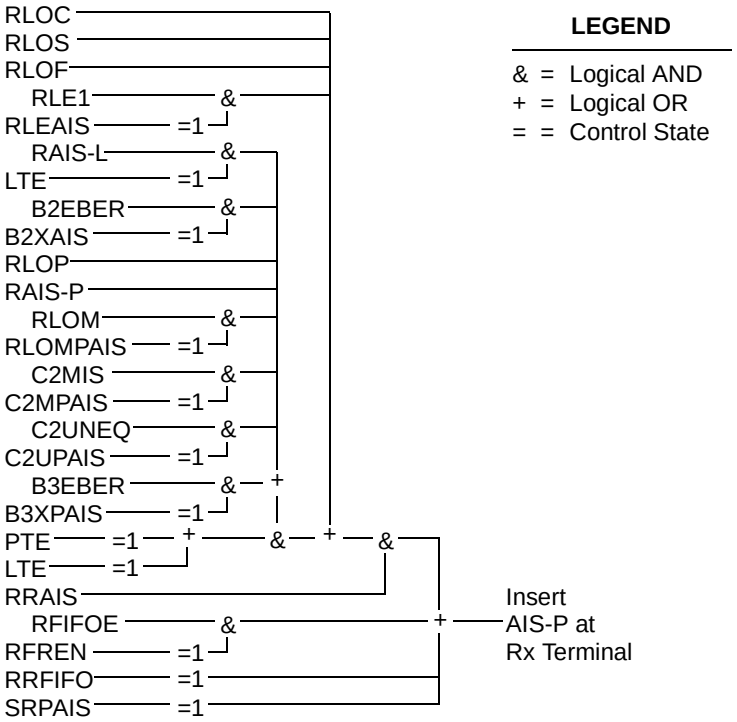
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F9	7	RRF1	**Rx Terminal Port F1 Byte Control:** outgoing Terminal Data contains F1 Byte from Rx TOH Insert RAM Location.	outgoing Terminal Data contains F1 Byte from the Rx Line or ISC Port.	Notes 1, 2
	6	RRC1	**Rx Terminal Port C1 Byte Control:** outgoing Terminal Data contains C1 Byte from Rx TOH Insert RAM Location.	outgoing Terminal Data contains C1 Byte from the Rx Line or ISC Port.	Notes 1, 2
	5	RRZ1	**Rx Terminal Port Z1 Byte Control:** outgoing Terminal Data contains Z1 Byte from Rx TOH Insert RAM Location.	outgoing Terminal Data contains Z1 Byte from the Rx Line or ISC Port.	Notes 1, 2
	4	RRZ2	**Rx Terminal Port Z2 Byte Control:** outgoing Terminal Data contains Z2 Byte from Rx TOH Insert RAM Location.	outgoing Terminal Data contains Z2 Byte from the Rx Line or ISC Port.	Notes 1, 2

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F9 (cont.)	3	RRAIS	**Rx Terminal Port AIS Insert Control:** enables the automatic insertion of AIS into Rx Terminal Data.	disables the automatic insertion of AIS into Rx Terminal Data.	

Rx Terminal AIS-L Insertion



Rx Terminal AIS-P Insertion



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0F9 (cont.)	2	LTE	**Line Terminating Equipment Enable**: defines Line Terminating Equipment Mode for AIS transmission and Introduction.	defines not Line Terminating Equipment Mode for AIS transmission and Introduction.	Section Terminating Equipment Mode if LTE = "0" and PTE = "0"
	1	RRFRM	**Rx Terminal Port Framing Bytes Control**: Framing Bytes are regenerated in Rx Terminal Data.	Rx Terminal Data has Framing Bytes from Rx Line.	Notes 1, 2
	0	RRB1	**Rx Terminal Port B1 Byte Control**: B1 Byte is recalculated for Rx Terminal Data and placed in Rx TOH Insert RAM Location.	outgoing Terminal Data contains B1 Byte from the Rx Line or the ISC Port.	Notes 1, 2, 3

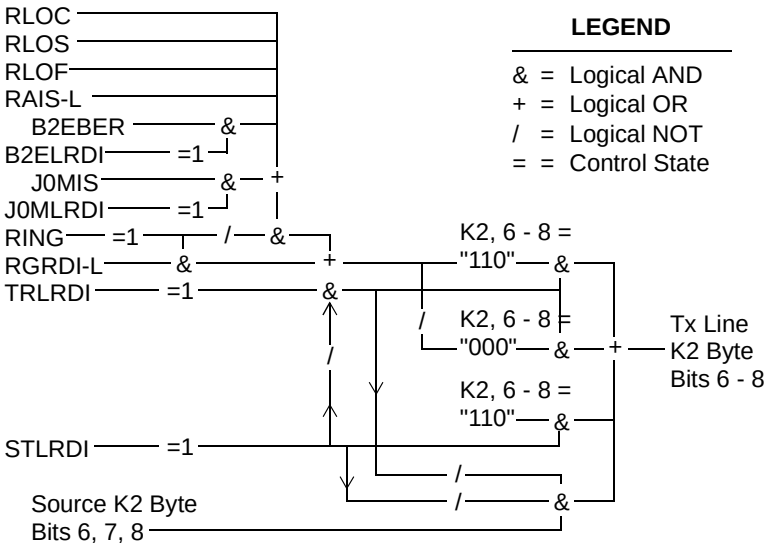
Notes:
1. If SPE-only Mode is selected, this control bit has no effect and neither condition occurs.
2. If TTOHEN = "1" or RCLK = "1" then ISC Port Data will be used if Bit Equal to “0”.
3. If STS1 = "1" this control is disabled and B1 Byte value is recalculated.

CONTROL REGISTER 2

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FA	7	STS1	**STS-1/STS-N Mode Control**: Line Side in STS-1 Mode. Rx and Tx Data scrambled. Rx and Tx B1 contains BIP-8 Parity.	Line Side in STS-N Mode. Data is not scrambled. Rx B1 Byte contains Error indication. Tx B1 Byte contains Error Mask.	
	6	PARA	**Parallel/Serial Mode Control**: Tx Terminal Port is Parallel. Rx Terminal Port has both Serial and Parallel Interfaces active.	Tx Terminal Port is Serial. Rx Terminal Port has both Serial and Parallel Interfaces active.	Notes 1, 2, 3. See Table 1.
	5	HWINE	**Hardware Interrupt Enable**: enables Hardware Interrupts via INT/$\overline{IRQ}$ Pin	disables INT/$\overline{IRQ}$ Pin	

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FA	4	TRLRDI	**Tx Line Port Line RDI Enable**: enables automatic insertion of RDI-L in Tx Line Data. K2 Byte Bits 6-8 controlled by alarm conditions.	K2 Byte Bits 6-8 are not modified and automatic insertion of RDI-L in Tx Line Data is disabled.	
	3	ALTOW	**Order Wire Mode Control**: OW Frame Pulse at OW/APS Port coincident with MSB of E1 and E2 Bytes	OW Frame Pulse at OW/APS Port leads MSB of E1 and E2 Bytes by 1 bit.	effective only if OA = "1"
	2	TIEN	**Transport Layer Interrupt Enable**: enables Transport Layer Interrupts	disables Transport Layer Interrupts	See Table 26.
	1	PIEN	**Path Layer Interrupt Enable**: enables Path Layer Interrupts	disables Path Layer Interrupts	See Table 27.
	0	-VE	**Interrupt Edge Control**: interrupts on both positive and negative edges of alarms	interrupts only on positive edges of alarms	

Tx Line RDI-L Insertion



Notes:
1. If SPE-only mode is selected, this control is disabled. Only the Serial Interfaces are active at Both the Tx and Rx Terminal Ports.
2. If Pin $\overline{\text{MBEI}}$ is Low, this control is disabled. Only the Parallel Interfaces, operating at 19.44 Mbyte/s, are active at Both the Tx and Rx Terminal Ports.
3. If PARA = "1", RCLK = "1" and RETSEL = "0", only the Parallel Interfaces, operating at 6.48 Mbyte/s, are active at Both the Tx and Rx Terminal Ports.

CONTROL REGISTER 3

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FB	7	RRFIEN	**Rx Reference Frame Input Enable**: failure of RRFI Input is part of LORR Equation.	RRFI failure is not part of LORR Equation.	
	6	RFREN	**Rx FIFO Reset Enable**: automatic recovery from Rx FIFO underflow/overflow enabled.	automatic recovery from Rx FIFO underflow/overflow disabled.	Note 1
	5	RRFIFO	**Reset Rx FIFO**: Transition from “0” to “1” causes a reset of the Rx FIFO. Control bit is reset to "0" upon completion of operation.	normal operation.	Note 1
	4	SBPE	**Send Bus Parity Errors**: continuously creates Bus Parity Errors at the Rx Terminal Port.	Parity Error creation disabled.	
	3	DISRLAL	**Disable Rx Line Alarms**: Rx Line Level Alarms and B1, B2 and FEBE-L Counters disabled.	Rx Line Level Alarms and B1, B2, FEBE-L Counters enabled.	
	2	CNT16EN	**Counter 16-Bit Enable**: enables 16-bit count mode for Rx Side B1, B2, B3, FEBE-L and FEBE-P Counters.	Rx Side B1, B2, B3, FEBE-L and FEBE-P Counters are 8 bits.	
	1	RSWRES	**Rx Software Reset**: resets all Rx Side counters and clears Rx Side Status Bits. Normal operation is inhibited.	terminates Rx Side Reset. Normal operation resumed.	
	0	TTOHEN	**Terminal TOH Enable**: ISC Port has access to Rx TOH Insert RAM Locations whose contents can be read by µPro.	µPro has Write and Read access to Rx TOH Insert RAM Locations.	

Notes:

1. The following operations are performed during a FIFO Reset:
   (1) AIS-P output at Rx Terminal Port,
   (2) FIFO is re-centered,
   (3) New Pointer Value is calculated,
   (4) AIS-P is terminated with the New Pointer value and active NDF indication.

CONTROL REGISTER 4

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FC	7	SRLAIS	**Send Rx Line AIS**: AIS-L inserted in Rx Terminal Port Data	AIS-L not forced in Rx Terminal Port Data	See RRAIS
	6	B2XAIS	**B2 Excess BER Line AIS Enable**: Excess B2 Error condition included in equations for AIS-L and AIS-P insertion at Rx Terminal Port	Excess B2 Error condition excluded from equations for AIS-L and AIS-P insertion at Rx Terminal Port	See RRAIS
	5	SRPAIS	**Send Rx Path AIS**: AIS-P inserted in Rx Terminal Port Data	AIS-P not forced in Rx Terminal Port Data	See RRAIS
	4	B3XPAIS	**B3 Excess BER Path AIS Enable**: Excess B3 Error condition included in equation for AIS-P insertion at Rx Terminal Port	Excess B3 Error condition excluded from equation for AIS-P insertion at Rx Terminal Port	See RRAIS
	3	RLOMPAIS	**Rx Loss of Multiframe Path AIS Enable**: RLOM condition included in equation for AIS-P insertion at Rx Terminal Port	RLOM condition excluded from equation for AIS-P insertion at Rx Terminal Port	See RRAIS
	2	C2MPAIS	**C2 Mismatch Path AIS Enable**: C2 Mismatch condition included in equation for AIS-P insertion at Rx Terminal Port	C2 Mismatch condition excluded from equation for AIS-P insertion at Rx Terminal Port	See RRAIS
	1	C2UPAIS	**C2 Unequipped Path AIS Enable**: Rx C2 Unequipped condition included in equation for AIS-P insertion at Rx Terminal Port	Rx C2 Unequipped condition excluded from equation for AIS-P insertion at Rx Terminal Port	See RRAIS
	0	RLEAIS	**RLE1 Path AIS Enable**: RLE1 condition included in equations for AIS-P and AIS-L insertion at Rx Terminal Port	RLE1 condition excluded from equation for AIS-P and AIS-L insertion at Rx Terminal Port	See RRAIS

CONTROL REGISTER 5

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FD	7	DIEN	**Device Layer Interrupt Enable**: enables Device Layer Interrupts	disables Device Layer Interrupts	See Table 28
	6	DATACOM	**DATACOM Mode Control**: places device in DATACOM Mode	device not in DATACOM Mode	Notes 1, 2
	5	ENDCMPOH	**Enable Datacom POH**: RSPE and TSPEI/O are High during POH Byte times	RSPE and TSPEI/O are Low during POH Byte times	Effective only in Datacom Mode Note 3
	4	DISPCKG	**Disable Parallel Clock Gapping**: TPCO is continuous	TPCI/O and TPCO are gapped during TOH Byte times and when ENDCMPOH = "0", also during POH Byte times.	Effective only in Datacom Mode Note 3
	3	INVPCK	**Invert Parallel Clock**: TPDO(0-7), RSPE, RSYN and TPARO occur on the Rising Edge of TPCO. When DATACOM = "0", TPDI(0-7), TSPEI/O, TSYNI/O and TPARI are clocked in on the Falling Edge of TPCI/O. When DATACOM = "1", TPDI(0-7) and TPARI are clocked in on and TSYNI/O and TSPEI/O are clocked out on, the Rising Edge of TPCI/O.	TPDO(0-7), RSPE, RSYN and TPARO occur on the Falling Edge of TPCO. When DATACOM = "0", TPDI(0-7), TSPEI/O, TSYNI/O and TPARI are clocked in on the Rising Edge of TPCI/O. When DATACOM = "1", TPDI(0-7) and TPARI are clocked in on and TSYNI/O and TSPEI/O are clocked out on, the Falling Edge of TPCI/O.	Note 1
	2	MBSEL1	**Multiplex Bus Select (1,0)**: determines time slot assignment in 19.44 Mbyte/s modes for Rx Terminal Port (and Tx Terminal Port). MBSEL1 / MBSEL0 / Time Slot 0 / 0 / Unassigned 0 / 1 / First 1 / 0 / Second 1 / 1 / Third		only enabled if Pin $\overline{\text{MBEI}}$ is Low see ENFSTUA and ENLSTUA see TMBSEL0 and TMBSEL1
	1	MBSEL0			
	0	INVINT	**Invert Interrupt**: Pin INT/$\overline{\text{IRQ}}$ transitions Low to indicate interrupt when pins µPSEL0, µPSEL1 = High, Low or High, High (Intel or multiplexed A/D). Pin INT/$\overline{\text{IRQ}}$ transitions High to indicate interrupt when µPSEL0, µPSEL1 = Low, Low (Motorola).	Pin INT/$\overline{\text{IRQ}}$ transitions High to indicate interrupt when pins µPSEL0, µPSEL1 = High, Low or High, High (Intel or multiplexed A/D). Pin INT/$\overline{\text{IRQ}}$ transitions Low to indicate interrupt when µPSEL0, µPSEL1 = Low, Low (Motorola).	

Notes:
1. If SPE-only Mode is selected, this control is disabled and Bit Equal to "0" condition applies.
2. If either (SPE and DATACOM = "0") or (SPE = "1", Pin $\overline{\text{MBEI}}$ is Low and DATACOM = "0") then the device is in SONET Mode. See Table 1.
3. RSPE is always High, and TPCO is never gapped, during fixed stuff Bytes times (columns 30 and 59).

CONTROL REGISTER 6

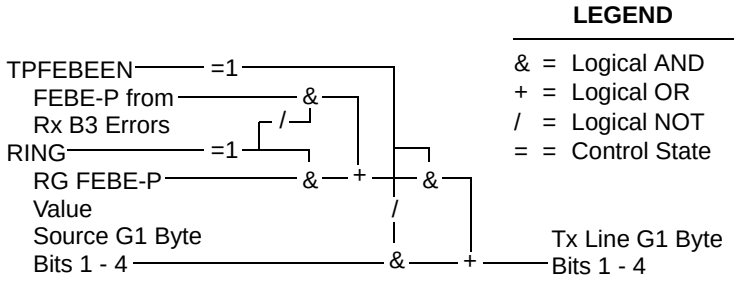
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FE	7	B2FREN	**B2 Framing Check Enable:** The accumulated B2 byte must match the received B2 byte following the second valid framing pattern to declare in frame.	Two valid framing patterns (A1/A2 = F628 Hex) found one STS-1 frame apart are used to declare in frame.	Note 4
	6	RAMTSTEN	**RAM Test Enable**: Internal operations are inhibited from writing to RAM Locations	normal operation	Note 1
	5	H4INT	**H4 Internal**: Rx Side: H4 Byte output at Rx Terminal Port is regenerated. If SONET or Datacom Modes are selected then RSYN = C1J1V1. If SPE-only Mode is selected then RSYN = J1V1. Tx Side: If either Datacom Mode is selected or SONET Mode is selected and C1J1EN = "1" then TSYNI/O = C1J1V1 If SPE-only Mode is selected then TSYNI/O = J1V1	Rx Side: H4 Byte output at Rx Terminal Port as received from Rx Line. If SONET or Datacom Modes are selected then RSYN = C1J1 If SPE-only Mode is selected then RSYN = J1 Tx Side: If either Datacom Mode is selected or SONET Mode is selected and C1J1EN = "1" then TSYNI/O = C1J1 If SPE-only Mode is selected then TSYNI/O = J1	See RPATH, TXH4INS, TPATH
	4	J1SYNCEN	**J1 Synchronization Enable**: incoming J1 Message is stored such that the byte following ASCII (CR) and (LF) characters is stored in the Lowest address location.	incoming J1 Bytes are stored in rotating fashion with no specific starting point.	Note 1
	3	S1	**Pointer S1 Bit**: H1 Byte Bit 5 = "1"	H1 Byte Bit 5 = "0"	Note 2
	2	S0	**Pointer S0 Bit**: H1 Byte Bit 6 = "1"	H1 Byte Bit 6 = "0"	
	1	C1J1EN	**C1/J1 Enable**: TSYNI/O and TSPEI/O are used for Frame and SPE alignment at Tx Terminal Port.	A1/A2 and H1/H2 are used for Frame and SPE alignment at Tx Terminal Port.	Note 3
	0	OA	**OW/APS Port or All TOH Port Mode Control**: E1, E2, K1 and K2 Bytes output and input at Rx and Tx OA/TOH Ports, respectively	all TOH Bytes output and input at Rx and Tx OA/TOH Ports, respectively	

Notes:
1. This applies to inputs from Rx Line, Tx Terminal and Tx TOH Port.
2. This applies to Tx and Rx Side Pointer Generation.
3. If SPE-only or Datacom Modes are selected, this control is disabled. The methodologies for Frame Delineation are inherent to these operations.
4. Do not set to “1” in STS-N Mode (control bit STS1="0" in control register 2, bit 7).

CONTROL REGISTER 7

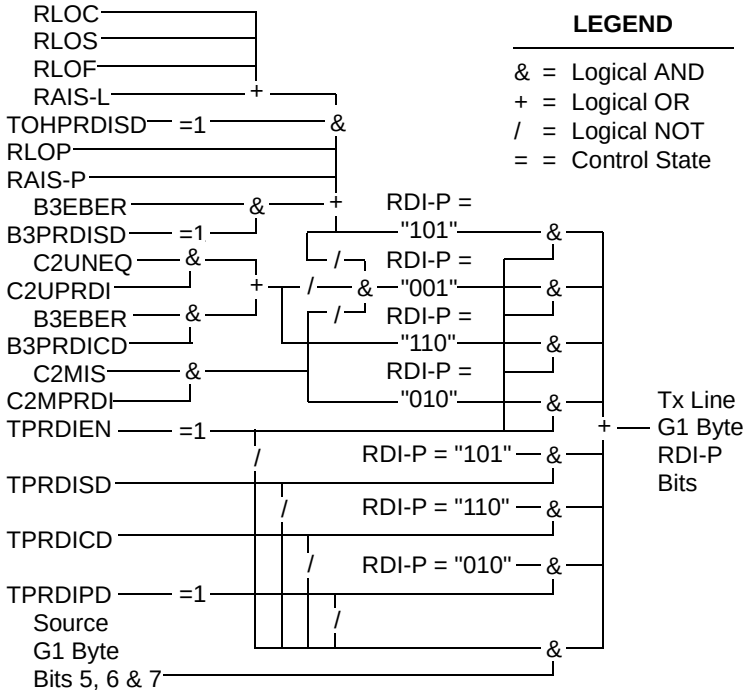
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DE	7	TIDL	**Tx Idle**: Path Idle signal is inserted at the Tx Line Port.	Path Idle signal is not inserted at the Tx Line Port.	Notes 1, 2
	6	IDLSEL	**Idle Signal Select**: all SPE bytes except POH Bytes are set to "0".	all SPE Bytes including POH Bytes are set to "0".	Notes 1, 2, 3
	5	TPFEBEEN	**Path FEBE Enable**: Bits 1-4 of the G1 Byte in the Tx Line Port Data are overwritten by FEBE-P derived from Rx B3 Byte or Tx Ring Port value.	Bits 1-4 of the G1 Byte in the Tx Line Port Data are not overwritten.	

Tx Line FEBE-P Insertion

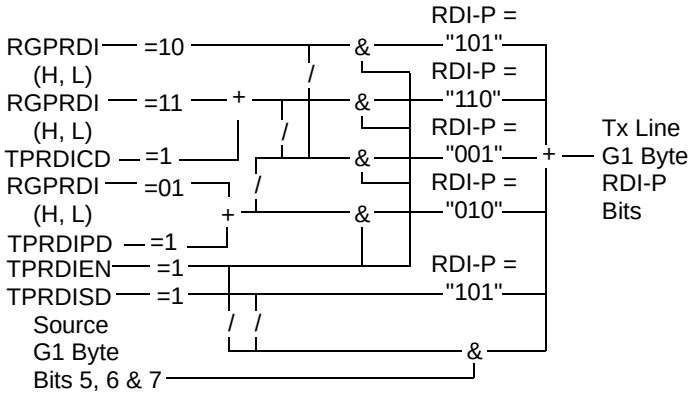


Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DE (cont.)	4	TPRDIEN	**Tx Line Port Path RDI Enable**: automatic insertion of RDI-P in Tx Line Port Data enabled. G1 Byte RDI-P Bits are controlled by alarm conditions.	G1 Byte RDI-P Bits are not modified and automatic insertion of RDI-P in Tx Line Port Data disabled.	See note 5.
	3	C2MPRDI	**C2 Mismatch Path RDI Enable**: C2 Mismatch condition included in equation for RDI-PPD insertion at Tx Line Port.	C2 Mismatch condition excluded from equation for RDI-PPD insertion at Tx Line Port.	

Tx Line RDI-P Insertion - RING = "0"



Tx Line RDI-P Insertion - RING = "1"



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DE (cont.)	2	C2UPRDI	**C2 Unequipped Path RDI Enable**: Rx C2 Unequipped condition included in equation for RDI-PCD insertion at Tx Line Port.	Rx C2 Unequipped condition excluded from equation for RDI-PCD insertion at Tx Line Port.	
	1	ENFSTUA	Enables Rx Terminal Outputs during the first unassigned slot in 19.44 Mbyte/s mode.	Rx Terminal Outputs are tri-stated during the first unassigned slot in 19.44 Mbyte/s mode.	Note 4
	0	ENLSTUA	Enables Rx Terminal Outputs during the last unassigned slot in 19.44 Mbyte/s mode.	Rx Terminal Outputs are tri-stated during the last unassigned slot in 19.44 Mbyte/s mode.	Note 4

Notes:
1. If TIDL and IDLSEL = "1", TPATH is disabled and the POH Bytes are taken from the Tx POH Insert locations. The controls TXH4INS, TPFEBEEN, TPRDIEN, TPRDICD, TPRDISD and TPRDIPD are functional.
2. If TIDL = "1" and IDLSEL = "0" the Tx POH Bytes are forced to "0" and all Tx POH selection controls are disabled.
3. This control is effective only if TIDL = "1".
4. These controls are for use when the 19.44 Mbyte/s bus will be only partly populated.
5. If multiple alarm conditions exist simultaneously, the transmitted RDI follows the following priority; RDI-P = "101" first, RDI-P = "110" second and RDI-P = "010" third; if no alarm is present RDI-P = "001".

CONTROL REGISTER 8

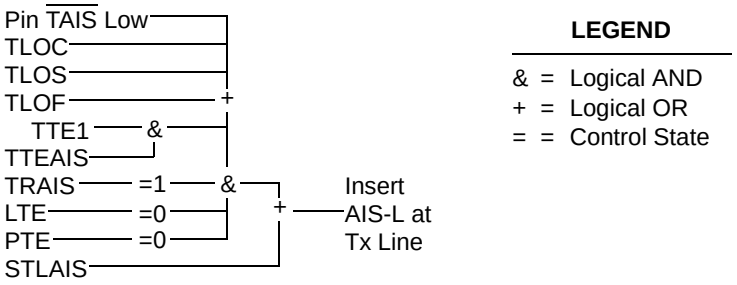
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1F8	7	TRSD	**Tx Line Port Section Datacom Bytes Control**: outgoing Line Data contains D1-D3 Bytes from Tx TOH Insert RAM Locations.	outgoing Line Data contains D1-D3 Bytes from Tx Terminal Port.	Note 1 See TXSDEXT
	6	TRLD	**Tx Line Port Line Datacom Bytes Control**: outgoing Line Data contains D4-D12 Bytes from Tx TOH Insert RAM Locations.	outgoing Line Data contains D4-D12 Bytes from Tx Terminal Port.	Note 1 See TXLDEXT
	5	TRE1	**Tx Line Port E1 Byte Control**: outgoing Line Data contains E1 Byte from Tx TOH Insert RAM Location.	outgoing Line Data contains E1 Byte from Tx Terminal Port.	Notes 1, 2 See TXE1EXT
	4	TRE2	**Tx Line Port E2 Byte Control**: outgoing Line Data contains E2 Byte from Tx TOH Insert RAM Location.	outgoing Line Data contains E2 Byte from Tx Terminal Port.	Note 1 See TXE2EXT
	3	TPATH	**Tx Line Port POH Bytes Control**: outgoing Line Data contains POH Bytes from Tx POH Insert RAM Locations.	outgoing Line Data contains POH Bytes from the Tx Terminal Port. The Tx POH Insert Locations contain J1 Bytes input at Tx Terminal Port.	Notes 3, 4 See J1SYNCEN
	2	TRAPS	**Tx Line Port APS Bytes Control**: outgoing Terminal Data contains K1 and K2 Bytes from Tx TOH Insert RAM Locations.	outgoing Terminal Data contains K1 and K2 Bytes from the Tx Terminal Port.	Note 1 See EXAPS
	1	EXAPS	**External APS Bytes Control**: Tx TOH RAM Insert K1 and K2 Byte Locations contain data from Tx OA/TOH Port.	Tx TOH RAM Insert K1 and K2 Byte Locations written by µPro.	Note 5
	0	RTLOOP	**Rx-Tx Loop Back Enable**: Rx Terminal Output looped back to Tx Terminal Input.	normal operation	

Notes:
1. If SPE-only Mode is selected or TCLK = "1", this control is disabled and Bit Equal to "1" condition applies.
2. This control is only enabled if TA2E = "0".
3. If TIDL = "1", this control is disabled and Bit Equal to "1" condition applies.
4. The H4 Byte is also controlled by H4INT and TXH4INS. The Tx POH Insert RAM B3 Location contains the recalculated B3 Value. If TPATH = "0" and H4INT, TPFEBEEN, TPRDIEN, TPRDICD, TPRDISD, or TPRDIPD = "1" then B3 will be recalculated and the Insert Location will be used. See TJ1EXT, TC2EXT, TG1EXT, TF2EXT, TZ3EXT, TZ4EXT and TZ5EXT for Insert Location usage.
5. This control is enabled if SPE-only Mode is selected or TRAPS = "1".

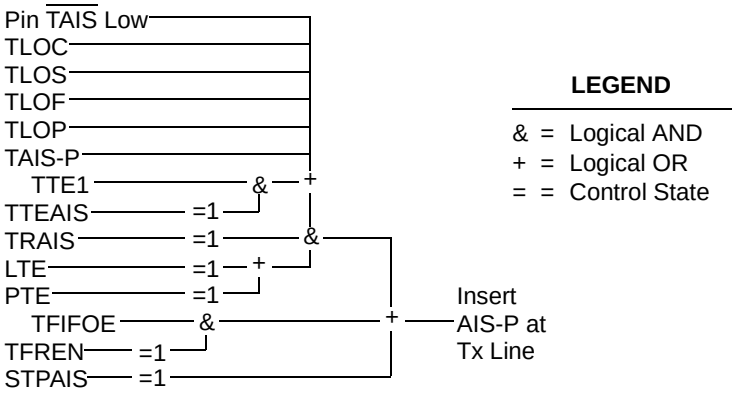
CONTROL REGISTER 9

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1F9	7	TRF1	**Tx Line Port F1 Byte Control**: outgoing Line Data contains F1 Byte from Tx TOH Insert RAM Locations.	outgoing Line Data contains F1 Byte from Tx Terminal Port	Note 1 See TXF1EXT
	6	TRC1	**Tx Line Port C1/J0 Byte Control**: outgoing Line Data contains C1/J0 Byte(s) from Tx TOH Insert RAM Locations.	outgoing Line Data contains C1/J0 Byte(s) from Tx Terminal Port	Note 1 See TXC1EXT J0EN(0,1)
	5	TRZ1	**Tx Line Port Z1 Byte Control**: outgoing Line Data contains Z1 Byte from Tx TOH Insert RAM Locations	outgoing Line Data contains Z1 Byte from Tx Terminal Port	Note 1 See TXZ1EXT
	4	TRZ2	**Tx Line Port Z2 Byte Control**: outgoing Line Data contains Z2 Byte from Tx TOH Insert RAM Locations	outgoing Line Data contains Z2 Byte from Tx Terminal Port	Note 1 See TXZ2EXT
	3	TRAIS	**Tx Line Port AIS Insert Control**: enables the automatic insertion of AIS into Tx Line Data	disables the automatic insertion of AIS into Tx Line Data	

Tx Line AIS-L Insertion



Tx Line AIS-P Insertion



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1F9 (cont.)	2	PTE	**Path Terminating Equipment Enable**: defines Path Terminating Equipment Mode for AIS transmission and Introduction.	defines Not-Path Terminating Equipment Mode for AIS transmission and Introduction.	Section Terminating Equipment Mode if LTE = "0" and PTE = "0"
	1	RXRTM	**Rx Re-Timing Mode Control**: Rx Re-timing disabled.	Rx Re-timing enabled.	note 2
	0	RRB2	**Rx Terminal Port B2 Byte Control**: B2 Byte is recalculated in Rx Terminal Data and placed in Rx TOH Insert RAM Location.	outgoing Terminal Data contains B2 Byte from the Rx Line or the ISC Port.	notes 3, 4

Notes:
1. If SPE-only Mode is selected or TCLK = "1", this control is disabled and Bit Equal to "1" condition applies.
2. If SPE-only Mode is selected, Pin MBEI is Low, or RCLK = "1" then this control is disabled and Bit Equal to "0" condition applies. Rx Re-timing is only optional for Serial or 6.48 Mbyte/s Parallel SONET and Datacom Modes.
3. If SPE-only Mode is selected, this control has no effect and neither condition occurs.
4. If TTOHEN = "1" or RCLK = "1", ISC Port Data will be used when Bit Equal to "0".

CONTROL REGISTER 10

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FA	7	SPE	**SPE-only Mode Select**: places the device in SPE-only Mode	device not in SPE-only Mode	notes 1, 2
	6	TCLK	**Tx Clock Source Select**: External Timing; TLCO derived from TLCI and start of Tx Frame derived from TFRI See Tables 3 and 4.	Datacom Mode selected and Pin MBEI is High and either PARA = "0" or DETSEL = "1" - Terminal Timing; TLCO derived from DRCI and start of Tx Frame derived from DFRI.	notes 3, 4, 5, 6
				Datacom Mode selected and either Pin MBEI is Low or PARA = "1" and DETSEL = "0" - External Timing; TLCO derived from TLCI and start of Tx Frame derived from TFRI.	notes 3, 4, 5, 6, 7
				DATACOM = "0", PARA = "0" and Pin MBEI is High - Terminal Timing; TLCO derived from TTCI/O and start of Tx Frame derived from TSYNI/O if C1J1EN = "1" or A1 and A2 Bytes input at the Tx Terminal Port if C1J1EN = "0"	notes 3, 4, 5, 6
				either DATACOM = "0" and PARA = "1" or Pin MBEI is Low - External Timing; TLCO derived from TLCI and start of Tx Frame derived from TFRI.	notes 3, 4, 5, 6, 7
	5	RCLK	**Rx Clock Source Select**: External Timing; Rx Terminal Port Clock is derived from RRCI and start of Rx Frame is derived from RRFI/RRFI.	Line Timing; Rx Terminal Port Clock is derived from RXCK and start of Rx Frame is derived from RXFR.	notes 5, 8, 9 See RETSEL Table 2
	4	DISTBPE	**Disable Terminal Bus Parity Error**: parity checking disabled at Tx Terminal Port Input	parity checking enabled at Tx Terminal Port Input.	
	3	TXRTM	**Tx Re-Timing Mode Control**: Tx Re-timing enabled	Tx Re-timing disabled	note 10
	2	DETSEL	**Datacom External Timing Select**: DRCI is 51.84 Mbit/s and Datacom Reference Frame Input is DFRI.	DRCI is 6.48 Mbit/s and Datacom Reference Frame Input is DFRI	effective only if Pin MBEI is High and PARA = "1"

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FA (cont.)	1	INC	**Tx Pointer Increment**: forces Pointer Increments in every 4th frame in Tx Line Data. This bit may be reset immediately after setting and still guarantee the pointer movement.	normal operation	These bits must be used with extreme caution. Consecutive PJs will cause downstream alarms. Multiple PJs can cause FIFO spills.
	0	DEC	**Tx Pointer Decrement**: forces Pointer Decrements in every 4th frame in Tx Line Data. This bit may be reset immediately after setting and still guarantee the pointer movement.	normal operation	

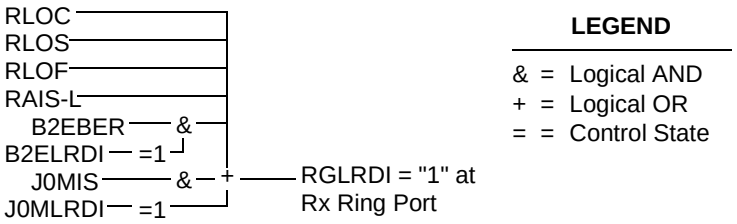
Notes:
1. If Pin $\overline{\text{MBEI}}$ is Low, this control is disabled and Bit Equal to "0" condition applies.
2. If either (SPE and DATACOM = "0") or (SPE = "1", Pin $\overline{\text{MBEI}}$ is Low and DATACOM = "0") then the device is in SONET Mode. See Table 1.
3. If SPE-only Mode is selected, this control is disabled and Bit Equal to "1" condition applies.
4. If TCLK = "1", the Tx Terminal Option for Tx Line TOH Bytes and the option to turn off Tx re-timing are disabled. If TCLK = "0", these options are enabled.
5. If a Frame Pulse is not supplied the starting point of the generated frame will be arbitrary.
6. See TRC1, TRE1, TRE2, TRF1, TRSD, TRLD, TRZ1 and TRZ2.
7. If TCLK = "0" and the Terminal Port is in a mode that does not have a 51.84 Mbit/s Clock then TLCI and $\overline{\text{TFRI}}$ must adhere to the relationship shown in Figure 20.
8. If Pin $\overline{\text{MBEI}}$ is High and RCLK = "1", External Source Selection is controlled by RETSEL.
9. If Pin $\overline{\text{MBEI}}$ is Low, control is disabled and Bit Equal to "1" condition applies. RRCI/RRFI are 19.44 Mbit/s Reference Clock and Frame.
10. If SPE Mode is selected, SONET Mode is selected and C1J1EN = "1", or TCLK = "1", this control is disabled and Bit Equal to "1" condition applies. Tx Re-timing is only an option if Datacom Mode is selected or if SONET Mode is selected and C1J1EN = "0".

CONTROL REGISTER 11

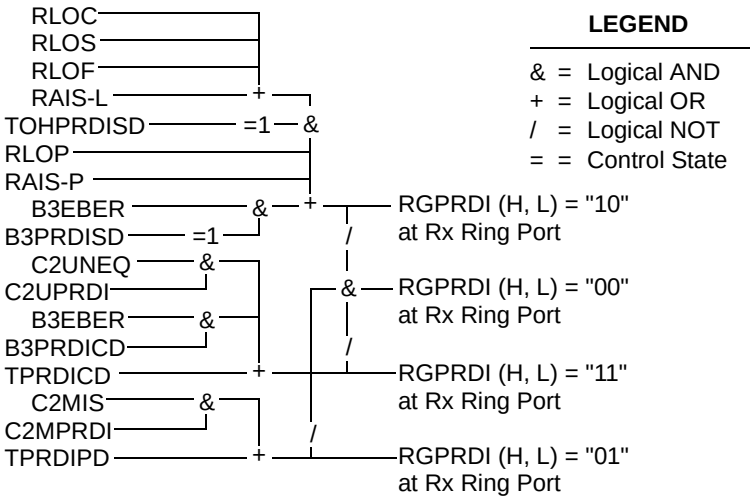
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FB	7	TRFRM	**Tx Line Port Framing Bytes Control**: A1 and A2 Bytes in the Tx Line Port Data are generated internally and placed in Tx TOH Insert RAM Locations for µPro Read.	outgoing Line Data contains A1 and A2 Bytes from Tx TOH Insert RAM Locations.	See TFRMEXT
	6	TRERR	**Tx Parity Error Control**: automatic reset of Tx Side B1, B2 and B3 Error Masks after one frame	automatic reset of Error Masks disabled	
	5	STPAIS	**Send Tx Path AIS**: AIS-P inserted in Tx Line Port Data	AIS-P not forced in Tx Line Port-Data	See TRAIS

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FB (cont.)	4	RING	**Ring Mode Control**: Ring Port enabled. Tx Side RDI-L, RDI-P, FEBE-L and FEBE-P generation are controlled by Tx Ring Port input information.	Ring Port Disabled. Tx Side RDI-L, RDI-P, FEBE-L and FEBE-P generation are controlled by Rx Side conditions	Rx Ring Port Information is always generated and output See TRLRDI, TPRDIEN, TLFEBEEN and TPFEBEEN.
	3	RE2A	**Rx E1 to AIS Mode Control**: E1 Byte incoming at Rx Line Port interpreted as AIS Indication	E1 Byte incoming at Rx Line Port not interpreted as AIS Indication	See RLE1

Rx Ring Port RDI-L Generation

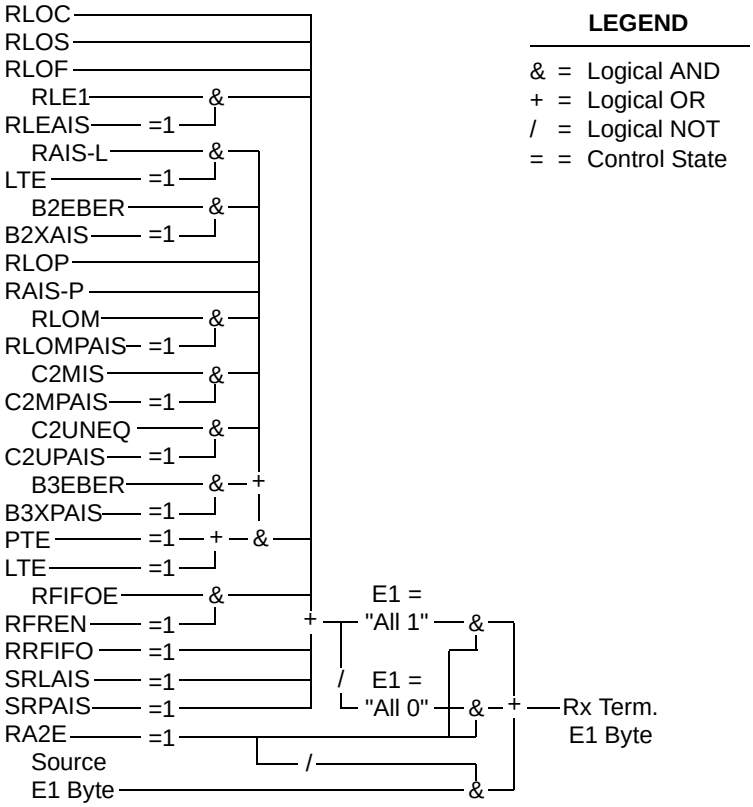


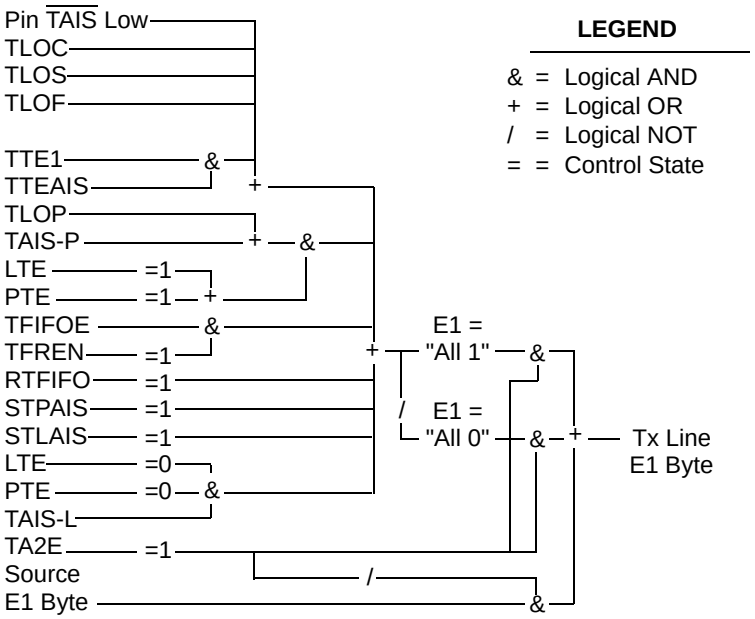
Rx Ring Port RDI-P Generation



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FB (cont.)	2	RA2E	**Rx AIS to E1 Mode Control**: E1 Byte outgoing at Rx Terminal Port used for AIS Indication	E1 Byte outgoing at Rx Terminal Port not used for AIS Indication	
	1	TE2A	**Tx E1 to AIS Mode Control**: E1 Byte incoming at Tx Terminal Port interpreted as AIS Indication.	E1 Byte incoming at Tx Terminal Port not interpreted as AIS Indication.	

Rx Terminal E1 Alarm Insertion



Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FB (cont.)	0	TA2E	**Tx AIS to E1 Mode Control**: E1 Byte outgoing at Tx Line Port used for AIS Indication.	E1 Byte outgoing at Tx Line Port not used for AIS Indication.	
			Tx Line E1 Alarm Insertion 		

CONTROL REGISTER 12

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FC	7	TFREN	**Tx FIFO Reset Enable**: automatic recovery from Tx FIFO underlow/overflow enabled	automatic recovery from Tx FIFO underflow/overflow disabled	Note 1
	6	RTFIFO	**Reset Tx FIFO**: Transition from “0” to “1” causes a reset of the Tx FIFO. Control bit is reset to "0" upon completion of operation.	normal operation	Note 1
	5	DISTLAIS	**Disable Tx Line AIS Detection**: detection of AIS-L at Tx Terminal Port disabled	detection of AIS-L at Tx Terminal Port enabled	
	4	LPAISEN	**Loop Back AIS Generation Enable**: generate AIS in Tx Line Port Data during Tx-Rx Loop	looped data is output at Tx Line Port during Tx-Rx Loop	Note 2

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FC (cont.)	3	LPAISSEL	**Loop Back AIS Select**: AIS-L generated (all Bytes = "1" except the 9 SOH Bytes)	AIS-P Generated (H1, H2, H3 and all POH Bytes = "1")	effective only if LPAISEN = "1"
	2	TFRIEN	**Tx Frame Reference Input Enable**: failure at $\overline{\text{TFRI}}$ pin included in LOTR equation	status of $\overline{\text{TFRI}}$ pin disregarded in LOTR equation.	
	1	DFRIEN	**Datacom Frame Reference Input Enable**: failure at DFRI/$\overline{\text{DFRI}}$ pin included in LOTR equation	status of DFRI/$\overline{\text{DFRI}}$ Pin disregarded in LOTR equation.	
	0	TDDLY	**Tx Terminal Datacom Data Delay**: delay time from Rising Edge of TSPEI/O to sampling of data at Tx Terminal Port is: Serial Datacom - 4½ bit times to MSB of serial data (See Figure 62) Parallel Datacom - 3 clock times (See Figures 64 and 66)	delay time from Rising Edge of TSPEI/O to sampling of data at Tx Terminal Port is: Serial Datacom - 1½ bit times to MSB of serial data (See Figure 62) Parallel Datacom - 2 clock times (See Figures 64 and 66)	effective only in Datacom Mode

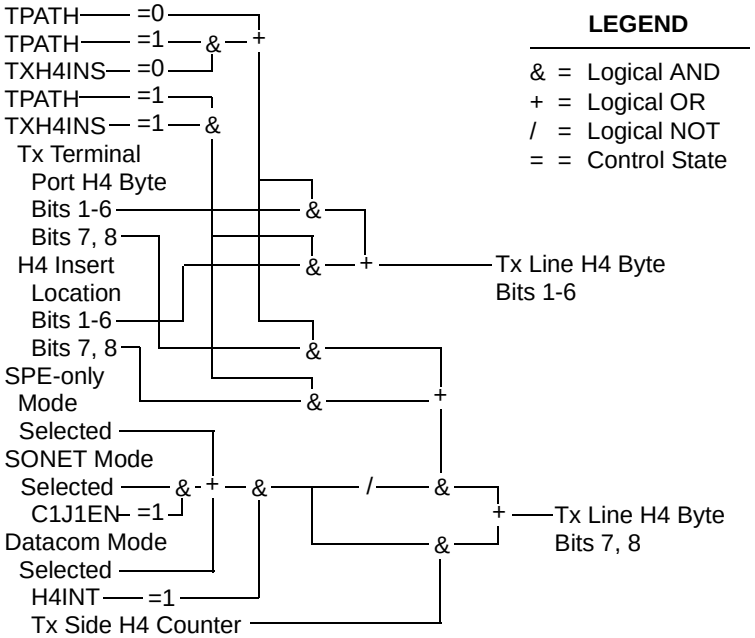
Notes:
1. The following operations are performed during a FIFO Reset:
   (1) AIS-P output at Tx Line Port,
   (2) FIFO is re-centered,
   (3) New Pointer Value is calculated,
   (4) AIS-P is terminated with the New Pointer value and active NDF indication.
2. This control is only enabled if TRLOOP = "1"

CONTROL REGISTER 13

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FD	7	TJ1EXT	**Tx J1 Bytes External Control**: J1 Bytes input at Tx POH Port will be written to Tx POH Insert Locations	Tx POH Insert RAM J1 Locations will be written by µPro	See TPATH, J1SYNCEN and J0RWEN.
	6	TC2EXT	**Tx C2 Byte External Control**: C2 Byte input at Tx POH Port will be written to the Tx POH Insert RAM Location	Tx POH Insert RAM C2 Location will be written by µPro	See TPATH.
	5	TG1EXT	**Tx G1 Byte External Control**: G1 Byte input at Tx POH Port will be written to the Tx POH Insert RAM Location	Tx POH Insert RAM G1 Location will be written by µPro	See TPATH.

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FD (cont.)	4	TF2EXT	**Tx F2 Byte External Control**: F2 Byte input at Tx POH Port will be written to the Tx POH Insert RAM Location.	Tx POH Insert RAM F2 Location will be written by µPro.	See TPATH.
	3	TXH4INS	**Tx H4 Byte Control**: outgoing Line Data contains H4 Byte from Tx POH Insert RAM Location.	outgoing Line Data contains H4 Byte from the Tx Terminal Port.	
	2	TZ3EXT	**Tx Z3 Byte External Control**: Z3 Byte input at Tx POH Port will be written to the Tx POH Insert RAM Location.	Tx POH Insert RAM Z3 Location will be written by µPro.	See TPATH.
	1	TZ4EXT	**Tx Z4 Byte External Control**: Z4 Byte input at Tx POH Port will be written to the Tx POH Insert RAM Location.	Tx POH Insert RAM Z4 Location will be written by µPro.	See TPATH.
	0	TZ5EXT	**Tx Z5 Byte External Control**: Z5 Byte input at Tx POH Port will be written to the Tx POH Insert RAM Location.	Tx POH Insert RAM Z5 Location will be written by µPro.	See TPATH.

Tx Line H4 Byte Selection



CONTROL REGISTER 14

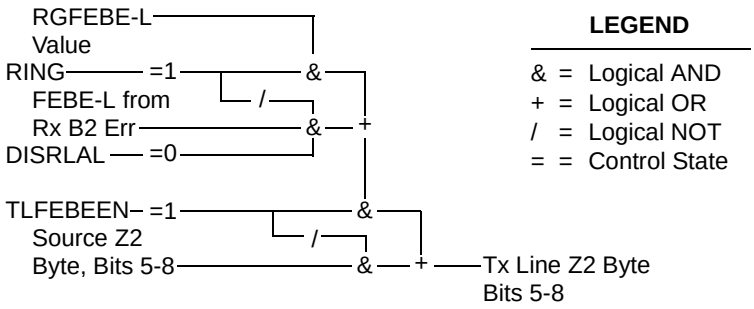
Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1FE	7	TFRM-EXT	**Tx Framing Bytes External Control**: Insert Tx TOH RAM Locations contain A1 and A2 Bytes from Tx TOH port.	Insert Tx TOH RAM Locations for A1 and A2 Bytes written by µPro.	Notes 1, 2. See TRFRM.
	6	TXC1-EXT	**Tx C1/J0 Byte External Control**: Insert Tx TOH RAM Location(s) contains C1 Byte(s) from Tx TOH Port.	Insert Tx TOH RAM Location(s) for C1 Byte(s) written by µPro.	Notes 1, 2. See TRC1 and J0EN(0,1).
	5	TXE1-EXT	**Tx E1 Byte External Control**: Insert Tx TOH RAM Location contains E1 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for E1 Byte written by µPro.	Notes 2, 3. See TRE1.
	4	TXF1EXT	**Tx F1 Byte External Control:** Insert Tx TOH RAM Location contains F1 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for F1 Byte written by µPro.	Notes 1, 2. See TRF1.
	3	TXSD-EXT	**Tx D1-D3 Bytes External Control:** Insert Tx TOH RAM Locations contain D1-D3 Bytes from Tx TOH Port or Tx Section DCC Port.	Insert Tx TOH RAM Locations for D1-D3 Bytes written by µPro.	Note 2. See TRSD and SDCCEN.
	2	TXZ1EXT	**Tx Z1 Byte External Control:** Insert Tx TOH RAM Location contains Z1 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for Z1 Byte written by µPro.	Notes 1, 2. See TRZ1.
	1	TXZ2EXT	**Tx Z2 Byte External Control:** Insert Tx TOH RAM Location contains Z2 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for Z2 Byte written by µPro.	Notes 1, 2. See TRZ2.
	0	TXE2-EXT	**Tx E2 Byte External Control:** Insert Tx TOH RAM Location contains E2 Byte from Tx TOH Port.	Insert Tx TOH RAM Location for E2 Byte written by µPro.	Note 2. See TRE2.

Notes:
1. If OA = "1", Control is disabled and Bit Equal to "0" condition applies.
2. The settings for the appropriate 1^{ST} Level Control (TRFRM, TRC1, TRE1, TRF1, TRSD, TRZ1, TRZ2 or TRE2) must be such that the Tx TOH Insert RAM Location(s) is(are) enabled for output at the Tx Line Port.
3. This control is only enabled if TA2E = "0"

CONTROL REGISTER 15

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DF	7	TXLD-EXT	**Tx D4-D12 Bytes External Control**: Insert Tx TOH RAM Locations contain D4-D12 Bytes from Tx TOH Port or Tx Section DCC Port	Insert Tx TOH RAM Locations for D4-D12 Bytes written by µPro	See TRLD and LDCCEN.
	6	TSWRES	**Tx Software Reset**: resets all Tx Side counters and clears Tx Side Status Bits. Normal operation is inhibited.	terminates Tx Side Reset. Normal operation resumed.	
	5	TTEAIS	**Tx Terminal Enable AIS**: automatic insertion of AIS-L at Tx Line Port due to Tx Terminal Port or Tx Alarm Port conditions enabled	automatic insertion of AIS-L at Tx Line Port due to Tx Terminal Port or Tx Alarm Port conditions disabled	
	4	TLFEBEEN	**Line FEBE Enable**: Bits 5-8 of the Z2 Byte in the Tx Line Port Data are overwritten by FEBE-L derived from Rx B2 Byte or Tx Ring Port value.	Bits 5-8 of the Z2 Byte in the Tx Line Port Data are not overwritten.	
	3	INHTB1C	**Inhibit Tx B1 Counter**: accumulation of B1 errors at Tx Terminal Port inhibited.	accumulation of B1 errors at Tx Terminal Port enabled.	
	2	INHTB2C	**Inhibit Tx B2 Counter**: accumulation of B2 errors at Tx Terminal Port inhibited.	accumulation of B2 errors at Tx Terminal Port enabled.	
	1	STLRDI	**Send Tx Line RDI**: RDI-L inserted in Tx Line Port output data.	insertion of RDI-L at Tx Line Port Data not forced.	See TRLRDI.
	0	B2ELRDI	**B2 Excess BER Line RDI Enable**: Excess B2 Error condition included in equation for RDI-L insertion at Tx Line Port.	Excess B2 Error condition excluded from equation for RDI-L insertion at Tx Line Port.	Note 1 See TRLRDI.

Tx Line FEBE-L Insertion



Note 1. If B2MULT(2-0) = "110" or "111", control is disabled and Bit Equal to "0" condition applies.

CONTROL REGISTER 16

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
0FF	7	RETSEL	**Rx External Timing Select**: RRCI is 51.84 Mbit/s and Rx Reference Frame Input is $\overline{\text{RRFI}}$.	RRCI is 6.48 Mbit/s and Rx Reference Frame Input is RRFI	Note 1. See RCLK, Table 2.
	6	PRDISEL	**Path RDI Select**: RDI-P indication must be received for 5 consecutive frames for alarm declaration	RDI-P indication must be received for 10 consecutive frames for alarm declaration	
	5 4 3	B2MULT2 B2MULT1 B2MULT0	**B2 Excess BER Multiplier**: supplies the exponent for the B2BLK Parameter and disables the B2 Excess BER function. Normally set to 000. See Note 2. B2MULT2 / B2MULT1 / B2MULT0 / Scale Factor 0 0 0 10^0 0 0 1 10^1 0 1 0 10^2 0 1 1 10^3 1 0 0 10^4 1 0 1 10^5 1 1 0 disabled 1 1 1 disabled		B2 Excess BER calculation must be disabled when Parameters or the B2 Multiplier are changed
	2 1 0	B3MULT2 B3MULT1 B3MULT0	**B3 Excess BER Multiplier**: supplies the exponent for the B3BLK Parameter and disables the B3 Excess BER function. Normally set to 000. See Note 2. B3MULT2 / B3MULT1 / B3MULT0 / Scale Factor 0 0 0 10^0 0 0 1 10^1 0 1 0 10^2 0 1 1 10^3 1 0 0 10^4 1 0 1 10^5 1 1 0 disabled 1 1 1 disabled		B3 Excess BER calculation must be disabled when Parameters or the B3 Multiplier are changed.

Notes

1. This control is not effective if Pin $\overline{\text{MBEI}}$ is Low or if PARA or RCLK = "0".
2. When set to a non-zero value other than 110 or 111, the entire excessive BER Algorithm is scaled by the power of 10 listed. For example, setting B2MULT(2-0) = “010” multiplies the B2M value by 100, effectively multiplying the number of frames in a block by 100, making the threshold 100 times more sensitive to errors and extending the detection and clearing times 100 times longer.

CONTROL REGISTER 17

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DD	7	SDCCEN	**Section Datacom Select**: External D1-D3 Bytes are accepted from the Tx TOH Port.	External D1-D3 Bytes are accepted from the Tx Section DCC Port.	Note 1 See TRSD and TXSDEXT.
	6	LDCCEN	**Line Datacom Select**: External D4-D12 Bytes are accepted from the Tx TOH Port.	External D4-D12 Bytes are accepted from the Tx Line DCC Port.	Note 1 See TRLD and TXLDEXT.
	5	STLAIS	**Send Tx Line AIS**: AIS-L inserted in Tx Line Port Data	Insertion of AIS-L in Tx Line Port Data not forced	See TRAIS.
	4	TEST1	**TXC Test Mode 1**: test active	normal operation	
	3	TEST2	**TXC Test Mode 2**: test active	normal operation	
	2	LINLOOP	**Line Loop Back**: Rx Line input looped back to Tx Line output	normal operation	
	1	DISTB2R	**Disable Tx B2 Recalculation**: B2 Byte input at Tx Terminal Port is output at Tx Line Port.	B2 Byte output at Tx Line Port is calculated.	
	0	TPRDI20	**Transmit Path RDI 20 Times**: RDI-P sent for 20 frames or the duration of the causative event, whichever is longer.	RDI-P is sent for the duration of the causative event	

Note 1. If OA = "1", control is disabled and Bit Equal to "0" condition applies.

CONTROL REGISTER 18

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DC	7	J0RWEN	**J0 Read/Write Enable**: J0 Bytes accessed by µPro at addresses 080[H] - 0BF[H] (Rx Port J0 RAM Location) and 180[H] - 1BF[H] (Tx J0 Insert RAM Location)	J1 Bytes accessed by µPro at addresses 080[H] - 0BF[H] (Rx Port J1 RAM Location) and 180[H] - 1BF[H] (Tx J1 Insert RAM Location)	
	6	J0MLRDI	**J0 Mismatch Line RDI Enable**: J0 Mismatch condition included in equation for RDI-L insertion at Tx Line Port	J0 Mismatch condition excluded from equation for RDI-L insertion at Tx Line Port	effective only if J0EN(1,0) = "01" See TRLRDI.
	5	J0MLAIS	**J0 Mismatch Line AIS Enable**: J0 Mismatch condition included in equation for AIS-L insertion at Rx Terminal Port	J0 Mismatch condition excluded from equation for AIS-L insertion at Rx Terminal Port	effective only if J0EN(1,0) = "01"
	4 3	J0EN1 J0EN0	**J0 Enable(1,0)**: selects the J0 processing configuration J0EN1 J0EN0 Function 0 0 J0 processing inhibited. The Byte following A2 is a C1 Byte. 0 1 Single Byte J0 processing: J0MIS declared if Rx Side mismatch 1 0 16 or 64-byte message received and transmitted with incoming message (at Rx Line Port, Tx TOH Port, or Tx Terminal Port) stored in rotating fashion with no specific starting point. 1 1 64-byte message received and transmitted with incoming message (at Rx Line Port, Tx TOH Port, or Tx Terminal Port) stored such that the byte following ASCII (CR) and (LF) characters is stored in the Lowest address location		Notes 1, 2 See J0RWEN, TRC1 and TXC1EXT.
	2 1	TMBSEL1 TMBSEL0	**Tx Multiplex Bus Select (1,0)**: determines time slot assignment in 19.44 Mbyte/s modes for Tx Terminal Port. TMBSEL1 TMBSEL0 Time Slot 0 0 MBSEL(1,0) assignments used 0 1 First 1 0 Second 1 1 Third		effective only if Pin MBEI is Low See MBSEL0 and MBSEL1
	0	CHPRES	**Chip Reset:** ___ Acts like pin RST except that control registers and µPro interface are not affected. Normal operation is inhibited.	Terminates chip reset. Normal operation is resumed	

Notes:
1. If J0EN1 = "0" the Rx Line C1/J0 RAM Location is 01C[H] and the C1/J0 Tx Insert RAM Location is 13C[H].
2. If J0EN1 = "1" the Rx Line J0 Message RAM locations are accessed at 080[H] - 0BF[H] and the J0 Message Tx Insert RAM Locations are accessed at 180[H] - 1BF[H]. (J0RWEN must be set to access these J0 bytes.)

CONTROL REGISTER 19

Address [H]	Bit	Symbol	Conditions		Comments
			Bit Equal to "1"	Bit Equal to "0"	
1DB	7	Reserved	This bit must be set to "0".		
	6	Reserved	This bit must be set to "0".		
	5	TPRDISD	**Transmit Path RDI-SD**: RDI-PSD inserted in Tx Line Port Data	RDI-PSD not forced in Tx Line Port Data	Note 1
	4	TPRDICD	**Transmit Path RDI-CD**: RDI-PCD inserted at Ring Port Output and conditionally in Tx Line Port Data	RDI-PCD not forced in Tx Line Port Data	Notes 1, 2
	3	TPRDIPD	**Transmit Path RDI-PD**: RDI-PPD inserted at Ring Port Output and conditionally in Tx Line Port Data	RDI-PPD not forced in Tx Line Port Data	Notes 1, 2
	2	B3PRDISD	**B3 Excess BER Path RDI-SD Enable**: Excess B3 Error condition included in equation for RDI-PSD insertion at Tx Line Port	Excess B3 Error condition excluded from equation for RDI-PSD insertion at Tx Line Port	Note 3
	1	B3PRDICD	**B3 Excess BER Path RDI-CD Enable**: Excess B3 Error condition included in equation for RDI-PCD insertion at Tx Line Port	Excess B3 Error condition excluded from equation for RDI-PCD insertion at Tx Line Port	Note 3
	0	TOHPRDISD	**TOH Alarms Path RDI-SD Enable**: TOH conditions (RLOC, RLOS, RLOF, RAIS-P) included in equation for RDI-PSD insertion at Tx Line Port	TOH conditions excluded from equation for RDI-PSD insertion at Tx Line Port	

Notes:

1. RDI-PxD (where x = S, C or P) is inserted at the Tx Line Port by overwriting the selected bits of the G1 Byte. See TPRDIEN.
2. If RING = "0", TPRDICD or TPRDIPD = "1" will result in RDI-PCD/PD being inserted in the Tx Line Port Data. If RING and TPRDIEN = "1" then insertion of RDI-PCD/PD in the Tx Line Port Data will be controlled by the Ring Port Input Data.
3. This control is only enabled if B3MULT(2-0) ≠ "110" or "111".

OPERATION

In this section the following nomenclature is used to identify memory map register and bit locations:

(CRn; $y^{256}y^{16}y^{0}$[H], Bit z), (SRn; $y^{256}y^{16}y^{0}/y^{0}/y^{0}$[H], Bit z) and $y^{256}y^{16}y^{0}$[H]

where:	CRn	=	Control Register number n (0-19)
	SRn	=	Status Register number n (0-9)
	$y^{256}y^{16}y^{0}$	=	the Register's Address in Hex
	z	=	the Bit Number (0-7)

In the text which follows, the first occurrence of a Control Bit, Status Bit or Memory Location will be identified by the Bit's Symbol or Memory Location's name, and the location as described above. Subsequent references to that entity will not have the location identified. The locations of all Control and Status Bits can be found on pages 79 and 84.

PRIMARY OPERATING MODES

The PHAST-1 may be operated in any of three Primary Operating Modes (P.O.M.):

1. SONET
2. Datacom
3. SPE-only

The P.O.M. of the device determines the form and content of the information at the Rx and Tx Terminal Ports.

In SONET Mode the Terminal Side information consists of the full SONET Format (TOH and SPE consisting of POH and Payload). The Control Signals are used to differentiate between the TOH and SPE portions. The Rx Terminal Port Data, Clock and Control Signals are all outputs. The Tx Terminal Port Data, Clock and Control Signals are all inputs. When this mode of operation is used, an external source is required to create the Tx Terminal Port Timing and Control signals.

The Terminal Side information in Datacom Mode is the same as for SONET Mode. However, the Control Signals can be configured to gap out the POH byte times. The Rx Terminal Port Data, Clock and Control Signals are all outputs. The Tx Terminal Port Clock and Control Signals are outputs and the Data is input. With this operating mode an external timing generator, for Tx Terminal Port timing and control, is not required.

The Terminal I/O in SPE-only mode consists only of the SPE portion of the SONET signal. The TOH Bytes are not present. The Rx Terminal Port Data, Clock and Control Signals are all outputs. The Tx Terminal Port Data, Clock and Control Signals are all inputs. When this mode of operation is used an external source is required to create the Tx Terminal Port Timing and Control Signals.

In SONET and Datacom modes, the Rx and Tx Terminal Ports can be configured for Serial I/O at 51.84 Mbit/s or Parallel I/O at either 6.48 Mbyte/s or 19.44 Mbyte/s. When SPE-only Mode is selected, Rx and Tx Terminal Port operation is restricted to Serial I/O. The controls SPE (CR10; 1FA[H], Bit 7), DATACOM (CR5; 0FD[H], Bit 6) and the Pin $\overline{\text{MBEI}}$ are used to define the P.O.M. Serial or parallel operation is invoked with the control PARA (CR2; 0FA[H], Bit 6) The interaction of these controls is hierarchical in nature as shown in Table 1.

Pin $\overline{\text{MBEI}}$	SPE	DATACOM	PARA	P.O.M.
Low	-	0	-	Parallel SONET - 19.44 Mbyte/s
Low	-	1	-	Parallel Datacom - 19.44 Mbyte/s
High	0	0	0	Serial SONET
High	0	0	1	Parallel SONET - 6. 48 Mbyte/s
High	0	1	0	Serial Datacom
High	0	1	1	Parallel Datacom - 6. 48 Mbyte/s
High	1	-	0	SPE-only

Table 1. Primary Operating Modes

There are two additional Tx Terminal Port Modes that are invoked when SONET Mode is selected. These are C1J1 Mode and Framing Mode. They are controlled by C1J1EN (CR6; 0FE[H], Bit 1). When set to "1", Frame Delineation is accomplished with the signals TSYNI/O and TSPEI/O. When set to "0", the incoming A1/A2 and H1/H2 Bytes are used to determine Frame and SPE alignment.

TIMING GENERATORS

The PHAST-1 contains two timing generators. They are the Terminal Timing Generator and the Line Timing Generator. These reside in the Receive Side and Transmit Side, respectively (see Figure 14).

Terminal Timing Generator

The Terminal Timing Generator (TTG) creates the signals required for the Rx Re-timing FIFO (when Receive Re-timing is enabled), the Rx Terminal Generator and the Rx Terminal Port. The external inputs to the TTG are the pins RRCI and RRFI/$\overline{\text{RRFI}}$. RRFI/$\overline{\text{RRFI}}$ is active High when RRCI is 6.48 or 19.44 Mbit/s and active Low when RRCI is 51.84 Mbit/s. The use of RRFI/$\overline{\text{RRFI}}$ is optional. If a frame pulse is not supplied, the start of the frame generated at the Rx Terminal Port will be arbitrary. If it is not used, RRFIEN (CR3; 0FB[H], Bit 7) should be set to "0" to prevent alarm generation. When employed, the generated frame will track the reference frame. If RRFI/$\overline{\text{RRFI}}$ fails, the alignment of the generated frame will be maintained. Any change in position of RRFI/$\overline{\text{RRFI}}$ is reported as Rx Reference Change of Frame Alignment - RRCOFA (SR4; 1F2/3/5[H], Bit 7). The Loss Of Rx Reference (RRCI and/or RRFI/$\overline{\text{RRFI}}$) is reported as LORR (SR4; 1F2/3/5[H], Bit 6).

The combination of RRCI and $\overline{\text{RRFI}}$, where RRCI is 51.84 Mbit/s, must be used when serial outputs are desired at the Rx Terminal Port and may optionally be used for 6.48 Mbyte/s parallel outputs. RRCI at 6.48 Mbit/s and RRFI may optionally be used when the Rx Terminal Port is operating in parallel mode at 6.48 Mbyte/s. The combination of RRCI and RRFI, where RRCI is 19.44 Mbit/s, must be used when the Rx Terminal Port is operating in parallel mode at 19.44 Mbyte/s. In addition to the external signals mentioned above, the TTG may also utilize internal signals generated by the Rx TOH Processor. These internal signals are referred to as RXCK (51.84 Mbit/s clock) and $\overline{\text{RXFR}}$ (frame). This latter combination may only be used for 51.84 Mbit/s serial and 6.48 Mbyte/s parallel output modes. The availability of internal or external inputs to the TTG provides two Receive Timing Modes: Line Timing or External Rx Timing.

Reference Clock selection is controlled by RCLK (CR10; 1FA[H], Bit 5), RETSEL (CR16; 0FF[H], Bit 7) and the Pin $\overline{\text{MBEI}}$. The settings for these controls are given in Table 2. RCLK determines whether Line Timing or External Rx Timing is employed. When External Receive Timing is selected (RCLK = "1"), RETSEL Selects Parallel or Serial Reference sets for 6.48 Mbit/s. Parallel Reference is selected when RETSEL = "0". $\overline{\text{MBEI}}$, when Low, selects 19.44 Mbit/s operation. In those configurations where RXCK or RRCI at 51.84 Mbit/s are selected, both serial and 6.48 Mbyte/s parallel outputs are active.

Pin $\overline{\text{MBEI}}$	RCLK	RETSEL	Timing Mode	Clock Input	Frame Input	Rx Terminal Output
Low	-	-	External Rx Timing	RRCI 19.44 Mbit/s	RRFI	19.44 Mbyte/s Parallel
High	0	-	Line Timing	RXCK 51.84 Mbit/s	$\overline{\text{RXFR}}$	1. Serial 2. 6.48 Mbyte/s Parallel
High	1	0	External Rx Timing	RRCI 6.48 Mbit/s	RRFI	Serial SONET
High	1	1	External Rx Timing	RRCI 51.84 Mbit/s	$\overline{\text{RRFI}}$	1. Serial 2. 6.48 Mbyte/s Parallel

Table 2. Rx Timing Selection

Line Timing Generator

The Line Timing Generator (LTG) creates the signals required for the Tx Re-timing FIFO (when Transmit Re-timing is enabled) and the Tx TOH Generator. In addition, it supplies the timing information to the Tx Terminal Port in Datacom Mode. There are two sets of external inputs. The pins TLCI (51.84 Mbit/s clock) and $\overline{\text{TFRI}}$ are used for Tx Line Timing. In Datacom Mode, pins DRCI and DFRI/$\overline{\text{DFRI}}$) are used for Tx Terminal Port Timing. DFRI/$\overline{\text{DFRI}}$ is active High when DRCI is 6.48 or 19.44 Mbit/s and active Low when DRCI is 51.84 Mbit/s. The use of $\overline{\text{TFRI}}$ and/or DFRI/$\overline{\text{DFRI}}$ is optional. If they are not used the start of the frame output at the Tx Line Port ($\overline{\text{TFRI}}$) and the Tx Terminal Port, in Datacom Mode, ($\overline{\text{DFRI}}$/$\overline{\text{DFRI}}$) will be arbitrary. If $\overline{\text{TFRI}}$ and/or DFRI/$\overline{\text{DFRI}}$ are not used the controls TFRIEN (CR12; 1FC[H], Bit 2) and/or DFRIEN (CR12; 1FC[H], Bit 1) should be set to "0" to prevent alarm generation. Loss Of Tx Reference is reported as LOTR (SR5; 1E8/9/C[H], Bit 1). This alarm is for clock and frame of both reference sets.

In Datacom Mode, the Tx Terminal Port clock and control signals (TTCI/O, TPCI/O, TSYNI/O and TSPEI/O are outputs generated from DRCI and DFRI/$\overline{\text{DFRI}}$. The Pin $\overline{\text{MBEI}}$ and the controls PARA and DETSEL (CR10; 1FA[H], Bit 2) select 51.84, 6.48, or 19.44 Mbit/s reference sets as shown in Table 3. The Generated Frame will always track the Reference Frame. As long as the clock input is valid, loss of DFRI/$\overline{\text{DFRI}}$ does not impair the output at the Tx Terminal Port. The Frame alignment prior to the framing pulse loss will be maintained. Any DFRI/$\overline{\text{DFRI}}$ pulse that varies from the previous position will be reported as a Datacom Reference Change Of Frame Alignment - DRCOFA (SR5; 1E8/9/C[H], Bit 2). If DFRI/$\overline{\text{DFRI}}$ is not present then the generated frame alignment will be arbitrary.

Pin $\overline{\text{MBEI}}$	PARA	DETSEL	DRCI Mbit/s	Frame Input	Tx Terminal Port Mode
Low	-	-	19.44	DFRI	19.44 Mbyte/s Parallel
High	0	-	51.84	$\overline{\text{DFRI}}$	Serial
High	1	0	6.48	DFRI	6. 48 Mbyte/s Parallel
High	1	1	51.84	$\overline{\text{DFRI}}$	6. 48 Mbyte/s Parallel

Table 3. Datacom Mode Timing Selection

The timing source for the Tx Line may be either the external references TLCI and $\overline{\text{TFRI}}$, DRCI and $\overline{\text{DFRI}}$ in Datacom Mode, or the Tx Terminal Port signals TTCI/O and TSYNI/O. The first option is referred to as External Tx Timing. The latter two options constitute Terminal Timing, which can only be used in the serial, SONET or Datacom Modes. The selection is controlled by TCLK (CR10; 1FA[H], Bit 6), DETSEL, PARA and the Pin $\overline{\text{MBEI}}$. The settings for these controls are shown in Table 4. If TCLK = "0" and the Tx Terminal Port is in a configuration which does not have a 51.84 Mbit/s clock, TLCI and $\overline{\text{TFRI}}$ must be supplied with the relationship shown in Figure 20. This setting (TCLK = "0") is used in those special applications where the line clock (TLCO) needs to be synchronous with the terminal clock (TPCI) so that either transmit re-timing can be turned off (TXRTM = "0") or some of the Tx terminal TOH bytes (TPDI(7-0)) can be relayed to the Tx line output TLDO. If an external frame signal is not present when External Tx Timing is employed then the generated frame alignment will be arbitrary. When present, $\overline{\text{TFRI}}$, $\overline{\text{DFRI}}$, or TSYNI/O is used to synchronize the transmitted frame to the reference frame. The Transmit frame will always track the Reference Frame. As long as the associated clock (TLCI, DRCI, or TTCI/O) input is valid, loss of the framing pulse does not impair the output at the Tx Line. The Frame alignment prior to the framing pulse loss will be maintained. Any frame pulse ($\overline{\text{TFRI}}$) that varies from the previous position will be reported as a Transmit Reference Change Of Frame Alignment - TRCOFA (SR5; 1E8/9/C[H], Bit 3). In SONET Mode, if C1J1EN = "0", the A1 and A2 Bytes of the Input Signal at the Tx Terminal Port are used for Frame Delineation instead of TSYNI/O. If Terminal Timing is selected, with this option enabled, the start of the generated Tx Line Port Frame will be determined by the A1 and A2 bytes and not by TSYNI/O.

Pin $\overline{\text{MBEI}}$	P.O.M.	TCLK	PARA	DETSEL	Timing Mode	Clock Input	Frame Input
Low	-	-	-	-	External Tx Timing	TLCI	$\overline{\text{TFRI}}$
High	SPE-only	-	0	-	External Tx Timing	TLCI	$\overline{\text{TFRI}}$
	Datacom	0	0	-	Terminal Timing	DRCI	$\overline{\text{DFRI}}$
		0	1	0	External Tx Timing	TLCI	$\overline{\text{TFRI}}$
		0	1	1	Terminal Timing	DRCI	$\overline{\text{DFRI}}$
		1	-	-	External Tx Timing	TLCI	$\overline{\text{TFRI}}$
	SONET	0	0	-	Terminal Timing	TTCI/O	TSYNI/O or A1/A2
		0	1	-	External Tx Timing	TLCI	$\overline{\text{TFRI}}$
		1	-	-	External Tx Timing	TLCI	$\overline{\text{TFRI}}$

Table 4. Tx Timing Selection

RE-TIMING

Re-timing can be independently selected in the Transmit and Receive Sides. When not enabled, the Rx Re-timing and/or Tx Re-timing FIFOs are bypassed.

Rx Side

Receive re-timing is always performed in SPE-only Mode and all parallel modes operating at 19.44 Mbyte/s. Receive Re-timing is an option for the following modes:

1. Serial and 6.48 Mbyte/s Parallel SONET
2. Serial and 6.48 Mbyte/s Parallel Datacom

Receive re-timing is controlled by the Pin $\overline{\text{MBEI}}$, RCLK and RXRTM (CR9; 1F9[H], Bit 1). As shown in Table 5, the interaction of these bits is hierarchical in nature.

Pin $\overline{\text{MBEI}}$	P.O.M.	RCLK	RXRTM	Rx Re-Timing
Low	-	-	-	Enabled
High	SPE-only	-	-	Enabled
	Serial and 6. 48 Mbyte/s Parallel SONET or Data-com	0	0	Enabled
		0	1	Disabled
		1	-	Enabled

Table 5. Rx Re-Timing Control

When Rx Re-timing is performed, the Rx Re-timing FIFO is the elastic store between the Rx POH Processor and the Rx Terminal Generator. The inputs to the FIFO are the SPE Portion of the Rx Line signal. Information is clocked in at the line rate. The Terminal Timing Generator provides the read clock and the signals necessary for Pointer Generation. The new Pointer is calculated and Positive or Negative Justifications are made, as necessary, to prevent FIFO overflow or underflow. The values placed in the "SS" Bit positions of the H1 Byte are determined by the controls S0 and S1 (CR6; 0FE[H], Bits 2 and 3). All justifications are accumulated by the Local PJ Counter (022[H]). Counter overflow is indicated by LPJOF (SR7; 0F6[H], Bit 0). FIFO underflow or overflow is reported as Rx FIFO Error - RFIFOE (SR4; 1F2/3/5[H], Bit 5). Automatic recovery from an underflow or overflow condition can be enabled with RFREN (CR3; 0FB[H], Bit 6). The FIFO may also be re-centered with RRFIFO (CR3; 0FB[H], Bit 5).

Tx Side

Transmit re-timing is always performed in SPE-only Mode, SONET Mode where TSYNI/O is enabled and when TCLK = "1". It is an option for Datacom Mode and SONET Modes having valid A1, A2, H1 and H2 Bytes at the Tx Terminal Port. Transmit re-timing is controlled by the bits C1J1EN, TCLK and TXRTM (CR10; 1FA[H], Bit 3). As shown in Table 6, the interaction of these bits is hierarchical in nature.

The Tx Re-timing FIFO is the elastic store between the Tx Terminal Processor and the Tx OH Generator, when re-timing is performed. The inputs to the FIFO are the SPE Portion of the Tx Terminal Signal. Information is clocked in at the terminal rate. The LTG provides the read clock and the signals necessary for Pointer Generation. The new Pointer is calculated and Positive or Negative Justifications are made, as necessary, to prevent FIFO overflow or underflow. The values used for the H1 Byte "SS" bits are determined by the controls S0 and S1. Pointer Increments and Decrements can be forced with INC and DEC (CR10; 1FA[H], Bits 1 and 0)*. FIFO underflow or overflow is reported as Tx FIFO Error - TFIFOE (SR5; 1E8/9/C[H], Bit 0). Automatic recovery from an underflow or overflow condition can be enabled with TFREN (CR12; 1FC[H], Bit 7). The FIFO may also be re-centered with RTFIFO (CR12; 1FC[H], Bit 6).

P.O.M.	TCLK	C1J1EN	TXRTM	Tx Re-Timing
SPE-only	-	-	-	Enabled
Datacom	0	-	0	Disabled
	0	-	1	Enabled
	1	-	-	Enabled
SONET	0	0	0	Disabled
	0	0	1	Enabled
	0	1	-	Enabled
	1	-	-	Enabled

Table 6. Tx Re-Timing Control

* These features must be used judiciously. If either is enabled, disabling must occur within two Frames to prevent multiple PJs. In addition, consecutive, forced PJs may cause FIFO spills.

LINE FORMATS

The Line Formats for the PHAST-1 are designed for use in two applications. The first is for use in a native STS-1 Environment. The second is for use in a situation where the PHAST-1 is preceded, on the Line Side, by additional circuitry such as an STS-1 to STS-N multiplexer. The choice of applications is controlled by STS1 (CR2; 0FA[H], Bit 7). When set to "1", the Line Side signals are treated as an STS-1.

Rx Line Port Format

The inputs at the Rx Line Port are RLDI, $\overline{\text{RFRI}}$, RLCI and $\overline{\text{RXLOS}}$. RLDI and $\overline{\text{RFRI}}$ are clocked in on the Rising Edge of RLCI. $\overline{\text{RXLOS}}$ is an optional asynchronous input from an external LOS detector.

If STS1 = "1":
1. Full framing is performed using the A1 and A2 Bytes and $\overline{\text{RFRI}}$ is ignored.
2. The B1 Errors are calculated using the B1 Byte.
3. Unscrambling is performed.

If STS1 = "0":
1. The input $\overline{\text{RFRI}}$ is enabled and a partial framing algorithm is employed where the A1 and A2 Bytes are used to verify the frame position defined by $\overline{\text{RFRI}}$.
2. The content of the B1 Byte is interpreted as a count of B1 Errors.
3. Unscrambling is not performed.

Tx Line Port Format

If STS1 = "1"
1. B1 Parity is calculated and placed in the B1 Byte.
2. Scrambling is performed.

If STS1 = "0"
1. The outgoing B1 Byte contains a mask that can be used to create B1 Parity errors.
2. Scrambling is not performed.

The Tx Line Port Outputs are TLDO and TLCO, where TLDO is clocked out on the Falling Edge of TLCO. The relationship between TLCO, TLDO and the reference inputs used by the LTG is shown in Figure 53. When External Transmit Timing is employed the MSB of the A1 Byte on TLDO occurs 3½ bit times after $\overline{\text{TFRI}}$ is sampled. If Terminal Timing is employed the MSB of the A1 Byte is as follows:

Serial SONET
1. C1J1EN = "0" - 22½ bit times after the MSB of the A1 Byte input at TTDI is sampled by TTCI/O
2. C1J1EN = "1" - 6½ bit times after the Rising Edge of TSYNI/O and the Falling Edge of TSPEI/O is sampled by TTCI/O

Datacom Mode, PARA = "0"
1. TDDLY = "0" - 7½ bit times after $\overline{\text{DFRI}}$ is sampled by DRCI
2. TDDLY = "1" - 10½ bit times after $\overline{\text{DFRI}}$ is sampled by DRCI

Datacom Mode, PARA = "1"
1. TDDLY = "0" - 12 bit times after DFRI is sampled by DRCI
2. TDDLY = "1" - 20 bit times after DFRI is sampled by DRCI

TDDLY is (CR12; 1FC[H], Bit 0).

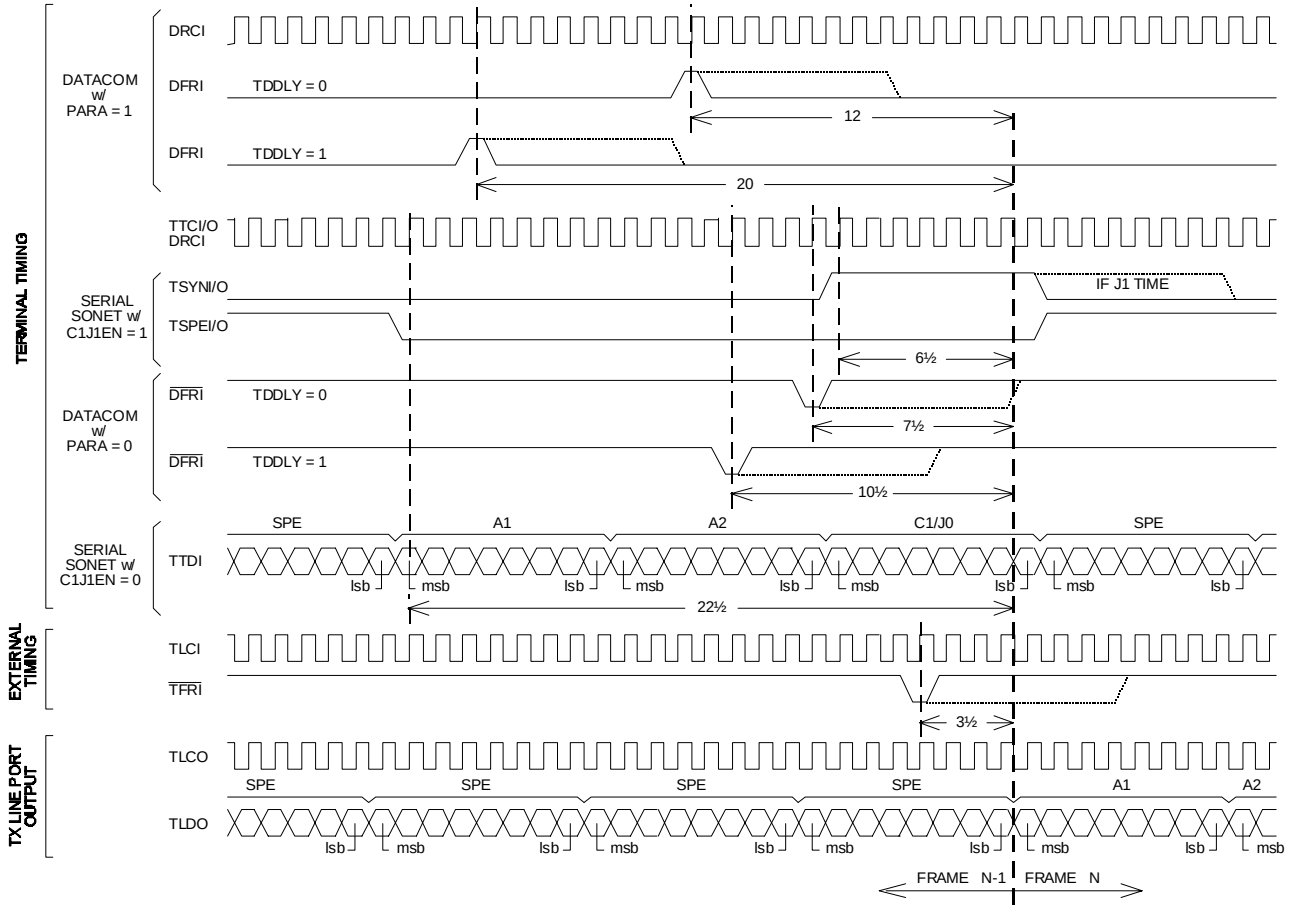


Figure 53. Tx Line Format

TERMINAL FORMATS

All of the following descriptions assume that the generated frame is synchronized to a reference frame pulse. If the applicable reference frame signal is not provided then the start of the generated frame at the Rx Terminal Port and/or the Tx Terminal Port, in Datacom Mode, will be arbitrary.

Serial SONET

The Rx Terminal Port Serial SONET Format is shown in Figure 54. The Reference inputs may be either RRCI/RRFI or RXCK/RXFR. The external reference frame pulse (RRFI) may be from one to eight clock periods in duration. RTDO is output on the Falling Edge of RTCO. The order of output is MSB → LSB. RSPE is Low during the TOH Byte Times. RSYN is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control bit H4INT (CR6; 0FE[H], Bit 5) is set to "1".

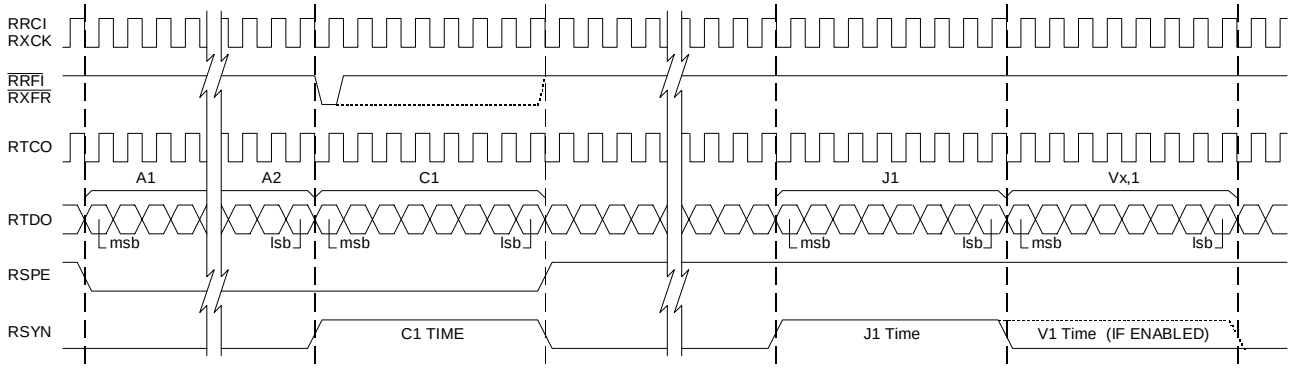


Figure 54. Rx Terminal Port Serial SONET Format

The Tx Terminal Port Serial SONET Format is shown in Figure 55. TTCI/O is the 51.84 Mbit/s input clock. TTDI is the serial data where the order of input is MSB → LSB. TTDI, TSPEI/O and TSYNI/O are clocked in on the Rising Edge of TTCI/O. Input Frame Delineation is controlled by C1J1EN. When set to "0", TSYNI/O and TSPEI/O are disregarded and the incoming A1/A2 and H1/H2 Bytes are used to determine Frame and SPE alignment. If C1J1EN = "1" the information content of the A1, A2, H1 and H2 Bytes is disregarded and TSPEI/O and TSYNI/O are enabled. TSPEI/O is Low during the TOH Byte Times. TSYNI/O is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1".

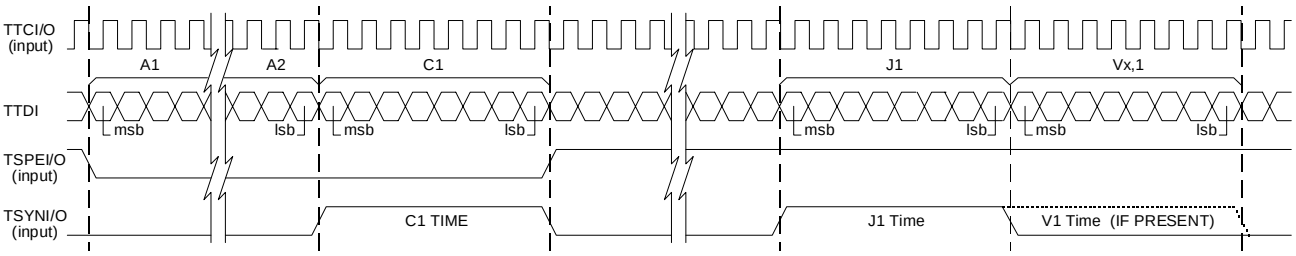


Figure 55. Tx Terminal Port Serial SONET Format

6.48 Mbyte/s Parallel SONET

Figure 56 depicts the Rx Terminal Port Parallel 6.48 Mbyte/s SONET Format. The Reference inputs may be either RRCI/RRFI, RXCK/RXFR, or RRCI/RRFI. The external reference frame pulses (RRFI or RRFI) may be from one to eight clock periods in duration. TPDO0 through TPDO7 are the byte wide data outputs where the LSB is TPDO0. RSPE is Low during the TOH Byte Times. RSYN is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". The polarity of TPCO can be inverted with the control INVPCK (CR5; 0FD[H], Bit 3). A value of "0" results in TPDO(0-7), RSPE, RSYN and TPARO being output on the Falling Edge. When INVPCK = "1", the information is output on the Rising Edge of TPCO.

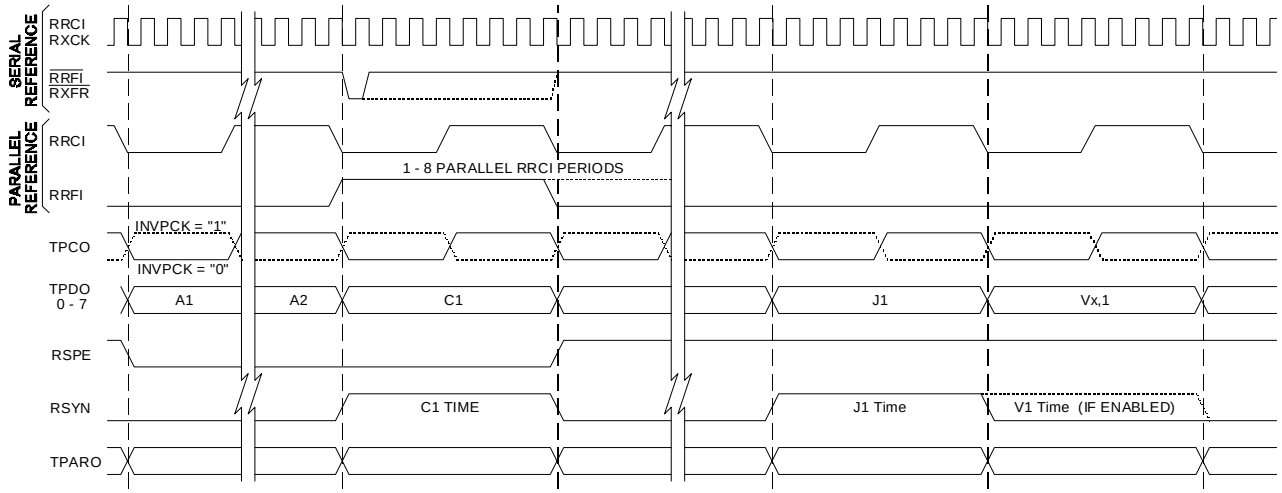


Figure 56. Rx Terminal Port Parallel 6.48 Mbyte/s SONET Format

Figure 57 depicts the Tx Terminal Port Parallel 6.48 Mbyte/s SONET Format. TPCI/O is the 6.48 Mbit/s input clock. TPDI0 through TPDI7 are the byte wide data inputs where the LSB is TPDI0. When INVPCK = "0", TPDI(0-7), TSPEI/O, TSYNI/O and TPARI are clocked in on the Rising Edge of TPCI/O. TPDI(0-7), TSPEI/O, TSYNI/O and TPARI are clocked in on the Falling Edge of TPCI/O if INVPCK = "1". Input Frame Delineation is controlled by C1J1EN. When set to "0", TSYNI/O and TSPEI/O are disregarded and the incoming A1/A2 and H1/H2 Bytes are used to determine Frame and SPE alignment. If C1J1EN = "1" the information content of the A1, A2, H1 and H2 Bytes is disregarded and TSPEI/O and TSYNI/O are enabled. TSPEI/O is Low during the TOH Byte Times. TSYNI/O is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1".

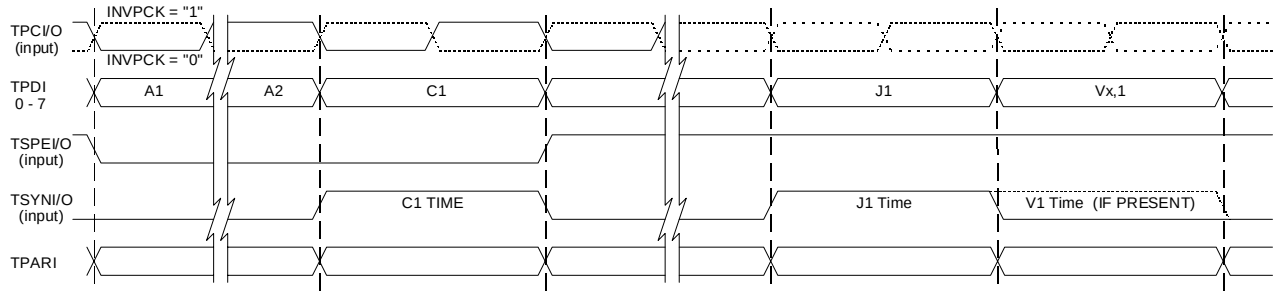


Figure 57. Tx Terminal Port Parallel 6.48 Mbyte/s SONET Format

19.44 Mbyte/s Parallel SONET

The Rx Terminal Port Parallel 19.44 Mbyte/s SONET Format is shown, generically, in Figure 58. This represents the complete bus structure. It consists of three 6.48 Mbyte/s parallel buses multiplexed together. The TOH Byte positions are aligned. The SPE Portions may not be aligned. The Reference inputs must be RRCI and RRFI. RRFI may be from one to three clock periods in duration. TPCO is the 19.44 Mbit/s output clock. TPDO0 through TPDO7 are the byte wide data outputs, where the LSB is TPDO0. RSPE is Low during the TOH Byte Times. RSYN is High during the C1 (slot #1 only), J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". The polarity of TPCO can be inverted with the control INVPCK. A value of "0" results in TPDO(0-7), RSPE, RSYN and TPARO being output on the Falling Edge. When INVPCK = "1", the information is output on the Rising Edge of TPCO. The outputs TPDO(0-7), RSPE, RSYN and TPARO will only be active for the portion of the bus the PHAST-1 is generating. Any single PHAST-1 will create one third of the composite bus. STS-1 Selection is controlled by MBSEL0 and MBSEL1 (CR5; 0FD[H], Bits 1 and 2). However, if the bus is only partially populated, outputs can be activated for either one or both of the unassigned slots. ENFSTUA and ENLSTUA (1DE[H] bits 1 and 0) will cause the first or last unassigned slots, respectively, to be driven rather than tri-stated.

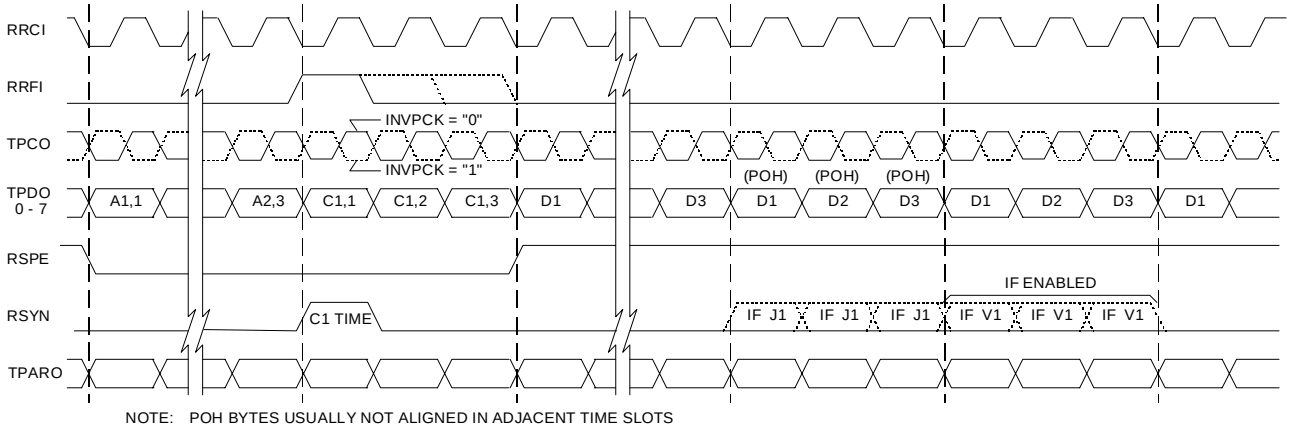


Figure 58. Rx Terminal Port Parallel 19.44 Mbyte/s SONET Format

Figure 59 shows the outputs of a PHAST-1 configured for the first STS-1 in the 19.44 Mbyte/s Bus.

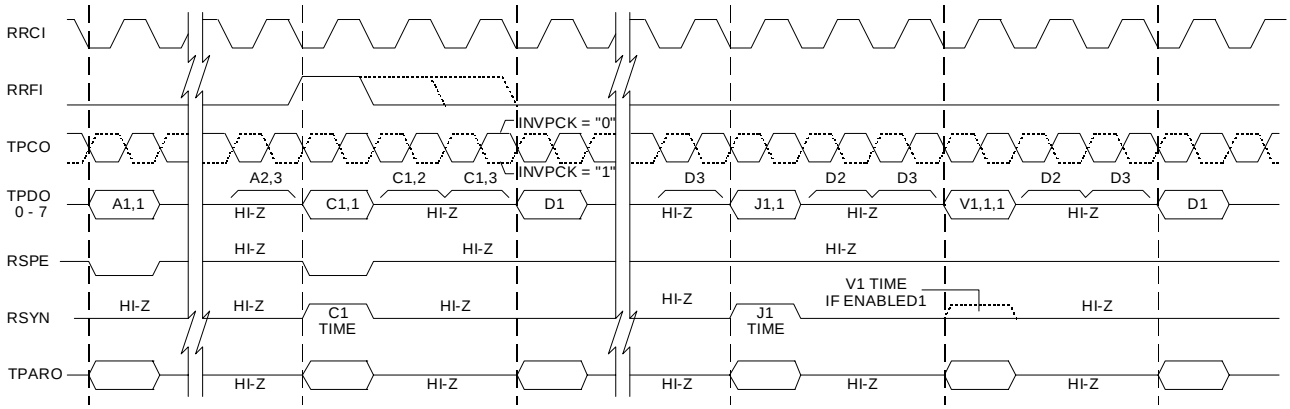


Figure 59. Rx Terminal Port Parallel 19.44 Mbyte/s SONET FORMAT Example

Figure 60 depicts the Tx Terminal Port Parallel 19.44 Mbyte/s SONET Format which, again, consists of three 6.48 Mbyte/s parallel buses multiplexed together. The TOH Byte positions are aligned. The SPE Portions may not be aligned. TPCI/O is the 19.44 Mbit/s input clock. TPDI0 through TPDI7 are the byte wide data inputs where the LSB is TPDI0. When INVPCK = "0", TPDI (0-7), TSPEI/O, TSYNI/O and TPARI are clocked in on the Rising Edge of TPCI/O. TPDI(0-7), TSPEI/O, TSYNI/O and TPARI are clocked in on the Falling Edge of TPCI/O if INVPCK = "1". Input Frame Delineation is controlled by C1J1EN. When set to "0", TSYNI/O and TSPEI/O are disregarded and the incoming A1/A2 and H1/H2 Bytes are used to determine Frame and SPE alignment. If C1J1EN = "1" the information content of the A1, A2, H1 and H2 Bytes is disregarded and TSPEI/O and TSYNI/O are enabled. TSPEI/O is Low during the TOH Byte Times. TSYNI/O is High during the C1 (slot #1 only), J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". TMBSEL0 and TMBSEL1 (CR18; 1DC[H], Bits 1 and 2) determine which third of the bus is used.

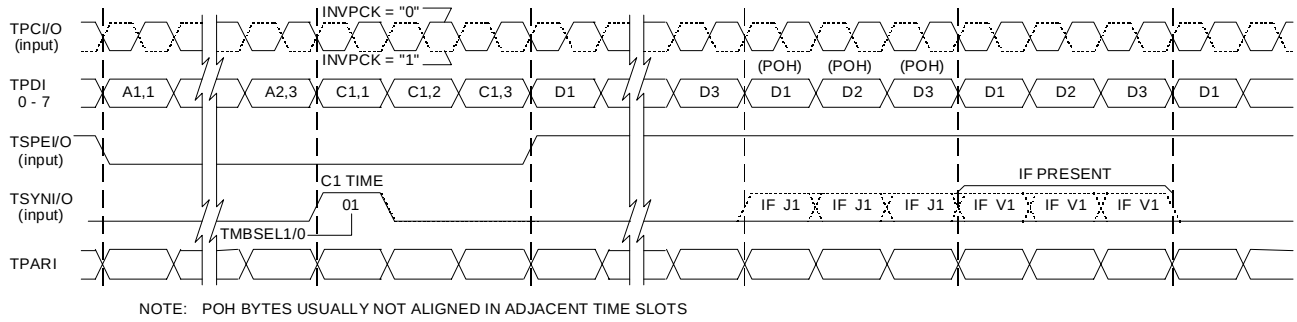


Figure 60. Tx Terminal Port Parallel 19.44 Mbyte/s SONET Format

Serial Datacom

The Rx Terminal Port Serial Datacom Format is shown in Figure 61. The Reference inputs may be either RRCI/RRFI or RXCK/RXFR. The external reference frame pulse (RRFI) may be from one to eight clock periods in duration. RTDO is output on the Falling Edge of RTCO. The order of output is MSB → LSB. RSPE is Low during the TOH and, optionally, the POH Byte Times. ENDCMPOH (CR5; 0FD[H], Bit 5) controls the state of RSPE during the POH Byte times. ENDCMPOH = "0" results in RSPE transitioning Low during these Byte times. If ENDCMPOH = "1", RSPE remains High during these Byte times. RSYN is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1".

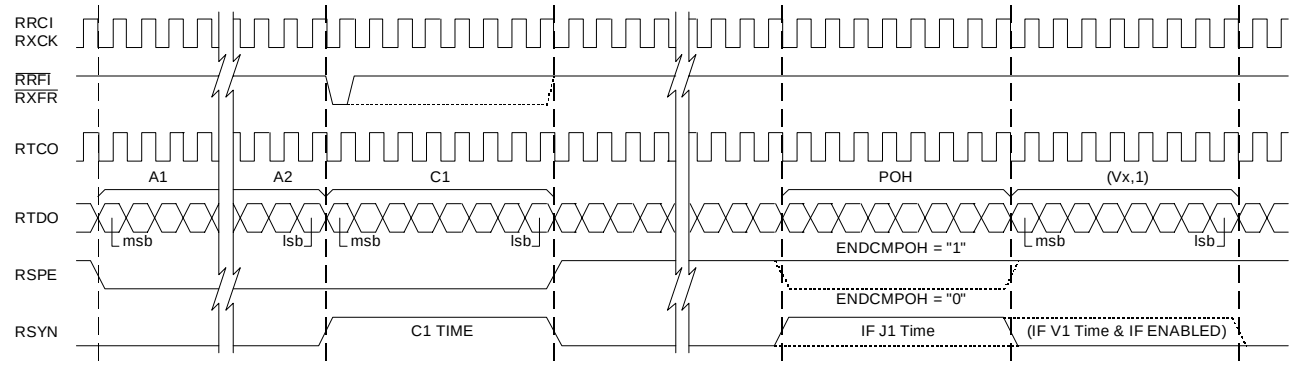


Figure 61. Rx Terminal Port Serial Datacom Format

The Tx Terminal Port Serial Datacom Format is shown in Figure 62. DRCI/$\overline{\text{DFRI}}$ are the Reference Inputs. TTCI/O, TSPEI/O and TSYNI/O are outputs. TSPEI/O is used by the sourcing device for clock gapping. TSPEI/O is Low during the TOH Byte Times. ENDCMPOH controls the state of TSPEI/O during the POH Byte times. ENDCMPOH = "0" results in TSPEI/O transitioning Low during these Byte times. If ENDCMPOH = "1", TSPEI/O remains High during these Byte times. TSYNI/O is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". The Falling Edge of TTCI/O is used to output TSPEI/O and TSYNI/O and the Rising Edge is used to input TTDI. The order of input is MSB → LSB. TDDLY is used to determine the delay time from TSPEI/O transitioning High to sampling of the MSB. The sending device will normally output data on the Rising Edge. A setting of "0" results in a 1½ bit delay. When set to "1" the delay is 4½ bits.

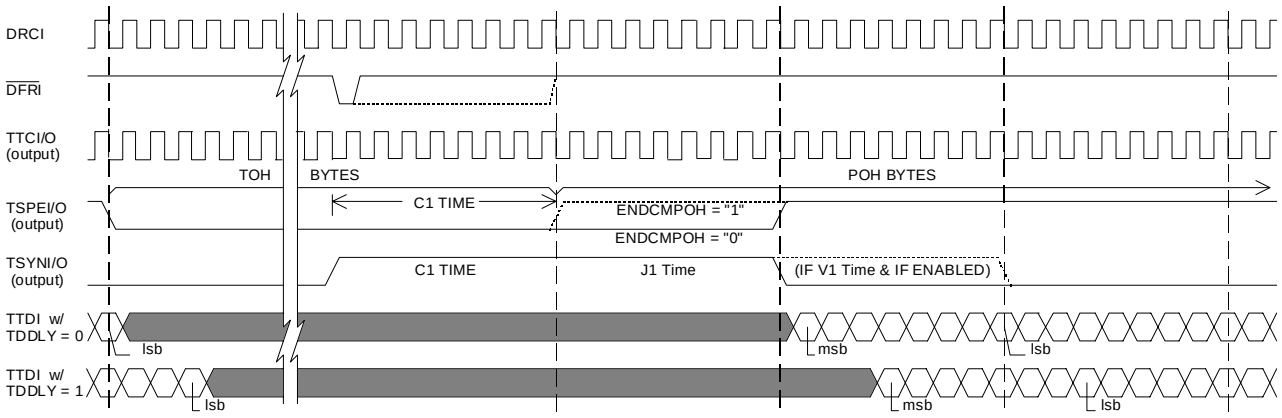


Figure 62. Tx Terminal Port Serial Datacom Format

6.48 Mbyte/s Parallel Datacom

Figure 63 depicts the Rx Terminal Port Parallel 6.48 Mbyte/s Datacom Format. The Reference inputs may be either RRCI/RRFI, RXCK/RXFR, or RRCI/RRFI. The external reference frame pulses (RRFI or RRFI) may be from one to eight clock periods in duration. TPCO is the 6.48 Mbit/s output clock, which may be continuous or may be gapped. TPDO0 through TPDO7 are the byte wide data outputs where the LSB of the byte is output on TPDO0. RSPE is Low during the TOH and, optionally, POH Byte Times. RSYN is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". Two controls regulate TPCO gapping. They are DISPCKG (CR5; 0FD[H], Bit 4) and ENDCMPOH. DISPCKG is only effective in this mode. When DISPCKG is set to "1" TPCO will be continuous. A setting of "0" will introduce gaps in TPCO during the TOH Byte Times. ENDCMPOH controls the gapping of the POH Bytes when DISPCKG = "0". If ENDCMPOH = "0", TPCO is also gapped during the POH Byte times. When ENDCMPOH = "1", there will be no gaps in TPCO during these Byte times if DISPCKG = "0". ENDCMPOH also controls the state of RSPE during these Byte times. This function is independent of the setting of DISPCKG. ENDCMPOH = "0" results in RSPE transitioning Low during the POH Byte times. If ENDCMPOH = "1", RSPE remains High during these Byte times. The polarity of TPCO can be inverted with the control INVPCK. A value of "0" results in TPDO(0-7), RSPE, RSYN and TPARO being output on the Falling Edge. When INVPCK = "1", these signals are instead output on the Rising Edge of TPCO.

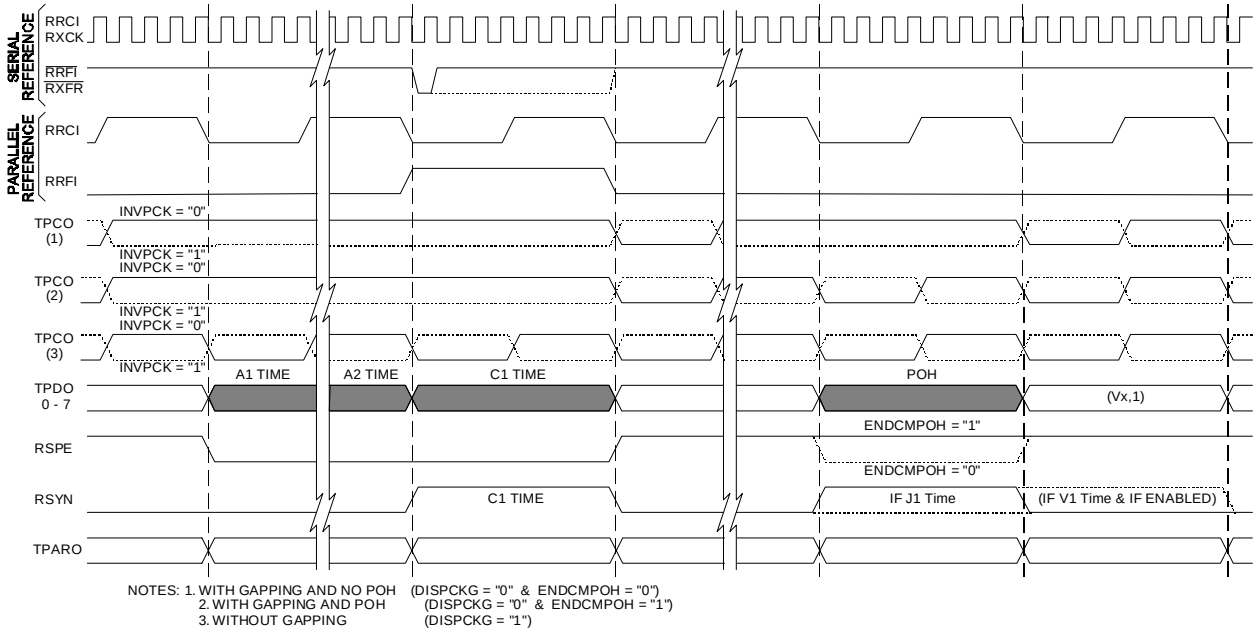


Figure 63. Rx Terminal Port Parallel 6.48 Mbyte/s Datacom Format

Figure 64 shows the Tx Terminal Port Parallel 6.48 Mbyte/s Datacom Format. DRCI/DFRI is shown for both serial and parallel Reference Inputs. The reference frame pulses may be from one to eight clock periods in duration. TPCI/O is the 6.48 Mbit/s output clock, which may be continuous or may be gapped. TPDI0 through TPDI7 are the byte wide data inputs where the LSB is TPDI0. TSPEI/O is Low during the TOH and, optionally, POH Byte Times. TSYNI/O is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". The control DISPCKG regulates TPCI/O gapping. When DISPCKG is set to "1", TPCI/O is continuous. A setting of "0" introduces gaps in TPCI/O during the TOH Byte times (when ENDCMPOH = "1"), or during both TOH and POH Byte times (when ENDCMPOH = "0"). ENDCMPOH also controls the state of TSPEI/O during POH Byte times. This function is independent of the setting of DISPCKG. ENDCMPOH = "0" results in TSPEI/O transitioning Low during the POH Byte times. If ENDCMPOH = "1", TSPEI/O remains High during these Byte times. The polarity of TPCI/O can be inverted with the control INVPCK. INVPCK = "0" results in TSPEI/O and TSYNI/O being output on the Falling Edge and TPDI(0-7) and TPARI being sampled on the Falling Edge. When INVPCK = "1", the Rising Edge is used for both output and input. TDDLY is used to determine the delay time from TSYNI/O transitioning High to sampling of the data on TPDI(0-7) and TPARI. The sending device will normally output data on the same edge it is sampled by the PHAST-1. A setting of "0" results in a two-clock delay. When set to "1" the delay is three clocks.

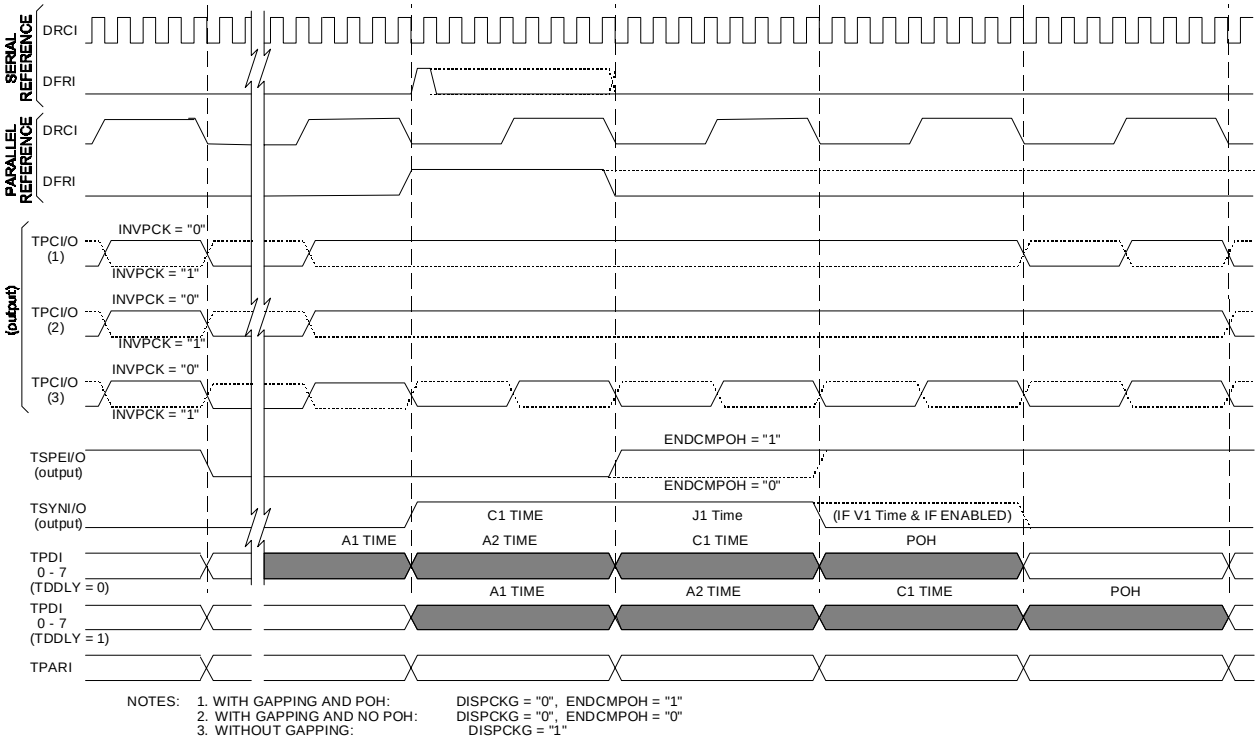


Figure 64. Tx Terminal Port Parallel 6.48 Mbyte/s Datacom Format

19.44 Mbyte/s Parallel Datacom

The Rx Terminal Port Parallel 19.44 Mbyte/s Datacom Format is shown, generically, in Figure 65, which represents the complete bus structure. In actual operation the PHAST-1 would only supply one third of the output information as was shown in Figure 59. The Reference inputs must be RRCI and RRFI. RRFI may be from one to three clock periods in duration. TPCO is the 19.44 Mbit/s output clock. TPDO0 through TPDO7 are the byte wide data outputs where the LSB is TPDO0. RSPE is Low during the TOH and, optionally, the POH Byte times. The POH Byte option is controlled by ENDCMPOH. When set to "1", RSPE remains High during these Byte times. A value of "0" results in RSPE transitioning Low during these Byte times. RSYN is High during the C1 (all three slots), J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". The polarity of TPCO can be inverted with the control INVPCK. A value of "0" results in TPDO(0-7), RSPE, RSYN and TPARO being output on the Falling Edge. When INVPCK = "1", the information is output on the Rising Edge of TPCO.

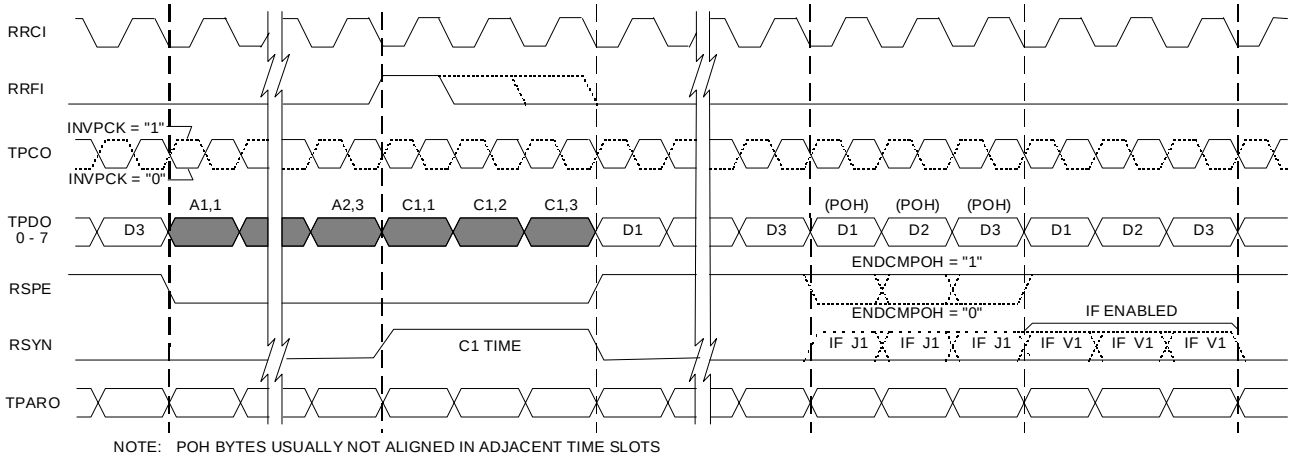


Figure 65. Rx Terminal Port Parallel 19.44 Mbyte/s Datacom Format

The Tx Terminal Port Parallel 19.44 Mbyte/s Datacom Format is shown in Figure 66. TPCI/O, TSPEI/O and TSYNI/O are all outputs that are active at all times. It is assumed that one PHAST-1 will be used to create the control signals for the entire bus. TPDI(0-7) and TPARI are inputs. TMBSEL0 and TMBSEL1 determine which third of the bus is sampled by a PHAST-1. DRCI and DFRI are the Reference Inputs. DFRI may be from one to three clock periods in duration. TPCI/O is the 19.44 Mbit/s output clock. TPDI0 through TPDI7 are the byte wide data inputs where the LSB is TPDI0. TSPEI/O is Low during the TOH and, optionally, POH Byte Times. ENDCMPOH controls the state of TSPEI/O during the POH Byte times. ENDCMPOH = "0" results in TSPEI/O transitioning Low during these Byte times. If ENDCMPOH = "1", TSPEI/O remains High during these Byte times. TSYNI/O is High during the C1, J1 and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". The polarity of TPCI/O can be inverted with the control INVPCK. A value of "0" results in TSPEI/O and TSYNI/O being output on the Falling Edge and TPDI(0-7) being sampled on the Falling Edge. When INVPCK = "1", the Rising Edge is used for both output and input. TDDLY is used to determine the delay time from TSYNI/O transitioning High to sampling of the data on TPDI(0-7). The sending device will normally output data on the same edge it is sampled by the PHAST-1. A setting of "0" results in a two-clock delay. When set to "1" the delay is three clocks. Note that, in contrast to the Rx side, the Tx C1 is High during all three slots of the C1 byte time.

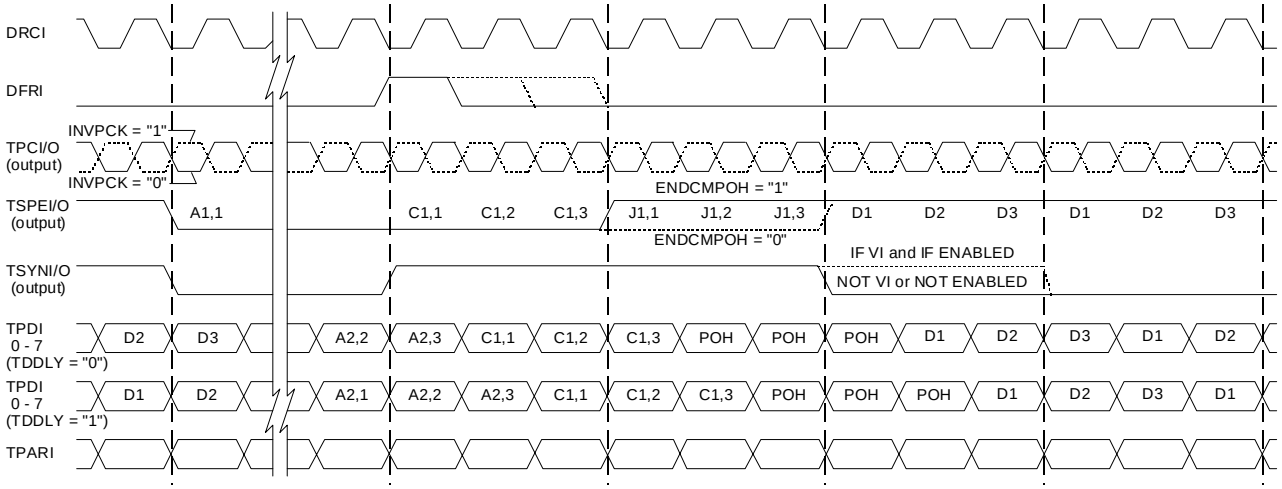


Figure 66. Tx Terminal Port Parallel 19.44 Mbyte/s Datacom Format

SPE-only

Figure 67 shows the Rx Terminal Port SPE-only Format. This is a serial, 51.84 Mbit/s format in which TOH Bytes are not present in the output. In their place, one bit gaps are inserted, uniformly, in the data stream. The Reference inputs may be either RRCI/RRFI or RXCK/RXFR. The external reference frame pulse (RRFI) may be from one to eight clock periods in duration. RTDO is output on the Falling Edge of RTCO. The order of output is MSB → LSB. RSPE is Low during the gaps in RTDO. RSYN is High during the J1 Byte time and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". For gapping purposes, the signal is divided into nine contiguous subframes. The start of the first subframe occurs eight bit times before RRFI or RXFR transitions Low. Each Subframe contains 720 bit times. Normally there will be 696 data bits per subframe. In this situation the resulting 24 gaps will be performed every 30 bits, with the first gap in the subframe occurring at the thirtieth bit time. Subframes containing Pointer Decrements will contain 704 data bits and will require 16 gaps. These will be introduced every 45 bit times with the first gap occurring at the forty-fifth bit position. Subframes containing Pointer Increments will contain 688 data bits and will require 32 gaps. These Subframes will have the gaps occurring in pairs of 22 and 23 bit times i.e., two gaps in 45 bit times. The first gap will occur at the twenty-second bit position.

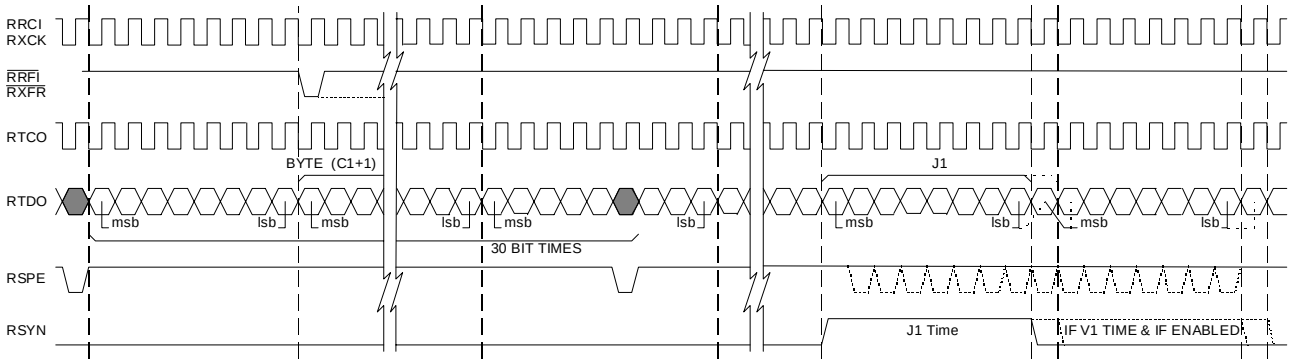


Figure 67. Rx Terminal Port SPE-only Format

The Tx Terminal Port SPE-only Format is shown in Figure 68. This is a serial, 51.84 Mbit/s format in which TOH Bytes are not present. In their place, gaps are inserted in the data stream. TTDI is clocked in on the Rising Edge of TTCI/O. The order of input is MSB → LSB. TSPEI/O is Low during the gaps in TTDI. TSYNI/O is High during the J1 Byte time and, optionally, V1 Byte times. The V1 Byte time option is enabled when the control H4INT is set to "1". As indicated, the J1 or V1 Byte may have a gap(s) within it. For gapping purposes, the signal is divided into nine contiguous subframes. Each Subframe contains 720 bit times. Normally there will be 696 data bits per subframe. This situation requires 24 gaps. Subframes containing Pointer Decrements will contain 704 data bits and will require 16 gaps. Subframes containing Pointer Increments will contain 688 data bits and will require 32 gaps. In all subframes the required gaps may occur at any time. Figure 68 depicts spacing identical to the Rx Terminal Port output.

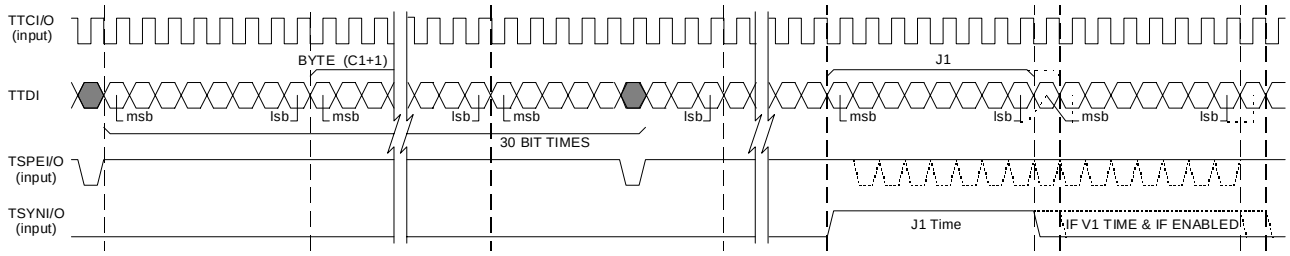


Figure 68. Tx Terminal Port SPE-only Format

E_X-K_X / TOH PORTS

The PHAST-1 has two ports for external access to the TOH Bytes. These are the Rx and Tx E_X-K_X / TOH Ports. They may be operated in either of two operating modes. The first is OW/APS, which affords access to the E1, E2, K1 and K2 Bytes. The second operating mode is All TOH. In this mode of operation all TOH bytes are accessible. The operating mode is controlled by OA (CR6; 0FE[H], Bit 0). When set to "1" the OW/APS Mode is selected. A Logic level of "0" selects All TOH Mode. The pins for these ports are shown below.

Rx OW/APS - TOH Port			Tx OW/APS - TOH Port		
ORCO	-	Clock; 576 kbit/s in OW/APS Mode 1.728 Mbit/s in All TOH Mode	OTCO	-	Clock; 576 kbit/s in OW/APS Mode 1.728 Mbit/s in All TOH Mode
ORDO	-	Output Data	OTDI	-	Input Data
SRFR	-	E1 Byte Identifier	STFR	-	E1 Byte Identifier
LRFR	-	E2 Byte Identifier	LTFR	-	E2 Byte Identifier
$\overline{\text{RAP}}$/$\overline{\text{RTS}}$	-	K1, K2 Byte Strobe in OW/APS Mode A1 Byte Identifier in All TOH Mode	$\overline{\text{TAP}}$/$\overline{\text{TTS}}$	-	K1, K2 Byte Strobe in OW/APS Mode A1 Byte Identifier in All TOH Mode

OW/APS Mode

The Rx E_X-K_X / TOH Port operation is shown in Figure 69. All outputs occur on the Rising Edge of ORCO. The output data (ORDO) consists of the E1 Byte, four Null Bytes, the K1 Byte, the K2 Byte, one Null Byte and the E2 Byte. The order of output is MSB → LSB. SRFR and LRFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW (CR2; 0FA[H], Bit 3). When set to a "0" value, SRFR occurs one clock period before the MSB of E1 and LRFR occurs one clock period before the MSB of E2. A Setting of "1" results in SRFR and LRFR occurring coincident with the MSB of the E1 and E2 Bytes, respectively. The signal $\overline{RAP}$ is an active Low pulse that occurs one clock time after the LSB of the K2 Byte.

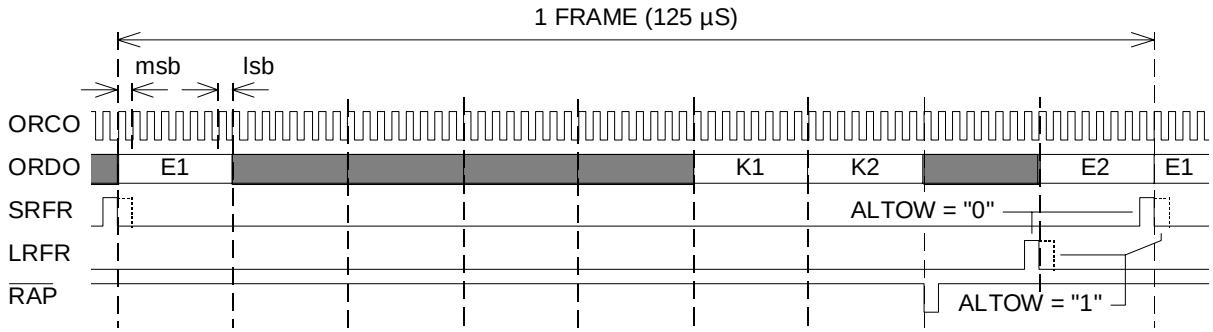


Figure 69. Rx OW/APS Port

Figure 70 depicts the operation of the Tx E_X-K_X / TOH Port. STFR and LTFR are output on the Rising Edge of OTCO. The input data (OTDI) is clocked in and $\overline{TAP}$ is clocked out on the Falling Edge. OTDI consists of the E1 Byte, one Null Byte, the K1 and K2 Bytes, three Null Bytes, the E2 Byte and a Null Byte. The order of input is MSB → LSB. STFR and LTFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW. When ALTOW is "0", STFR occurs 1½ clock periods before the MSB of E1 is sampled and LTFR occurs 1½ clock periods before the MSB of E2 is sampled. A Setting of "1" for ALTOW results in STFR and LTFR occurring one half clock cycle before the MSB of the E1 and E2 Bytes, respectively, is sampled. The signal $\overline{TAP}$ is an active Low pulse that occurs one clock time before the MSB of the K1 Byte is sampled.

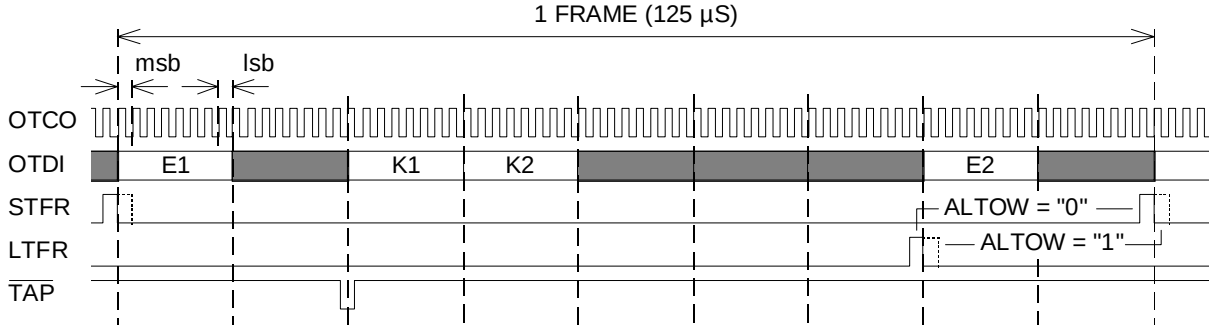


Figure 70. Tx OW/APS Port

All TOH Mode

The operation of the Rx E_X-K_X / TOH Port in All TOH Mode is shown in Figure 71. All outputs occur on Rising Edge of ORCO. The output data (ORDO) consists of all 27 TOH Bytes. They are output in the order in which they are received from the line, with the MSB occurring first. The signal $\overline{RTS}$ is an active Low pulse that occurs one clock time before the MSB of the A1 Byte. SRFR and LRFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW. The operation is as explained above.

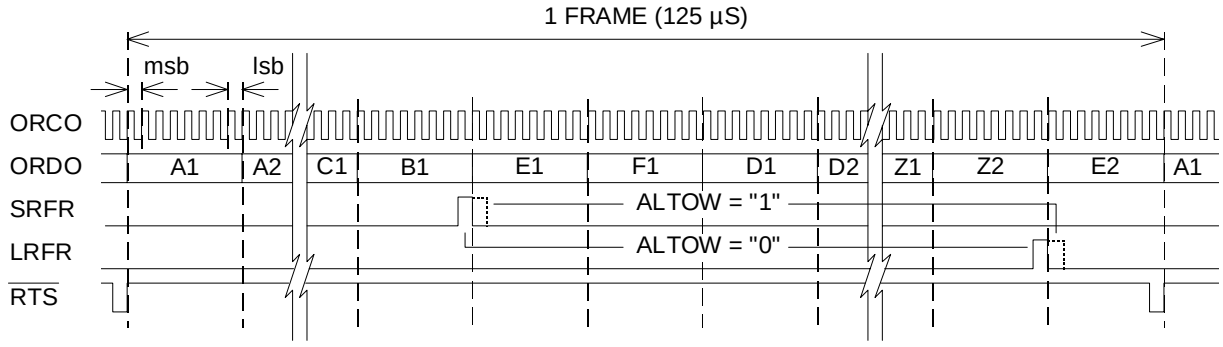


Figure 71. Rx All TOH Port

The operation of the Tx E_X-K_X / TOH Port in All TOH Mode is shown in Figure 72. STFR and LTFR are output on the Rising Edge of OTCO. The input data (OTDI) is clocked in and $\overline{TTS}$ is clocked out on the Falling Edge. OTDI consists of all 27 TOH Bytes. They are input in the order in which they are sent to the line with the MSB of each Byte occurring first. Although byte times are afforded for the B1, B2, H1, H2 and H3 Bytes, they are discarded inside the PHAST-1. STFR and LTFR are used to identify the E1 and E2 Bytes, respectively. The position of these two signals is determined by ALTOW, as was explained earlier. The signal $\overline{TTS}$ is an active Low pulse that occurs one clock time before the MSB of the A1 Byte is sampled.

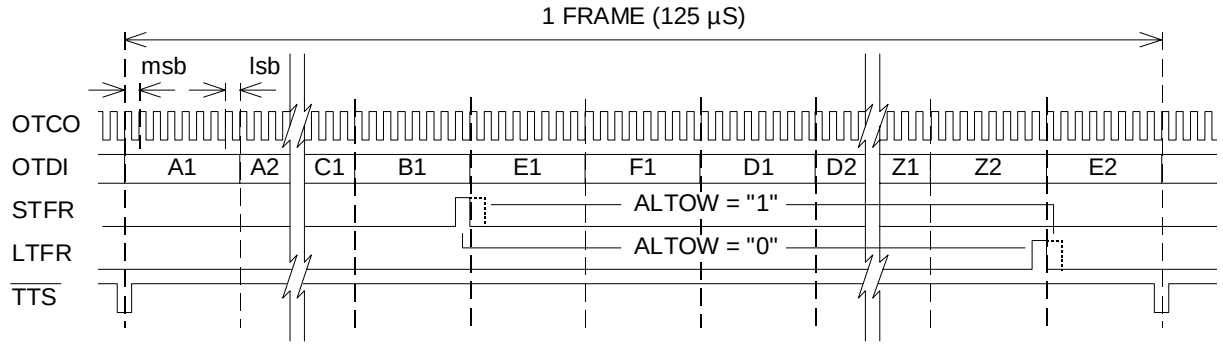


Figure 72. Tx All TOH Port

DCC PORTS

The PHAST-1 has four ports that provide external access to the Datacom Channels. Two are used for the Section DCC Bytes. These are the Rx Section DCC Port and Tx Section DCC Port. The other two ports are the Rx and Tx Line DCC Ports which afford access to the Line DCC Bytes. The pins are listed below.

Rx Section DCC Port			Rx Line DCC Port		
SRCO	-	192 kbit/s Clock	LRCO	-	576 kbit/s Clock
SRDO	-	Output Data (serial, D1-D3 Bytes)	LRDO	-	Output Data (serial, D4-D12 Bytes)
Tx Section DCC Port			**Tx Line DCC Port**		
STCO	-	192 kbit/s Clock	LTCO	-	576 kbit/s Clock
STDI	-	Input Data (serial, D1-D3 Bytes)	LTDI	-	Input Data (serial, D4-D12 Bytes)

SRDO and LRDO are clocked out on the Falling Edges of SRCO and LRCO, respectively. STDI and LTDI are clocked in on the Rising Edges of STCO and LTCO, respectively. The Data is input or output in the order it is sent to or received from the line, with the MSB of a byte occurring first.

POH PORTS

The Rx POH and Tx POH Ports provide hardware access to the POH Bytes. The pin definitions are shown below.

Rx POH Port Pins			Tx POH Port Pins		
PRCO	-	576 kbit/s Clock	PTCO	-	576 kbit/s Clock
PRDO	-	Output Data	PTDI	-	Input Data
$\overline{\text{RPS}}$	-	J1 Byte Identifier	$\overline{\text{TPS}}$	-	J1 Byte Identifier

The operation of the Rx POH Port is shown in Figure 73. All outputs occur on the Rising Edge of PRCO which is gapped during the TOH Byte Times. The output data (PRDO) consists of all nine POH Bytes. They are output in the order in which they are received from the line with the MSB of each byte appearing first. The signal $\overline{\text{RPS}}$ is an active Low pulse that occurs one clock time before the MSB of the J1 Byte.

The Tx POH Port operation is depicted in Figure 74. Serial data (PTDI) is sampled on the Rising Edge and $\overline{\text{TPS}}$ is output on the Falling Edge, of PTCO. $\overline{\text{TPS}}$ occurs one and a half bit times before the MSB of the J1 Byte is sampled. PTDI consists of all nine POH Bytes. They are input in the order in which they are sent to the line with the first bit of each byte being the MSB. Although B3 and H4 byte times are provided, both bytes are discarded.

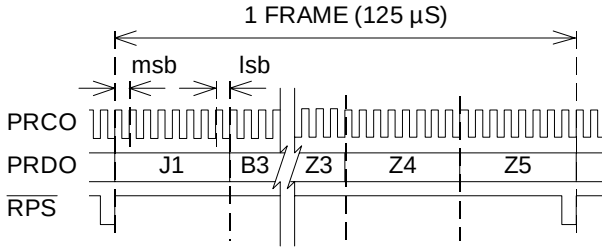


Figure 73. Rx POH Port

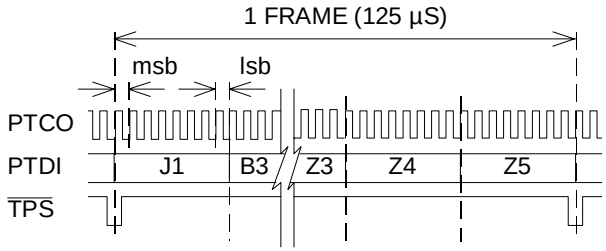


Figure 74. Tx POH Port

RING PORTS

The Rx and Tx Ring Ports are used to communicate RDI and FEBE information between matched PHAST-1s in PPS Ring Applications. The Pins are listed below.

Rx Ring Port Pins			Tx Ring Port Pins		
RGCO	-	Gapped, 648 kbit/s Clock	RGDI	-	Data Input = 648 kbit/s, nominal
RGDO	-	Output Data			
$\overline{\text{RGFR}}$	-	Frame Pulse			

RGDO and $\overline{\text{RGFR}}$ are clocked out on the Rising Edge of RGCO. RGCO and $\overline{\text{RGFR}}$ are provided to allow hardware access to the Ring Port Information. The Tx Terminal Ring Port data input (RGDI) is self clocking. The operation of both ports is depicted in Figure 75.

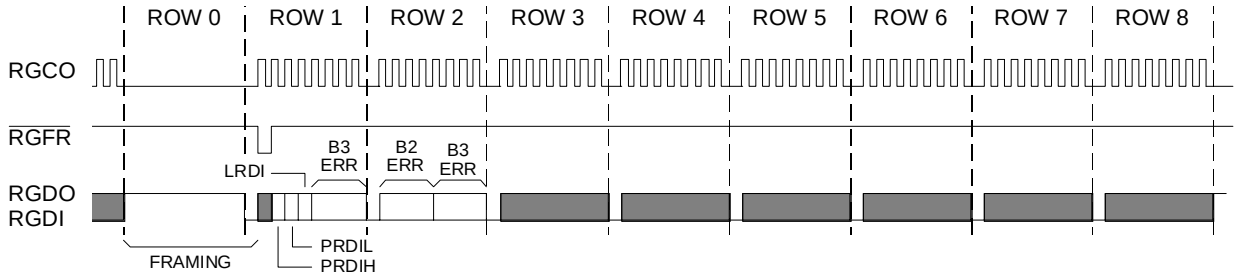


Figure 75. Rx and Tx Ring Ports

The Rx Ring Port information is divided into nine Segments, where each Segment corresponds to a Row of the SONET Format. The first Segment is a synchronization segment. The remaining eight segments are used for information transfer. RGCO is derived from the Rx Line Clock unless there is a Rx Line failure, in which case the Tx Line clock is used. Each Segment is nine RGCO clock periods in length (13.89 µs). In the First Segment (Row 0) RGCO is gapped and RGDO is output as a "1". In each of the remaining eight Segments (Rows 1 - 8), RGCO is gapped for the first bit period and RGDO is always "0" for this bit period. Thus there are eight usable information bit times per Segment. RGFR is output coincident with the first information bit time in the Second Segment. The information output in the Second Segment consists of one undefined bit, followed by two RDI-P bits (PRDIH and PRDIL), an 1RDI-L bit (LRDI) and four bits of B3 Error information encoded in Path FEBE Format. The information in the Third Segment consists of four bits of B2 Error information and four bits of B3 Error information, both encoded in FEBE format. The two B3 Error information times are for use in those Frames where there may be two B3 bytes. In those cases where there is only one B3 Byte, one of the B3 Error opportunity sequences will be output as all "0"s. The information content of the remaining six Segments (Rows 3 - 8) is undefined at this time.

The Tx Ring Port information format is as described above. The first 10 bits ("1111111110") constitute a framing pattern. The frame pattern must be present for the succeeding information to be accepted. Ring port failure is reported as LORG (SR4; 1F2/3/5[H], Bit 2). The receipt of RDI-L (PRDIL = "1") or RDI-P (PRDIL and/or PRDIH = "1") indications at the Ring Port is reported as RGRDI-L and RGRDI-P (SR4; 1F2/3/5[H], Bits 0 and 1), respectively.

ISC PORT

The Internal Systems Communications (ISC) Port provides access to selected TOH Bytes moving to and from the Terminal Interfaces. The bytes handled at the ISC Port are: C1, B1, E1, F1, D1, D2, D3, B2, K1, K2, D4, D5, D6, D7, D8, D9, D10, D11, D12, Z1, Z2 and E2. Externally generated bytes that are input at the ISC Port will, if enabled, appear in the outgoing signal at the Rx Terminal Port. Bytes entering the Tx Terminal Port will always be output by the ISC Port. The pins of the ISC Port are given below. Clocks ISCICO and ISCOCO are gapped during what would be the A1, A2 (which follows E2), H1, H2, and H3 (which follows D3) times.

Input Pins			Output Pins		
ISCICO	-	1.408 Mbit/s Clock (output, a gapped 1.728 Mbit/s clock)	ISCOCO	-	1.408 Mbit/s Clock (a gapped 1.728 Mbit/s clock)
ISCIDI	-	Input Data	ISCODO	-	Output Data
$\overline{\text{ISCIFO}}$	-	Frame Pulse (output)	$\overline{\text{ISCOFO}}$	-	Frame Pulse

The input operations are shown in Figure 76. Serial data (ISCIDI) is sampled on the Rising Edge and $\overline{\text{ISCIFO}}$ is output on the Falling Edge, of ISCICO. $\overline{\text{ISCIFO}}$ occurs one and a half bit times before the MSB of the C1 Byte is sampled. ISCIDI consists of the 22 Bytes listed above. They are input in the order in which they are output at the Rx Terminal Port.

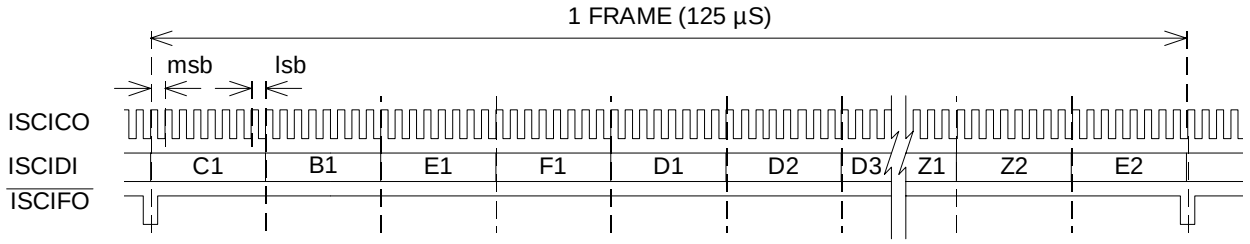


Figure 76. ISC Port Input

The output operations are shown in Figure 77. All outputs occur on the Rising Edge of ISCOCO. ISCODO consists of the 22 Bytes listed above. They are output in the order in which they are received at the Tx Terminal Port. ISCOFO occurs one bit time before the MSB of the C1 Byte is output.

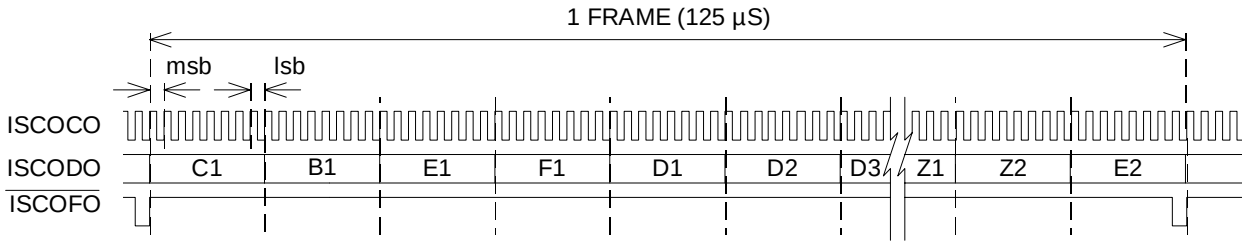


Figure 77. ISC Port Output

RX TOH PROCESSING

The Rx TOH Processing Block is responsible for Framing, De-scrambling (if STS1 = "1"), Overhead Distribution, Overhead Processing and Pointer Tracking. As discussed in the section "Rx Line Port Format," the external inputs are RLDI (data), RLCI (clock), RFRI (frame) and RXLOS (LOS Input). When used, RFRI consists of an active Low Pulse during the MSB Time of the C1 Byte. RLCI, RLDI and RFRI are monitored for presence. An absence of transitions is reported as RLOC (SR0; 0F0/1/4[H], Bit 7), RLOS (SR0; 0F0/1/4[H], Bit 0) and RLFRI (SR3; 0E8/9/C[H], Bit 7), respectively. As previously discussed, external access to the Rx TOH Bytes is available at the Rx E_X-K_X / All TOH Port, the Rx Section DCC Port and the Rx Line DCC Port.

Framing

The Framing portion detects Framing Errors - RFE (SR3; 0E8/9/C[H], Bit 6), Severely Errored Frame - RSEF (SR0; 0F0/1/4[H], Bit 1) and Loss of Frame - RLOF (SR0; 0F0/1/4[H], Bit 2). The Framer is a full off Line synchronizer, i.e., upon declaration of RSEF the previous frame alignment will be maintained until frame acquisition is completed and RSEF cleared. The framing algorithm used, when STS1 = "1", meets the Bellcore requirement that a BER of 10^{-3}, assuming a Poisson distribution of bit errors, will not cause an RSEF more than once in six minutes. If STS1 = "0" it is assumed that there is a framing device (such as an STS-N Multiplexer) between the PHAST-1 and the Line. The upstream device may provide the signal RFRI, which is used to set the Frame Delineation Counters to the appropriate value such that the subsequent A1 and A2 Bytes may be detected at the expected positions in the required time.

When control bit B2FREN is set to 1 (CR6; 0FE[H], Bit 7) a B2 check is made before declaring in frame. This can be used when handling payloads that may contain a framing pattern after scrambling that could mimic the true framing pattern. The accumulated B2 byte must match the received B2 byte following the second valid A1/A2 pattern received. A mismatch causes the framer to go out of frame and begin searching for a new framing pattern at the bit just after the subsequent A1/A2 position.

Rx TOH Byte Storage

On a per frame basis, all Received TOH Bytes are written into RAM Segment 005[H] - 01F[H] for µPro access. The Memory Locations are given in Table 7.

	Byte	Location	Byte	Location	Byte	Location
Section	A1	016[H]	A2	017[H]	C1	01C[H]
	B1	014[H]	E1	018[H]	F1	01D[H]
	D1	005[H]	D2	006[H]	D3	007[H]
Line	H1	011[H]	H2	012[H]	H3	013[H]
	B2	015[H]	K1	01E[H]	K2	01F[H]
	D4	008[H]	D5	009[H]	D6	00A[H]
	D7	00B[H]	D8	00C[H]	D9	00D[H]
	D10	00E[H]	D11	00F[H]	D12	010[H]
	Z1	01A[H]	Z2	01B[H]	E2	019[H]

Table 7. Received TOH Locations

The C1, F1, K1, K2, Z1 and Z2 bytes are also debounced. This function provides the means for detecting and reporting persistent changes that occur. Debouncing is performed on a per byte basis and occurs over a three frame period. The values for each individual byte in frames n, n-1 and n-2 are stored and compared. Any byte received with a new value that is the same for three consecutive frames is stored as the debounced value and will cause the indicator RTNEW (SR1; 0F2/3/5[H], Bit 6) to be set to "1". The intermediate and debounced values are stored in RAM and are accessible by the µPro. The Locations are given in Table 8.

Byte	Frame n	Frame n-1	Frame n-2	Debounced Value
Z1	01A[H]	04A[H]	052[H]	05A[H]
Z2	01B[H]	04B[H]	053[H]	05B[H]
C1	01C[H]	04C[H]	054[H]	05C[H]
F1	01D[H]	04D[H]	055[H]	05D[H]
K1	01E[H]	04E[H]	056[H]	05E[H]
K2	01F[H]	04F[H]	057[H]	05F[H]

Table 8. Debounced TOH Locations

Rx TOH Alarms

Two Transport Alarms are extracted from Bits 6-8 of the K2 Byte. Line AIS is reported as RAIS-L (SR0; 0F0/1/4[H], Bit 4) and is detected as a "111" condition. Line RDI is reported as RRDI-L (SR1; 0F2/3/5[H], Bit 3) and is detected as "110". A Received APS Alarm - RAPS (SR1; 0F2/3/5[H], Bit 2) is derived from a consistency check of the K1 and K2 Bytes. Additionally, a Received Line E1 Alarm - RLE1 (SR4; 1F2/3/5[H], Bit 4) is extracted from the E1 Byte, when so optioned. RLE1 detection assumes that some upstream entity has detected an AIS condition and uses the E1 Byte for in-band communication of the condition. Use of the Rx Line E1 Byte in this manner is enabled when RE2A (CR11; 1FB[H], Bit 3) is set to "1".

Rx C1/J0 Processing

In addition to the debouncing described earlier, optional processing of the C1 Byte can be performed to support J0 Functionality (Section Trace). Four forms of J0 Processing are supported. They consist of:

1. One Byte J0 Hardware Compare
2. Reception and Storage of a 16-Byte message
3. Reception and Storage of a 64-Byte message with ASCII CR/LF alignment
4. Reception and Storage of a 64-Byte message without ASCII CR/LF alignment

J0 Processing is controlled by bits J0EN0 and J0EN1 (CR18; 1DC[H], Bits 3 and 4)

One Byte Processing consists of comparing the content of the received C1 Byte to the value in the J0 EXPECT RAM Location (067[H]). Mismatch results in an alarm which is reported to the µPro as J0MIS (SR6; 0EA/B/D[H], Bit 3).

When multiple byte J0 options are selected no mismatch detection is performed by hardware. It is assumed that this will be performed by software. Received, multiple byte J0 messages are stored in a 64-byte RAM segment. This means that there will be four copies of a 16-byte message or one copy of a 64-byte message. The RAM Segment is accessible by the µPro through addresses 080[H] - 0BF[H]. This address space is shared by the 64-byte memory segment used to store the received J1 Bytes. The control J0RWEN (CR18; 1DC[H], Bit 7) is used to control the address space. When set to "1", the J0 Bytes are available.

Rx B1 Processing

B1 Errors are accumulated in an eight or sixteen-bit saturating counter designated Rx B1 Error Count (046[H]), which is readable by the µPro. The selection of Eight-Bit Mode or Sixteen-Bit Mode is controlled by CNT16EN (CR3; 0FB[H], Bit 2). CNT16EN = "0" defines Eight-Bit Mode. Counter overflow is indicated by RB1COF (SR7; 0F6[H], Bit 5). The manner in which B1 Byte errors are determined is dependent on the setting of STS1. When set to "0" the incoming B1 Byte may contain from zero to eight ones. Each "1" represents an error detected by an upstream device. The number of bits at the "1" Level is accumulated. If STS1 = "1" the B1 Byte, extracted after unscrambling, is compared to a B1 value calculated before unscrambling. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions. The errors (up to eight per frame) are accumulated.

Rx B2 Processing

B2 Errors are readable by the µPro at the location Rx B2 Error Count (047[H]) and counter overflow is indicated by RB2COF (SR7; 0F6[H], Bit 6). They are accumulated in the same manner as with the B1 Byte, with STS1 = “1”, except that the B2 calculation is performed after unscrambling and excludes the nine Section Bytes. The number of received errors (including zero) is made available to the Transmit Side and to the Ring Port for use as a Line FEBE.

Additional processing is performed to develop an Excess B2 BER Alarm. The threshold is determined by the following parameters:

Parameter	Location	Definition
B2WIN	061[H]	Window equals this number of blocks (see B2M, B2MULT)
B2M	060[H] Bits 0-3	Block size in number of SONET frames (125 microseconds each)
B2MULT(2-0)	Control Register 16; 0FF[H] Bits 5-3	Power of 10 that multiplies B2M parameter
B2SET	063[H]	Minimum number of blocks with errors $\geq$ B2SCV in window, B2WIN, to declare B2 EBER alarm.
B2SCV	062[H] Bits 4-7	Minimum number of errors per block to be considered an errored block.
B2CLR	064[H]	Minimum number of blocks with errors < B2CCV in window B2WIN, to declare B2 EBER alarm cleared.
B2CCV	062[H] Bits 0-3	The number of errors per block must be less this value to be considered an error free block (range 1 to N).

The parameter values to be used are given in Table 9. Exceeding the programmed threshold is reported as B2EBER (SR3; 0E8/9/C[H], Bit 5).

BER Threshold	B2WIN	B2M	B2MULT	B2SET	B2SCV	B2CLR	B2CCV
10^{-3}	67	1	0	37	3	23	2
10^{-4}	64	5	0	13	4	31	2

Table 9. B2EBER Parameters For Signal Degradation or Failure

The PHAST-1 implements a reset window algorithm to detect and clear 1 x 10^{-3} line error rates. The recommended values provide the threshold performance shown in Table 10 under random error conditions and will resist burst errors of up to 37 STS-1 frames. 37 or more single frame blocks with 3 or more errors out of a window of 67 frames will set B2EBER. It will clear if 23 or more single frame blocks with 1 or less errors out of 67 frames are detected.

BER	Mean time to alarm (sec)	Probability of alarm in a window	Mean time to clear (sec)	Probability of clear in a window
1.0×10^{-2}	0.0054	1.00		
1.2×10^{-3}	0.0063	1.00		
1.0×10^{-3}	0.0068	0.99		
9.0×10^{-4}	0.0072	0.94		
7.0×10^{-4}	0.0078	0.42		
5.0×10^{-4}		0.0026		
3.0×10^{-4}			0.0053	1.00
1.0×10^{-4}			0.0032	1.00
8.0×10^{-5}			0.0031	1.00

Table 10. B2 Error Alarm Performance For BER Threshold of 10^{-3}

Table 11 gives the value performance under conditions of a 10^{-4} BER threshold. Note that at an error rate of 10^{-3} the EBER alarm is declared in under 8.0 msec, but that it takes approximately 40 msec. to declare EBER.

The verification of the EBER threshold detection requires the test equipment to generate truly random errors at the desired rate. Some test equipment injects error on the B2 byte itself. Such error injection is not random and does not allow for the effect of error cancellation due to double error on the same bit position of the bytes in the same frame or errors that are not counted because they happen in the section overhead bytes. Therefore, if tests are conducted by injecting error to the B2 byte, the effective random error rate is expected to be higher than the injected error rate.

BER	Mean time to alarm (sec)	Probability of alarm in a window	Mean time to clear (sec)	Probability of clear in a window
1.0×10^{-3}	0.0081	1.00		
1.2×10^{-4}	0.012	1.00		
1.0×10^{-4}	0.014	1.00		
9.0×10^{-5}	0.016	0.99		
7.0×10^{-5}	0.021	0.66		
5.0×10^{-5}	0.023	0.03	0.025	0.003
3.0×10^{-5}			0.024	0.53
1.0×10^{-5}			0.020	1.00
8.0×10^{-6}			0.020	1.00

Table 11. B2 Error Alarm Performance For BER Threshold of 10^{-4}

Rx Line FEBE Processing

Processing of FEBE-L consists of recording the number of errors received in Z2 Byte Bits 5 - 8. Line FEBE Errors are accumulated in an eight or sixteen-bit saturating counter designated FEBE-L Count (040[H]). Counter overflow is indicated by RLFEBEOF (SR7; 0F6[H], Bit 3).

Rx Pointer Tracking

The H1 and H2 Bytes are used to determine the Received J1 Position and are interpreted for:

1. New Pointer - RNPTR (SR0; 0F0/1/4[H], Bit 6)
2. Concatenation - RCPTR (SR3; 0E8/9/C[H], Bit 3)
3. Loss of Pointer - RLOP (SR0; 0F0/1/4[H], Bit 3)
4. Path AIS - RAIS-P (SR0; 0F0/1/4[H], Bit 5)
5. Pointer Increment
6. Pointer Decrement

RCPTR is not an alarm per se. Reception of a Concatenation Indication will always result in the declaration of RLOP. RCPTR serves as an indication of an illegal condition that has caused the RLOP Alarm. Pointer Increments and Decrements are accumulated in four-bit Counters which are accessed at the RAM Location designated Rx Inc Count/Dec Count (045[H]). Bits 0 through 3 indicate the Decrement Count. Bits 4 through 7 are for Increments. In addition, both Pointer Increments and Decrements are accumulated in an eight-bit counter which can be read by the µPro in the RXPJCNT Location (044[H]). RPMOVOF (SR7; 0F6[H], Bit 2) is the overflow indication for the Inc and Dec counters and RPJOF (SR7; 0F6[H], Bit 1) indicates overflow of RXPJCNT.

RX POH PROCESSING

All received POH processing is performed by the Rx POH Processor Block. All Received POH Bytes are written into RAM for access by the µPro. They are also externally available at the Rx POH Port. Selected bytes are debounced. Further processing is executed for alarm extraction and for performance monitoring.

Received POH Byte Locations

The Memory Locations for the Received POH Bytes are given in Table 12. The locations 080[H] - 0BF[H] are shared with the J0 bytes and access is controlled by J0RWEN. J1 Byte storage is controlled by J1SYNCEN (CR6; 0FE[H], Bit 4). When set to "0" the J1 Bytes are stored in the 64-Byte Segment, in rotating fashion, with no specific starting point. If J1SYNCEN = "1" reception of ASCII characters CR and LF, in sequence, will cause the next J1 Byte to be written at address 080[H], with subsequent bytes being stored in succeeding locations.

Byte	Location
J1	080[H] - 0BF[H]
B3	0C0[H]
C2	0C1[H]
G1	0C2[H]
F2	0C3[H]
H4	0C4[H]
Z3	0C5[H]
Z4	0C6[H]
Z5	0C7[H]

Table 12. Received POH Locations

The C2, F2, Z3, Z4 and Z5 bytes are debounced. This function provides the means for detecting and reporting persistent changes that occur. The debouncing operation is identical to the TOH Debouncing Mechanism. The interstitial and debounced value locations are given in Table 13. Any byte that is received with a new value and that new value is constant for three consecutive frames, will cause the indicator RPNEW (SR1; 0F2/3/5[H], Bit 5) to be set to "1".

Byte	Frame n	Frame n-1	Frame n-2	Debounced Value
C2	0C1[H]	0D9[H]	0E1[H]	0D1[H]
F2	0C3[H]	0DB[H]	0E3[H]	0D3[H]
Z3	0C5[H]	0DD[H]	0E5[H]	0D5[H]
Z4	0C6[H]	0DE[H]	0E6[H]	0D6[H]
Z5	0C7[H]	0DF[H]	0E7[H]	0D7[H]

Table 13. Debounced POH Locations

Rx POH Alarm Processing

At present, the only Path level alarm that is defined is Path RDI. The mechanism that is implemented is the new Three Bit RDI-P format. This format is compatible with previous equipment (One Bit RDI-P - old Path Yellow) and the new Four State RDI-P. The Three Bit PRDI FORMAT uses bits 5, 6 and 7 of the G1 Byte. The coding is shown in Table 14. Four Status Bits are used to report Path RDI. These are RRDI-P (SR1; 0F2/3/5[H], Bit 4), RRDI-PSD (SR6; 0EA/B/D[H], Bit 7), RRDI-PCD (SR6; 0EA/B/D[H], Bit 6) and RRDI-PPD (SR6; 0EA/B/D[H], Bit 5). The first represents codes that are received only from old equipment. The latter three are used to identify new equipment. PRDISEL (CR16; 0FF[H], Bit 6) is used to select either a five or ten frame filter for Path RDI detection.

G1 Byte, Bit			Interpretation	Alarm Bit Affected
5	6	7		
0	0	0	No Remote Defect[1]	RRDI-P
0	0	1	No Remote Defect[2]	RRDI-P (PD, SD and CD)
0	1	0	Remote Payload Defect[2]	RRDI-PPD
0	1	1	No Remote Defect[1]	RRDI-P
1	0	0	Remote Defect[1]	RRDI-P
1	0	1	Remote Server Defect[2]	RRDI-PSD
1	1	0	Remote Connectivity Defect[2]	RRDI-PCD
1	1	1	Remote Defect[1]	RRDI-P

Notes:
1. This code is only transmitted by Old Equipment. New Equipment can therefore identify that it is interworking with old Equipment.
2. This code is only generated by New Equipment.

Table 14. RDI-P Format

Rx B3 Processing

B3 Errors are readable by the µPro at the location Rx B3 Error Count (0D4[H]). Counter overflow is indicated by RB3COF (SR7; 0F6[H], Bit 7). Their accumulation is identical to B2 accumulation, except that only the SPE bytes are included in the calculation. The number of received errors (including zero) is made available to the Transmit Side and to the Ring Port for use as a Path FEBE.

Additional processing is performed to develop an Excess B3 BER Alarm. The threshold is determined by the following parameters:

Parameter	Location	Definition
B3WIN	069[H]	Window equals this number of blocks (see B3M, B3MULT)
B3M	068[H] Bits 0-3	Block size in number of SONET frames (125 microseconds each)
B3MULT(2-0)	Control Register 16; 0FF[H] Bits 2-0	Power of 10 that multiplies B3M parameter
B3SET	06B[H]	Minimum number of blocks with errors $\geq$ B3SCV in window, B3WIN, to declare B3 EBER alarm.
B3SCV	06A[H] Bits 4-7	Minimum number of errors per block to be considered an errored block.
B3CLR	06C[H]	Minimum number of blocks with errors < B3CCV in window B3WIN, to declare B3 EBER alarm clear.
B3CCV	06A[H] Bits 0-3	The number of errors per block must be less this value to be considered an error free block (range 1 to N).

The parameter values to be used are given in Table 15. Exceeding the programmed threshold is reported as B3EBER (SR3; 0E8/9/C[H], Bit 4).

BER Threshold	B3WIN	B3M	B3MULT	B3SET	B3SCV	B3CLR	B3CCV
10^{-5}	64	5	1	16	4	29	1

Table 15. B3EBER Parameters For Signal Degradation or Failure

This is the same algorithm that is used for B2 EBER. The values in Tables 10 and 11 can be used for signal Failure performance based on the signal failure parameter settings. The values given in Table 16 give the results of using B3EBER to indicate signal degradation.

BER Threshold	Mean time to alarm (sec)	Probability of alarm in a window	Mean time to clear (sec)	Probability of clear in a window
1.0×10^{-4}	0.100	1.00		
1.2×10^{-5}	0.195	1.00		
1.0×10^{-5}	0.263	0.99		
9.0×10^{-6}	0.307	0.88		
7.0×10^{-6}	0.361	0.09		
5.0×10^{-6}	0.377	1.12×10^{-5}	0.352	0.25
3.0×10^{-6}			0.255	0.99
8.0×10^{-7}			0.129	1.00

Table 16. B3 ERROR Alarm Performance For BER Threshold of 10^{-5}

Rx C2 Processing

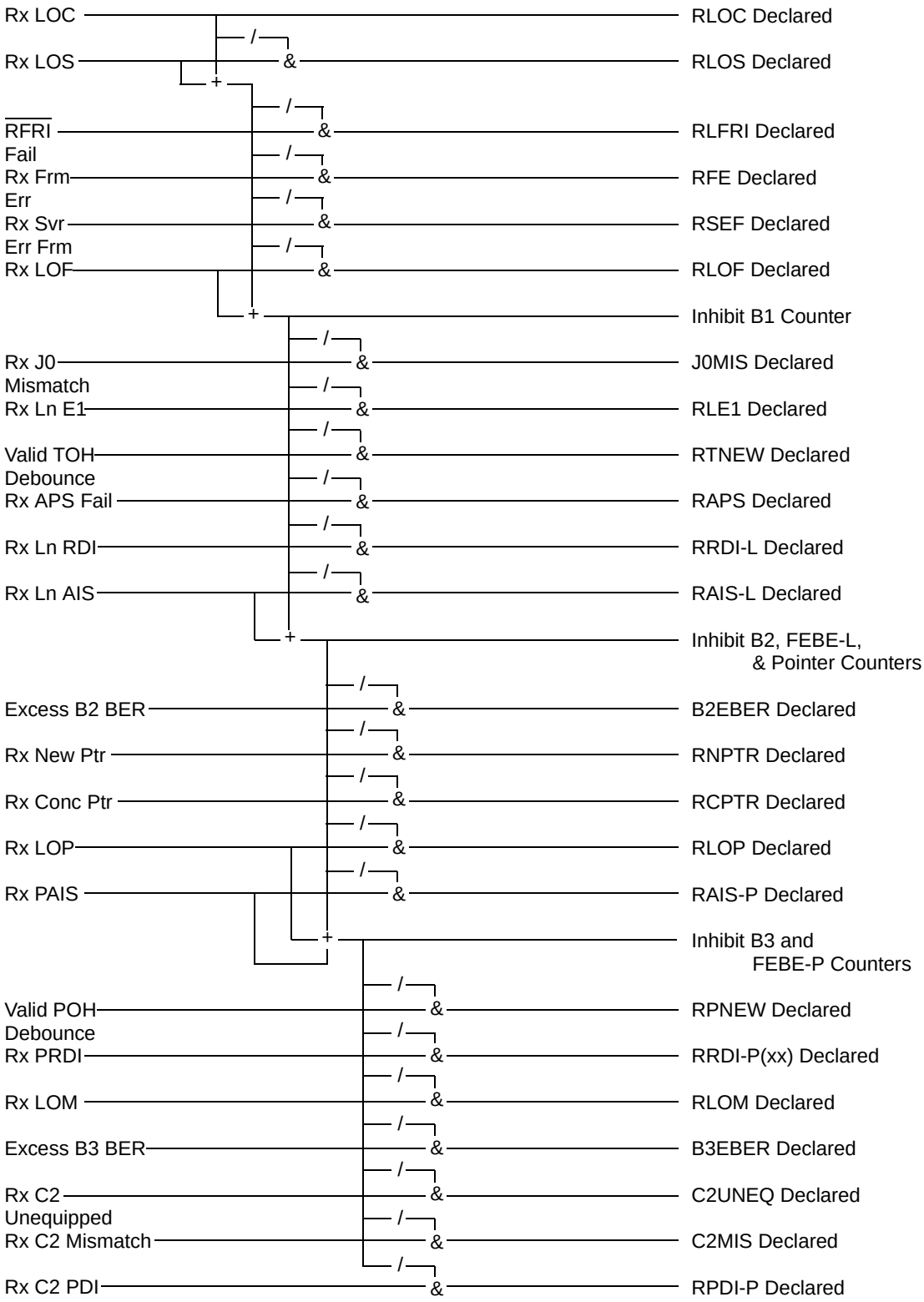
All C2 processing is based on the receipt of five consecutive C2 Bytes with the specified value. The Received C2 Byte is compared to the value written by the µPro in EXPECTC2 (0E4[H]). Mismatch results in the alarm C2MIS (SR3; 0E8/9/C[H], Bit 2). The Received C2 Byte is also checked for the Unequipped Value - C2UNEQ (SR3; 0E8/9/C[H], Bit 1) and Payload Defect Indication - RPDI-P (SR6; 0EA/B/D[H], Bit 4).

Rx H4 Processing

The H4 Byte sent to the Terminal Bus Interface may be either the received, unaltered H4 Byte received from the Rx Line or it may be the output of a two-bit, H4 Counter. Selection is made by the control H4INT. When optioned for local generation (H4INT = "1"), Bits 7 and 8 of the received H4 Byte are used to synchronize a two-bit, modulo four counter. If the H4 Pattern incoming to the PHAST-1 from the Rx Line does not match the pattern generated by the counter, a Loss of Multiframe Alarm - RLOM (SR3; 0E8/9/C[H], Bit 0) is generated. When in the RLOM State, the phase of the previous Multiframe will be maintained until the new Multiframe phase is determined. The output of the counter is used to create the V1 Portion of C1J1V1. When optioned for H4 pass through (H4INT = "0"): the V1 portion of C1J1V1 will be suppressed, i.e., the Signal will be C1J1, the Modulo Four Counter will not be activated and declaration of RLOM will be inhibited.

Rx Path FEBE Processing

Rx Path FEBE Processing consists of recording the number of errors received in G1 Byte Bits 1 - 4. Path FEBE Errors are accumulated in an eight or sixteen-bit saturating counter designated FEBE-P Count (0D2[H]). Counter overflow is indicated by RPFEBEOF (SR7; 0F6[H], Bit 4).



Equation 1. Reporting Hierarchy for Received Alarms

RX SIDE ALARM HIERARCHY

A compilation of the hierarchical scheme used for Rx Side Alarm reporting is given in Equation 1 where: + represents the "OR" function, & represents the "AND" function, and / denotes the "NOT" function. It does not include the complete definitions for declaring or clearing each individual alarm. It is a reference that portrays the suppression effect of higher order alarms. The order of precedence is top to bottom. Also included are the conditions that inhibit the various performance counters.

RX TERMINAL OUTPUT GENERATION

The Rx Terminal Generator and the Rx Terminal Port are responsible for assembling the information that appears at the Rx Side Terminal Output. The input to the Rx Terminal Generator is either the output from the Rx Re-timing FIFO, if Rx Re-timing is enabled, or the Rx POH Processor, if Rx Re-timing is disabled. Terminal Line AIS, Path AIS and the E1 alarm are also generated at this point.

Rx Terminal TOH Creation

The format is determined by the P.O.M. of the PHAST-1. The TOH Bytes output at the Rx Terminal Port are dependent on the reference source being used by the Terminal Timing Generator (Line Timing or External Receive Timing) and by the enabling or disabling of Received Re-timing. When SPE-only mode is active no TOH bytes are output at the Rx Terminal Port.

In general, the TOH bytes output at the Rx Terminal Port may be either those received from the line or may be selected from the Terminal Insert Locations shown in Table 17. The Insert Locations may be either Written by the µPro or may be filled by the ISC Port. The µPro can write all bytes except A1, A2, B1 and B2. The ISC Port can access all Insert Locations except A1, A2, H1, H2 and H3. ISC Port Access is controlled by TTOHEN (CR3; 0FB[H], Bit 0). When set to "1" the ISC Port has access. A value of "0" provides µPro access to the Insert Locations. Table 18 shows the Terminal TOH Byte options. TOH Byte selection is controlled by the 13 listed Control Bits, RCLK and TTOHEN.

	Byte	Location	Byte	Location	Byte	Location
Section	(A1)	036[H]	(A2)	037[H]	C1	03C[H]
	(B1)	034[H]	E1	038[H]	F1	03D[H]
	D1	025[H]	D2	026[H]	D3	027[H]
Line	H1	031[H]	H2	032[H]	H3	033[H]
	(B2)	035[H]	K1	03E[H]	K2	03F[H]
	D4	028[H]	D5	029[H]	D6	02A[H]
	D7	02B[H]	D8	02C[H]	D9	02D[H]
	D10	02E[H]	D11	02F[H]	D12	030[H]
	Z1	03A[H]	Z2	03B[H]	E2	039[H]

Note: Parentheses indicate addresses not written by µPro.

Table 17. Terminal Insert TOH Locations

Byte(s)	Control Bit	Location CR#; Reg, Bit	RCLK="1" + TTOHEN="1"		RCLK="0" & TTOHEN="0"	
			Control="0"	Control="1"	Control="0"	Control="1"
A1, A2	RRFRM	CR1; 0F9[H], 1	Line[1]	Insert[5]	Line	Insert[5]
C1	RRC1	CR1; 0F9[H], 6	ISC Port[6]	Insert	Line	Insert
B1	RRB1	CR1; 0F9[H], 0	ISC Port[6]	Insert[4]	Line[8]	Insert[4]
E1	RRE1	CR0; 0F8[H], 5	ISC Port[6]	Insert	Line	Insert
F1	RRF1	CR1; 0F9[H], 7	ISC Port[6]	Insert	Line	Insert
D1-D3	RRSD	CR0; 0F8[H], 7	ISC Port[6]	Insert	Line	Insert
H1-H3	RRPTR	CR0; 0F8[H], 1	Line[2,7]	Insert[3]	Line[2,7]	Insert[3]
B2	RRB2	CR1; 1F9[H], 0	ISC Port[6]	Insert[4]	Line[8]	Insert[4]
K1, K2	RRAPS	CR0; 0F8[H], 2	ISC Port[6]	Insert	Line	Insert
D4-D12	RRLD	CR0; 0F8[H], 6	ISC Port[6]	Insert	Line	Insert
Z1	RRZ1	CR1; 0F9[H], 5	ISC Port[6]	Insert	Line	Insert
Z2	RRZ2	CR1; 0F9[H], 4	ISC Port[6]	Insert	Line	Insert
E2	RRE2	CR0; 0F8[H], 4	ISC Port[6]	Insert	Line	Insert

Notes:
1. Control Bit Disabled - insert values used if RCLK = "1"
2. H1 and H2 = value calculated by Rx Re-timing if Re-timing enabled.
3. This is for test purposes only - payload does not track pointer value.
4. Calculated B1 and B2 written to Insert Locations.
5. Generated A1 and A2 written to Insert Locations.
6. ISC Port Input written to Insert Location. If TTOHEN = "0", Control Bit is disabled and Insert Value is used.
7. Insert Value used for H3 Byte if Control Bit is disabled and re-timing is enabled.
8. Control Bit Disabled - Insert Value Used if Re-timing enabled or for B1 if STS1 = "1".

Table 18. Terminal TOH Options

When generated internally, A1 and A2 Bytes contain the values F6[H] and 28[H], respectively. Internally generated B1 and B2 Bytes contain calculated Section and Line BIP-8 values. The Calculation is Even Parity, independently performed, in parallel, over the eight bit positions of the outgoing bytes. The B1 calculation will be performed over all bytes. The B2 calculation excludes the nine Section Bytes. The value calculated for Frame n is placed in the B1 or B2 Byte of Frame n+1. Prior to output, the B1 and B2 Bytes are Exclusive-OR gated, respectively, with the B1 and B2 Error Masks. These are Locations 049[H] and 051[H].

Rx Terminal POH Creation

The Received J1 Bytes are always passed through to the Rx Terminal Port. The H4 Byte may be either the unaltered H4 Byte from the Rx Line or the internally generated output of the two-bit, H4 Counter. H4INT (CR6; 0FE[H], Bit 5) controls the selection. When set to "0" the Received H4 Byte is selected. A value of "1" selects the counter output.

The remaining POH Bytes may be selected from the Rx Line or the Insert Locations given in Table 19. All locations except 0C8[H] are written by the µPro. The B3 Location is the calculated BIP-8. The Calculation is Even Parity, independently performed, in parallel, over the eight bit positions of the outgoing SPE Bytes. The value calculated for Frame n is placed in the B3 Byte of Frame n+1. Prior to output, the B3 value is Exclusive-OR gated with the B3 Error Mask. This is Location 0D0 [H].

Byte	Location
(B3)	0C8[H]
C2	0C9[H]
G1	0CA[H]
F2	0CB[H]
Z3	0CD[H]
Z4	0CE[H]
Z5	0CF[H]

Table 19. Terminal Insert POH Locations

Selection is controlled by RPATH (CR0; 0F8[H], Bit 3). A Setting of "0" selects the Bytes from the Rx Line. When set to "1" the Insert POH Bytes will appear at the Rx Terminal Port.

Rx Terminal Alarm Generation

Line AIS insertion consists of forcing all Line Overhead Bytes (H1, H2, ..., Z2, E2) and all SPE Bytes to "1". AIS-L insertion is directly controlled by the µPro via the command SRLAIS (CR4; 0FC[H], Bit 7). In addition AIS-L may, as an option, be automatically inserted upon certain Receive Side anomalies. Enabling of automatic insertion is controlled by RRAIS (CR1; 0F9[H], Bit 3) and LTE (CR1; 0F9[H], Bit 2). The Inclusion of B2EBER is enabled by B2XAIS (CR4; 0FC[H], Bit 6) and the Inclusion of J0MIS is enabled by J0MLAIS (CR18; 1DC[H], Bit 5). When re-timing is employed, the insertion of AIS-L will terminate with the sending of a valid pointer with the NDF Bits active ("1001") for one frame. Subsequent pointer values are transmitted with an inactive NDF ("0110") indication. If re-timing is disabled, termination will consist of removing the "1" forcing function. If the conditions are such that a Line AIS will be inserted (if enabled by RRAIS) it will be indicated by RLAISC (SR8; 1F6[H], Bit 2).

Path AIS insertion consists of setting the H1, H2 and H3 Bytes and all SPE Bytes to "1". AIS-P insertion is directly controlled by the µPro via the command SRPAIS (CR4; 0FC[H], Bit 5). PAIS insertion will also occur on Receive FIFO underflow or overflow, if the automatic FIFO recovery option is set. In addition, AIS-P may, as an option, be automatically inserted upon certain received alarms. Five of the conditions for autonomous insertion are options. They are B3EBER, RLOM, C2MIS, C2UNEQ and RLE1. They are enabled, respectively, by the controls: B3XPAIS, RLOMPAIS, C2MPAIS, C2UPAIS and RLEAIS (CR4; 0FC[H], Bits 4, 3, 2, 1, and 0). Enabling of automatic insertion is controlled by RRAIS, LTE and PTE (CR9; 1F9[H], Bit 2). If re-timing is enabled the insertion of AIS-P will terminate with the sending of a valid pointer with the NDF Bits active ("1001") for one frame. Subsequent pointer values are transmitted with an inactive NDF ("0110") indication. When re-timing is disabled, termination of AIS-P will consist of removing the "1" forcing function. When the conditions are such that a Path AIS will be inserted (if enabled by RRAIS) it will be indicated by RPAISC (SR8; 1F6[H], Bit 3).

The E1 Byte sent to the Rx Terminal Port may optionally be used to communicate an in-band AIS Indication. This is controlled by command RA2E (CR11; 1FB[H], Bit 2). When Enabled:

1. The Setting of RRE1 (in Line Timing Mode) will be disregarded.
2. The normal state of the E1 Byte will be all "0".
3. The occurrence of certain anomalies will result in the E1 Byte being set to all "1".

If the conditions are such that the E1 Alarm will be inserted (if enabled by RA2E) it will be indicated by the setting of RPAISC or RLAISC.

RX TERMINAL OUTPUTS

The Receive Side Signal Outputs from the Rx Terminal Port are RTDO (Serial Data), RTCO (serial Clock), TPCO (Parallel Clock), TPDO0-TPDO7 (Parallel Data), RSPE (Payload Indication), RSYN (Sync Pulse) and TPARO (Parity). Parity errors can be created with SBPE (CR3; 0FB[H], Bit 4). One additional output $\overline{\text{TPDVO}}$ and two additional inputs $\overline{\text{TPDVI0}}$ and $\overline{\text{TPDVI1}}$ are optionally used in 19.44 Mbyte/s Multiplexed Bus configurations to prevent bus collisions. When employed, bus collisions are reported as RBUSCOL (SR1; 0F2/3/5[H], Bit 1).

Two Alarm Port pins $\overline{\text{RSF}}$ (Rx Signal Fail) and $\overline{\text{RAIS}}$ (Rx AIS) are used to provide an external indication of Receive Side anomalies.

TX TERMINAL INPUTS

The Inputs to the Tx Terminal Port are TTDI (Serial Data), TPDI0-TPDI7 (Parallel Data) and TPARI (Parity). Four other pins TTCI/O (Serial Clock), TPCI/O (Parallel Clock), TSPEI/O (Payload Indication) and TSYNI/O (Sync Pulse) are bidirectional. In SONET or SPE-only Modes they are inputs. In Datacom mode they are outputs. Failures at the Tx Terminal Port are indicated by TLOC (SR2; 1F0/1/4[H], Bit 7), TLOS (SR2; 1F0/1/4[H], Bit 0) and TBPE (SR5; 1E8/9/C[H], Bit 7). Parity checking can be disabled with DISTBPE (CR10; 1FA[H], Bit 4).

The Alarm Port input pin $\overline{\text{TAIS}}$ can be used to force an AIS condition at the Tx Line output. Pin $\overline{\text{TAIS}}$ at the Low level results in the setting of TAISV (SR4; 1F2/3/5[H], Bit 3).

TX TERMINAL OVERHEAD PROCESSING

The Tx Terminal Port and Tx TOH Processing Blocks are responsible for Signal Failure Detection, Frame Delineation, Overhead Distribution and Overhead Processing. The Tx Terminal Port routes the C1, B1, E1, F1, D1, D2, D3, B2, K1, K2, D4, D5, D6, D7, D8, D9, D10, D11, D12, Z1, Z2 and E2 Bytes to the ISC Port if SPE-only Mode is not enabled.

Input Frame Delineation

In all SONET Modes there are two methodologies for determining the start of the Frame and the SPE: Framing Mode and C1J1 Mode. The selection is determined by C1J1EN. The setting of C1J1EN is disregarded in SPE-only and Datacom Modes.

Framing Mode

In this mode of operation (C1J1EN = "0") TSYNI/O and TSPEI/O are disregarded. The A1/A2 and H1/H2 Bytes incoming to the Tx Terminal Port are used to determine Frame and SPE alignment. In Parallel modes the F6[H], 28[H] Framing Pattern (A1 and A2) must occur on byte boundaries. When the 19.44 Mbyte/s format is employed, Framing is found and checked on the First F6[H] and 28[H] bytes occurring in the same numbered slot. The Framing Circuitry detects Framing Errors - TFE (SR5; 1E8/9/C[H], Bit 6), Severely Errored Frame - TSEF (SR2; 1F0/1/4[H], Bit 1) and Loss of Frame - TLOF (SR2; 1F0/1/4[H], Bit 2).

Line AIS detection is optionally performed using the K2 Byte. This function is enabled by DISTLAIS = "0" (CR12; 1FC[H], Bit 5) and the alarm reported as TAIS-L (SR2; 1F0/1/4[H], Bit 4).

Pointer Processing results in the generation of the following alarms: Loss of Pointer - TLOP (SR2; 1F0/1/4[H], Bit 3), New Pointer - TNPTR (SR2; 1F0/1/4[H], Bit 6), Concatenated Pointer - TCPTR (SR5; 1E8/9/C[H], Bit 5), Path AIS - TAIS-P (SR2; 1F0/1/4[H], Bit 5). TCPTR is not a true alarm. Detection of a Concatenation Indication will always result in the declaration of TLOP. TCPTR serves as an indication of an illegal condition that has caused the TLOP Alarm. Pointer Increments and Decrements are accumulated in four-bit counters which are accessed at the RAM Location designated Tx Inc/Dec Count (145[H]). Bits 0 through 3 indicate the Decrement Count. Bits 4 through 7 are for Increments. Overflow of either counter is indicated by TPMOVOF (SR8; 1F6[H], Bit 4).

C1J1 Mode

Under this condition (C1J1EN = "1") the TSYNI/O and TSPEI/O signals are enabled. The information content of the A1, A2, H1 and H2, Bytes is disregarded. Framing and Pointer Tracking are not performed and the associated alarms are inhibited. If bits 6,7 and 8 of the K2 Byte are indeterminate then DISTLAIS must be set to "1" to inhibit the TAIS-L Alarm.

In SONET modes, TSYNI/O is an input and contains C1, J1 and optional V1 Information. The relationships of TSPEI/O and TSYNI/O to the input data and clock are shown in Figures 55, 57 and 60. The V1 portion of TSYNI/O is enabled when the control H4INT = "1". Under these conditions the V1 pulse is used to synchronize a two-bit, modulo four counter which creates the information for the H4 Byte that is sent to the Tx Line.

In Datacom modes, TSYNI/O is an output which contains C1, J1 and optional V1 Information. The relationships of the TSPEI/O and TSYNI/O outputs to the input data are shown in Figures 62, 64 and 66. The V1 portion of TSYNI/O is enabled when the control H4INT = "1". Under these conditions the external Datacom Reference Signal ($\overline{\text{DFRI}}$ or DFRI) must occur once every 500 µs. When the reference signal is active, the two-bit modulo 4 counter is set such that the H4 Byte sent to the Tx Line contains "00" and the V1 Portion of TSYNI/O will be output. If $\overline{\text{DFRI}}$/DFRI is not supplied when H4INT = "1", the two-bit counter will still count, producing the V1 indicator at TSYNI/O and inserting its value in the two LSB's of H4, although its initial value will be arbitrary. If DFRI/$\overline{\text{DFRI}}$ is lost the operation will not be disturbed and the same V1 alignment will be maintained.

Input TOH Storage

On a per frame basis all Overhead Bytes are written into RAM Segment 105[H] - 11F[H] for µPro access. The Memory Locations for the TOH Bytes are given in Table 20. In SPE-only mode these bytes will be "Don't Care".

	Byte	Location	Byte	Location	Byte	Location
Section	A1	116[H]	A2	117[H]	C1	11C[H]
	B1	114[H]	E1	118[H]	F1	11D[H]
	D1	105[H]	D2	106[H]	D3	107[H]
Line	H1	111[H]	H2	112[H]	H3	113[H]
	B2	115[H]	K1	11E[H]	K2	11F[H]
	D4	108[H]	D5	109[H]	D6	10A[H]
	D7	10B[H]	D8	10C[H]	D9	10D[H]
	D10	10E[H]	D11	10F[H]	D12	110[H]
	Z1	11A[H]	Z2	11B[H]	E2	119[H]

Table 20. Terminal TOH Locations

Input B1 Processing

When enabled by INHTB1C (CR15; 1DF[H], Bit 3), the B1 Byte is compared to a calculated B1 value. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of all incoming bytes. The errors (up to eight per frame) are accumulated in an eight-bit Roll Over counter designated Tx B1 Error Count (146[H]) which is readable by the µPro. There is no Counter overflow indicator.

Input B2 Processing

B2 Errors are accumulated in the same manner as with the B1 Byte, except that the nine SOH Bytes are excluded, the function is enabled by INHTB2C (CR15; 1DF[H], Bit 2) and the Roll Over counter is designated Tx B2 Error Count (147[H]). There is no Counter overflow indicator.

Input E1 Processing

A Transmit Terminal E1 Alarm - TTE1 (SR5; 1E8/9/C[H], Bit 4) is extracted from the E1 Byte, when so optioned by TE2A (CR11; 1FB[H], Bit 1). TTE1 detection assumes that some terminal side entity has detected an AIS condition and uses the E1 Byte for in-band communication of the condition. TTE1 can be used for autonomous generation of AIS at the Tx Line Port.

Input POH Storage

On a per frame basis, the B3 through Z5 bytes incoming at the Tx Terminal Port are stored in the RAM Segment 1CO[H] - 1C7[H]. If the Control TPATH (CR8; 1F8[H], Bit 3) = "0", the J1 Bytes will be stored in memory locations that are accessible at the RAM Segment 180[H] - 1BF[H]. This address space is shared with the Tx J0 Bytes. J1 Access is enabled when J0RWEN = "0". The Memory Locations for the POH Bytes are given in Table 21. When enabled, J1 Byte storage is controlled by J1SYNCEN. J1SYNCEN = "0" results in the J1 Bytes being stored in the 64-Byte Segment, in rotating fashion, with no specific starting point. When J1SYNCEN is set to "1" reception of ASCII characters CR and LF, in sequence, will cause the next J1 Byte to be written at address 180 [H] with subsequent J1 bytes being written in succeeding locations.

Byte	Location
J1	180[H] - 1BF[H]
B3	1C0[H]
C2	1C1[H]
G1	1C2[H]
F2	1C3[H]
H4	1C4[H]
Z3	1C5[H]
Z4	1C6[H]
Z5	1C7[H]

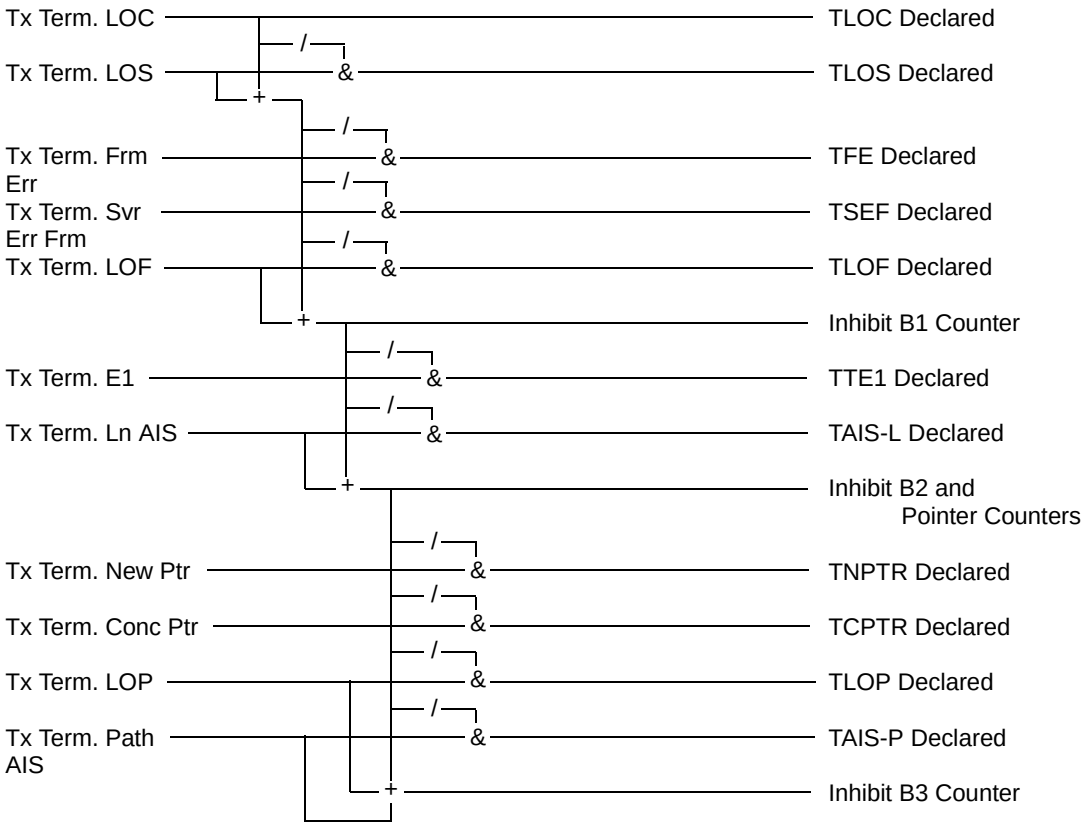
Table 21. Terminal POH Locations

Input B3 Processing

Input B3 processing is identical to B2 Processing except that only the SPE bytes are included in the calculation. The errors are accumulated in the Roll Over counter designated Tx B3 Error Count (1D4[H]). There is no overflow indicator.

TX SIDE ALARM HIERARCHY

A compilation of the hierarchical scheme used for Transmit Side alarm reporting is given in Equation 2 where: + represents the "OR" function, & represents the "AND" function, and / denotes the "NOT" function. It does not include the complete definitions for declaring or clearing each individual alarm. It is a reference that portrays the suppression effect of higher order alarms. The order of precedence is top to bottom. Also included are the conditions that inhibit the various performance counters.



Equation 2. Reporting Hierarchy for Transmit Alarms

TRANSMIT POH ASSEMBLY

The Tx OH Generator is responsible for assembling the POH that will be output on the Tx Line. The Payload portion of the SPE is input from the Tx Terminal Processor. In general, the POH Bytes have three possible sources:

1. The POH Bytes input at the Tx Terminal Port
2. Information written by the µPro.
3. The POH Bytes input at the Tx POH Port

TPATH = "0" selects Option One. When set to "1", options two or three are enabled. These two options make use of the Tx Insert POH Byte locations shown in Table 22.

Byte	Location
J1	180[H] - 1BF[H]
(B3)	1C8[H]
C2	1C9[H]
G1	1CA[H]
F2	1CB[H]
H4	1CC[H]
Z3	1CD[H]
Z4	1CE[H]
Z5	1CF[H]

Note: Used for Insert if TPATH = "1"

Table 22. Tx Insert POH Locations

The 64-Byte J1 Segment is common to Tx Terminal Input storage and Tx Line Insert storage. When TPATH = "1" the designated Insert J1 Values occupy these locations. When the J1 Locations are being filled from the Tx POH Port, J1SYNCEN controls whether the storage is rotating or synchronized as explained above in the "Input POH Storage" section. The B3 location contains an internally generated value. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of the SPE Bytes to be transmitted. The value calculated for Frame n is placed in the B3 Byte of Frame n+1. All other locations, when enabled, are available for writing by the µPro. Table 23 presents the available options for Transmit POH.

Byte(s)	Control Bit	Location CR#; Reg, Bit	TPATH	TPATH="1"	
				Control="0"	Control="1"
J1[1]	TJ1EXT	CR13; 1FD, 7	Tx Terminal J1 Byte	µPro J1 Bytes	Tx POH Port J1 Bytes
B3[1]	-	-	Tx Terminal B3 Byte[2]	Calculated Value	
C2[1]	TC2EXT	CR13; 1FD, 6	Tx Terminal C2 Byte	µPro C2 Bytes	Tx POH Port C2 Bytes
G1[1]	TG1EXT	CR13; 1FD, 5	Tx Terminal G1 Byte	µPro G1 Bytes	Tx POH Port G1 Bytes
F2[1]	TF2EXT	CR13; 1FD, 4	Tx Terminal F2 Byte	µPro F2 Bytes	Tx POH Port F2 Bytes
H4[1]	TXH4INS	CR13; 1FD, 3	Tx Terminal H4 Byte	Tx Terminal H4 Byte[3]	µPro H4 Bytes[3]
Z3[1]	TZ3EXT	CR13; 1FD, 2	Tx Terminal Z3 Byte	µPro Z3 Bytes	Tx POH Port Z3 Bytes
Z4[1]	TZ4EXT	CR13; 1FD, 1	Tx Terminal Z4 Byte	µPro Z4 Bytes	Tx POH Port Z4 Bytes
Z5[1]	TZ5EXT	CR13; 1FD, 0	Tx Terminal Z5 Byte	µPro Z5 Bytes	Tx POH Port Z5 Bytes

Notes:
1. Selection options are affected by the generation of Path Idle. See "Idle Insertion" below.
2. Only if H4INT, TPFEBEEN, TPRDIEN, TPRDIPD, TPRDICD and TPRDISD = "0". If H4INT, TPFEBEEN, TPRDIEN, TPRDIPD, TPRDICD or TPRDISD = "1" then Calculated Value will be used.
3. In SPE-only Mode, Datacom Mode, or SONET Mode with C1J1EN = "1" and if H4INT = "1", and RTLOOP = "0" then the two LSBs will be overwritten by the Internal H4 Counter value.

Table 23. Tx Line POH Options

The selected B3 Byte will be Exclusive-OR gated with the Tx B3 Error Mask (1D0[H]). If B3 is not internally calculated, then the number of errors generated will be doubled. TRERR (CR11; 1FB[H], Bit 6) is used to enable an automatic reset to all "0" of the B3 Error Mask. When set to "1" the B3 Error Mask will be reset after one frame. A value of "0" disables the automatic reset feature.

Tx Path FEBE Insertion

The Path FEBE (FEBE-P) function is enabled by TPFEBEEN. When activated, Bits 1 through 4 of the G1 Byte selected above are overwritten with a value of "0000" - "1000". If RING (CR11; 1FB[H], Bit 4) = "0" the number of received B3 Errors is the source for the FEBE-P Value. When RING = "1" the FEBE-P Value is supplied by the Ring Port. Since the received and transmitted SPE Rates may differ, an accumulation mechanism is employed to ensure that the FEBE-P Count returned will equal the B3 Errors received.

Tx Path RDI Insertion

Path RDI (RDI-Pxx where: xx = SD, PD, or CD) transmission is accomplished using the coding described in Table 14. Transmission of RDI-Pxx consists of overwriting bits 5-7 of the G1 Byte selected above with the appropriate code. There are ten controls associated with Path RDI insertion. Automatic RDI-Pxx insertion is enabled by TPRDIEN. B3PRDISD, B3PRDICD and TOHPRDISD (CR19; 1DB[H], Bits 2, 1, and 0) enable the B3 Excessive Bit Error Rate and TOH Faults in the appropriate RDI-Pxx equations. C2MPRDI and C2UPRDI (CR7; 1DE[H], Bits 3 and 2) enable Signal Label Mismatch and Signal Label Unequipped in the appropriate RDI-Pxx equations. The duration for sending RDI-Pxx is controlled by TPRDI20 (CR17; 1DD[H], Bit 0). If at the "0" Logic Level PRDI will be sent for the duration of the causative event. When set to "1", PRDI will be sent for a minimum of 20 Frames. TPRDISD, TPRDICD and TPRDIPD (CR19; 1DB[H], Bits 5, 4, and 3) are used to force the insertion of RDI-Pxx. When the control bit RING is activated the RDI-Pxx information to be inserted will come from the Ring Port. It should be noted that, when RING = "1", only the control TPRIDISD operates on the inserted Path RDI. The controls TPRDICD and TPRDIPD operate on the Ring Port output sent to the companion device. When RING = "0" all three controls operate on the inserted Path RDI.

Tx Idle Insertion

The Insertion of a Path Idle Signal is performed at the command of the µPro via the control TIDL (CR7; 1DE[H], Bit 7). The Path Idle Signal that is inserted may be one of two forms:

1. All bytes of the SPE (including the POH Bytes) are set to zero.
2. All bytes of the SPE except the POH Bytes are set to zero.

The form of the idle signal is selected by the control IDLSEL (CR7; 1DE[H], Bit 6). The first form is selected when IDLSEL = "0". The second type of Path Idle is selected when IDLSEL = "1". When TIDL = "0", POH byte selection is as described above. When TIDL = "1" and IDLSEL = "0", all POH selection controls are disregarded. When TIDL and IDLSEL both are set to "1", TPATH is disregarded and all POH bytes are taken from the Insert Locations.

TRANSMIT TOH ASSEMBLY

The Tx OH Generator is responsible for creating the signal that will be output on the Tx Line. The Tx Line Outputs consist of serial data - TLDO, and serial clock - TLCO. The functions performed include TOH Selection, Alarm Insertion, BIP-8 Calculations and Scrambling. The assembled SPE is taken from either the Tx Re-timing FIFO or the Tx Terminal Processor (Tx Re-timing disabled). In SONET Mode the TOH Bytes sent to the Tx Line have four possible sources:

1. The TOH Bytes input at the Tx Terminal Port
2. Information written by the µPro.
3. The TOH Bytes input at the Order Wire/APS Port, Section DCC Port, and Line DCC Port
4. The TOH Bytes input at the Tx TOH Port in All TOH Mode

Individual controls are used to select, on a per byte (or functional byte group) basis, between the various options. If SPE-only Mode is selected or TCLK = "1", then the settings which would enable option 1 are disregarded and only Options 2 through 4 are available.

Table 24 lists the TOH Insert Byte locations. These locations contain the TOH Bytes that will appear in the signal sent to the Tx Line when Option 1 is not selected. The B1 and B2 locations contain internally generated values. All other locations contain values written by the µPro or external values from the Tx TOH Port. In the OW/APS Mode, only the E1, E2, K1 and K2 Bytes may be externally created. In All TOH Mode, all TOH Bytes except B1, B2, H1, H2 and H3 may be externally generated.

	Byte	Location	Byte	Location	Byte	Location
Section	A1	136[H]	A2	137[H]	C1	13C[H]
	(B1)	134[H]	E1	138[H]	F1	13D[H]
	D1	125[H]	D2	126[H]	D3	127[H]
Line					H3	133[H]
	(B2)	135[H]	K1	13E[H]	K2	13F[H]
	D4	128[H]	D5	129[H]	D6	12A[H]
	D7	12B[H]	D8	12C[H]	D9	12D[H]
	D10	12E[H]	D11	12F[H]	D12	130[H]
	Z1	13A[H]	Z2	13B[H]	E2	139[H]

Table 24. Tx Insert TOH Locations

Tx A1 and A2 Selection

The A1 and A2 Bytes sent to the Tx Line are always taken from the Insert A1 and A2 Locations. TRFRM (CR11; 1FB[H], Bit 7) and TFRMEXT (CR14; 1FE[H], Bit 7) determine the Insert Location content. The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Generate	µPro	External
TRFRM = "1"	TRFRM = "0" & TFRMEXT = "0" + TRFRM = "0" & TFRMEXT = "1" & OA = "1"	TRFRM = "0" & TFRMEXT = "1" & OA = "0"

Tx C1/J0 Selection

Controls J0EN0, J0EN1, TXC1EXT (CR14; 1FE[H], Bit 6), TRC1(CR9; 1F9[H], Bit 6),and OA are used to control the C1 Selection. J0ENx selects the Insert Location as shown in Table 25. If J0EN1 = "1" the Insert locations consist of a 64-Byte RAM segment. Microprocessor access to these locations is by means of Locations 180[H] - 1BF[H], and is controlled by J0RWEN. When the Multiple Byte J0 messages are input via the TOH Port, the storage method is controlled by J0ENx. When J0EN(1,0) = "10" the bytes are stored in rotating fashion with no specific starting point. If J0EN(1,0) = "11" the reception of ASCII characters CR and LF, in sequence, will synchronize the J0 Counter so that the next J0 Byte will be written at the location that is accessed at address 180[H].

J0EN1	J0EN0	Transmit Function
0	-	Single Byte C1/J0 - 13C[H]
1	0	16/64-byte RAM segment used for J0 - accessed at 180[H]-1BF[H]. If external, storage is not aligned.
1	1	16/64-byte RAM segment used for J0 - accessed at 180[H]-1BF[H]. If external, storage is aligned.

Table 25. Tx C1/J0 Options

The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRC1 = "0"	SPE-only Mode selected & TXC1EXT = "0" + SPE-only Mode selected & OA = "1" + TRC1 = "1" & TXC1EXT = "0" + TRC1 = "1" & OA = "1"	SPE-only Mode selected & TXC1EXT = "1" & OA = "0" + TRC1 = "1" & TXC1EXT = "1" & OA = "0"

Tx B1 Selection

The B1 Byte sent to the Tx Line is dependent on the setting of STS1 and TRERR.

When STS1 = "0" the outgoing B1 Byte will contain the contents of the Tx B1 Error Mask (149[H]). The control TRERR is used to enable an automatic reset to all "0" of the B1 Mask. When set to "1" the B1 Error Mask will be reset after one frame. A value of "0" will disable the automatic reset feature.

In configurations where STS1 = "1", the B1 Byte is calculated and placed in the Insert B1 Location. The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of all bytes to be transmitted, after scrambling is performed. The value calculated for Frame n will be placed in the B1 Byte of Frame n+1 before scrambling is performed. The calculated value in the B1 Insert Location will be Exclusive-OR gated with the Tx B1 Error Mask prior to insertion in the transmit B1 Byte position. TRERR controls the resetting of the mask as explained above.

Tx E1 Selection

E1 Byte selection is controlled by TRE1 (CR8; 1F8[H], Bit 5) and TXE1EXT (CR14; 1FE[H], Bit 5). The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRE1 = "0"	SPE-only Mode selected & TXE1EXT = "0" + TRE1 = "1" & TXE1EXT = "0"	SPE-only Mode selected & TXE1EXT = "1" + TRE1 = "1" & TXE1EXT = "1"

These selections are not available if the E1 Byte is used for in-band alarm communication. See the section "Tx E1 Alarm Insertion," below.

Tx F1 Selection

Controls TXF1EXT (CR14; 1FE[H], Bit 4), TRF1(CR9; 1F9[H], Bit 7), and OA are used for F1 Selection. The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRF1 = "0"	SPE-only Mode selected & TXF1EXT = "0" + SPE-only Mode selected & OA = "1" + TRF1 = "1" & TXF1EXT = "0" + TRF1 = "1" & OA = "1"	SPE-only Mode selected & TXF1EXT = "1" & OA = "0" + TRF1 = "1" & TXF1EXT = "1" & OA = "0"

Tx D1-D3 Selection

D1-D3 Byte selection is controlled by TRSD (CR8; 1F8[H], Bit 7) and TXSDEXT (CR14; 1FE[H], Bit 3) The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRSD = "0"	SPE-only Mode selected & TXSDEXT = "0" + TRSD = "1" & TXSDEXT = "0"	SPE-only Mode selected & TXSDEXT = "1" + TRSD = "1" & TXSDEXT = "1"

In the OW/APS Application, the external source for the Bytes will be the Tx Section DCC Port. In the All TOH Application, the external source will be either the Tx Section DCC Port or the Tx TOH Port, as controlled by OA and SDCCEN (CR17; 1DD[H], Bit 7).

Tx H1-H3 Selection

The sources for the H1 and H2 Bytes may be either the Tx Terminal Port or the calculated values. The H3 Byte Sources are either the Tx Terminal Port or the Insert Location. If transmit re-timing is disabled, the Tx Terminal Locations are used for H1, H2 and H3. When transmit re-timing is enabled, the calculated H1 and H2 values, and the H3 Insert Location value, are used. The H3 value taken from the Insert Location will be overwritten by SPE data when a Pointer Decrement is performed. The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location - Internal
SPE-only Mode not selected & C1J1EN = "0" & TXRTM = "0" & TCLK = "0"	SPE-only Mode selected + C1J1EN = "1" + TXRTM = "1" +TCLK = "1"

Tx B2 Selection

The B2 Byte is calculated and placed in the Insert B2 Location when DISTB2R (CR17; 1DD[H], Bit 1) = "0". The calculation is Even Parity, independently performed, in parallel, over the eight bit positions of all bytes except the nine Section Overhead Bytes. The value calculated for Frame n is placed in the B2 Byte of Frame n+1. If DISTB2R = "1" and if TCLK = "0", the B2 Byte Incoming at the Tx Terminal Port will be output at the Tx Line Port.

The B2 value output on the Tx Line will be Exclusive-OR gated with the Tx B2 Error Mask (151[H]) prior to insertion. As has been discussed previously, TRERR controls the resetting of the mask.

Tx K1 and K2 Selection

K1 and K2 Byte Selection is controlled by TRAPS and EXAPS (CR8; 1F8[H], Bits 2 and 1). The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRAPS = "0"	SPE-only Mode selected & EXAPS = "0" + TRAPS = "1" & EXAPS = "0"	SPE-only Mode selected & EXAPS = "1" & OA = "0" + TRAPS = "1" & EXAPS = "1"

Tx D4-D12 Selection

D4-D12 Byte selection is controlled by TRLD (CR8; 1F8[H], Bit 6) and TXLDEXT (CR15; 1DF[H], Bit 7). The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRLD = "0"	SPE-only Mode selected & TXLDEXT = "0" + TRLD = "1" & TXLDEXT = "0"	SPE-only Mode selected & TXLDEXT = "1" + TRLD = "1" & TXLDEXT = "1"

In the OW/APS Application, the external source for the Bytes will be the Tx Line DCC Port. In the All TOH Application, the external source will be either the Tx Line DCC Port or the Tx TOH Port, as controlled by OA and LDCCEN (CR17; 1DD[H], Bit 6).

Tx Z1 Selection

The controls TXZ1EXT (CR14; 1FE[H], Bit 2), TRZ1 (CR9; 1F9[H], Bit 5), and OA are used to control the Z1 Selection. The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRZ1 = "0"	SPE-only Mode selected & TXZ1EXT = "0" + SPE-only Mode selected & OA = "1" + TRZ1 = "1" & TXZ1EXT = "0" + TRZ1 = "1" & OA = "1"	SPE-only Mode selected & TXZ1EXT = "1" & OA = "0" + TRZ1 = "1" & TXZ1EXT = "1" & OA = "0"

Tx Z2 Selection

TXZ2EXT (CR14; 1FE[H], Bit 1), TRZ2 (CR9; 1F9[H], Bit 4), and OA are used to control the Selection of Z2. The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRZ2 = "0"	SPE-only Mode selected & TXZ2EXT = "0" + SPE-only Mode selected & OA = "1" + TRZ2 = "1" & TXZ2EXT = "0" + TRZ2 = "1" & OA = "1"	SPE-only Mode selected & TXZ2EXT = "1" & OA = "0" + TRZ2 = "1" & TXZ2EXT = "1" & OA = "0"

Tx E2 Selection

E2 Byte selection is controlled by TRE2 (CR8; 1F8[H], Bit 4) and TXE2EXT (CR14; 1FE[H], Bit 0). The source selection is shown below where: & = the logical "AND" function, + = the logical "OR" function, and = represents a control state.

Tx Terminal Port	Insert Location	
	µPro	External
SPE-only Mode not selected & TRE2 = "0"	SPE-only Mode selected & TXE2EXT = "0" + TRE2 = "1" & TXE2EXT = "0"	SPE-only Mode selected & TXE2EXT = "1" & OA = "0" + TRE2 = "1" & TXE2EXT = "1"

Tx Line FEBE Insertion

FEBE-L insertion is enabled by the control TLFEBEEN. When enabled, the Line FEBE value ("0000" through "1000") overwrites Bits 5 through 8 of the Z2 Byte that has been selected. The FEBE-L Value can be obtained from the received B2 Errors or the Ring Port, as controlled by RING. An accumulation mechanism is used to account for differing transmit and receive rates.

Tx E1 Alarm Insertion

The E1 Byte sent to the Tx Line may optionally be used to communicate an in-band AIS Indication. This is controlled by command TA2E (CR11; 1FB[H], Bit 0). When Enabled :

1. The Settings of TRE1 and TXE1EXT will be disregarded.
2. The normal state of the E1 Byte will be all "0".
3. The occurrence of certain anomalies will result in the E1 Byte being set to all "1".

If the conditions are such that an E1 Alarm will be inserted (if enabled by TA2E) it will be indicated by the setting of TPAISC or TLAISC (SR8; 1F6[H], Bits 1 and 0). When E1 Alarm insertion is disabled the functioning of TRE1 and TXE1EXT is enabled.

Tx Path AIS Insertion

Path AIS (AIS-P) insertion consists of setting the H1, H2 and H3 Bytes and all SPE Bytes to "1". This function is enabled if TRAIS (CR9; 1F9[H], Bit 3) = "1" and either PTE (CR9; 1F9[H], Bit 2) or LTE (CR1; 0F9[H], Bit 2) = "1". AIS-P insertion is directly controlled by the µPro via the command STPAIS (CR11; 1FB[H], Bit 5). Path AIS insertion will also occur on Transmit FIFO underflow or overflow, if the automatic FIFO recovery option is set. In addition, AIS-P may, as an option, be automatically inserted upon certain Tx Terminal Port alarms and when the Alarm Port Input is active (Pin is Low). Use of the Tx Terminal E1 Alarm is enabled by TTEAIS (CR15; 1DF[H], Bit 5). The insertion of PAIS will terminate with the sending of a valid pointer with the NDF Bits active ("1001") for one frame. Subsequent pointer values will be transmitted with an inactive NDF ("0110") indication. If the conditions are such that a PAIS will be inserted (if enabled by TRAIS), this will be indicated by the setting of TPAISC.

Tx Line RDI Insertion

RDI-L is transmitted by setting K2, Bits 6, 7, and 8 to "110". LRDI may be inserted upon command from the µPro or the Ring Port and, if so enabled, autonomously upon certain Receive Side anomalies. The µPro command is STLRDI (CR15; 1DF[H], Bit 1). Automatic Line RDI insertion is enabled by the control TRLRDI (CR2; 0FA[H], Bit 4). The inclusion of B2EBER, as a condition for automatic insertion, is enabled by the control B2ELRDI (CR15; 1DF[H], Bit 0). The inclusion of J0MIS, as a condition for automatic insertion, is enabled by the control J0MLRDI (CR18; 1DC[H], Bit 6).

Tx Line AIS Insertion

Line AIS (AIS-L) insertion consists of setting all bytes of the Line Level Signal to "1". It is enabled if TRAIS = "1" and LTE and PTE = "0". AIS-L insertion is directly controlled by the µPro via the command STLAIS (CR17; 1DD[H], Bit 5). If enabled, AIS-L will be inserted if the Alarm Port input is active (Pin $\overline{\text{TAIS}}$ is Low) or if certain Tx terminal alarms exist. If the conditions are such that a AIS-L will be inserted (if enabled by TRAIS), this will be indicated by the setting of TLAISC. The insertion of AIS-L will terminate with the sending of a valid pointer with the NDF Bits active ("1001") for one frame. Subsequent pointer values will be transmitted with an inactive NDF ("0110") indication.

LOOPBACKS

Three loopbacks are available: Line Loopback, Tx-Rx Line Loopback, and Rx-Tx Terminal Loopback. These are indicated in the Block Diagram (Figure 14) and as the shaded multiplexers in Figure 78. The italicized designations in Figure 78 are control bits.

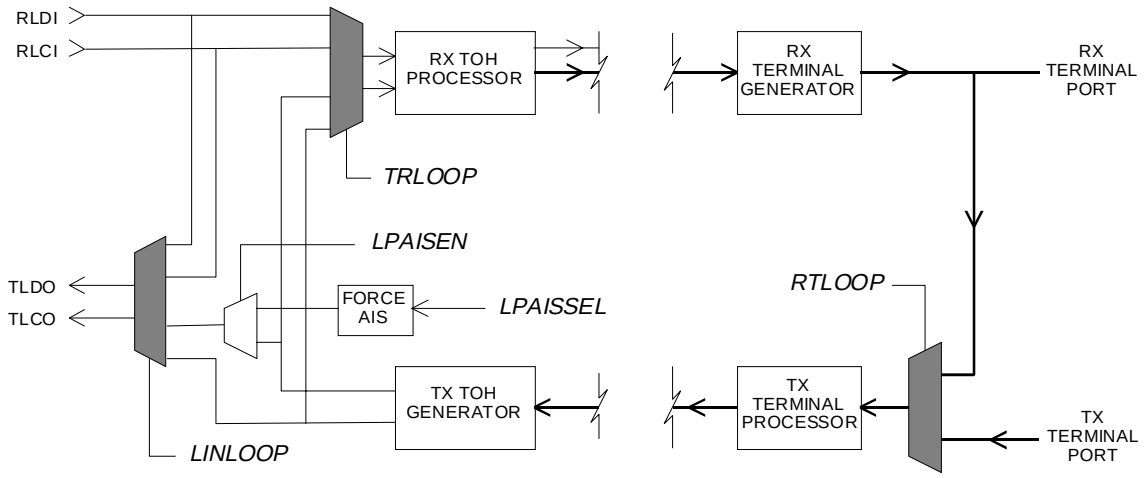


Figure 78. Loopbacks

Line Loopback

Line Loopback disconnects the Clock and Data Outputs from the Tx TOH Generator and substitutes the information incoming on RLCI and RLDI. This is controlled by LINLOOP (CR17; 1DD[H], Bit 2).

Tx-Rx Line Loopback

Tx-Rx Line Loopback disconnects the RLDI and RLCI Inputs and substitutes the Tx TOH Generator Clock and Data outputs. When Tx-Rx Line Loopback is initiated RFRI is disregarded. This Loopback is controlled by TRLOOP (CR0; 0F8[H], Bit 0).

When a Tx-Rx Line Loopback is enabled the signal exiting on TLDO may be either the information that is looped back, i.e., the information input at the Tx Terminal Port, or it may be a forced AIS signal. This is controlled by LPAISEN (CR12; 1FC[H], Bit 4). When the Forced AIS option is selected LPAISSEL (CR12; 1FC[H], Bit 3) determines if AIS-L or AIS-P is output. Termination of AIS Insertion by removing the loopback or changing the state of LPAISEN will not cause an NDF to be transmitted. AIS termination with an NDF indication can be achieved by performing the following sequence:

1. forcing the Tx OH Generator to Insert the appropriate AIS
2. removing the loopback or changing LPAISEN
3. Terminating the AIS Insertion at the Tx OH Generator.

Activation of Tx-Rx Line Loopback will inhibit RLFRI from creating interrupts or downstream alarms. The RLOC and RLOS Detectors will monitor the looped signal.

Rx-Tx Terminal Loopback

Rx-Tx Terminal Loopback disconnects the path between the Tx Terminal Port and the Tx Terminal Processor and substitutes the Rx Terminal Generator output for the Tx Terminal Port Input. Rx-Tx Terminal Loopback is controlled by RTLOOP (CR8; 1F8[H], Bit 0). When Rx-Tx Terminal Loopback is enabled the signal at the Rx Terminal Port is unaffected. Activation of Rx-Tx Terminal Loopback will inhibit TLOC and TLOS from creating interrupts or upstream alarms if TTOHEN = "0". If TTOHEN = "1" during Rx-Tx Terminal Loopback, the TLOC and TLOS circuits will monitor the terminal inputs. The looped data is not processed by the Tx terminal framer (which continues to monitor the Tx terminal input data) but rather has a frame indicator sent with it to the Tx Terminal Processor from the Rx side.

RESETS

The PHAST-1 has four reset mechanisms: Hardware Reset, Software Receive Side Reset, Software Transmit Side Reset and Chip Reset.

Hardware Reset is accomplished with the pin $\overline{\text{RST}}$, which is active Low. This is a level sensitive input. The device remains in the reset condition until $\overline{\text{RST}}$ is returned to the High Level. When activated, the reset process will:

1. Reset all Counters
2. Reset all Control Registers
3. Clear All Status Bits
4. Re-center the FIFOs
5. Set HWRST (SR1; 0F2/3/5[H], Bit 0)
6. Set INT (SR1; 0F2/3/5[H], Bit 7)

A Receive Software Reset is initiated by RSWRES (CR3; 0FB[H], Bit 1). A Transmit Software Reset is Controlled by TSWRES (CR15; 1DF[H], Bit 6). A Software Reset consists of resetting the Counters and Status Bits associated with the Transmit or Receive Sides. A Chip Reset is initiated by CHPRES (CR18; 1DC[H], Bit 0). A Chip Reset is similar to a Hardware Reset (pin $\overline{\text{RST}}$), except that control registers and the µPro interface are not affected. A Software Reset or Chip Reset is initiated by setting the appropriate control bit to "1". The reset state will remain in effect until the control bit is returned to the "0" logic level. Note that RSWRES will disable the Frame Pulse and clock of the Rx Ring Port. Ring Port Data will continue to be sent out but B3 errors may be repeated.

MICROPROCESSOR INTERFACE

The µPro Interface is the means by which PHAST-1 is queried and controlled. Three microprocessor types are supported: Intel, Motorola and Multiplexed Address/Data bus. The pins µPSEL0 and µPSEL1 determine the interface type.

Software Operations

All Memory Locations are Read and Write except for: 000[H] - 004[H], Clear on Read Status Registers and Unlatched Status Registers which are Read Only. Status or Control Register bit positions marked "Unused" are not equipped. Bit 7 of CR6 (0FE[H]), and Bits 7 and 6 of CR19 (1DB[H]) are marked "Reserved". These bits should be set to "0". Failure to do so may jeopardize software compatibility in future device revisions. The Control bit RAMTSTEN (CR6; 0FE[H], Bit 6) is provided to allow memory testing. When it is set to "1" RAM access by all internal operations is inhibited. Two controls: TEST1 and TEST2 (CR17; 1DD[H], Bits 4 and 3) are used for Internal TXC tests. These must be set to "0" for normal operation.

All Counters clear on Read. Writing to a 16-Bit Counter is accomplished by first writing the HIBYTE Location (1FF[H]) then writing to the Lower Order Register. Reading is accomplished by reading the lower order register then reading HIBYTE. Registers 0F6[H] and 1F6[H] are non-latching registers used for Receive Side and Transmit Side counter overflows, respectively. One bit is provided for each counter except for the Pointer Increment and Decrement Counters. The Rx Pointer Increment and Decrement Counters use the same bit to indicate overflow. Similarly, the Tx Pointer Increment and Decrement Counters are combined into a single bit. There are no overflow indication bits for the Tx B1, B2 or B3 counters.

Alarm reporting is accomplished with seven sets of three Status Registers (SR0 - SR6), each of which is composed of two latching locations and one non-latching location, and three single Status Registers (SR7 - SR9), which provide only unlatched values. In either case, the alarm is indicated by the appropriate bit being set to "1". In SR0 - SR6, each alarm occupies the same bit position in each of the three registers. The First Register of the set provides latched values that clear (reset to "0") when the register is read. The Second Register contains latched values that are cleared, on a per bit basis, by writing a "1" to the bit that is to be cleared (multiple bit positions may be simultaneously cleared). It must be noted that the clearing of either latched register is reflected in the contents of the other register. For example, reading the First Register clears all alarms in both the First and Second Registers. Similarly, Writing a "1" to a bit in the Second Register clears that alarm bit in both the First and Second Registers. For test purposes, writing a "1" to any bit(s) with the address of the Third Register of SR0 - SR6 will set to "1" the corresponding bit(s) in the First and Second Registers. The Third Register of the set and SR7 - SR9 contain unlatched values that provide a real time indication of the alarm status. Bits in these locations will be at a logical "1" for the duration of the causative event.

Interrupt Structure

In general, interrupts are created on alarms or counter overflows. Alarm-related interrupts may occur either on the positive edge (event start) or, if so enabled, on both the positive and negative edges (event start and end) of the causative incident. Counter overflow interrupts are initiated only on the detection of the overflow condition. Clearing the counter does not create an interrupt. The creation of an interrupt is reported as INT in Register 0F2[H]. Any time that an interrupt is created this bit will be set to "1".

To simplify interrupt handling an unlatched Polling Register is provided (0F7[H]). It is used to indicate the condition of the six Status Registers and the two Counter Overflow Registers. Each of the eight registers is assigned a bit in this register. One or more bits set in a Status or Counter overflow register will cause the appropriate Polling Register bit to be set.

There are six controls that manage the creation of interrupts. They are:

1. HWINE (CR2; 0FA[H], Bit 5)
2. INVINT (CR5; 0FD[H], Bit 0)
3. -VE (CR2; 0FA[H], Bit 0)
4. TIEN (CR2; 0FA[H], Bit 2)
5. PIEN (CR2; 0FA[H], Bit 1)
6. DIEN (CR5; 0FD[H], Bit 7)

HWINE is the master hardware interrupt enable. When set to "1" the interrupt output to the µPro (pin INT/$\overline{\text{IRQ}}$) is enabled. A value of "0" disables the creation of interrupts at the pin. INVINT is used to logically invert the pin INT/$\overline{\text{IRQ}}$. Setting this bit to "1" causes the signal to become $\overline{\text{INT}}$/IRQ. -VE is the edge control for alarm-generated interrupts. A value of "0" creates the interrupts on the positive edge only. When set to "1" interrupts will be created on both the positive and negative edges. -VE has no effect on the generation of interrupts by counters that overflow. TIEN, PIEN and DIEN enable categories of events for interrupt creation. These three controls are discussed below.

Transport Layer Interrupts

Interrupt enabling for Transport Layer events is controlled by TIEN. TIEN = "0" will disable interrupts. When set to "1" the creation of interrupts is enabled. Transport Layer Events are defined in Table 26.

Event	Source	-VE Control
RLOS	Rx Line Interface	Yes
RFE	Rx Framer	Yes
RSEF	Rx Framer	Yes
RLOF	Rx Framer	Yes
RAIS-L	Rx TOH Processor	Yes
RLE1	Rx TOH Processor	Yes
RRDI-L	Rx TOH Processor	Yes
B2EBER	Rx TOH Processor	Yes
RTNEW	Rx TOH Processor	No
RAPS	Rx TOH Processor	Yes
RAIS-P	Rx Pointer Tracking	Yes
RLOP	Rx Pointer Tracking	Yes
RB1COF	Rx TOH Processor	No
RB2COF	Rx TOH Processor	No
RLFEBEOF	Rx TOH Processor	No
Rx Inc OF	Rx Pointer Tracking	No
Rx Dec OF	Rx Pointer Tracking	No
RPJOF	Rx Pointer Tracking	No
RNPTR	Rx Pointer Tracking	No
RCPTR	Rx Pointer Tracking	Yes
RGLRDI	Ring Port	Yes
LPJOF	Rx Pointer Generation	No
TLOS	Tx Terminal Port	Yes
TFE	Tx Terminal Framer	Yes
TSEF	Tx Terminal Framer	Yes
TLOF	Tx Terminal Framer	Yes
TAIS-L	Tx Terminal Processor	Yes
TTE1	Tx Terminal Processor	Yes
TAIS-P	Tx Terminal Pointer Tracking	Yes
TLOP	Tx Terminal Pointer Tracking	Yes
Tx Inc OF	Tx Terminal Pointer Tracking	No
Tx Dec OF	Tx Terminal Pointer Tracking	No
TCPTR	Tx Terminal Pointer Tracking	Yes
TNPTR	Tx Terminal Pointer Tracking	No

Table 26. Transport Layer Events

Path Layer Interrupts

Interrupt enabling for Path Layer events is controlled by PIEN. PIEN = "0" will disable interrupts. When set to "1" the creation of interrupts is enabled. Path Layer Events are defined in Table 27.

Event	Source	-VE Control
RRDI-P	Rx POH Processor	Yes
B3EBER	Rx POH Processor	Yes
C2MIS	Rx POH Processor	Yes
C2UNEQ	Rx POH Processor	Yes
RLOM	Rx POH Processor	Yes
RPNEW	Rx POH Processor	No
RB3COF	Rx POH Processor	No
RPFEBEOF	Rx POH Processor	No
RGPRDI	Tx Ring Port	Yes

Table 27. Path Layer Events

Device Layer Interrupts

Interrupt enabling for Device Layer events is controlled by DIEN. DIEN = "0" will disable interrupts. When set to "1" the creation of interrupts is enabled. Device Layer Events are defined in Table 28.

Event	Source	-VE Control
RLOC	Rx Line Interface	Yes
RLFRI	Rx Line Interface	Yes
LORR	Terminal Timing Gen.	Yes
RRCOFA	Terminal Timing Gen.	No
RFIFOE	Rx Re-timing FIFO	No
TAISV	Alarm Port	Yes
TBPE	Tx Terminal Port	No
RBUSCOL	Rx Terminal Port	Yes
TLOC	Tx Terminal Port	Yes
LOTR	Line Timing Gen.	Yes
TRCOFA	Line Timing Gen.	No
DRCOFA	Line Timing Gen.	No
TFIFOE	Tx Re-timing FIFO	No
LORG	Tx Ring Port	Yes

Table 28. Device Layer Events

TEST AND DIAGNOSTICS

For testing and diagnostic purposes the PHAST-1 provides Loopbacks (previously discussed), Output Disable capability and Boundary Scan.

Output Disable

The pin $\overline{\text{TEST}}$ is a control that when taken Low, with $\overline{\text{RST}}$ held Low, will force all output and bidirectional pins to a high impedance state. $\overline{\text{TEST}}$ at the Low Level by itself invokes a TXC Device Test Mode. For normal operation $\overline{\text{TEST}}$ must be at the High Level.

Boundary Scan

Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and test data registers, and a boundary scan register path bordering the input and output pins, as illustrated in Figure 79. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCKI), Test Mode Select (TMSI), Test Data Input (TDI) and Test Reset ($\overline{\text{TRESI}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCKI) signal, a Test Mode Select (TMSI) signal, and a Test Reset ($\overline{\text{TRESI}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a three-bit serial instruction register and two or more serial test data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and test data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device pins to pass to and from the PHAST-1 device's internal logic, as illustrated in Figure 79. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 51.

Boundary Scan Support

The maximum frequency the PHAST-1 device will support for boundary scan is 10 MHz. The PHAST-1 device performs the following boundary scan test instructions (ID commands and ID Register are not supported):

- EXTEST (000) -SAMPLE/PRELOAD (010) -BYPASS (111)

It should be noted that the Capture - IR State (INSTRUCTION_CAPTURE attribute of BSDL) is 011.

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the PHAST-1 device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external PHAST-1 input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the PHAST-1 device remains fully operational. While in this test mode, PHAST-1 input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the PHAST-1 device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

Boundary Scan Reset

Specific control of the $\overline{\text{TRESI}}$ pin is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This pin should be held low whenever boundary scan operations are not being performed. Placing a pull down resistor from $\overline{\text{TRESI}}$ pin to ground, which can allow a tester to drive the $\overline{\text{TRESI}}$ pin high, is suggested when the boundary scan testing feature is used.

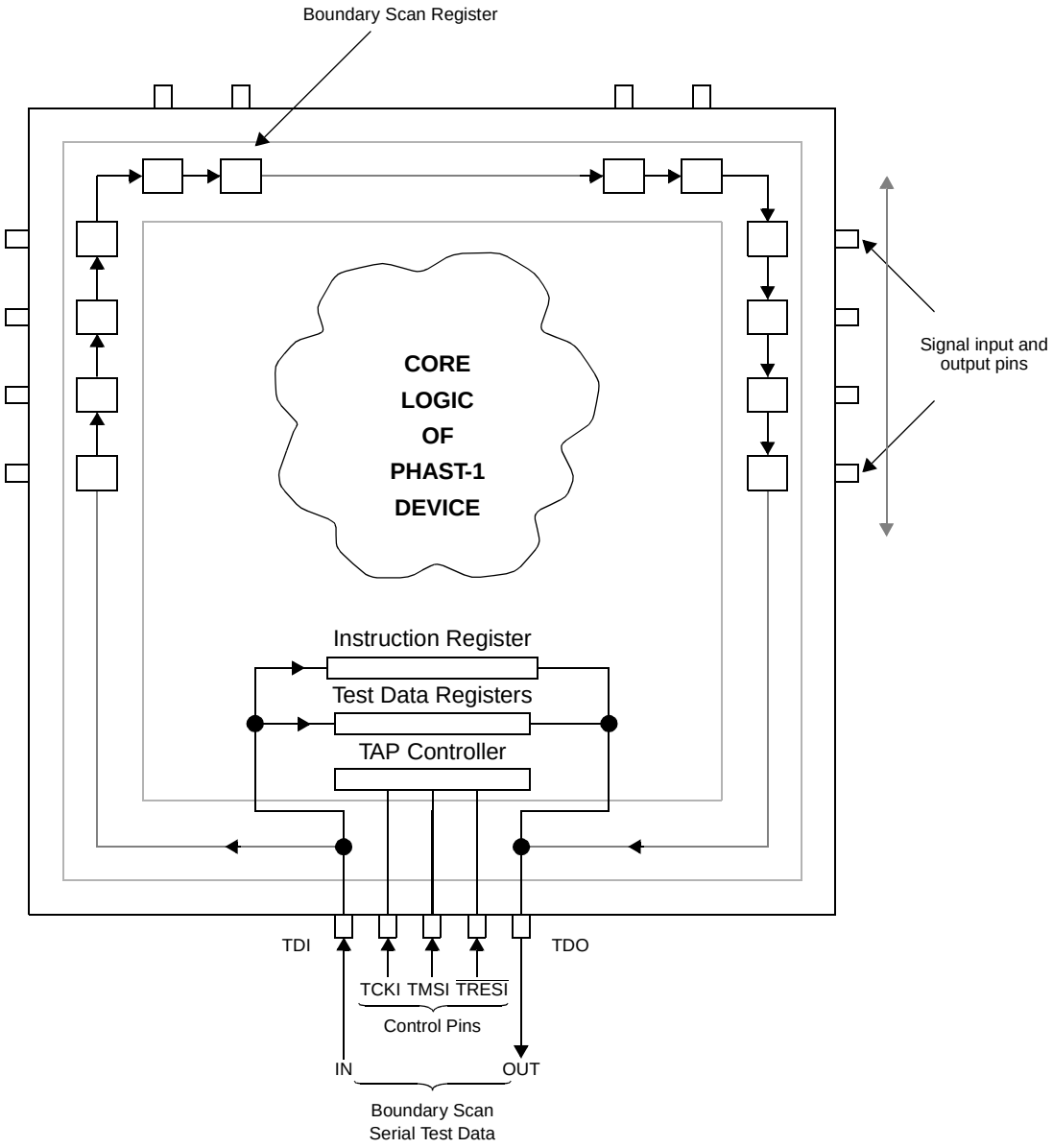


Figure 79. Boundary Scan Schematic

Boundary Scan Chain

There are 127 scan cells in the PHAST-1 boundary scan chain. Bidirectional device pins require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their functions. Cells that are not associated with a pin are marked "NA" in the Pin No. column.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
126	OUTPUT3	1	RSYN	
125	OUTPUT3	3	TPDO0	
124	OUTPUT3	5	TPDO1	
123	OUTPUT3	7	TPDO2	
122	OUTPUT3	9	TPDO3	
121	OUTPUT3	10	TPDO4	
120	OUTPUT3	12	TPDO5	
119	OUTPUT3	14	TPDO6	
118	OUTPUT3	16	TPDO7	
117	OUTPUT3	20	TPCO	
116	OUTPUT3	22	RTCO	
115	OUTPUT3	25	RTDO	
114	INPUT	28	RFRI_B	
113	INPUT	30	RLDI	
112	INPUT	31	RLCI	
111	INPUT	32	RXLOS_B	
110	OUTPUT3	34	RSPE	
109	OUTPUT3	36	RAIS_B	
108	INPUT	8	TPDVI1_B	
107	INPUT	2	TPDVI0_B	
106	OUTPUT3	11	TPDVO_B	
105	INPUT	15	RRFI_RRFI_B	
104	INPUT	13	RRCI	
103	OUTPUT3	18	RGFR_B	
102	OUTPUT3	19	RGCO	
101	OUTPUT3	23	RGDO	
100	OUTPUT3	26	RPS_B	
99	OUTPUT3	29	PRCO	
98	OUTPUT3	35	PRDO	
97	OUTPUT3	38	RSF_B	

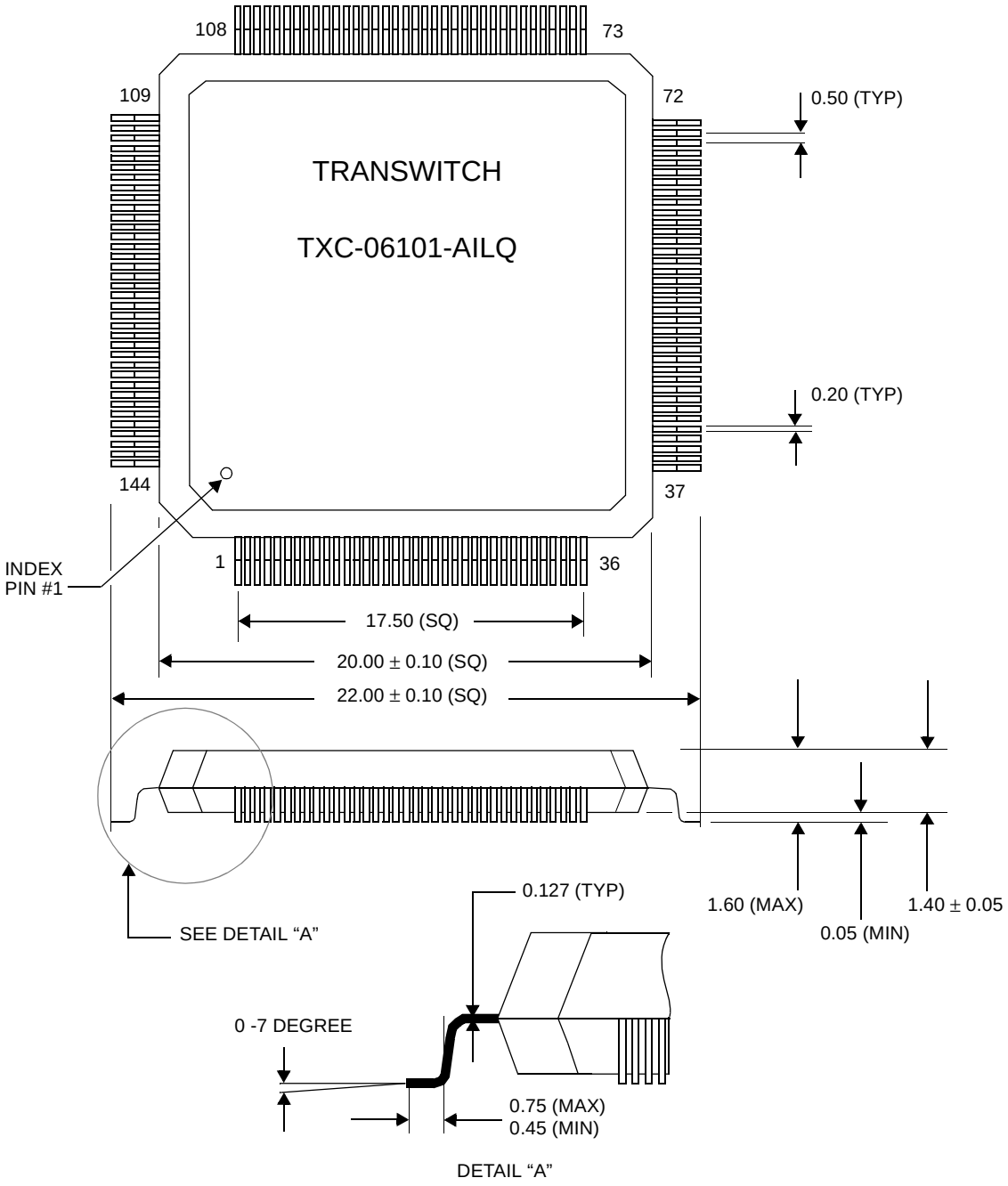
Scan Cell No.	I/O	Pin No.	Symbol	Comments
96	INPUT	37	MAD0/D0	
95	OUTPUT3	37	MAD0/D0	
94	INPUT	39	MAD1/D1	
93	OUTPUT3	39	MAD1/D1	
92	INPUT	42	MAD2/D2	
91	OUTPUT3	42	MAD2/D2	
90	INPUT	43	MAD3/D3	
89	OUTPUT3	43	MAD3/D3	
88	INPUT	46	MAD4/D4	
87	OUTPUT3	46	MAD4/D4	
86	INPUT	48	MAD5/D5	
85	OUTPUT3	48	MAD5/D5	
84	INPUT	50	MAD6/D6	
83	OUTPUT3	50	MAD6/D6	
82	INPUT	52	MAD7/D7	
81	OUTPUT3	52	MAD7/D7	
80	INPUT	53	AD8	
79	INPUT	56	WRB_RD_WRB	
78	INPUT	61	RD_B	
77	OUTPUT3	63	TLDO	
76	OUTPUT3	64	TLCO	
75	INPUT	67	TLCI	
74	INPUT	68	TFRI_B	
73	INPUT	72	ALE	
72	OUTPUT3	60	RDY_DTK_B	
71	INPUT	40	AD0	
70	INPUT	44	AD1	
69	INPUT	47	AD2	
68	INPUT	51	AD3	
67	INPUT	54	AD4	
66	INPUT	55	AD5	
65	INPUT	57	AD6	
64	INPUT	59	AD7	
63	INPUT	65	UPSEL0	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
62	INPUT	71	UPSEL1	
61	OUTPUT3	69	PTCO	
60	INPUT	83	PTDI	
59	OUTPUT3	73	INT_IRQ_B	
58	INPUT	75	SEL_B	
57	INPUT	77	TAIS_B	
56	INPUT	78	TSPEI_O	
55	OUTPUT3	78	TSPEI_O	
54	INPUT	79	TSYNI_O	
53	OUTPUT3	79	TSYNI_O	
52	OUTPUT3	81	STFR	
51	OUTPUT3	82	LTFR	
50	OUTPUT3	84	TAP_B_TTS_B	
49	INPUT	86	OTDI	
48	OUTPUT3	88	OTCO	
47	INPUT	89	STDI	
46	OUTPUT3	92	STCO	
45	INPUT	94	LTDI	
44	OUTPUT3	97	LTCO	
43	INPUT	100	TPDI7	
42	INPUT	102	TPDI6	
41	INPUT	103	TPDI5	
40	INPUT	104	TPDI4	
39	INPUT	106	TPDI3	
38	INPUT	108	TPDI2	
37	INPUT	109	TPDI1	
36	INPUT	111	TPDI0	
35	OUTPUT3	91	TPS_B	
34	INPUT	95	RGDI	
33	INPUT	96	DRCI	
32	INPUT	101	DFRI_DFRI_B	
31	INPUT	114	TEST_B	
30	INPUT	117	TPCI_O	
29	OUTPUT3	117	TPCI_O	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
28	INPUT	118	TTCI_O	
27	OUTPUT3	118	TTCI_O	
26	INPUT	120	TTDI	
25	INPUT	124	RST_B	
24	OUTPUT3	125	SRFR	
23	OUTPUT3	128	LRFR	
22	OUTPUT3	130	RAP_B_RTS_B	
21	OUTPUT3	133	ORDO	
20	OUTPUT3	138	ORCO	
19	OUTPUT3	139	SRDO	
18	OUTPUT3	140	LRCO	
17	OUTPUT3	142	LRDO	
16	OUTPUT3	144	SRCO	
15	INPUT	119	TPARI	
14	OUTPUT3	112	ISCODO	
13	OUTPUT3	110	ISCOCO	
12	OUTPUT3	116	ISCOFO_B	
11	INPUT	123	SOT1E_B	This pin must be held Low.
10	INPUT	132	MBEI_B	
9	OUTPUT3	134	ISCIFO_B	
8	OUTPUT3	137	ISCICO	
7	INPUT	143	ISCIDI	
6	OUTPUT3	141	TPARO	
5	CONTROL	NA		Tri-state control for TSPEI_O, TSYNI_O, TPCI_O, TTCI_O. Set to 0 to enable.
4	CONTROL	NA		Tri-state control for MAD(0-7)/D(0-7). Set to 0 to enable.
3	CONTROL	NA		Tri-state control for all other outputs. Set to 0 to enable.
2	CONTROL	NA		Tri-state control for RSYN, TPDO(0-7), RSPE, TPARO. Set to 0 to enable.
1	NA	NA	NA	Extra cell, not used.
0	CONTROL	NA		Tri-state control for RDY_DTK_B. Set to 0 to enable.

PACKAGE INFORMATION

The PHAST-1 is packaged in a 144-pin low profile plastic quad flat package suitable for surface mounting, as shown in Figure 80. All linear dimensions are in millimeters and are nominal unless otherwise noted.



Note: This package complies with JEDEC Publication 95, Specification MS-026. All linear dimensions are in millimeters.

Figure 79. PHAST-1 TXC-06101 144-Pin Low Profile Plastic Quad Flat Package

APPLICATION DIAGRAM

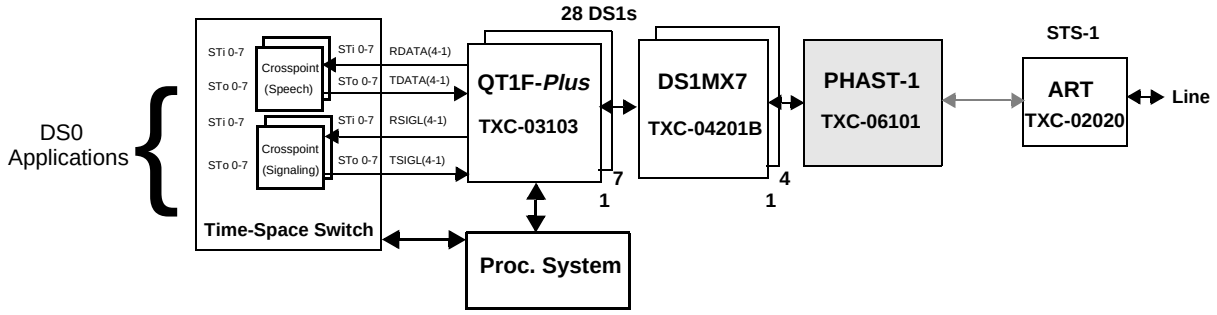


Figure 81. Asynchronous DS0 to/from Synchronous STS-1 Application

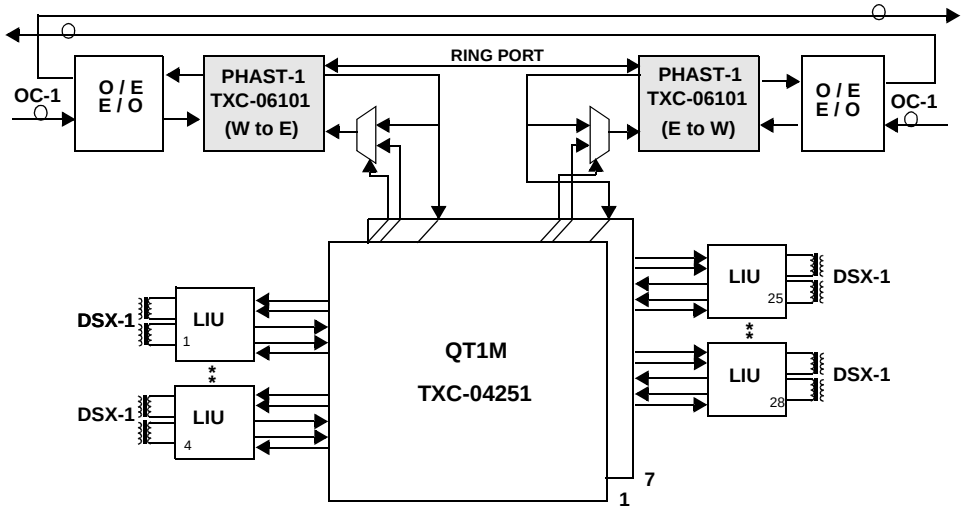


Figure 82. Asynchronous DSX-1 Mapped to OC-1 Ring-Protected Application

ORDERING INFORMATION

Part Number: TXC-06101-AILQ	144-pin Low Profile Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). The ART performs the transmit and receive line interface functions for interfacing STS-1 (51.84 Mbit/s) and DS3 (44.736 Mbit/s) signals at a coaxial interface.

TXC-02021, ARTE VLSI Device. The ARTE performs the same functions as the ART with some extended features that use more input/output pins. It has a larger package.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). In a single device, it provides the SONET interface to any payload. It provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal. This device has two operating modes, one for backwards compatibility with the predecessor TXC-03001 SOT-1 device (which is not recommended for use in new designs) and another which permits enabling of new features.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). In a single device, it provides the SONET interface to any payload. It provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal. This device has extended features relative to the TXC-03001B that use more input/output pins. It has a larger package.

TXC-03003 and TXC-03003B, SOT-3 VLSI Device (SONET STM-1/STS-3/STS-3c Overhead Terminator). SOT-3 performs Section (RS), Line (MS), and Path Overhead processing for STM-1, STS-3 or STS-3c signals. The TXC-03003B should be used in new designs instead of the TXC-03003.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). The QT1F-*Plus* is a four channel DS1 framer with extended features for voice and data communications.

TXC-03452 and TXC-03452B, L3M VLSI Device (Level 3 Mapper/Desynchronizer) - L3M maps a DS3 or E3 signal into an SDH/SONET signal formatted for STM-n (VC-3 via TU-3) or STS-n (via STS-1 SPE). The TXC-03452B should be used in new designs instead of the TXC-03452.

TXC-04001B, ADMA-T1 VLSI Device (Dual DS1 to VT1.5 Async, Mapper/Desynchronizer) - ADMA-T1 maps two asynchronous DS1 signals into any two VT1.5s of a SONET STS-1 SPE.

TXC-04011, ADMA-T1P VLSI Device (Dual DS1 to VT1.5 Async, Mapper/Desynchronizer) - ADMA-T1P performs the same functions as ADMA-T1 with support of Add Bus Timing Mode. It is packaged in a 120 pin PQFP.

TXC-04201, DS1MX7 VLSI DEvice (DS1 Mapper 7-Channel). The DS1MX7 maps seven DS1 signals into any seven selected asynchronous or byte synchronous mode VT1.5 or TU-11 tributaries in a SONET/SDH synchronous payload envelope.

TXC-04251, QT1M VLSI Device (Quad DS1 to TU-11/VT1.5 Async, Mapper/Desynchronizer) - QT1M maps four asynchronous DS1 signals into SDH (TU-11 via TUG-2 and TUG-3) or SONET (VT1.5 via VTG and STS-1 SPE).

TXC-04252, QE1M VLSI Device (Quad E1 to TU-12/VT2 Async, Mapper/Desynchronizer) - QE1M maps four asynchronous E1 signals into SDH (TU-12 via TUG-2 and TUG-3) or SONET (VT2 via VTG and STS-1 SPE).

TXC-05150, CDB VLSI Device (Cell Delineation Block) - CDB provides cell delineation for ATM cells carried in a physical line at rates of 1.544 Mbit/s to 155.52 Mbit/s.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator/Receiver) - XBERT is a programmable multi-rate test pattern generator and checker with serial, nibble or byte interface capabilities.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
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