Part 6

TMP68HC003DF-12
(TMP68HC000ASSP with Power-Down Function)

Chapter 1 Outline

Designed around the TMP68HC000 core, TMP68HC003 is equipped with a clock generator and power-down function for low power consumption applications.

Features:

- Built-in power-down function
- Built-in clock generator
- Includes all TMP68HC000 functions
- Built-in emulation mode for attaching in-circuit emulators
- Low power consumption (See figure 1.1 Typical Icc Data)
- Low-voltage operation (Vcc = 3.0V ±10%)

Figure 2.1 shows the pin assignment of TMP68HC003F; Figure 2.2 is the block diagram. To control the power-down function, the Vcc2, VCUT, OFFSET, and $\overline{\text{RELEASE}}$ pins are added to TMP68HC003F. To control the clock generator, the XTAL1, XTAL2, CLKOUT and ENABLE pins are added. For in-circuit emulation support, the NOR / $\overline{\text{EMU}}$, $\overline{\text{ERST}}$, and $\overline{\text{EHLT}}$ pins are provided.

Assuming a prior understanding of the TMP68HC000 core, this manual describes the power-down function and the clock generator. For detailed specifications on the TMP68HC000 core, refer to the Toshiba TLCS-68000 Microprocessor Data Book.

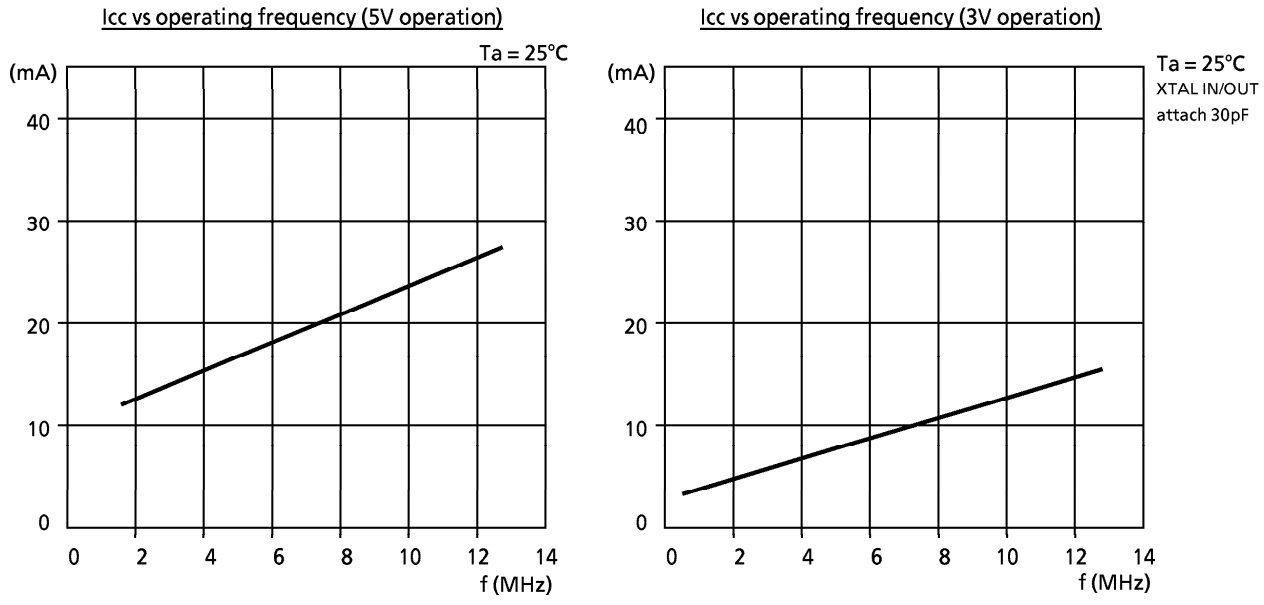

Figure 1.1 Typical Icc Data

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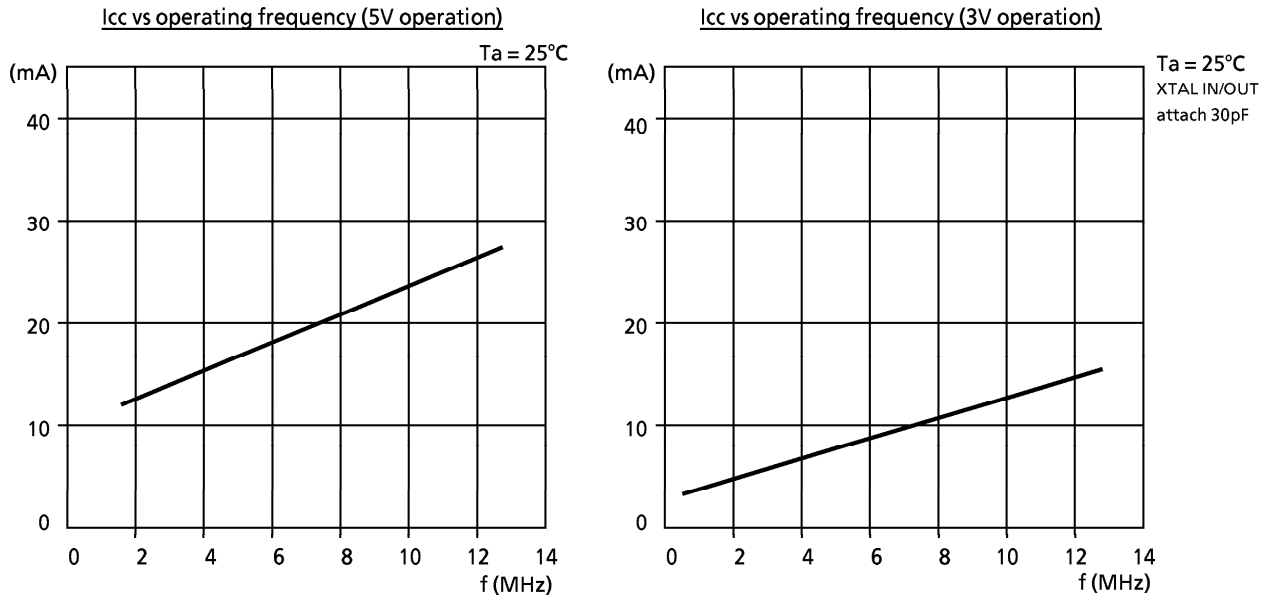


Figure 1.1 Typical Icc Data

Chapter 2 Pin Assignment and Function

2.1 Pin Assignment

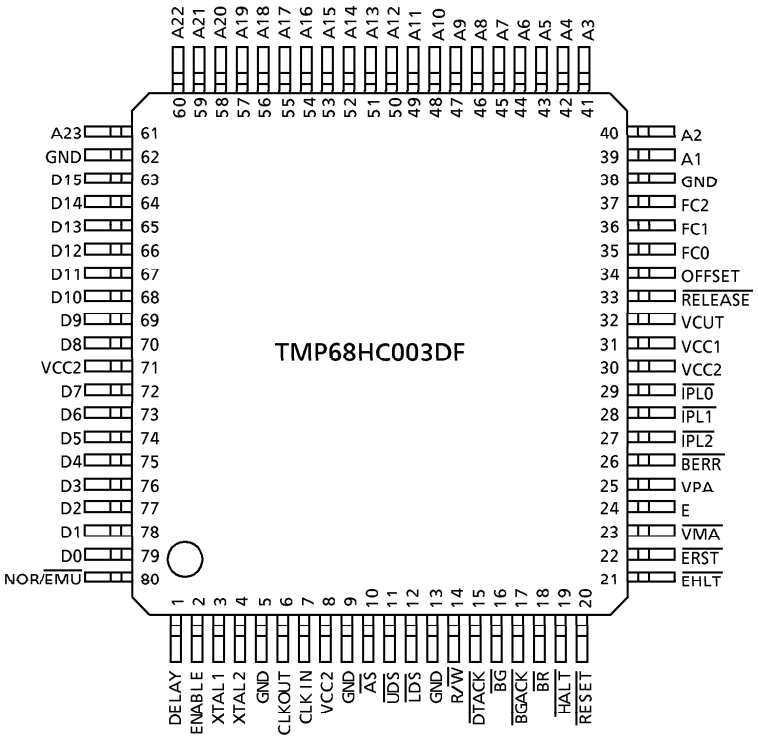


Figure 2.1 Pin Assignment

2.2 Pin Names and Functions (1/2)

The following describes pin states and functions in normal, emulation, and power-down modes.

NOR : Normal mode, EMU : Emulation mode, O.D : Open drain output,
O : Output, I: Input, I/O : Input/output

Signal name	Pin status			Function
	NOR	PDOWN	EMU	
A1~A23	O	I	I	23-bit address bus. Can directly access 16M bytes of memory.
FC0~FC2	O	O Note 1	I	These signals show the status of the processor and the current cycle type.
D0~D15	I/O	I Note 5	I	16-bit general-purpose data bus.
AS	O	O Note 1	I	This signal indicates that there is a valid address on the address bus.
R / W	O	O Note 1	I	This signal indicates whether the data transfer is read (high) or write (low).
$\overline{UDS}$ / $\overline{LDS}$	O	O	I	These signals control the data on the data bus.
$\overline{DTACK}$	I	I	I	This signal indicates the end of a data transfer.
BR	I	I Note 1	I	This signal is wire-ORed with all other devices that could become bus masters. The signal indicates that another device is requesting bus mastership.
BG	O	O	I	This signal indicates to devices that could become bus masters that the processor will release control of the bus at the end of the current bus cycle.
BGACK	I	I	I	This signal indicates that another device has become the bus master.
$\overline{IPL0~2}$	I	I	I	These signals are used to indicate the encoded priority level of the device requesting an interrupt. In power-down mode, the signals are also used as power-down release signals.
$\overline{BERR}$	I	I	I	This signal reports to the processor that there is a problem in the current cycle.
$\overline{RESET}$	I/O	I	I	In combination with $\overline{HALT}$, this signal resets the processor. If the $\overline{RESET}$ instruction is executed, this signal functions as a reset signal for external devices.
$\overline{HALT}$	I/O	I	I	As an input, this signal halts the processor when the current bus cycle ends. Also, the signal acts as an output when a double bus error exception occurs.
E	O	O Note 1	I	This signal is a common enable signal for all 6800-type peripheral devices. This signal is 1/10th the frequency of the system clock.
VPA	I	I	I	This signal is used to indicate that the addressed device is a 6800-family peripheral device.
VMA	O	O Note 1	I	This signal indicates that a valid address for a 6800 peripheral device is loaded on the address bus, and that the processor is synchronous with the E signal.

2.2 Pin Names and Functions (2/2)

NOR : Normal mode, EMU : Emulation mode, O.D : Open drain output,
O : Output, I: Input, I/O : Input/output

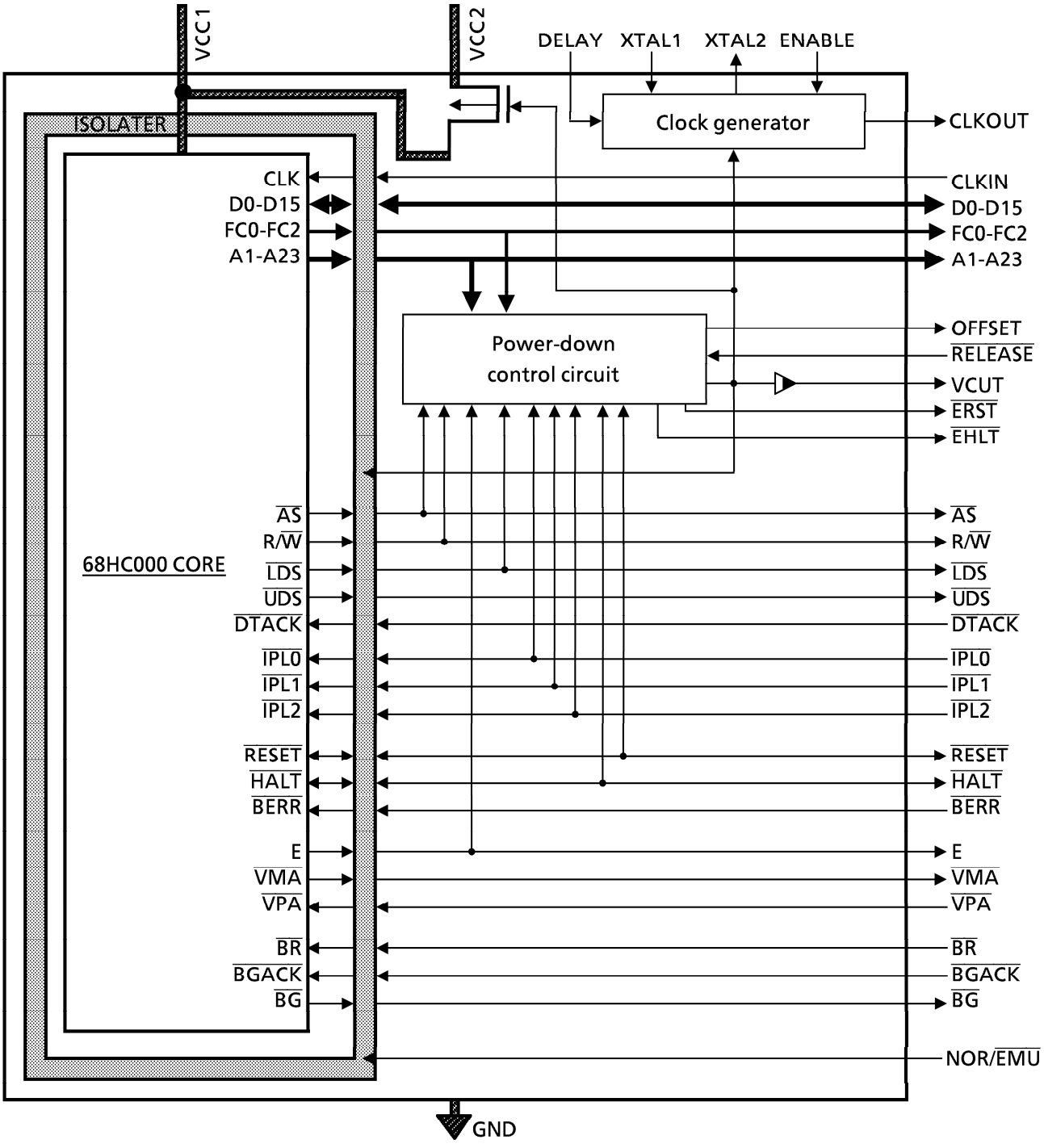
Signal name	Pin status			Function
	NOR	PDOWN	EMU	
Vcc1	–	–	–	As the power to the CPU core is output internally, Vcc1 is low in power-down mode. (Leave this pin open when in use.)
Vcc2	–	–	–	Supplies power to the power-down and clock generator circuits.
VCUT Note 3	O	O	O	This signal switches the CPU core power supply (Vcc1) on and off. The signal goes low at system reset or when triggered by an interrupt (IPLn) in the power-down state. Accessing the power-down control register sets the signal to Hi-Z level (open drain pin).
OFFSET	O	O	O	Releasing power-down using an interrupt (IPLn) sets this signal to high and resets the CPU core. Accordingly, by decoding this signal and the address lines, the reset vectors at power-down can be set to any address. If power-down is released by a system reset, this signal does not go high.
RELEASE	I	I	I	Input signal used to clear OFFSET (to low).
XTAL1 XTAL2	I	I	I	These are the crystal (or SERAROC) oscillator connection pins. The pins are connected to an oscillator with twice the frequency of the system clock (CLKOUT).
	O	O	O	
CLKOUT	O	O Note 3	O	Clock output pin. This signal is half the frequency of the oscillator connected to XTAL1/XTAL2.
CLKIN	I	I	I	Clock input pin. (This pin is normally connected to the CLKOUT pin.)
ENABLE	I	I	I	Setting this signal to high outputs the clock signal from CLKOUT. Oscillation stops when this signal goes low in power-down mode.
DELAY	I	I	I	When a crystal oscillator is connected, it is necessary to suppress CLKOUT until the oscillation stabilizes. The warm-up time until stabilization depends on the level of the DELAY pin. When the DELAY pin is high, divide the signal input to XTAL by 2^{17} to determine the warm-up time; when low, divide the signal input to XTAL by 2^{14}.
ERST / EHLT	I/O	I	I/O	This signal is connected to the ICE (note 4) $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ inputs (in emulation mode). Note 6
NOR / EMU	I	I	I	Switch signals between normal and emulation mode. When low, the CPU core is electrically isolated and operated according to the instructions from other CPUs (such as ICE (note 4)). Note 6

Notes :

1. Goes high at power-down.
2. When the ENABLE pin is low, goes high.
3. Open drain pin.
4. ICE (in-circuit emulator)
5. When power-down is released by $\overline{\text{IPL0}}$ - $\overline{2}$ (while $\overline{\text{ERST}}$ and $\overline{\text{EHLT}}$ are asserted), undefined data are output .
6. Pull up or down the input level by changing the resistance.

Chapter 3 Operational Description

3.1 Block Diagram



Note : Use with Vcc1 open and with power supplied to Vcc2.
Directly connect CLKIN and CLKOUT to external pins.

Figure 3.1 Block Diagram

3.2 Outline of Operation

As shown in Figure 3.1, TMP68HC003 basically consists of the processor block (henceforth, the "CPU core"), the power-down block, (henceforth, the "PDOWN block"), and the clock generator block (henceforth, the "CGC block").

3.2.1 Processor Block

The CPU block incorporates the Toshiba TMP68HC000 and utilizes all the functions the TMP68HC000 offers.

3.2.2 PDOWN Block

The PDOWN block controls the power supply to the CPU core. The Accessing the power-down control register (PDCR) in the PDOWN block enters power-down mode . In power-down mode, a VCUT signal is output from the PDOWN block (high: open drain). This signal turns off an internal transistor and halts power supply (Vcc1) to the CPU block. (Halting the power destroys the contents of all the registers in the CPU. Therefore, CPU register contents that need to be saved must be saved to external memory before accessing PDCR.) (See 3.3, Saving Registers at Power-Down and Restoring After Power-Down Release.)

In power-down mode, control signals ($\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$, R/$\overline{W}$, $\overline{VMA}$) go high, the data bus and address bus are at high impedance, and FC0 to 2 and E go high.

There are two methods of releasing power-down mode: release by system reset, or release via the interrupt pins. Either method immediately releases power-down mode and causes VCUT to go low (Vcc1 is supplied to the CPU core).

When power-down mode is released by an interrupt, the OFFSET signal (high) is output from the PDOWN block. The OFFSET signal is used to distinguish whether the source of the power-down mode release (the CPU core reset) was the system reset or the interrupt pins so that the vector fetch address after power-down mode release can be modified accordingly. For details on releasing power-down mode, see 3.3.4, Power-Down Mode Release.

3.2.3 CGC Block

All the clocks needed by the system can be generated simply by externally connecting a crystal (or CERAROC) oscillator to the CGC block. The CGC has an ENABLE pin to control the oscillator. In combination with the PDOWN function, this pin can be set to stop the oscillator in PDOWN mode. This substantially reduces the power consumption. A DELAY pin and warm-up circuit are built into the CGC block to control the power supply to the clocks while oscillation stabilizes.

3.3 Operational Description of PDOWN Block

The power-down function stops power supply to the TMP68HC000 core (hereafter, "CPU core") via software.

3.3.1 Power-Down Mode

Accessing the power-down control register (PDCR) by program enters power-down mode. Immediately after this mode is entered, the power supply to the CPU core is stopped. Therefore, any CPU register contents that need to be saved must be saved to external memory before accessing PDCR.

3.3.2 Accessing Power-Down Control Register (PDCR)

This register is used for reducing power. Access is based on :

- Access instruction TAS
- Access address $FF
- Processor state/supervisor data (eg, TAS, $FF)

3.3.3 Saving Registers at Power-Down and Restoring After Power-Down Release

To enter power-down mode for applications not requiring the preservation of CPU registers, execute the TAS instruction (TAS $FF).

However, to enter power-down mode for applications requiring the saving of CPU registers, the simple measures shown in Figure 3.3 must be taken. In this example, power-down mode is entered after executing program A where the TRAP instruction is used instead of a TAS instruction. Executing the TRAP instruction saves the start address of program B (to be executed next) on the stack along with the current status flag. Next, the TRAP processing routine stores all the registers in external RAM. Then, the TAS instruction is executed to enter power-down mode. (Figure 3.4 shows an outline of power-down mode processing.)

3.3.4 Power-Down Mode Release

There are two types of power-down mode release as shown in Figure 3.5. The first example shows release by an external reset; the second by interrupt input.

3.3.4.1 Releasing Power-Down Mode by External Reset

Setting the external reset signals ($\overline{\text{RESET}}$ and $\overline{\text{HALT}}$) to low releases power-down mode. To assure a correct reset of the CPU core (which supplies voltage to Vcc1), when entering power-down mode in CG operating mode, assert $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ continuously for at least 50 clocks after Vcc1 reaches the specified voltage. When entering power-down mode in CG non-operating mode, assert $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ continuously for at least 50 clocks after Vcc1 reaches the specified voltage and the CG clock has stabilized. (See figures 3.1-A and 3.1-B)

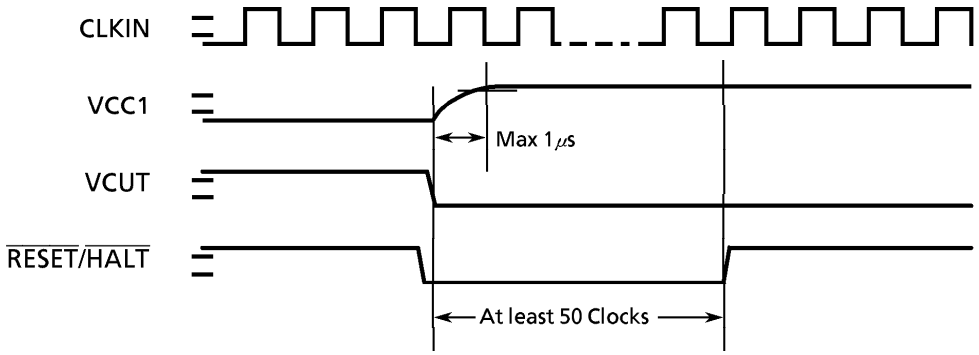
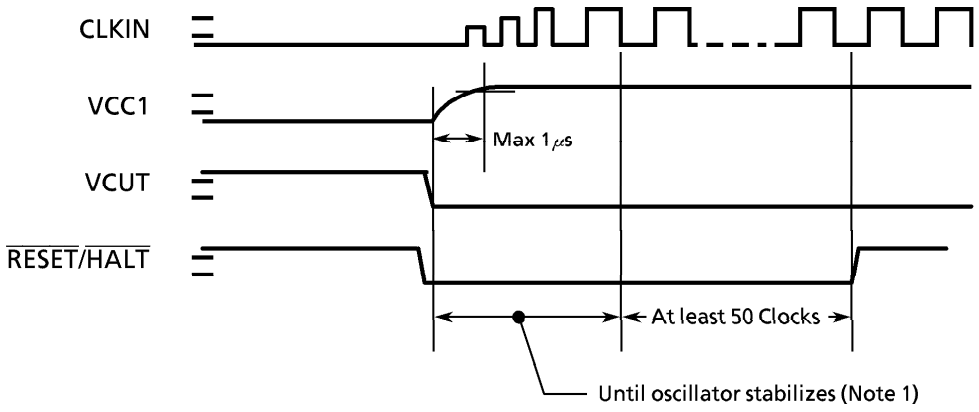


Figure 3.1-A Releasing Power-Down Mode by External $\overline{\text{RESET}}$ / $\overline{\text{HALT}}$ (CG Operating)



Note 1 : Depends on the characteristics of the oscillators used.

Figure 3.1-B Releasing Power-Down Mode by External $\overline{\text{RESET}}$ / $\overline{\text{HALT}}$ (CG Stopped)

3.3.4.2 Power-Down Release by Interrupt

Setting any interrupt pin ($\overline{IPL0}$ - $\overline{2}$) to low releases power-down mode and resets only the TMP68HC003 internal CPU core with no effect on the power supply to the CPU core or the rest of the system. ($\overline{ERST}$ and $\overline{EHLT}$ are asserted, the internal core is reset, and the status register is initialized.) Continuously asserting the interrupt pin after the release causes the interrupt processing routine to be executed. Execution of the interrupt processing routine only applies, however, to cases where the interrupt level on $\overline{IPL0}$ - $\overline{2}$ is higher than the CPU core status register (SR) interrupt mask. (But because the interrupt level is 7 after release, only non-maskable interrupts are received. To induce acceptance of other interrupts as well, it is necessary to update the interrupt mask level in the status register.) Also, when only internal CPU core reset is asserted ($\overline{ERST}$ and $\overline{EHLT}$ are asserted), all control signals such as $\overline{AS}$, $\overline{LDS}$ / $\overline{UDS}$, R/$\overline{W}$, $\overline{VMA}$, and FC0 to FC2 are negated. Undefined data are output to the data bus (D0 to D15).

As the OFFSET pin goes high in this mode, it is possible to set the reset vector (program counter and stack) to any address by decoding the specified address lines using external circuits. (See figures 3.2-A and 3.2-B)

At a reset by power-down mode release, the $\overline{ERST}$ and $\overline{EHLT}$ pins go low, while the $\overline{RESET}$ and $\overline{HALT}$ pins for system reset are not affected.

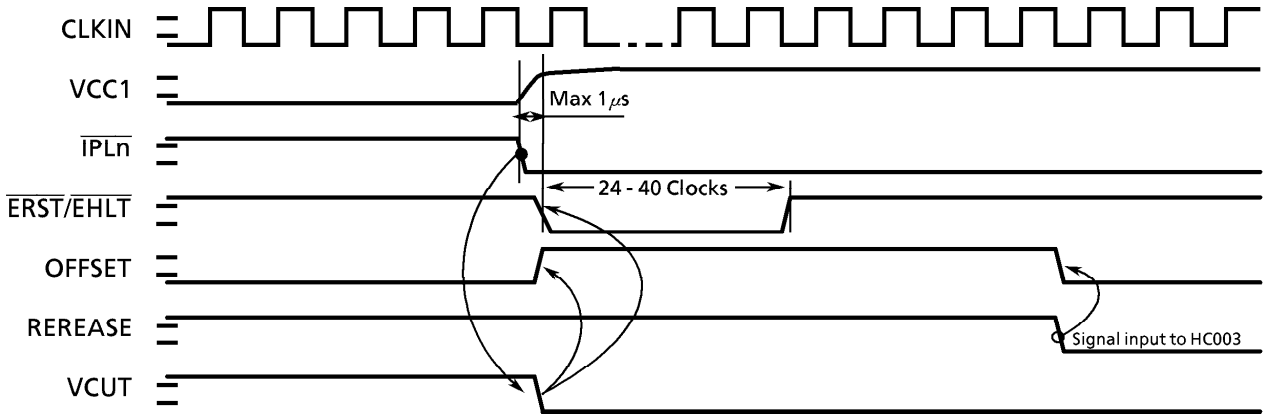


Figure 3.2-A Power-Down Mode Release by Interrupt Pin ($\overline{IPL1}$ - $\overline{2}$) (CG Operating)

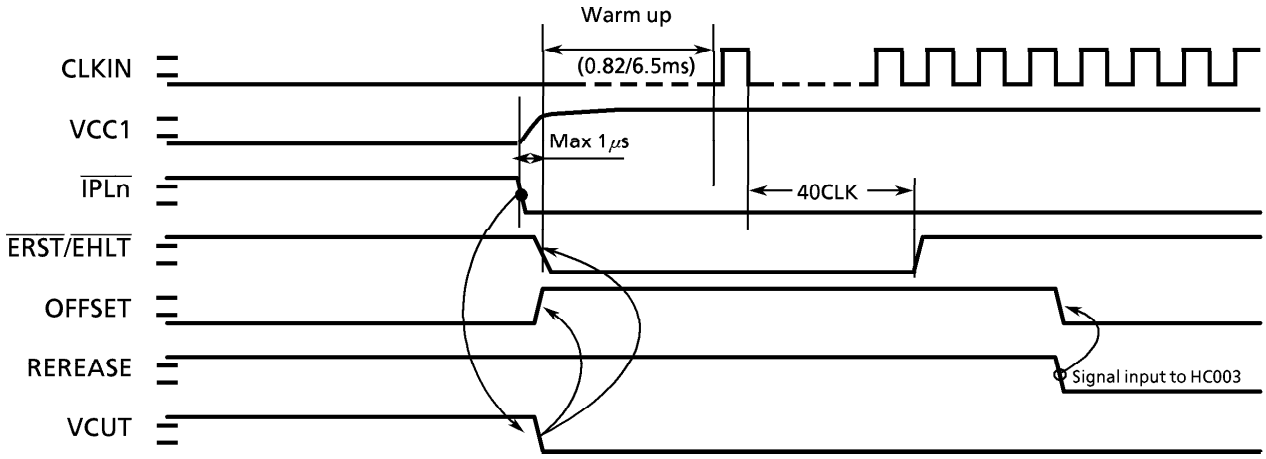


Figure 3.2-B Power-Down Mode Release by Interrupt Pin ($\overline{IPL1}$ - $\overline{2}$) (CG Stopped)

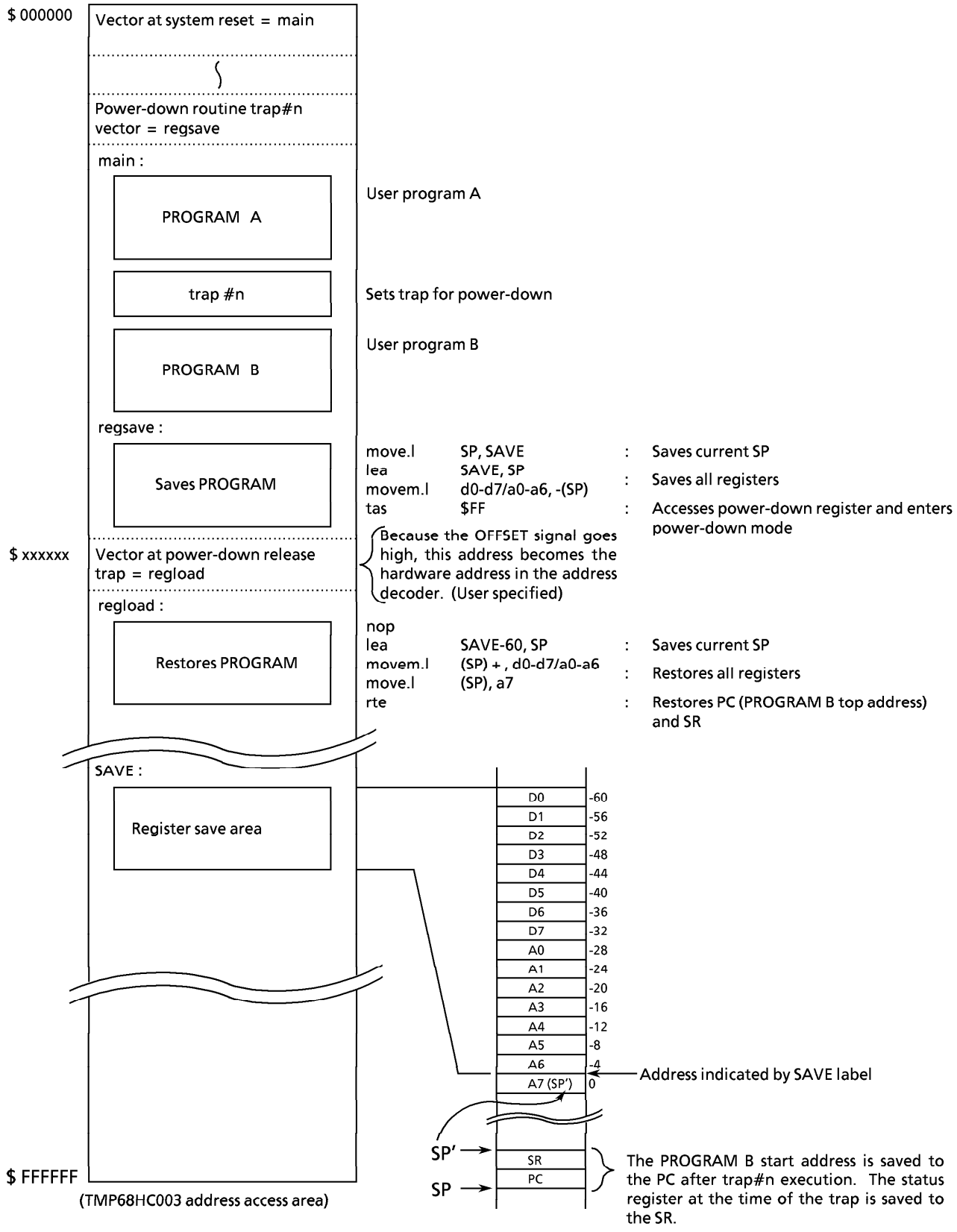
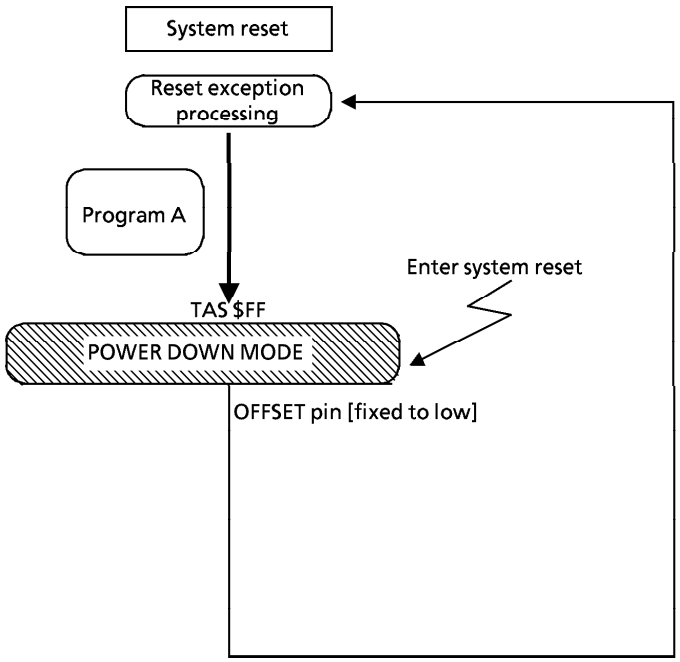


Figure 3.3 Saving CPU Registers at Power-Down and Restoring at Power-Down Release

- Where register saving/restoring not required



- Where register saving/restoring required (by software)

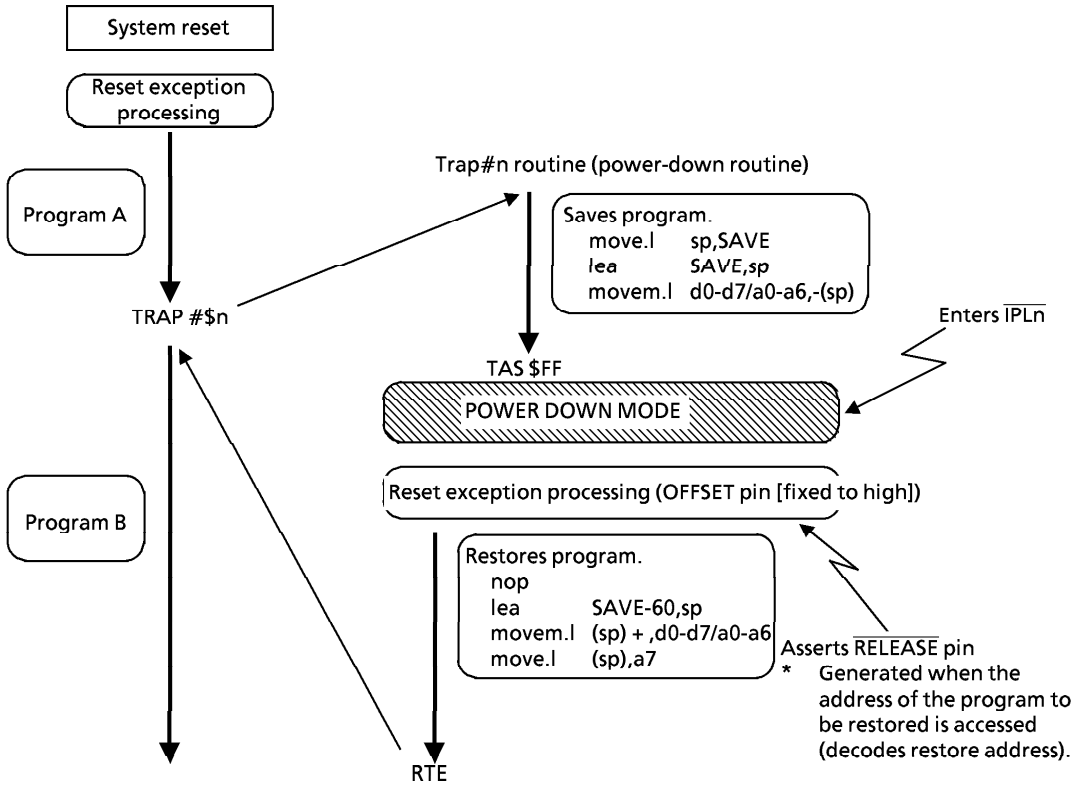


Figure 3.4 Outline of Power-Down Operation

3.4 Clock Generator (CGC)

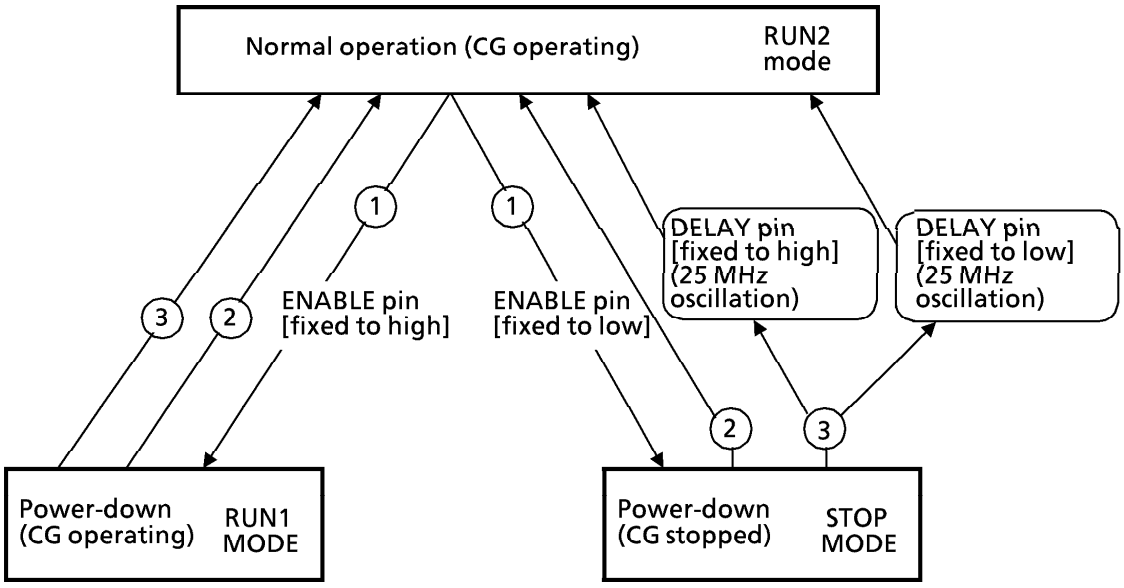
Connecting a crystal (or CERAROC) oscillator to XTAL1 and XTAL2 outputs half the oscillator frequency to the clock output pin (CLKOUT). Normally, this output is connected to the clock input pin (CLKIN). The CGC has an ENABLE pin for switching operating modes (RUN1 mode, RUN2 mode, STOP mode) and a DELAY pin for selecting the warm-up time.

The following shows the operating modes.

ENABLE	VCUT	Mode
1	X	RUN1 mode (clocks are continuously output from CGC in power-down mode)
0	0	RUN2 mode (normal operation)
0	1	STOP mode (power-down mode with clock stopped)

When switching from STOP to RUN2 mode by an interrupt, the CGC oscillation must stabilize before the clock is supplied. The CGC therefore incorporates a warm-up circuit for this purpose. The warm-up time can be set by the DELAY pin (as oscillation stops in power-down mode). The warm-up time is calculated by dividing the XTAL1 input by 2^{17} when DELAY is high, or 2^{14} when DELAY is low. (When using a 25MHz-crystal oscillator, warm-up times are 0.65ms max. with DELAY = 0 and 5.2ms max. with DELAY = 1.)

When using a system reset to switch to RUN2 mode, the warm-up circuit does not operate. In this case, use a sufficiently long reset signal (see figures 3.1-A and 3.1-B) to create a warm-up time. (See figure 3.5 Outline of Status Switching)



(1) POWER DOWN MODE IN — Access instruction: TAS $FF; Processor state: supervisor

(2) POWER DOWN MODE OUT — System reset input (OFFSET output [low])

(3) POWER DOWN MODE OUT — $\overline{\text{IPLn}}$ input (OFFSET output [high])

Figure 3.5 Outline of Status Switching

Chapter 4 TMP68HC003 Emulation Mode

4.1 Outline

TMP68HC003 supports emulation mode, in which the internal 68HC000 core is disconnected from the bus and power-down is externally implemented using an external 68HC000.

Switching from normal to emulation mode sets the TMP68HC003 NOR / $\overline{EMU}$ pin to low-level input. As a result, circuits other than the 68HC000 core in TMP68HC003 operate according to the address signals and control signals from the external 68HC000.

In TMP68HC003 emulation mode, signals are the same as those of the external 68HC000 signals except that the direction (input/output) of the following signals change. However, connect TMP68HC003 emulation mode reset pins $\overline{ERST}$ and $\overline{EHLT}$ to the external 68HC000 $\overline{RESET}$ and $\overline{HALT}$ pins.

Pin name	Normal mode	Emulation mode
A1~A23	Output	Input
FC2~FC0	Output	Input
D0~D15	Input / output	Hi - Z
E	Output	Input
BG	Output	Input
R/W	Output	Input
LDS	Output	Input
AS	Output	Input
VMA	Output	Hi - Z
VPA	Output	Hi - Z

Note : The direction of the other signals does not change in normal mode or emulation mode.

4.2 External 68HC000 Connection in Emulation Mode

To set emulation mode using a user-produced target board and enable operation using the external 68HC000, design a board as shown in Figure 4.1 and assert the necessary signals.

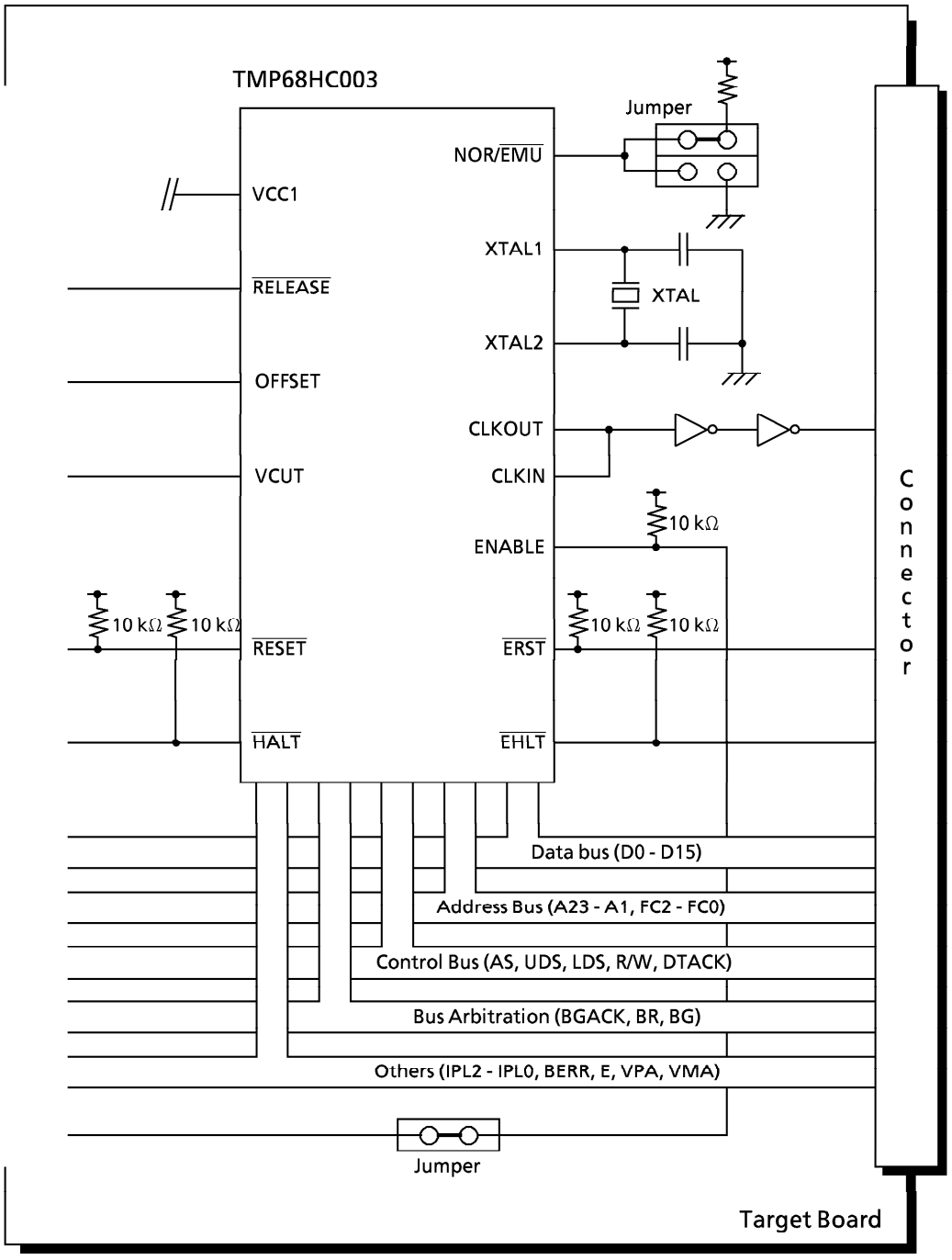

TMP68HC003
Jumper
NOR/EMU
VCC1
XTAL1
RELEASE
XTAL
XTAL2
OFFSET
CLKOUT
VCUT
CLKIN
10 kΩ
ENABLE
10 kΩ
10 kΩ
10 kΩ
10 kΩ
RESET
ERST
HALT
EHLT
Connector
Data bus (D0 - D15)
Address Bus (A23 - A1, FC2 - FC0)
Control Bus (AS, UDS, LDS, R/W, DTACK)
Bus Arbitration (BGACK, BR, BG)
Others (IPL2 - IPL0, BERR, E, VPA, VMA)
Jumper
Target Board

Figure 4.1

It is possible to connect and operate the 68HC000 externally if the 68HC000 is connected as shown in figure 4.2.

"*1" and "*2" in figure 4.2 differ from Figure 1.1. "*1" sets the NOR / $\overline{EMU}$ pin to low input to switch TMP68HC003 from normal to emulation mode. TMP68HC003 has a function to stop the clock generator when TMP68HC003 is in power-down mode. (When the ENABLE pin is set to low-level input, the clock generator stops oscillating in power-down mode.) However, when TMP68HC003 is set to power-down mode, no clock is input from TMP68HC003 to the external 68HC000. This can cause 68HC000 to malfunction. "*2" ensures clock output during emulation mode to avoid external 68HC000 malfunction caused by no clock input.

When the external 68HC000 $\overline{RESET}$ and $\overline{HALT}$ pins are asserted (at $\overline{RESET}$ instruction execution and at $\overline{HALT}$ assertion at a double bus error), connecting the TMP68HC003 $\overline{ERST}$ and $\overline{EHLT}$ pins as shown in figure 1.2 enables output of signals from the external 68HC000 without change and control of the external 68HC000 by signals from user target boards. This is because the TMP68HC003 $\overline{RESET}$ and $\overline{HALT}$ pins and $\overline{ERST}$ and $\overline{EHLT}$ pins become transfer gates (bi-directional I/O), except at power-down release.

4.3 Cautions on Software for Emulation Mode

Executing power-down in emulation mode requires some simple programming measures.

When TMP68HC003 enters power-down mode, executing the TAS $FF instruction in supervisor mode disconnect the internal 68HC000 from the bus and shuts off the power supply to the 68HC000 core. In emulation mode, instead of the TMP68HC003 internal core, the external 68HC000 controls the 68HC000 core. However, because there is no circuit to shut off power to the external 68HC000, and because the external 68HC000 cannot recognize the power-down execution instruction, directly issuing instructions after TAS $FF can cause the program to continue out of control.

Therefore, to use the power-down function in emulation mode, immediately after the TAS $FF instruction, stop external 68HC000 operation using the STOP#$2700 instruction. (See figure 4.3.)

Power-down mode can be released either by a system reset by simultaneous assertion of the TMP68HC003 $\overline{RESET}$ and $\overline{HALT}$ pins, or by by asserting one of interrupt pins $\overline{IPL0}$ to $\overline{IPL2}$. As the $\overline{ERST}$ signal and $\overline{ERST}$ pin are asserted whichever method is used, a system reset is always asserted for the external 68HC000. Accordingly, the external 68HC000 executes the STOP instruction, which allows the program to be restarted if the program stops.

4.4 Cautions on Electrical Characteristics in Emulation Mode

When TMP68HC003 enters power-down mode from normal mode, power consumption is greatly reduced. In emulation mode, however, the clock generator cannot be stopped, and power consumption cannot be emulated because the pins that operate in power-down mode (such as VCUT, OFFSET, $\overline{RELEASE}$, $\overline{ERST}$, and $\overline{EHLT}$) are controlled using signals from the external 68HC000. In other words, TMP68HC003 emulation mode is effective only for the software and hardware emulation described above and cannot be used to determine electrical characteristics.

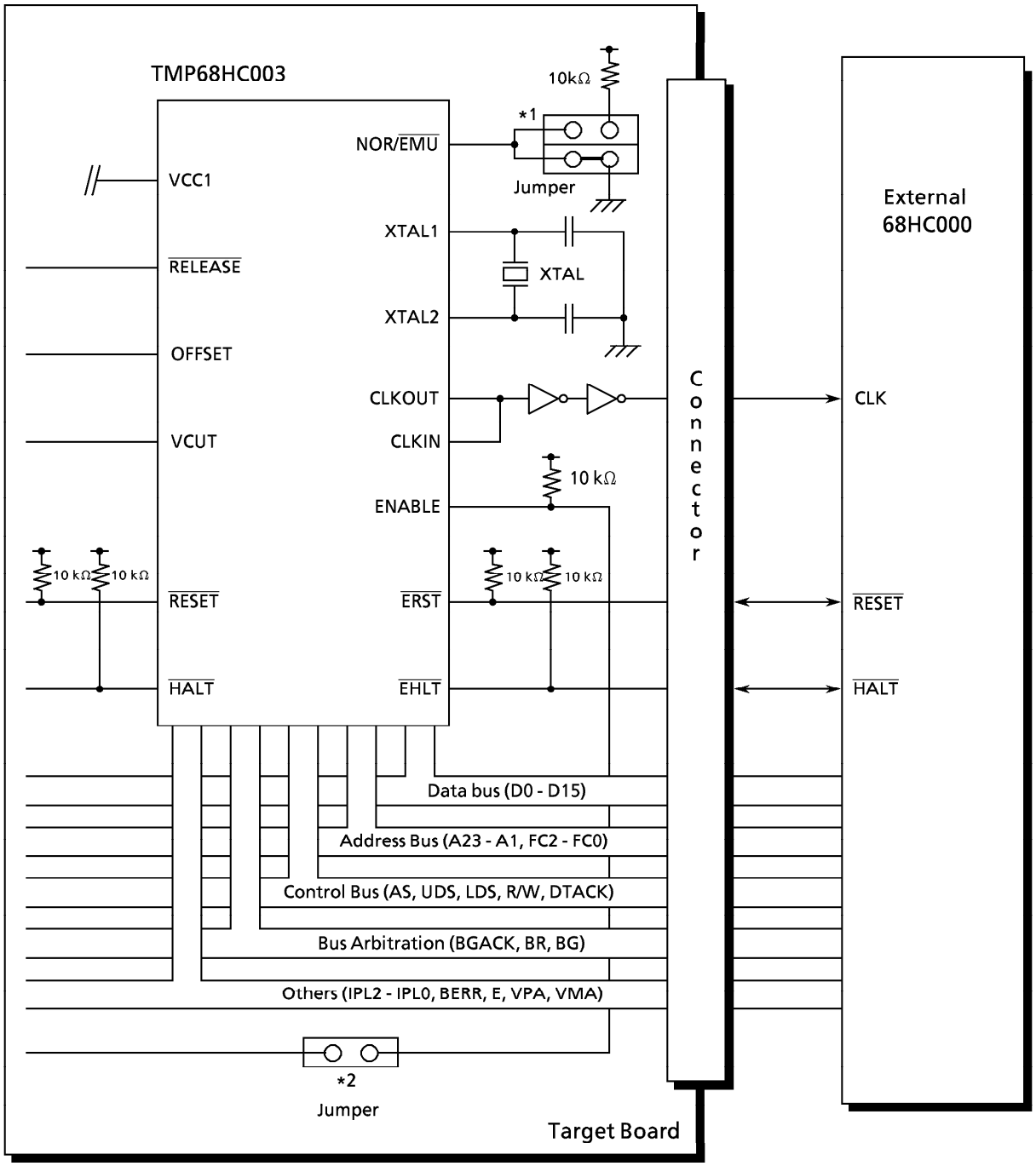

TMP68HC003
10kΩ
*1
NOR/EMU
Jumper
VCC1
XTAL1
RELEASE
XTAL
XTAL2
OFFSET
CLKOUT
CLK
VCUT
CLKIN
10 kΩ
ENABLE
10 kΩ
10 kΩ
10 kΩ
10 kΩ
RESET
ERST
RESET
HALT
EHLT
HALT
Connector
External
68HC000
Data bus (D0 - D15)
Address Bus (A23 - A1, FC2 - FC0)
Control Bus (AS, UDS, LDS, R/W, DTACK)
Bus Arbitration (BGACK, BR, BG)
Others (IPL2 - IPL0, BERR, E, VPA, VMA)
*2
Jumper
Target Board

Figure 4.2

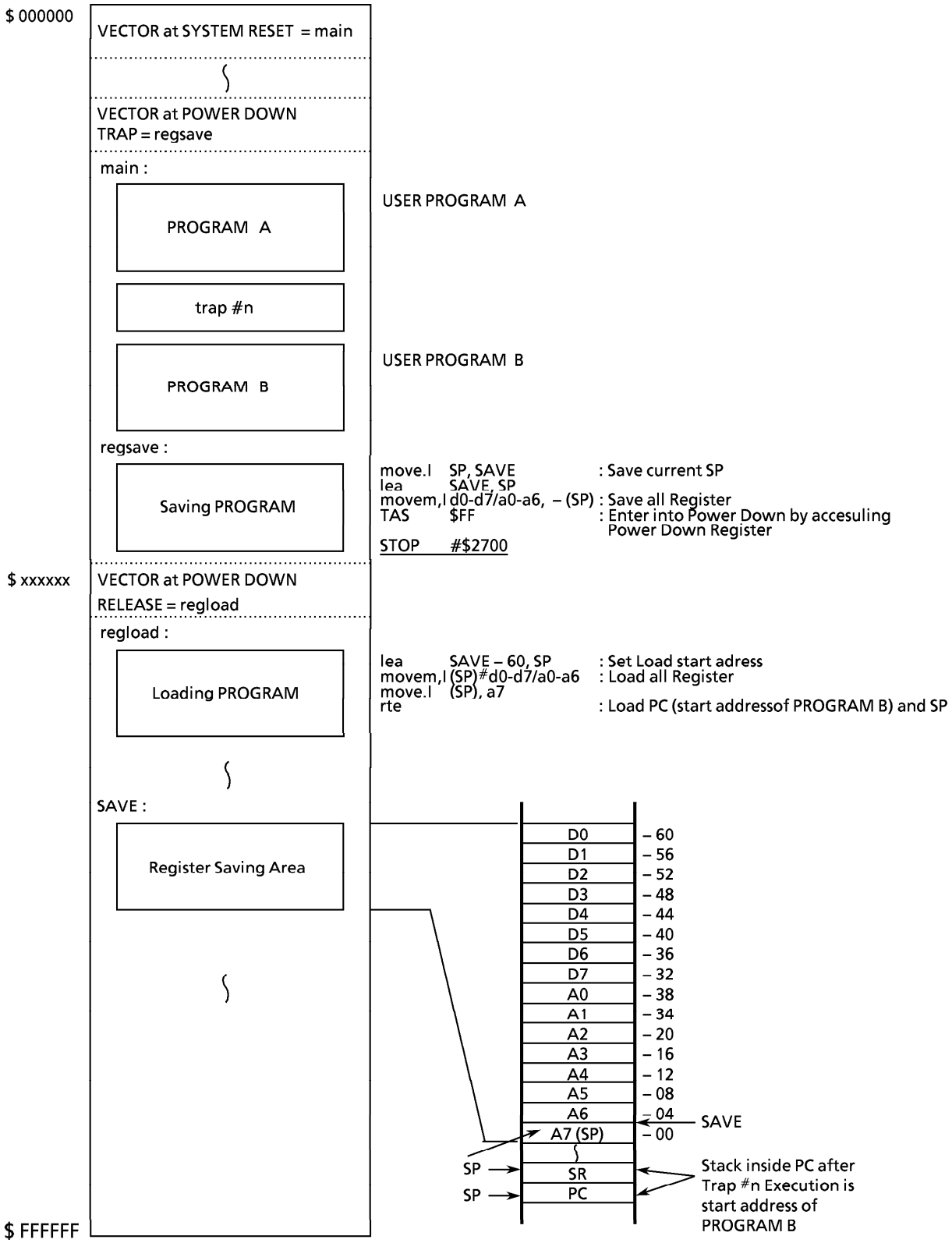

$ 000000
VECTOR at SYSTEM RESET = main
VECTOR at POWER DOWN
TRAP = regsave
main :
PROGRAM A
USER PROGRAM A
trap #n
PROGRAM B
USER PROGRAM B
regsave :
Saving PROGRAM
move.l SP, SAVE : Save current SP
lea SAVE, SP
movem,l d0-d7/a0-a6, – (SP) : Save all Register
TAS $FF : Enter into Power Down by accesuling Power Down Register
STOP #$2700
$ xxxxxx
VECTOR at POWER DOWN
RELEASE = regload
regload :
Loading PROGRAM
lea SAVE – 60, SP : Set Load start adress
movem,l (SP)#d0-d7/a0-a6 : Load all Register
move.l (SP), a7
rte : Load PC (start addressof PROGRAM B) and SP
SAVE :
Register Saving Area
D0 – 60
D1 – 56
D2 – 52
D3 – 48
D4 – 44
D5 – 40
D6 – 36
D7 – 32
A0 – 38
A1 – 34
A2 – 20
A3 – 16
A4 – 12
A5 – 08
A6 – 04
A7 (SP) – 00
SAVE
SP
SR
SP
PC
Stack inside PC after Trap #n Execution is start address of PROGRAM B
$ FFFFFF

Figure 4.3

Chapter 5 Electrical Characteristics

This section describes the electrical characteristics and timings of TMP68HC003.

5.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
		TMP68HC003	
Power supply voltage	Vcc	– 0.3 to + 6.5	V
Input voltage	Vin	– 0.3 to + 6.5	V
Operating temperature	Ta	– 20 to + 85	°C
Storage temperature	Tstg	– 55 to + 150	°C

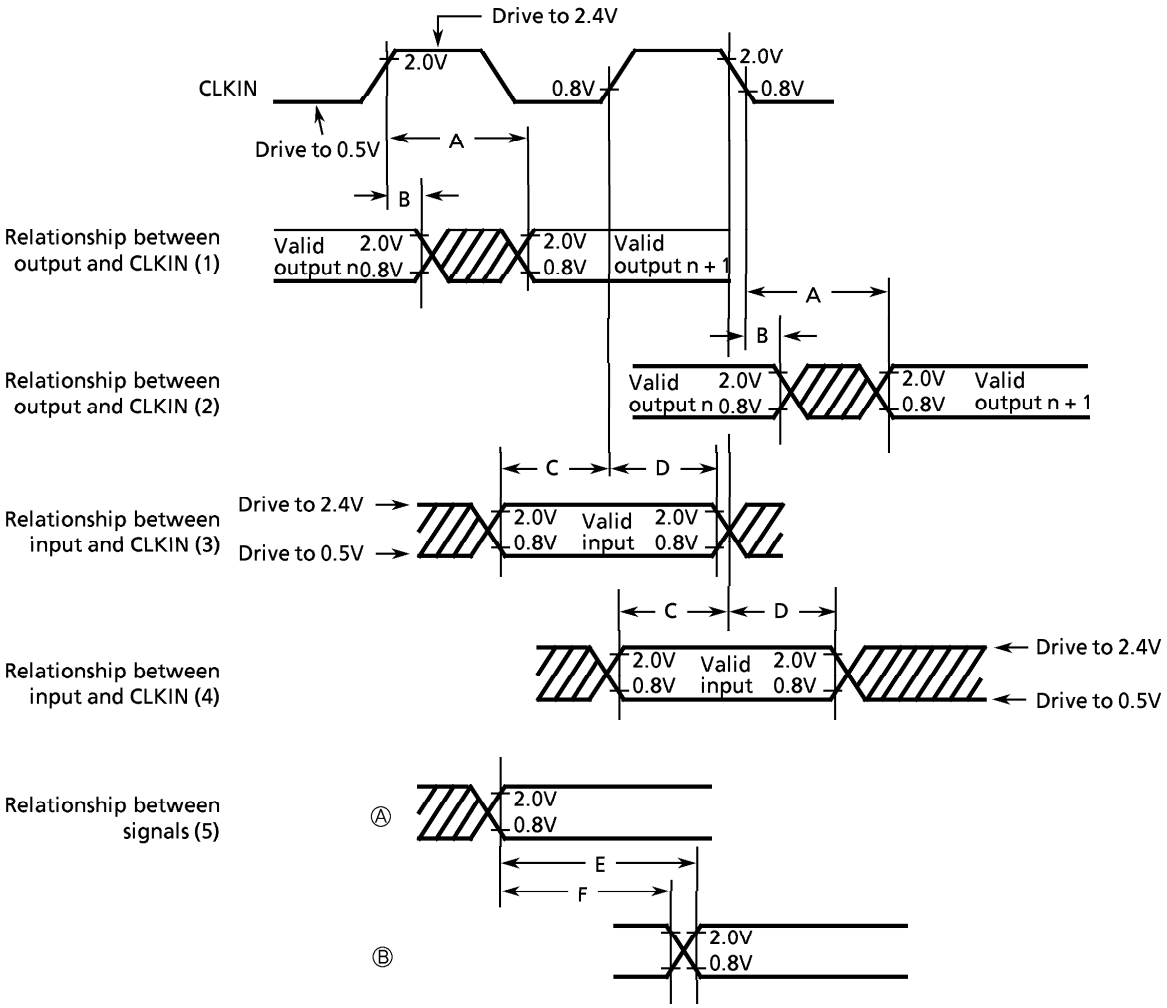
While this device includes input protection circuits against high-voltage static electricity or damage from electric fields, avoid using a voltage higher than the maximum rating. Connect input pins not in use to GND or VCC.

5.2 DC Characteristics

(GND = 0V, Ta = – 20 to 85°C)

Parameter	Symbol	VCC = 5.0 V ± 5 %		VCC = 3.0 V ± 10 %		Unit
		Min	Max	Min	Max	
High-level input voltage	V_{IH}	2.2	V_{CC}	2.2	V_{CC}	V
Low-level input voltage	V_{IL}	GND-0.3	0.8	GND-0.3	0.6	V
Input leakage current (5.25 V) $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$ to $\overline{IPL2}$, $\overline{VPA}$, NOR/$\overline{EMU}$, DELAY,	I_{IN}	–	2.5	–	2.5	μA
ENABLE, CLKIN, RELEASE $\overline{HALT}$, $\overline{RESET}$, $\overline{EHLT}$, $\overline{ERST}$		–	20	–	20	
Tri-state (off state) input current (2.4 V/0.4 V) $\overline{AS}$, A1 to A23, D0 to D15,	I_{TSI}	–	20	–	20	μA
FC0 to FC2, $\overline{LDS}$, R/$\overline{W}$,		–	20	–	20	
$\overline{UDS}$, $\overline{VMA}$		–	20	–	20	
VCUT	I_{CUT}	–	2.5	–	2.5	μA
High-level output voltage (IOH = – 400 μA) E, $\overline{AS}$, A1 to A23, $\overline{BG}$, CLKOUT,	V_{OH}	V_{CC}-0.75	–	V_{CC}-0.75	–	V
D0 to D15, OFFSET,		V_{CC}-0.75	–	V_{CC}-0.75	–	
FC0 to FC2, $\overline{LDS}$, R/$\overline{W}$,		V_{CC}-0.75	–	V_{CC}-0.75	–	
$\overline{UDS}$, $\overline{VMA}$		V_{CC}-0.75	–	V_{CC}-0.75	–	
$\overline{EHLT}$, $\overline{ERST}$*		V_{CC}-0.75	–	V_{CC}-0.75	–	
		V_{IH}-0.3	–	V_{IH}-0.3	–	
Low-level output voltage $\overline{EHLT}$, $\overline{ERST}$*	V_{OL}	–	V_{IL} + 0.3	–	V_{IL} + 0.3	V
$\overline{HALT}$, OFFSET,		–	(IOL = 1.0 mA) 0.5	–	(IOL = 1.0 mA) 0.5	
A1 to A23, $\overline{BG}$, FC0 to FC2		–	(IOL = 1.6 mA) 0.5	–	(IOL = 1.0 mA) 0.5	
$\overline{RESET}$		–	(IOL = 3.2 mA) 0.5	–	(IOL = 2.0 mA) 0.5	
E, AS, D0 to D15, VCUT		–	(IOL = 5.3 mA) 0.5	–	(IOL = 2.0 mA) 0.5	
$\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$						
CLKOUT		–	(IOL = 1.6mA) 0.5	–	(IOL = 1.0mA) 0.5	
Current dissipation			(XTAL 25 MHz)		(XTAL 16.67 MHz)	mA
(RUN1 mode)	I_{CL1}	–	10	–	3	
(RUN2 mode)	I_{CL2}	–	45	–	16	
(STOP mode)	I_{CL3}	–	0.05	–	0.05	
Input capacitance (Vin = 0 V, Ta = 25 °C, Frequency = 1 MHz)	C_{IN}	–	20.0	–	20.0	pF
Load capacitance CLKOUT	C_L	–	50	–	50	pF
HALT		–	70	–	70	
Others		–	100	–	100	

AC Electrical Characteristics



A : Maximum output delay

B : Minimum output hold time

C : Minimum input setup time

D : Minimum input hold time

E : Signal (A) valid - signal (B) valid time

F : Signal (A) valid - signal (B) invalid time

5.3 AC Electrical Characteristics - Read and Write Cycles (1/4)

(GND = 0 V, Ta = – 20 to 85 °C; See figures 5.1 and 5.2)

Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
1	Clock cycle	tCYC	80	250	125	500	ns
2	Clock width low	tCL	35	125	52	250	ns
3	Clock width high	tCH	35	125	52	250	ns
4	Clock fall time	tCf	–	5	–	10	ns
5	Clock rise time	tCr	–	5	–	10	ns
6	Clock low to address valid	tCLAV	–	50	–	80	ns
6A	Clock high to FC valid	tCHFCV	–	45	–	72	ns
7	Clock high to address, data bus high impedance (maximum)	tCHADZ	–	60	–	80	ns
8	Clock high to address, FC invalid (minimum)	tCHAFI	0	–	0	–	ns
9[1]	Clock high to $\overline{AS}$, $\overline{DS}$ low	tCHSL	3	40	3	60	ns
11[2]	Address valid to $\overline{AS}$, $\overline{DS}$ low (read) / Address valid to $\overline{AS}$ low (write)	tAVSL	15	–	20	–	ns
11A[2]	FC valid to $\overline{AS}$, $\overline{DS}$ low (read) / FC valid to $\overline{AS}$ low (write)	tFCVSL	60	–	90	–	ns
12[1]	Clock low to $\overline{AS}$, $\overline{DS}$ high	tCLSH	–	40	–	72	ns
13[2]	$\overline{AS}$, $\overline{DS}$ high to address / FC invalid	tSHAFI	20	–	40	–	ns
14[2]	$\overline{AS}$, $\overline{DS}$ width low (read) / $\overline{AS}$ width low (write)	tSL	160	–	270	–	ns
14A[2]	$\overline{DS}$ width low (write)	tDSL	80	–	140	–	ns
15[2]	$\overline{AS}$, $\overline{DS}$ width high	tSH	65	–	150	–	ns

Clock = CLKIN

5.3 AC Electrical Characteristics - Read and Write Cycles (2/4)

(GND = 0 V, Ta = – 20 to 85 °C; See figures 5.1 and 5.2)

Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
16	Clock high to control bus high impedance	tCHCZ	–	60	–	80	ns
17[2]	$\overline{AS}$, $\overline{DS}$ high to R/$\overline{W}$ high (read)	tSHRH	20	–	40	–	ns
18[1]	Clock high to R/$\overline{W}$ high	tCHRH	0	40	0	62	ns
20[1]	Clock to R/$\overline{W}$ low (write)	tCHRL	0	40	0	62	ns
20A[2,6]	$\overline{AS}$ low to R/$\overline{W}$ valid (write)	tASRV	–	10	–	10	ns
21[2]	Address valid to R/$\overline{W}$ low (write)	tAVRL	0	–	0	–	ns
21A[2]	FC valid to R/$\overline{W}$ low (write)	tFCVRL	30	–	60	–	ns
22[2]	R/$\overline{W}$ low to $\overline{DS}$ low (write)	tRLSL	30	–	80	–	ns
23	Clock low to data out valid (write)	tCLDO	–	50	–	80	ns
25[2]	$\overline{AS}$, $\overline{DS}$ high to data out invalid (write)	tSHDOI	20	–	40	–	ns
26[2]	Data out valid to $\overline{DS}$ low (write)	tDOSL	20	–	30	–	ns
27[5]	Data in to clock low (setup time on read)	tDICL	10	–	15	–	ns
28[2]	$\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high	tSHDAH	0	150	0	240	ns
28A	Clock high to $\overline{DTACK}$ negate	tCHDAH	0	–	0	240	ns

Clock = CLKIN

5.3 AC Electrical Characteristics - Read and Write Cycles (3/4)

(GND = 0 V, Ta = – 20 to 85 °C; See figures 5.1 and 5.2)

Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
29	$\overline{AS}$, $\overline{DS}$ negate to data invalid (hold time on read)	tSHDII	0	–	0	–	ns
29A	$\overline{AS}$, $\overline{DS}$ negate to input data high impedance	tSHDIZ	–	120	–	187	ns
30	$\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ high	tSHBEH	0	–	0	–	ns
31[2,5]	$\overline{DTACK}$ low setup time (input data)	tDALDI	–	50	–	90	ns
32	$\overline{HALT}$ and $\overline{RESET}$ input transition time	tRHr, f	0	200	0	200	ns
33	Clock high to $\overline{BG}$ low	tCHGL	–	40	–	62	ns
34	Clock high to $\overline{BG}$ high	tCHGH	–	40	–	62	ns
35	$\overline{BR}$ low to $\overline{BG}$ low	tBRLGL	1.5	3.5	1.5	3.5	Clk. Per.
36[7]	$\overline{BR}$ high to $\overline{BG}$ high	tBRHGH	1.5	3.5	1.5	3.5	Clk. Per.
37	BGACK low to BG low	tGALGH	1.5	3.5	1.5	3.5	Clk. Per.
37A[8]	$\overline{BGACK}$ low to $\overline{BR}$ high	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	ns
38	$\overline{BG}$ low to control, address, data bus, high impedance ($\overline{AS}$ high)	tGLZ	–	60	–	80	ns
39	$\overline{BG}$ width high	tGH	1.5	–	1.5	–	Clk. Per.
40	Clock low to $\overline{VMA}$ low	tCLVML	–	70	–	70	ns
41	Clock low to E transition time	tCLET	–	35	–	62	ns
42	Output rise / fall time	tEr, f	–	15	–	15	ns

Clock = CLKIN

5.3 AC Electrical Characteristics - Read and Write Cycles (4/4)

(GND = 0 V, Ta = – 20 to 85 °C; See figures 5.1 and 5.2)

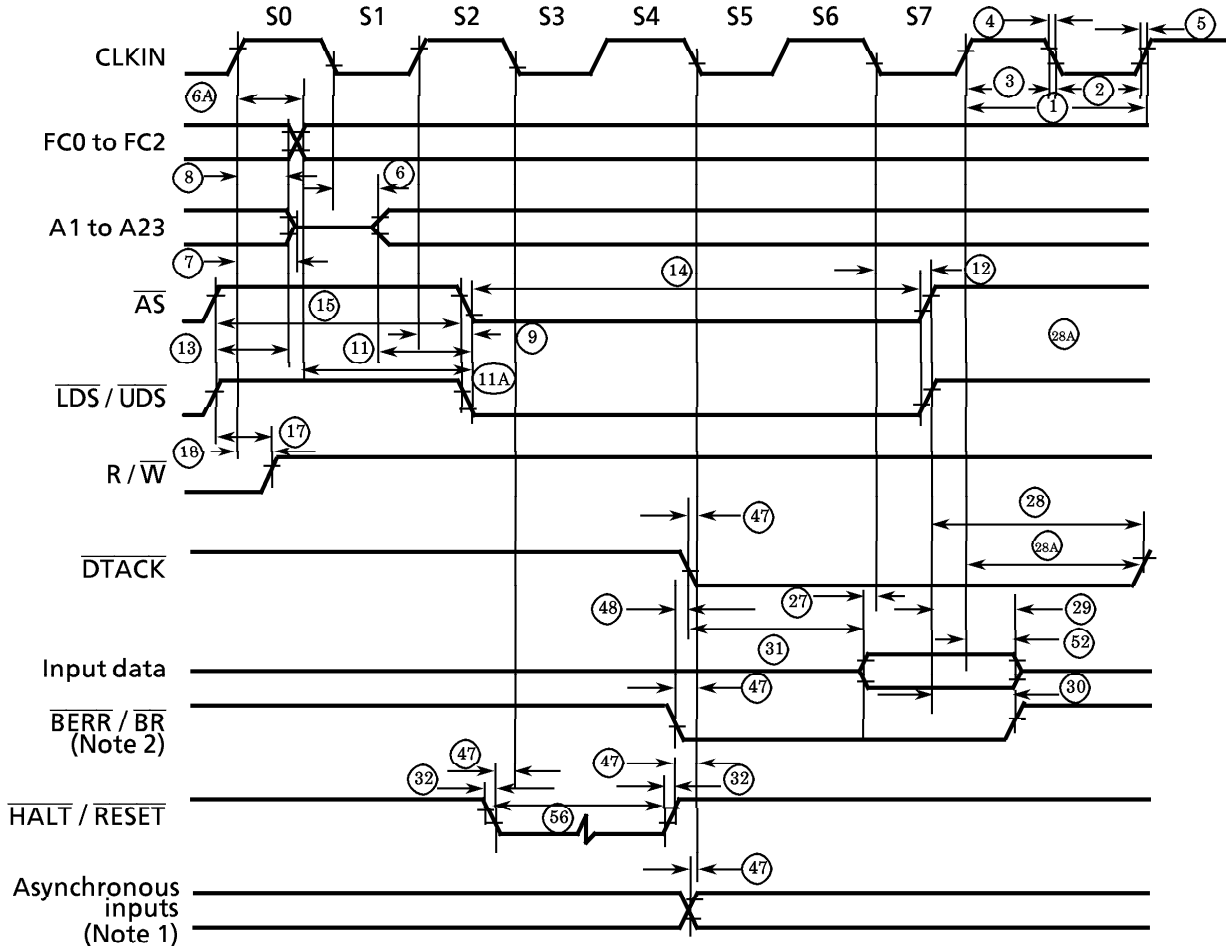
Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
43	$\overline{VMA}$ low to E high	tVMLEH	90	–	200	–	ns
44	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high	tSHVPH	0	70	0	120	ns
45	E low to control, address bus invalid to address hold time	tELCAI	10	–	30	–	ns
46	$\overline{BGACK}$ width low	tGAL	1.5	–	1.5	–	Clk. Per.
47[5]	Asynchronous input setup time	tASI	10	–	15	–	ns
48[2,3]	$\overline{BERR}$ low to $\overline{DTACK}$ low	tBELDAL	20	–	20	–	ns
49[9]	$\overline{AS}$, $\overline{DS}$ (HIGH)から E(LOW)まで	tSHEL	– 45	45	– 70	70	ns
50	E width high	tEH	280	–	450	–	ns
51	E width low	tEL	440	–	700	–	ns
52*	Clock high to input data hold time	tCHDII	0	–	0	–	ns
53	Clock high to data out invalid	tCHDOI	0	–	0	–	ns
54	E low to output data invalid	tELDOI	15	–	30	–	ns
55	R/$\overline{W}$ low to data bus drive	tRLDBD	0	–	30	–	ns
56[4]	$\overline{HALT}$ / $\overline{RESET}$ pulse width	tHRPW	10	–	10	–	Clk. Per.
57	$\overline{BGACK}$ high to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ drive	tGASD	1.5	–	1.5	–	Clk. Per.
57A	$\overline{BGACK}$ high to FC, $\overline{VMA}$ drive	tGAFD	1	–	1	–	Clk. Per.
58[7]	$\overline{BR}$ high to control bus drive	tRHSD	1.5	–	1.5	–	Clk. Per.
58A	$\overline{BR}$ high to FC, $\overline{VMA}$ drive	tRHFD	1	–	1	–	Clk. Per.

Clock = CLKIN

Notes :

1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. Actual value depends on clock cycle.
3. If #47 is satisfied for both $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$, #48 may be 0 ns.
4. At power on, hold reset status for 1 to 100 ms to stabilize MPU circuits. See #56 for the minimum reset times following power on.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{\text{DTACK}}$ low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (#27) requirement for the following cycle.
6. When $\overline{\text{AS}}$ and R/$\overline{\text{W}}$ are equally loaded ($\pm$20%), subtract 3 ns from the tASRV maximum values.
7. The processor will negate $\overline{\text{BG}}$ and begin driving the bus again if external arbitration logic negates $\overline{\text{BR}}$ before asserting $\overline{\text{BGACK}}$.
8. To guarantee proper operation, the minimum value must be met. If the maximum value is exceeded, $\overline{\text{BG}}$ may be reasserted.
9. Strobe ($\overline{\text{AS}}$ and $\overline{\text{xDS}}$) negate and enable (E) signal fall are triggered at the S6 fall. Depending on the loads on their signal lines, one of the signals is triggered first. #49 shows the maximum fluctuation between strobe ($\overline{\text{AS}}$, $\overline{\text{xDS}}$) rise and enable (E) signal fall.

The waveforms below should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Functional descriptions and their related device operation diagrams are given elsewhere.

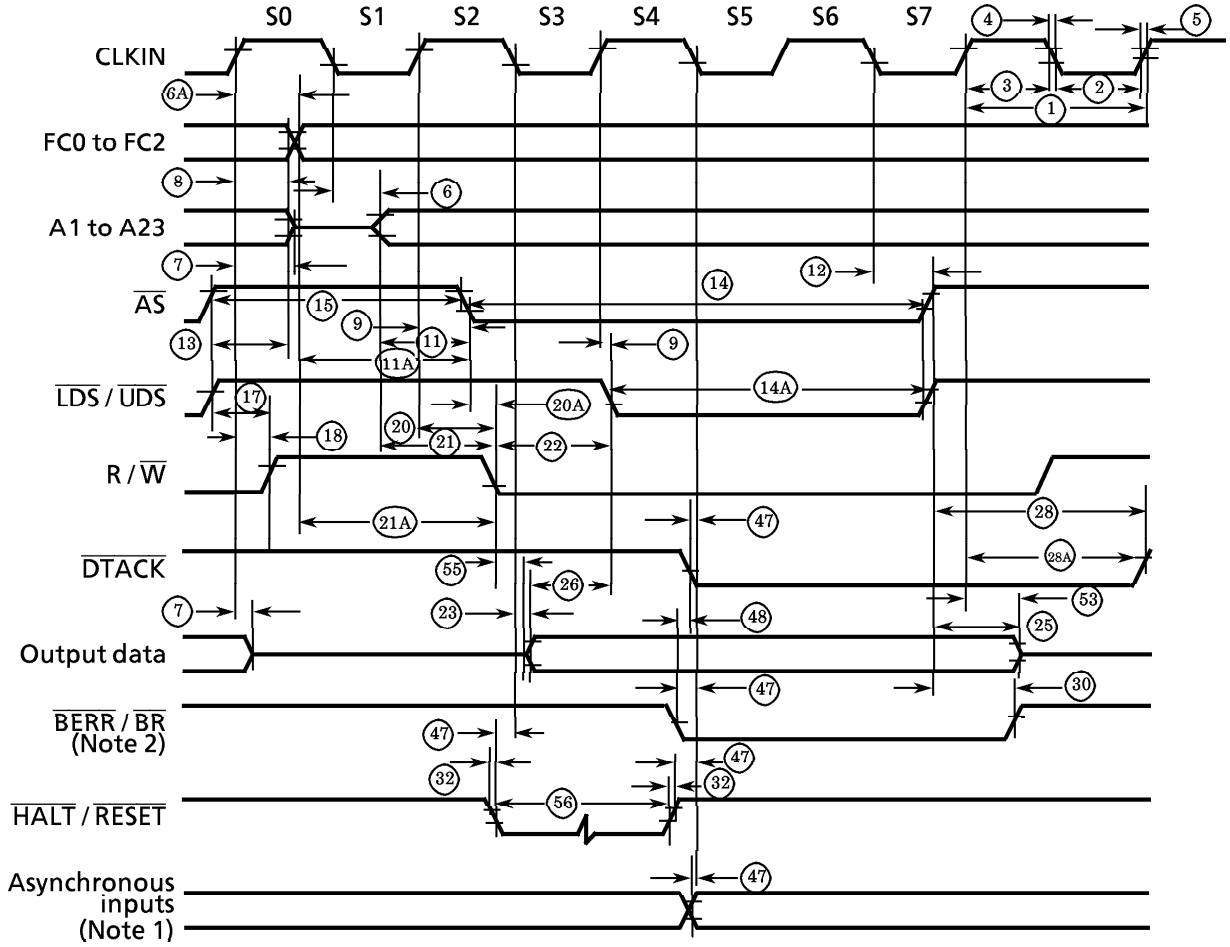


Notes :

1. Asynchronous inputs $\overline{\text{BGACK}}$, $\overline{\text{IPL0}}$ - $\overline{\text{IPL2}}$, and $\overline{\text{VPA}}$ are detected at the clock falling edge.
2. It is necessary to assert at this timing only if $\overline{\text{BR}}$ is recognized at the end of this bus cycle.
3. Unless otherwise specified, timings are measured between a low voltage of 0.8 V and a high voltage of 2.0 V. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 V and 2.0 V.

Figure 5.1 Read Cycle Timing

The waveforms below should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Functional descriptions and their related device operation diagrams are given elsewhere.



Notes :

1. Unless otherwise specified, timings are measured between a low voltage of 0.8 V and a high voltage of 2.0 V. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/$\overline{W}$ may become valid after $\overline{AS}$ even though both are asserted at the rising edge of S2 (#20A).

Figure 5.2 Write Cycle Timing

5.4 AC Electrical Characteristics - Between TMP68HC003 and 6800 Peripheral Devices

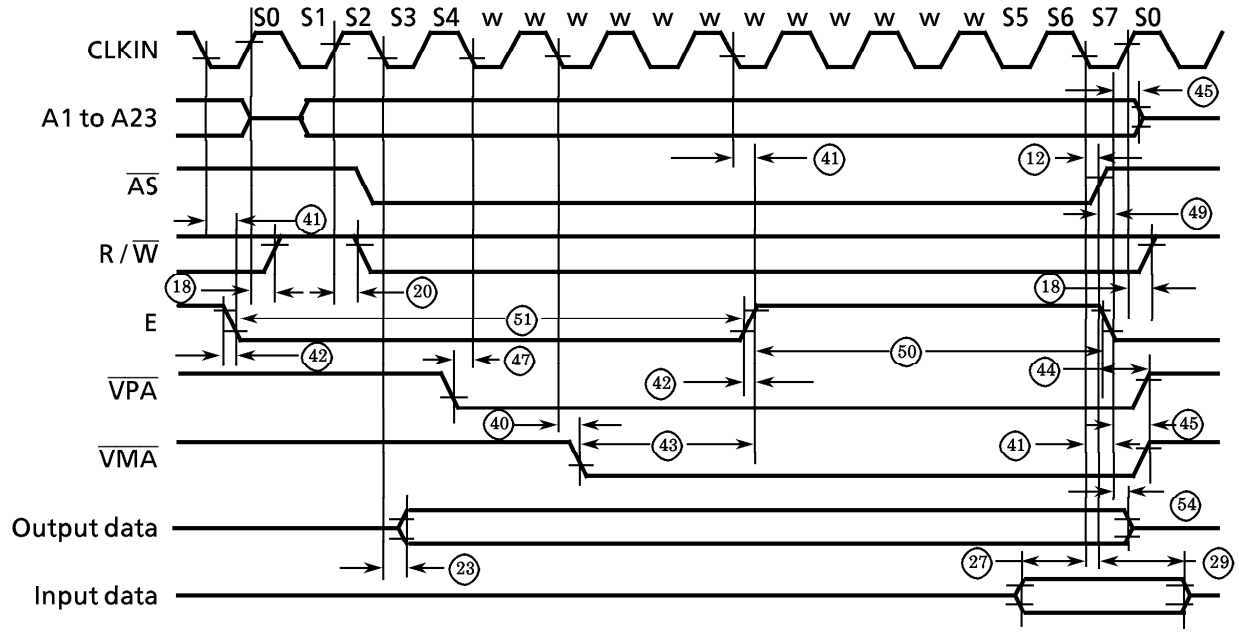
(GND = 0 V, Ta = – 20 to 85 °C; See figures 5.3 and 5.4)

Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
12[1]	Clock low to $\overline{AS}$, $\overline{DS}$ high	tCLSH	–	40	–	60	ns
18[1]	Clock low to R/$\overline{W}$ high	tCHRH	0	40	0	62	ns
20[1]	Clock high to R/$\overline{W}$ low (write)	tCHRL	0	40	0	62	ns
23	Clock low to output data valid (write)	tCLDO	–	50	–	80	ns
27	Input data setup time to clock low (read)	tCLDO	10	–	15	–	ns
29	$\overline{AS}$, $\overline{DS}$ negate to data invalid (hold time on read)	tSHDII	0	–	0	–	ns
40	Clock low to $\overline{VMA}$ low	tCLVML	–	70	–	70	ns
41	Clock low to E transition time	tCLET	–	35	–	62	ns
42	E output rise/fall time	tEr, f	–	15	–	15	ns
43	$\overline{VMA}$ low to E high	tVMLEH	90	–	200	–	ns
44	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high	tSHVPH	0	70	0	120	ns
45	E low to control address bus invalid (address hold time)	tELCAI	10	–	30	–	ns
47	Sync input setup time	tASI	10	–	15	–	ns
49[2]	$\overline{AS}$, $\overline{DS}$ high to E low	tSHEL	– 45	45	– 70	70	ns
50	E width high	tEH	280	–	450	–	ns
51	E width low	tEL	440	–	700	–	ns
54	E low to output invalid	tELDOI	15	–	30	–	ns

Notes :

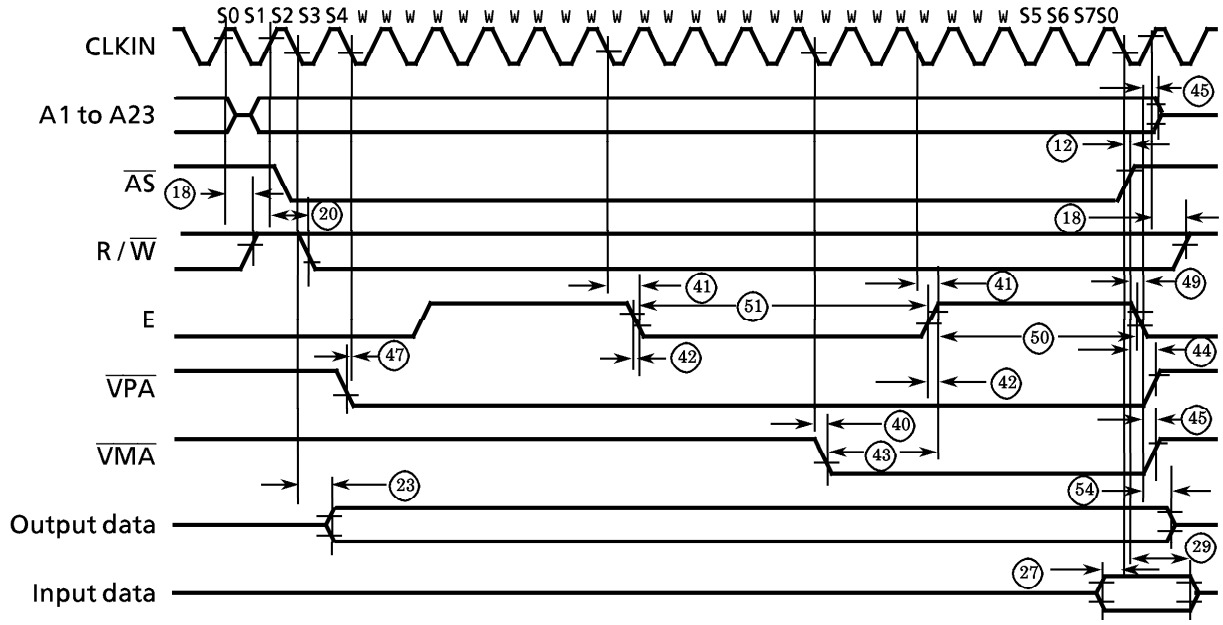
1. Strobe ($\overline{AS}$ and $\overline{xDS}$) negate and enable (E) signal fall are triggered at the S6 fall. Depending on the loads on their signal lines, one of the signals is triggered first. #49 shows the maximum fluctuation between strobe ($\overline{AS}$, $\overline{xDS}$) rise and enable (E) signal fall.

Clock = CLKIN



Note : This timing chart applies when designing an external circuit for generating $\overline{VMA}$. The chart shows the best case.

Figure 5.3 Timing Between TMP68HC003 and 6800 Peripheral Devices (Best Case)



Note : This timing chart applies when designing an external circuit for generating $\overline{VMA}$. The chart shows the worst case.

Figure 5.4 Timing Between TMP68HC003 and 6800 Peripheral Devices (Worst Case)

5.5 AC Electrical Characteristics - Bus Arbitration

(GND = 0 V, Ta = – 20 to 85 °C; See figure 5.5)

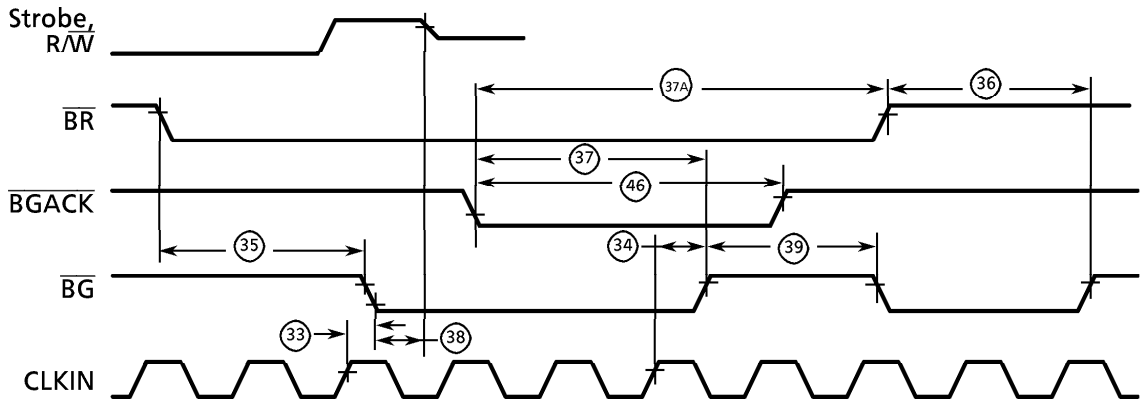
Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
7	Clock high to address, data bus high impedance	tCHADZ	–	60	–	80	ns
16	Clock high to control bus high impedance	tCHCZ	–	60	–	80	ns
33	Clock high to $\overline{BG}$ low	tCHGL	0	40	–	62	ns
34	Clock high to $\overline{BG}$ high	tCHGH	0	40	–	62	ns
35	$\overline{BR}$ low to $\overline{BG}$ low	tBRLGL	1.5	3.5	1.5	3.5	Clk. Per.
36[1]	$\overline{BR}$ high to $\overline{BG}$ high	tBKHGH	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{BGACK}$ low to $\overline{BG}$ high	tGALGH	1.5	3.5	1.5	3.5	Clk. Per.
37A[2]	$\overline{BGACK}$ low to $\overline{BR}$ high	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	ns
38	$\overline{BG}$ low to control, address, data bus high impedance ($\overline{AS}$ high)	tGLZ	–	60	–	80	ns
39	$\overline{BG}$ width high	tGH	1.5	–	1.5	–	Clk. Per.
46	$\overline{BGACK}$ width low	tGAL	1.5	–	1.5	–	Clk. Per.
47	Asynchronous input setup time	tASI	10	–	15	–	ns
57	$\overline{BGACK}$ high to control bus drive	tGABD	1.5	–	1.5	–	Clk. Per.
57A	$\overline{BGACK}$ high to FC, $\overline{VMA}$ drive	tGAFD	1	–	1	–	Clk. Per.
58[1]	$\overline{BG}$ high to control bus drive	tGHBD	1.5	–	1.5	–	Clk. Per.
58A	$\overline{BR}$ high to PC, $\overline{VMA}$ drive	tRHFD	1	–	1	–	Clk. Per.

Clock = CLKIN

Notes :

1. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
2. To guarantee proper operation, the minimum value must be met. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.

The waveforms below should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals.



Note : Asynchronous inputs $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL0}$ - $\overline{IPL2}$, and $\overline{VPA}$ are detected at the clock's falling edge.

Figure 5.5 Bus Arbitration Timing

5.6 AC Electrical Characteristics - Clock Generator

(GND = 0 V, Ta = – 20 to 85 °C; See figure 5.6)

Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
100	Clock cycle	tCLK	80	250	125	500	ns
101	Clock width high	tCCH	35	125	54	250	ns
102	Clock width low	tCCL	35	125	54	250	ns
103	Clock fall time	tCCF	–	8	–	8	ns
104	Clock rise time	tCCR	–	8	–	8	ns
110	Warm-up time 1 (DELAY = 0, ENABLE = 0)	tWARM1	XTAL = 25 MHz		XTAL = 16.67 MHz		ms
			–	0.65	–	0.98	
111	Warm-up time 2 (DELAY = 1, ENABLE = 0)	tWARM2	XTAL = 25 MHz		XTAL = 16.67 MHz		ms
			–	5.2	–	7.8	

5.7 AC Electrical Characteristics - Power-Down

(GND = 0 V, Ta = – 20 to 85 °C; See figure 5.6)

Number	Parameter	Symbol	V_{CC} = 5.0 V ± 5 %		V_{CC} = 3.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	
9	Clock high to $\overline{AS}$ low	tCHSL	3	40	3	60	ns
12	Clock low to $\overline{AS}$ high	tCLSH	–	40	–	62	ns
105	$\overline{AS}$ high to VCUT high impedance	tCUT	0	50	0	70	ns
106	$\overline{IPL}$ low to VCUT low	tON	–	100	–	100	ns
107	VCUT low to OFFSET high	tSET	0	50	0	70	ns
108	VCUT low to internal reset release (ENABLE = 1) ($\overline{RESET}$, $\overline{EHLT}$)	tSTART1	24	40	24	40	clk
109	$\overline{RELEASE}$ low to OFFSET low	tROF	–	100	–	100	ns

Clock = CLKIN

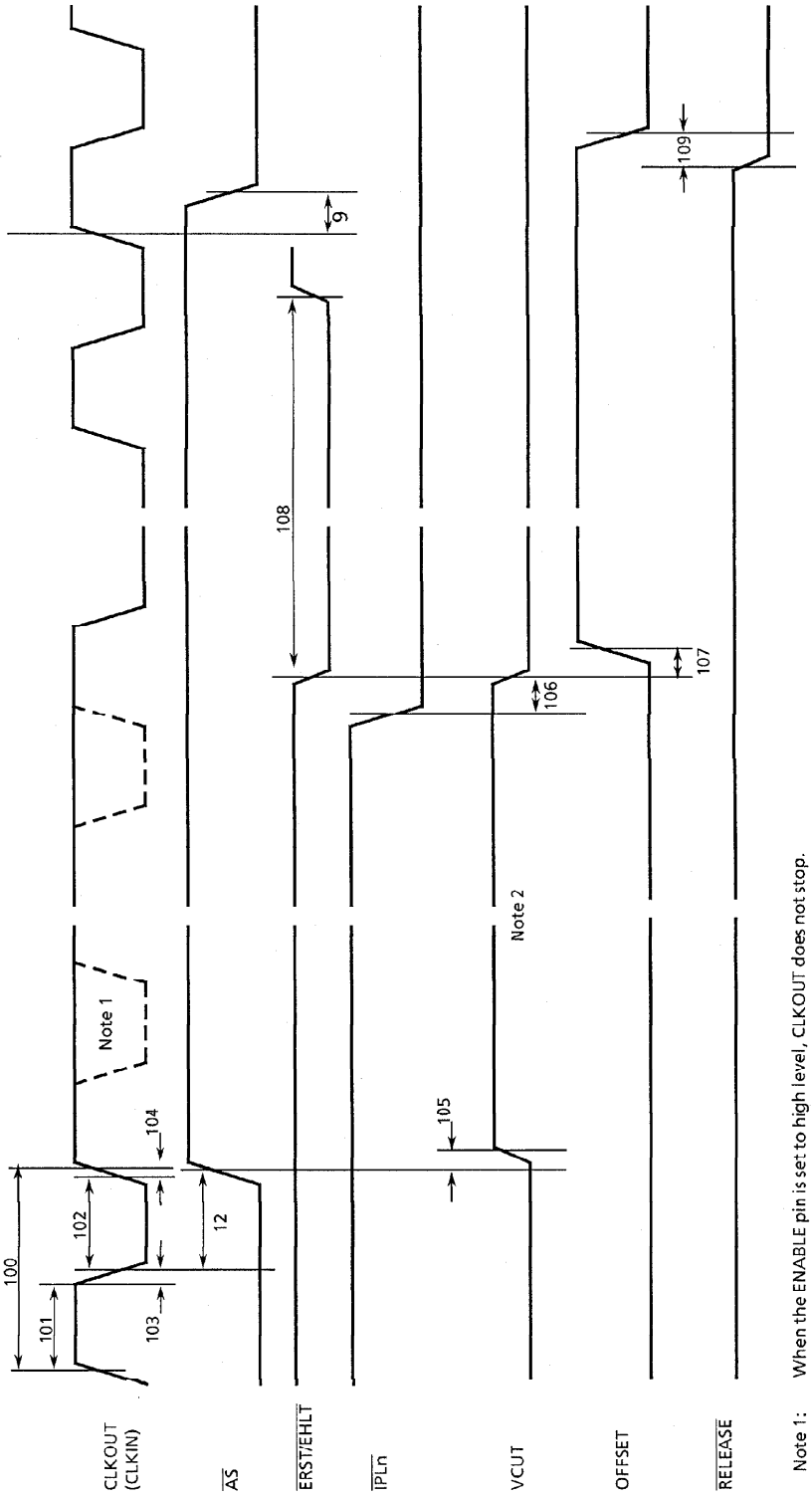


Figure 5.6 Clock Generator/Power-Down

Note 1: When the ENABLE pin is set to high level, CLKOUT does not stop.
Note 2: During power-down, VCUT is set to high impedance (open drain pin).