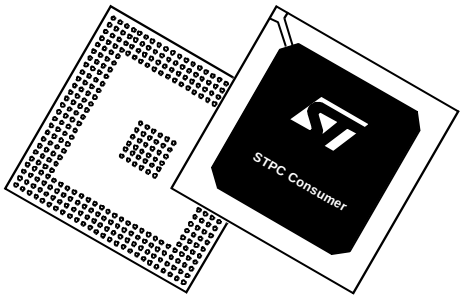
STPC® CONSUMER

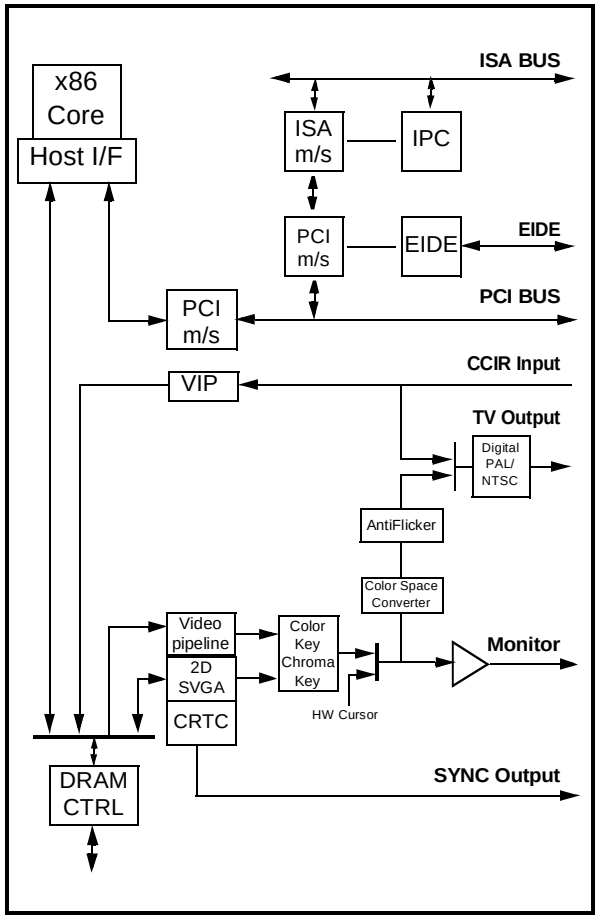
PC Compatible Embeded Microprocessor

- POWERFUL X86 PROCESSOR
- 64-BIT BUS ARCHITECTURE
- 64-BIT DRAM CONTROLLER
- SVGA GRAPHICS CONTROLLER
- UMA ARCHITECTURE
- VIDEO SCALER
- DIGITAL PAL/NTSC ENCODER
- VIDEO INPUT PORT
- CRT CONTROLLER
- 135MHz RAMDAC
- 3 LINE FLICKER FILTER
- SCAN CONVERTER
- PCI MASTER / SLAVE / ARBITER CTRL
- ISA MASTER/SLAVE INTERFACE
- IDE CONTROLLER
- DMA CONTROLLER
- INTERRUPT CONTROLLER
- TIMER / COUNTERS
- POWER MANAGEMENT



PBGA388

Figure 1. Logic Diagram



STPC CONSUMER OVERVIEW

The STPC Consumer integrates a standard 5th generation x86 core, a DRAM controller, a graphics subsystem, a video pipeline and support logic including PCI, ISA and IDE controllers to provide a single Consumer orientated PC compatible subsystem on a single device.

The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing the same memory array between the CPU main memory and the graphics and video frame buffers.

Extra facilities are implemented to handle video streams. Features include smooth scaling and color space conversion of the video input stream and mixing with graphics data. The chip also includes a built-in digital TV encoder and anti-flicker filters that allow stable, high-quality display on standard PAL or NTSC television sets without additional components.

The STPC Consumer is packaged in a 388 Plastic Ball Grid Array (PBGA).

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GBytes of external memory.
- 8KByte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Clock core speeds up to of 100 MHz.
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 3.3V operation.

- **DRAM Controller**
- Integrated system memory and graphic frame memory.
- Supports up to 128 MBytes system memory in 4 banks and down to as little as 2Mbytes.
- Supports 4MB, 8MB, 16MB, 32MB single-sided and double-sided DRAM SIMMs.
- Four quad-word write buffers for CPU to DRAM and PCI to DRAM cycles.
- Four 4-word read buffers for PCI masters.
- Supports Fast Page Mode & EDO DRAM.
- Programmable timing for DRAM parameters including CAS pulse width, CAS pre-charge time and RAS to CAS delay.
- 60, 70, 80 & 100ns DRAM speeds.
- Memory hole between 1 MByte & 8 MByte supported for PCI/ISA busses.
- Hidden refresh.

To check if your memory device is supported by the STPC, please refer to Table 6-24 in the Programming Manual.

- **Graphics Engine**
- 64-bit windows accelerator.
- Backward compatibility to SVGA standards.
- Hardware acceleration for text, bitblts, transparent blts and fills.
- Up to 64 x 64 bit graphics hardware cursor.
- Up to 4MB long linear frame buffer.
- 8-, 16-, and 24-bit pixels.
- Drivers for Windows and other operating systems.

- **VGA Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- Requires external frequency synthesizer and reference sources.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.
- **Video Input port**
- Accepts video inputs in CCIR 601/656 or ITU-R 601/656, and stream decoding.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- Video pass through to the onboard PAL/ NTSC encoder for full screen video images.
- HSYNC and B/T generation or lock onto external video timing source.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.
- Programmable two tap filter with gamma correction or three tap flicker filter.
- Progressive to interlaced scan converter.

- **Digital NTSC/PAL encoder**
- NTSC-M, PAL-M,PAL-B,D,G,H,I,PAL-N easy programmable video outputs.
- CCIR601 encoding with programmable color subcarrier frequencies.
- Line skip/insert capability
- Interlaced or non-interlaced operation mode.
- 625 lines/50Hz or 525 lines/60Hz 8 bit multiplexed CB-Y-CR digital input.
- CVBS and R,G,B simultaneous analog outputs through 10-bit DACs.
- Cross color reduction by specific trap filtering on luma within CVBS flow.
- Power down mode available on each DAC.

- **PCI Controller**
- Fully compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- *0.33X and 0.5X CPU clock PCI clock.*

- **ISA master/slave Interface**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- *Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.*
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus. NSP compliant.

- **IDE Interface**
- Supports PIO
- *Supports up to Mode 5 Timings*
- Transfer Rates to 22 MBytes/sec
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO modes) - 4 x 32-Bit Buffer FIFOs per channel
- Support for PIO mode 3 & 4.
- Support for 11.1/16.6 MB/s, I/O Channel Ready PIO data transfers.
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals
- Backward compatibility with IDE (ATA-1).
- Drivers for Windows and other Operating Systems

- **Integrated peripheral controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel ports.
- Supports RTC, interrupts and DMAs wake-up

1. GENERAL DESCRIPTION

At the heart of the STPC Consumer is an advanced processor block, dubbed the 5ST86. The 5ST86 includes a powerful x86 processor core along with a 64-bit DRAM controller, advanced 64bit accelerated graphics and video controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus) and EIDE controller.

The STPC Consumer has in addition to the 5ST86, a Video subsystem and high quality digital Television output.

The STMicroelectronics x86 processor core is embedded with standard and application specific peripheral modules on the same silicon die. The core has all the functionality of the STMicroelectronics standard x86 processor products, including the low power System Management Mode (SMM).

System Management Mode (SMM) provides an additional interrupt and address space that can be used for system power management or software transparent emulation of peripherals. While running in isolated SMM address space, the SMM interrupt routine can execute without interfering with the operating system or application programs.

Further power management facilities include a suspend mode that can be initiated from either hardware or software. Because of the static nature of the core, no internal data is lost.

The STPC Consumer makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This significantly reduces total system memory with system performances equal to that of a comparable solution with separate frame buffer and system memory. In addition, memory bandwidth is improved by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus.

The 64-bit wide memory array provides the system with 320MB/s peak bandwidth, double that of an equivalent system using 32 bits. This allows for higher screen resolutions and greater color depth. The processor bus runs at the speed of the processor (DX devices) or half the speed (DX2 devices).

The ‘standard’ PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated with the x86 processor core.

The PCI bus is the main data communication link to the STPC Consumer chip. The STPC Consumer translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports the generation of Configuration cycles on the PCI bus. The STPC Consumer, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

The STPC Consumer integrates an ISA bus controller. Peripheral modules such as parallel and serial communications ports, keyboard controllers and additional ISA devices can be accessed by the STPC Consumer chip set through this bus.

An industry standard EIDE (ATA 2) controller is built in to the STPC Consumer and connected internally via the PCI bus.

Graphics functions are controlled by the on-chip SVGA controller and the monitor display is managed by the 2D graphics display engine.

This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations, which include hardware acceleration of text, bitblts, transparent blts and fills. These operations can act on off-screen or on-screen areas. The frame buffer size ranges up to 4 Mbytes anywhere in the physical main memory.

The graphics resolution supported is a maximum of 1280x1024 in 65536 colours at 75Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate the above display resolution.

STPC Consumer provides several additional functions to handle MPEG or similar video streams. The Video Input Port accepts an encoded digital video stream in one of a number of industry standard formats, decodes it, optionally decimates it by a factor of 2:1, and deposits it into an off screen area of the frame buffer. An interrupt request can be generated when an entire field or frame has been captured.

The video output pipeline incorporates a video-scaler and color space converter function and provisions in the CRT controller to display a video window. While repainting the screen the CRT controller fetches both the video as well as the normal non-video frame buffer in two separate internal FIFOs (256-Bytes each). The video stream can be color-space converted (optionally) and smooth scaled. Smooth interpolative scaling in both horizontal and vertical directions are implemented. Color and Chroma key functions are also implemented to allow mixing video stream with non-video frame buffer.

The video output passes directly to the RAMDAC for monitor output or through another optional color space converter (RGB to 4:2:2 YCrCb) to the programmable anti-flicker filter. The flicker filter is configured as either a two line filter with gamma correction (primarily designed for DOS type text) or a 3 line flicker filter (primarily designed for Windows type displays). The flicker filter is optional and can be software disabled for use with video on large screen areas.

The Video output pipeline of the STPC Consumer interfaces directly to the internal digital TV encoder. It takes a 24 bit RGB non-interlaced pixel stream and converts to a multiplexed 4:2:2 YCrCb 8 bit output stream, the logic includes a progressive to interlaced scan converter and logic to insert appropriate CCIR656 timing reference codes into the output stream. It facilitates the high quality display of VGA or full screen video streams received via the Video input port to standard NTSC or PAL televisions.

The STPC Consumer core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit module (PMU) controls the power consumption by providing a comprehensive set of features that control the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides following hardware structures to assist the software in managing the power consumption by the system.

- System Activity Detection.
- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).
- House-keeping activity detection.
- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.
- Peripheral activity detection.
- Peripheral timer detecting peripheral inactivity
- SUSP# modulation to adjust the system performance in various power down states of the system including full power on state.
- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer period of times is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate SMI interrupt to allow the software to bring the system back up to full power on state. The chip-set supports up to three power down states: Doze state, Stand-by state and Suspend mode. These correspond to decreasing levels of power savings.

Power down puts the STPC Consumer into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped.

A reference design for the STPC Consumer is available including the schematics and layout files, the design is a PC ATX motherboard design. The design is available as a demonstration board for application and system development.

The STPC Consumer is supported by several BIOS vendors, including the super I/O device used in the reference design. Drivers for 2D accelerator, video features and EIDE are availaible on various operating systems.

The STPC Consumer has been designed using modern reusable modular design techniques, it is possible to add or remove the standard features of the STPC Consumer or other variants of the 5ST86 family. Contact your local STMicroelectonics sales office for further information.

Figure 1-1 Functionnal description

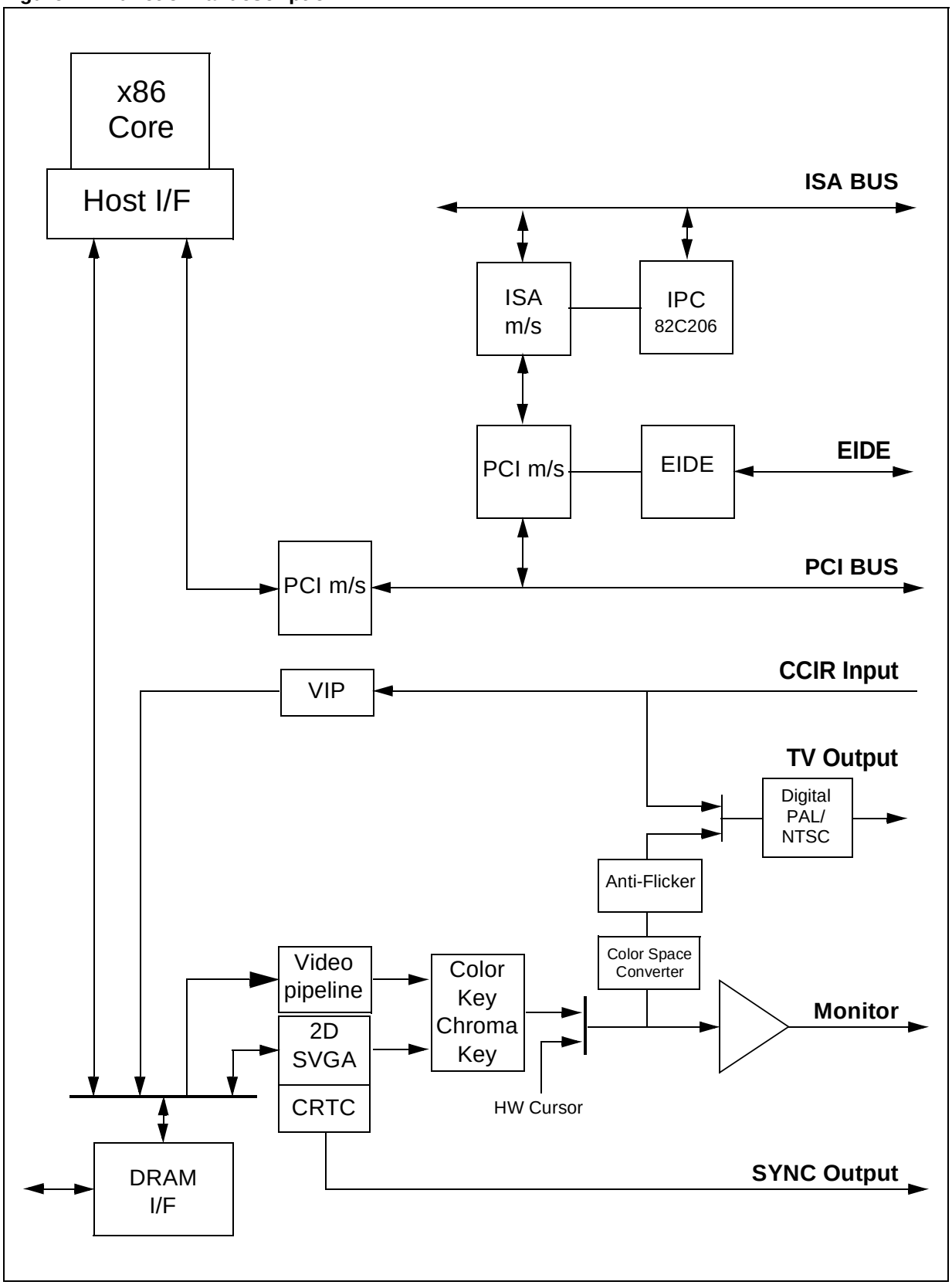
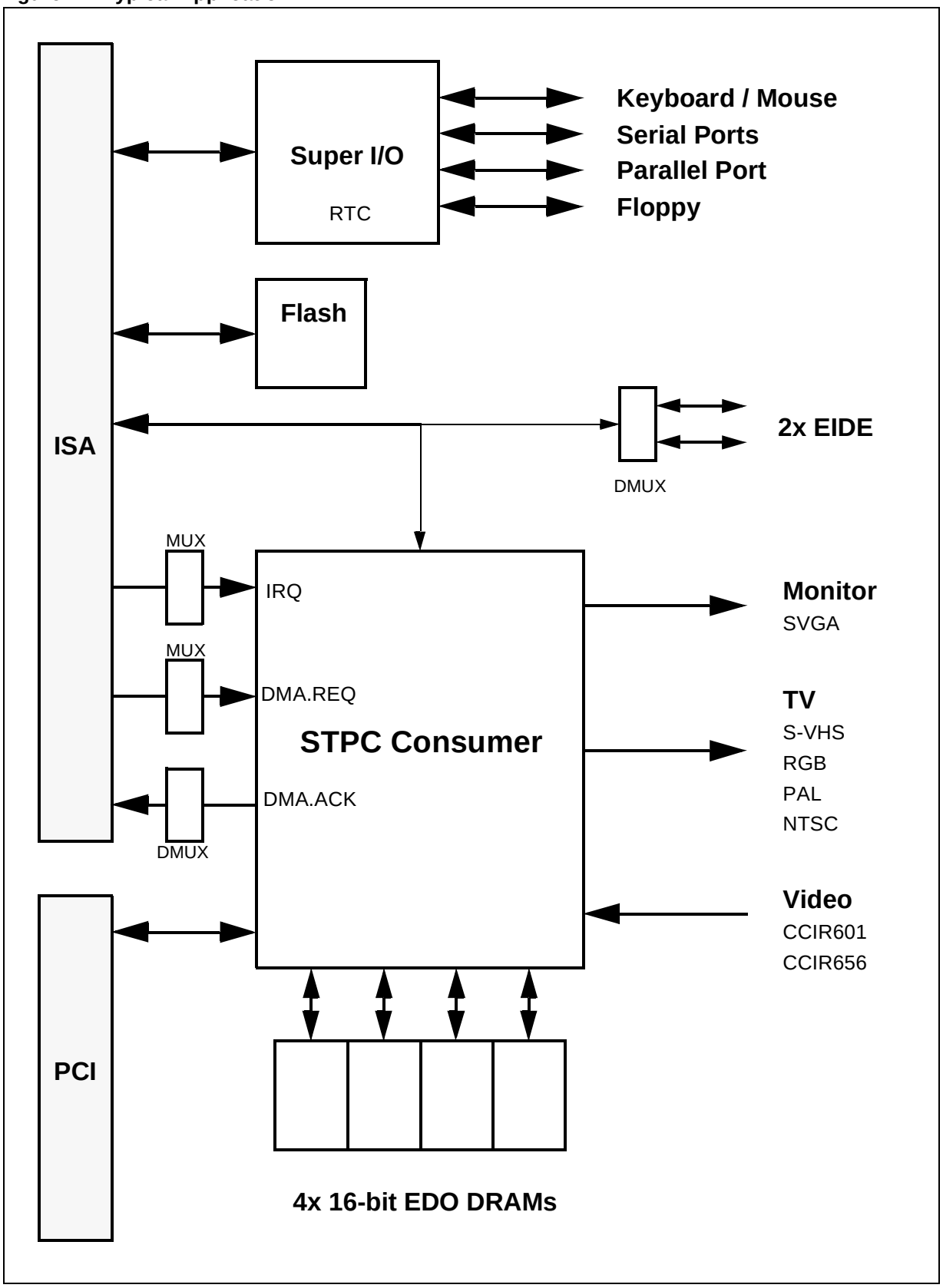


Figure 1-2 Typical Application



2. PIN DESCRIPTION

2.1 INTRODUCTION

The STPC Consumer integrates most of the functionalities of the PC architecture. As a result, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Consumer. This offers improved performance due to the tight coupling of the processor core and these peripherals. As a result many of the external pin connections are made directly to the on-chip peripheral functions.

Figure 2-1 shows the STPC Consumer's external interfaces. It defines the main busses and their function. Table 2-1 describes the physical implementation listing signal types and their functionalities. Table 2-2 provides a full pin listing and description. Table 2-3 provides a full listing of the STPC Consumer pin locations of package by physical connection. Please refer to the pin allocation drawing for reference.

Table 2-1. Signal Description

Group name	Qty
Basic Clocks reset & Xtal(SYS)	12
DRAM Controller	89
PCI interface (PCI)	58
ISA / IDE / IPC combined interface	88
Video Input (VIP)	9
TV Output	10
VGA Monitor interface	10
Grounds	69
V_{DD}	26
Analog specific V_{CC}/V_{DD}	12
Reserved	5
Total Pin Count	388

Note: Several interface pins are multiplexed with other functions, refer to the Pin Description section for further details

Figure 2-1. STPC Consumer External Interfaces

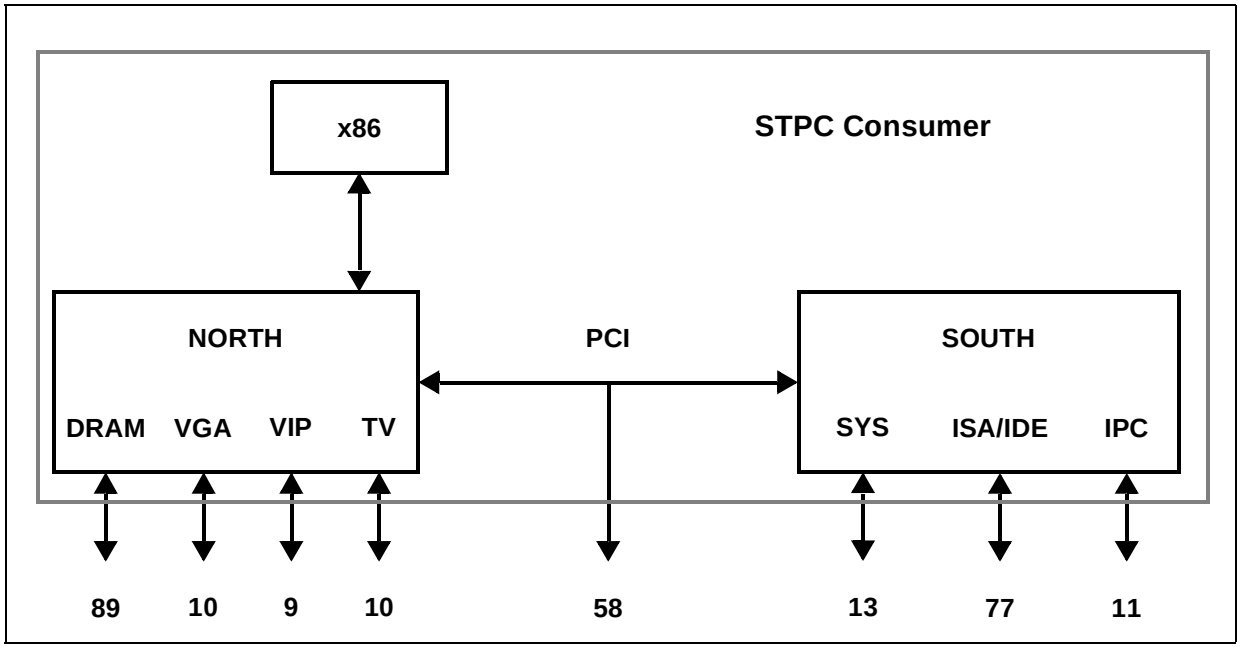


Table 2-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
BASIC CLOCKS AND RESETS			
SYSRSTI#	I	System Reset / Power good	1
XTALI	I	14.3MHz Crystal Input	1
XTALO	I/O	14.3MHz Crystal Output - External Oscillator Input	1
HCLK	O	Host Clock (Test)	1
DEV_CLK	O	24MHz Peripheral Clock (floppy drive)	1
GCLK2X	I/O	80MHz Graphics Clock	1
DCLK	I/O	135MHz Dot Clock	1
PCI_CLKI	I	33MHz PCI Input Clock	1
PCI_CLKO	O	33MHz PCI Output Clock (from internal PLL)	1
SYSRSTO#	O	Reset Output to System	1
ISA_CLK	O	ISA Clock Output - Multiplexer Select Line For IPC	1
ISA_CLK2X	O	ISA Clock x 2 Output - Multiplexer Select Line For IPC	1
MEMORY INTERFACE			
MA[11:0]	O	Memory Address	12
RAS#[3:0]	O	Row Address Strobe	4
CAS#[7:0]	O	Column Address Strobe	8
MWE#	O	Write Enable	1
MD[63:0]	I/O	Memory Data	64
PCI INTERFACE			
AD[31:0]	I/O	PCI Address / Data	32
CBE[3:0]	I/O	Bus Commands / Byte Enables	4
FRAME#	I/O	Cycle Frame	1
TRDY#	I/O	Target Ready	1
IRDY#	I/O	Initiator Ready	1
STOP#	I/O	Stop Transaction	1
DEVSEL#	I/O	Device Select	1
PAR	I/O	Parity Signal Transactions	1
SERR#	O	System Error	1
LOCK#	I	PCI Lock	1
PCIREQ#[2:0]	I	PCI Request	3
PCIGNT#[2:0]	O	PCI Grant	3
PCI_INT[3:0]	I	PCI Interrupt Request	4
VDD5	I	5V Power Supply for PCI ESD protection	4
ISA AND IDE COMBINED ADDRESS/DATA			
LA[23:22] / SCS3#,SCS1#	I/O	Unlatched Address (ISA) / Secondary Chip Select (IDE)	2
LA[21:20] / PCS3#,PCS1#	I/O	Unlatched Address (ISA) / Primary Chip Select (IDE)	2
LA[19:17] / DA[2:0]	O	Unlatched Address (ISA) / Address (IDE)	3
RMRTCCS# / DD[15]	I/O	ROM/RTC Chip Select / Data Bus bit 15 (IDE)	1
KBCS# / DD[14]	I/O	Keyboard Chip Select / Data Bus bit 14 (IDE)	1
RTCRW# / DD[13]	I/O	RTC Read/Write / Data Bus bit 13 (IDE)	1
RTCDS# / DD[12]	I/O	RTC Data Strobe / Data Bus bit 12 (IDE)	1
SA[19:8] / DD[11:0]	I/O	Latched Address (ISA) / Data Bus (IDE)	16
SA[7:0]	I/O	Latched Address (IDE)	4
SD[15:0]	I/O	Data Bus (ISA)	16

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
ISA/IDE COMBINED CONTROL			
IOCHRDY / DIORDY	I/O	I/O Channel Ready (ISA) - Busy/Ready (IDE)	1
ISA CONTROL			
OSC14M	O	ISA bus synchronisation clock	1
ALE	O	Address Latch Enable	1
BHE#	I/O	System Bus High Enable	1
MEMR#, MEMW#	I/O	Memory Read and Memory Write	2
SMEMR#, SMEMW#	O	System Memory Read and Memory Write	2
IOR#, IOW#	I/O	I/O Read and Write	2
MASTER#	I	Add On Card Owns Bus	1
MCS16#, IOCS16#	I	Memory/IO Chip Select16	2
REF#	O	Refresh Cycle.	1
AEN	O	Address Enable	1
ZWS#	I	Zero Wait State	1
IOCHCK#	I	I/O Channel Check.	1
ISAOE#	O	Bidirectional OE Control	1
RTCAS	O	Real Time Clock Address Strobe	1
GPIOCS#	I/O	General Purpose Chip Select	1
IDE CONTROL			
PIRQ	I	Primary Interrupt Request	1
SIRQ	I	Secondary Interrupt Request	1
PDRQ	I	Primary DMA Request	1
SDRQ	I	Secondary DMA Request	1
PDACK#	O	Primary DMA Acknowledge	1
SDACK#	O	Secondary DMA Acknowledge	1
PIOR#	I/O	Primary I/O Read	1
PIOW#	O	Primary I/O Write	1
SIOR#	I/O	Secondary I/O Read	1
SIOW#	O	Secondary I/O Write	1
IPC			
IRQ_MUX[3:0]	I	Multiplexed Interrupt Request	4
DREQ_MUX[1:0]	I	Multiplexed DMA Request	2
DACK_ENC[2:0]	O	DMA Acknowledge	3
TC	O	ISA Terminal Count	1
MONITOR INTERFACE			
RED, GREEN, BLUE	O	Red, Green, Blue	3
VSYNC	O	Vertical Sync	1
HSYNC	O	Horizontal Sync	1
VREF_DAC	I	DAC Voltage reference	1
RSET	I	Resistor Set	1
COMP	I	Compensation	1
COL_SEL	O	Colour Select	1
SCL / DDC[1]	I/O	I²C Interface - Clock / Can be used for VGA DDC[1] signal	1
SDA / DDC[0]	I/O	I²C Interface - Data / Can be used for VGA DDC[0] signal	1

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
VIDEO INPUT			
VCLK	I	Pixel Clock	1
VIN	I	YUV Video Data Input CCIR 601 or 656	8
TV OUTPUT			
RED_TV, GREEN_TV, BLUE_TV	O	Analog video outputs synchronized with CVBS	3
VCS	O	Composite Synch or Horizontal line SYNC output	1
ODD_EVEN	O	Frame Synchronisation	1
CVBS	O	Analog video composite output (luminance / chrominance)	1
IREF1_TV	I	Reference current of 9bit DAC for CVBS	1
VREF1_TV	I	Reference voltage of 9bit DAC for CVBS	1
IREF2_TV	I	Reference current of 8bit DAC for R,G,B	1
VREF2_TV	I	Reference voltage of 8bit DAC for R,G,B	1
VSSA_TV	I	Analog Vss for DAC	1
VDDA_TV	I	Analog Vdd for DAC	1
MISCELLANEOUS			
SPKRD	O	Speaker Device Output	1
SCAN_ENABLE	I	Reserved (Test pin)	1

2.2 SIGNAL DESCRIPTIONS

2.2.1 BASIC CLOCKS AND RESETS

SYSRSTI *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. SYSRSTI is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of SYSRSTI.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3MHz Crystal Input*
XTALO *14.3MHz Crystal Output.* These pins are the 14.318 MHz crystal input; This clock is used as the reference clock for the internal frequency synthesizer to generate the HCLK, CLK24M, GCLK2X and DCLK clocks.
A 14.318 MHz Series Cut Quartz Crystal should be connected between these two pins. Balance capacitors of 15 pF should also be added. In the event of an external oscillator providing the master clock signal to the STPC Consumer device, the TTL signal should be provided on XTALO.

HCLK *Host Clock.* This is the host 1X clock. Its frequency can vary from 25 to 75 MHz. All host transactions and PCI transactions are synchronized to this clock. The DRAM controller to execute the host transactions is also driven by this clock. In normal mode, this output clock is generated by the internal pll.

GCLK2X *80MHz Graphics Clock.* This is the Graphics 2X clock, which drives the graphics engine and the DRAM controller to execute the graphics and display cycles.
Normally GCLK2X is generated by the internal frequency synthesizer, and this pin is an output. By setting a bit in Strap Register 2, this pin can be made an input so that an external clock can replace the internal frequency synthesizer.

PCI_CLKI *33MHz PCI Input Clock*

This signal is the PCI bus clock input and should be driven from the PCI_CLKO pin.

PCI_CLKO *33MHz PCI Output Clock.* This is the master PCI bus clock output.

DCLK *135MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can go from 8MHz (using internal PLL) up to 135 MHz, and it is required to have a worst case duty cycle of 60-40.
This signal is either driven by the internal pll (VGA) or an external 27MHz oscillator (when the composite video output is enabled). The direction can be controlled by a strap option or an internal register bit.

ISA_CLK *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces the Clock signal for the ISA bus. It is also used with ISA_CLK2X as the multiplexor control lines for the Interrupt Controller Interrupt input lines. This is a divided down version of either the PCICLK or OSC14M.

ISA_CLKX2 *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces a signal that is twice the frequency of the ISA bus Clock signal. It is also used with ISA_CLK as the multiplexor control lines for the Interrupt Controller input lines.

DEV_CLK *24MHz Peripheral Clock Output.* This 24MHZ signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip.

OSC14M *ISA bus synchronisation clock Output.* This is the buffered 14.318 Mhz clock to the ISA bus.

2.2.2 MEMORY INTERFACE

MA[11:0] *Memory Address Output.* These 12 multiplexed memory address pins support external DRAM with up to 4K refresh. These include all 16M x N and some 4M x N DRAM modules. The address signals must be externally buffered to support more than 16 DRAM chips. The timing of these signals can be adjusted by software to match the timings of most DRAM modules.

MD[63:0] *Memory Data I/O.* This is the 64-bit memory data bus. If only half of a bank is populated, MD63-32 is pulled high, data is on MD31-0.
MD[40-0] are read by the device strap option registers during rising edge of SYSRSTI.

RAS#[3:0] *Row Address Strobe Output.* There are 4 active low row address strobe outputs, one for each bank of the memory. Each bank contains 4 or 8-Bytes of data. The memory controller allows half of a bank (4-bytes) to be populated to enable memory upgrade at finer granularity.
The RAS# signals drive the SIMMs directly without any external buffering. These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the RAS# signals at the pins.

CAS#[7:0] *Column Address Strobe Output.* There are 8 active low column address strobe outputs, one each for each byte of the memory.
The CAS# signals drive the SIMMs either directly or through external buffers.
These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the CAS# signals at the pins.

MWE# *Write Enable Output.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L). This single write enable controls all the DRAM. It can be externally buffered to boost the maximum number of loads (DRAM chips) supported.
The MWE# signals drive the SIMMs directly without any external buffering.

2.2.3 VIDEO INTERFACE

VCLK *Pixel Clock Input.*

VIN[7:0] *YUV Video Data Input CCIR 601 or 656.* Time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus interfaces with an MPEG video decoder output port and typically carries a stream of Cb,Y,Cr,Y digital video at VCLK frequency, clocked on the rising edge (by default) of VCLK. A 54-Mbit/s 'double' Cb, Y, Cr, Y input multiplex is supported for double encoding application (rising and falling edge of CKREF are operating).

2.2.4 TV OUTPUT

RED_TV / C_TV *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is the Chrominance Output.

GREEN_TV / Y_TV *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is the Luminance Output.

BLUE_TV / CVBS*Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is a second composite output.

VCS *Line synchronisation Output.* This pin is an input in ODDEV+HSYNC or VSYNC + HSYNC or VSYNC slave modes and an output in all other modes (master/slave)
The signal is synchronous to rising edge of CKREF. The default polarity uses a negative pulse

ODD_EVEN *Frame Synchronisation Ourput.* This pin supports the Frame synchronisation signal. It is an input in slave modes, except when sync is extracted from YCrCb data, and an output in master mode and when sync is extracted from YCrCb data
The signal is synchronous to rising edge of DCLK. The default polarity for this pin is:
- odd (not-top) field : LOW level
- even (bottom) field : HIGH level

IREF1_TV *Ref. current* for CVBS 10-bit DAC.

VREF1_TV *Ref. voltage* for CVBS 10-bit DAC.

IREF2_TV *Reference current* for RGB 9-bit DAC.

VREF2_TV *Reference voltage* for RGB 9-bit DAC.

VSSA_TV *Analog V_{SS} for DAC*

VDDA_TV *Analog V_{DD} for DAC*

CVBS *Analog video composite output (luminance/ chrominance).* CVBS is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended.

2.2.5 PCI INTERFACE

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

CBE#[3:0] *Bus Commands/Byte Enables.* These are the multiplexed command and byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the byte enable information. These pins are inputs when a PCI master other than the STPC Consumer owns the bus and outputs when the STPC Consumer owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Consumer owns the PCI bus.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Consumer is the target of the current bus transaction. It is used as an input when STPC Consumer initiates a cycle on the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Consumer initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Consumer to determine when the current PCI master is ready to complete the current transaction.

STOP# *Stop Transaction.* Stop is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Consumer and is used as an output when a PCI master cycle is targeted to the STPC Consumer.

DEVSEL# *I/O Device Select.* This signal is used as an input when the STPC Consumer initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Consumer is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE#[3:0], and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Consumer initiated PCI transaction. Its assertion by either the STPC Consumer or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

PCIREQ#[2:0] *PCI Request.* This pin are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

PCIGNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCIREQ#.

2.2.6 ISA/IDE COMBINED ADDRESS/DATA

LA[23]/SCS3# *Unlatched Address (ISA)/Secondary Chip Select (IDE).* This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 23 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high secondary slave IDE chip select signal. This signal is to be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[22]/SCS1# *Unlatched Address (ISA)/Secondary Chip Select (IDE)*

This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 22 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high secondary slave IDE chip select signal. This signal is to be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[21]/PCS3# *Unlatched Address (ISA)/Primary Chip Select (IDE).* This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 21 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA-bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high primary slave IDE chip select signal. This signal is to be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[20]/PCS1# *Unlatched Address (ISA)/Primary Chip Select (IDE).* This pin has two functions, depending on whether the ISA bus is active or the IDE bus is active.
When the ISA bus is active, this pins is ISA Bus unlatched address bit 20 for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, this pin is in output mode. When an ISA bus master owns the bus, this pins is in input mode.
When the IDE bus is active, this signals is used as the active high primary slave IDE chip select signal. This signal is to be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

LA[19:17]/DA[2:0] *Unlatched Address (ISA)/Address (IDE).* These pins are multi-function pins. They are used as the ISA bus unlatched address bits [19:17] for ISA bus or the three address bits for the IDE bus devices.
When used by the ISA bus, these pins are ISA Bus unlatched address bits 19-17 on 16-bit devices. When ISA bus is accessed by any cycle initiated from the PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are tristated.

For IDE devices, these signals are used as the DA[2:0] and are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed before being connected to the IDE devices.

SA[19:8]/DD[11:0] *Unlatched Address (ISA)/Data Bus (IDE).* These are multifunction pins. When the ISA bus is active, they are used as the ISA bus system address bits 19-8. When the IDE bus is active, they serve as IDE signals DD[11:0].
These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.
IDE devices are connected to SA[19:8] directlyand ISA bus is connected to these pins through two LS245 transceivers. The $\overline{OE}$ of the transceivers are connected to ISAOE# and DIR is connected to MASTER#. A bus signals of the transceivers are connected to CPC and IDE DD bus and B bus signals are connected to ISA SA bus.

DD[15:12] *Databus (IDE).* The high 4 bits of the IDE databus are combined with several of the X-bus lines. Refer to the following section for X-bus pins for further information.

SA[7:0] *ISA Bus address bits [7:0].* These are the 8 low bits of the system address bus of ISA on 8-bit slot. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus (ISA).* These pins are the external databus to the ISA bus.

2.2.7 ISA/IDE COMBINED CONTROL

IOCHRDY/DIORDY *Channel Ready (ISA)/Busy/ Ready (IDE).* This is a multi-function pin. When the ISA bus is active, this pin is IOCHRDY. When the IDE bus is active, this serves as IDE signal DIORDY.
IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Consumer. The STPC Consumer monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh.
ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Consumer since the access to the system memory can be considerably delayed due to CRT refresh or a write back cycle.

2.2.8 ISA CONTROL

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Consumer to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Consumer.
ALE is driven low after reset.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Consumer generates SMEMR# signal of the ISA bus only when the address is below one megabyte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Consumer generates SMEMW# signal of the ISA bus only when the address is below one megabyte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Consumer ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Consumer does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Consumer is executed as an extended 8-bit IO cycle.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Consumer performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Consumer performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

ZWS# *Zero Wait State.* This signal, when asserted by addressed device, indicates that current cycle can be shortened.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

ISAOE# *Bidirectional OE Control.* This signal controls the $\overline{OE}$ signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

GPIOCS# *I/O General Purpose Chip Select 1.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices to power down or any other desired function.

2.2.9 IDE CONTROL

PIRQ *Primary Interrupt Request.* Interrupt request from primary IDE channel.

SIRQ *Secondary Interrupt Request.* Interrupt request from secondary IDE channel.

PDRQ *Primary DMA Request.* DMA request from primary IDE channel.

SDRQ *Secondary DMA Request.* DMA request from secondary IDE channel.

PDACK# *Primary DMA Acknowledge.* DMA acknoledge to primary IDE channel.

SDACK# *Secondary DMA Acknowledge.* DMA acknoledge to secondary IDE channel.

PIOR# *Primary I/O Read.* Primary channel read. Active low output.

PIOW# *Primary I/O Write*. Primary channel write. Active low output.

SIOR# *Secondary I/O Read* Secondary channel read. Active low output.

SIOW# *Secondary I/O Write* Secondary channel write. Active low output.

2.2.10 IPC

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They are to be encoded before connection to the STPC Consumer using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the $\overline{IRQ}$ pin of the RTC.

PCI_INT[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals. They are to be encoded before connection to the STPC Consumer using ISACLK and ISACLKX2 as the input selection strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Consumer using ISACLK and ISACLKX2 as the input selection strobes.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Consumer before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the byte count expires.

SPKRD *Speaker Drive.* This the output to the speaker and is AND of the counter 2 output with bit 1 of Port 61, and drives an external speaker driver. This output should be connected to 7407 type high voltage driver.

2.2.11 X-Bus Interface pins / IDE Data

RMRTCCS# / DD[15] *ROM/Real Time clock chip select.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RMRTCCS#. This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During a IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR or IOW# signals to properly access the real time clock.
When ISAOE# is inactive, this signal is used as IDE DD[15] signal.
This signal must be ORed externally with ISAOE# and is then connected to ROM and RTC. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor.

KBCS# / DD[14] *Keyboard Chip Select.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as KBCS#. This signal is asserted if a keyboard access is decoded during a I/O cycle.
When ISAOE# is inactive, this signal is used as IDE DD[14] signal.
This signal must be ORed externally with ISAOE# and is then connected to keyboard. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor.

RTCRW# / DD[13] *Real Time Clock* $R\overline{W}$*.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCRW#. This signal is asserted for any I/O write to port 71H.
When ISAOE# is inactive, this signal is used as IDE DD[13] signal. This signal must be ORed externally with ISAOE# and then connected to the RTC. An LS244 or equivalent function can be used if OE is connected to ISAOE# and the output is provided with a weak pull-up resistor.

RTCDS# / DD[12] *Real Time Clock DS*. This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCDS#. This signal is asserted for any I/O read to port 71H. Its polarity complies with the DS pin of the MT48T86 RTC device when configured with Intel timings.
When ISAOE# is inactive, this signal is used as IDE DD[12] signal. This signal must be ORed externally with ISAOE# and is then connected to RTC. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor.

RTCAS *Real time clock address strobe.* This signal is asserted for any I/O write to port 70H.

2.2.12 Monitor Interface

RED, GREEN, BLUE *RGB Video Outputs.* These are the 3 analog color outputs from the RAMDACs. These signals are sensitive to interference, therefore they need to be properly shielded.

VSYNC *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

HSYNC *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

VREF_DAC *DAC Voltage reference.* An external voltage reference is connected to this pin to bias the DAC.

RSET *Resistor Current Set.* This is reference current input to the RAMDAC is used to set the full-scale output of the RAMDAC.

COMP *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and V_{DD} to damp oscillations.

DDC[1:0] *Direct Data Channel Serial Link.* These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I^2C electrical specifications, they have open-collector output drivers which are internally connected to V_{DD} through pull-up resistors.

They can instead be used for accessing I²C devices on board. DDC1 and DDC0 correspond to SCL and SDA respectively.

2.2.13 MISCELLANEOUS

SCAN_ENABLE *Reserved.* The pins are reserved for Test and Miscellaneous functions)

Table 2-3. Pinout.

Pin #	Pin name
AF3	SYSRSTI
A3	XTALI
C4	XTALO
G23	HCLK
F25	DEV_CLK
AF15	GCLK2X
AF9	DCLK
AD15	MA[0]
AF16	MA[1]
AC15	MA[2]
AE17	MA[3]
AD16	MA[4]
AF17	MA[5]
AC17	MA[6]
AE18	MA[7]
AD17	MA[8]
AF18	MA[9]
AE19	MA[10]
AF19	MA[11]
AD18	RAS#[0]
AE20	RAS#[1]
AC19	RAS#[2]
AF20	RAS#[3]
AE21	CAS#[0]
AC20	CAS#[1]
AF21	CAS#[2]
AD20	CAS#[3]
AE22	CAS#[4]
AF22	CAS#[5]
AD21	CAS#[6]
AE23	CAS#[7]
AC22	MWE#
AF23	MD[0]
AE24	MD[1]
AF24	MD[2]
AD25	MD[3]
AC25	MD[4]
AC26	MD[5]
AB24	MD[6]
AA25	MD[7]
AA24	MD[8]
Y25	MD[9]
Y24	MD[10]
V23	MD[11]
W24	MD[12]
V26	MD[13]
V24	MD[14]
U23	MD[15]
U24	MD[16]
R26	MD[17]
P25	MD[18]
P26	MD[19]
N25	MD[20]
N26	MD[21]
M25	MD[22]
M26	MD[23]
M24	MD[24]
M23	MD[25]
L24	MD[26]
J25	MD[27]
J26	MD[28]
H26	MD[29]
G25	MD[30]
G26	MD[31]
AD22	MD[32]
AD23	MD[33]
AE26	MD[34]
AD26	MD[35]
AC24	MD[36]
AB25	MD[37]
AB26	MD[38]
Y23	MD[39]
AA26	MD[40]
Y26	MD[41]
W25	MD[42]
W26	MD[43]
V25	MD[44]
U25	MD[45]
U26	MD[46]
T25	MD[47]
R25	MD[48]
T24	MD[49]
R23	MD[50]
R24	MD[51]
N23	MD[52]
P24	MD[53]
N24	MD[54]
L25	MD[55]
L26	MD[56]
K25	MD[57]
K26	MD[58]
K24	MD[59]
H25	MD[60]
J24	MD[61]
H23	MD[62]
H24	MD[63]
F24	PCI_CLKI
D25	PCI_CLKO
A20	AD[0]
C20	AD[1]
B19	AD[2]
A19	AD[3]
C19	AD[4]
B18	AD[5]
A18	AD[6]
B17	AD[7]
C18	AD[8]
A17	AD[9]
D17	AD[10]
B16	AD[11]
C17	AD[12]
B15	AD[13]
A15	AD[14]
C16	AD[15]
D15	AD[16]
A14	AD[17]
C15	AD[18]
B13	AD[19]
D13	AD[20]
A13	AD[21]
C14	AD[22]
C13	AD[23]
A12	AD[24]
B11	AD[25]
C12	AD[26]
A11	AD[27]
D12	AD[28]
B10	AD[29]
C11	AD[30]
A10	AD[31]
D10	CBE[0]
C10	CBE[1]
A9	CBE[2]
B8	CBE[3]
A8	FRAME#
B7	TRDY#
D8	IRDY#
A7	STOP#
C8	DEVSEL#
B6	PAR
D7	SERR#
A6	LOCK#
C21	PCI_REQ#[0]
A21	PCI_REQ#[1]
B20	PCI_REQ#[2]
C22	PCI_GNT#[0]

Pin #	Pin name
B21	PCI_GNT#[1]
D20	PCI_GNT#[2]
A5	PCI_INT[0]
C6	PCI_INT[1]
B4	PCI_INT[2]
D5	PCI_INT[3]
F2	LA[17]/DA[0]
G4	LA[18]/DA[1]
F3	LA[19]/DA[2]
F1	LA[20]/PCS1#
G2	LA[21]/PCS3#
G3	LA[22]/SCS1#
H2	LA[23]/SCS3#
J4	SA[0]
H1	SA[1]
H3	SA[2]
J2	SA[3]
J1	SA[4]
K2	SA[5]
J3	SA[6]
K1	SA[7]
K4	SA[8]/DD[0]
L2	SA[9]/DD[1]
K3	SA[10]/DD[2]
L1	SA[11]/DD[3]
M2	SA[12] / DD[4]
M1	SA[13] / DD[5]
L3	SA[14] / DD[6]
N2	SA[15] / DD[7]
M4	SA[16] / DD[8]
N1	SA[17] / DD[9]
M3	SA[18] / DD[10]
P4	SA[19] / DD[11]
P3	RTCDS# / DD[12]
R2	RTCRW# / DD[13]
N3	KBCS# / DD[14]
P1	RMRTCCS# / DD[15]
R1	SD[0]
T2	SD[1]
R3	SD[2]
T1	SD[3]
R4	SD[4]
U2	SD[5]
T3	SD[6]
U1	SD[7]
U4	SD[8]
V2	SD[9]
U3	SD[10]

Pin #	Pin name
V1	SD[11]
W2	SD[12]
W1	SD[13]
V3	SD[14]
Y2	SD[15]
Y1	IOCHRDY
AE4	SYSRSTO#
AD4	ISA_CLK
AE5	ISA_CLK2X
AF8	OSC14M
W3	ALE
AC9	ZWS#
AA2	BHE#
Y4	MEMR#
AA1	MEMW#
Y3	SMEMR#
AB2	SMEMW#
AA3	IOR#
AC2	IOW#
AB4	MASTER#
AC1	MCS16#
AB3	IOCS16#
AD2	REF#
AC3	AEN
AD1	IOCHCK#
AF2	ISAOE#
A4	RTCAS
AE3	GPIOCS#
B1	PIRQ
C2	SIRQ
C1	PDRQ
D2	SDRQ
D3	PDACK#
D1	SDACK#
E2	PIOR#
E4	PIOW#
E3	SIOR#
E1	SIOW#
E23	IRQ_MUX[0]
D26	IRQ_MUX[1]
E24	IRQ_MUX[2]
C25	IRQ_MUX[3]
A24	DREQ_MUX[0]
B23	DREQ_MUX[1]
C23	DACK_ENC[0]

Pin #	Pin name
A23	DACK_ENC[1]
B22	DACK_ENC[2]
D22	TC
C5	SPKRD
AE6	RED
AD6	GREEN
AF6	BLUE
AD5	VSYNC
AC5	HSYNC
AD7	VREF_DAC
AE8	RSET
AF5	COMP
C7	SDA / DDC[0]
B5	SCL / DDC[1]
AC12	VCLK
AE13	VIN[0]
AD14	VIN[1]
AD12	VIN[2]
AE14	VIN[3]
AC14	VIN[4]
AF14	VIN[5]
AD13	VIN[6]
AE15	VIN[7]
AF10	RED_TV
AC10	GREEN_TV
AF11	BLUE_TV
AE10	VCS
AD9	ODD_EVEN
AD11	CVBS
AD8	IREF1_TV
AE9	VREF1_TV
AE11	IREF2_TV
AD10	VREF2_TV
B3	SCAN_ENABLE
AF12	VDDA_TV
AC7	VDD_DAC1
AF4	VDD_DAC2
AD19	VDD_GCLK_PLL
AF13	VDD_DCLK_PLL
F26	VDD_HCLK_PLL
G24	VDD_DEVCLK_PLL
A16	VDD5
B12	VDD5
B9	VDD5

Pin #	Pin name
D18	VDD5
A22	VDD
B14	VDD
C9	VDD
D6	VDD
D11	VDD
D16	VDD
D21	VDD
F4	VDD
F23	VDD
G1	VDD
K23	VDD
L4	VDD
L23	VDD
P2	VDD
T4	VDD
T23	VDD
T26	VDD
W4	VDD
AA4	VDD
AA23	VDD
AB1	VDD
AB23	VDD
AC6	VDD
AC11	VDD
AC16	VDD
AC21	VDD
AE12	VSSA_TV
AE7	VSS_DAC1
AF7	VSS_DAC2
E25	VSS_DLL
E26	VSS_DLL
A1:2	VSS
A26	VSS
B2	VSS
B25:26	VSS
C3	VSS
C24	VSS
D4	VSS
D9	VSS
D14	VSS
D19	VSS
D23	VSS
H4	VSS
J23	VSS
L11:16	VSS
M11:16	VSS
N4	VSS

Pin #	Pin name
N11:16	VSS
P11:16	VSS
P23	VSS
R11:16	VSS
T11:16	VSS
V4	VSS
W23	VSS
AC4	VSS
AC8	VSS
AC13	VSS
AC18	VSS
AC23	VSS
AD3	VSS
AD24	VSS
AE1:2	VSS
AE16	VSS
AE25	VSS
AF1	VSS
AF25	VSS
AF26	VSS
C26	RESERVED
D24	RESERVED
B24	RESERVED
A25	RESERVED

3. STRAP OPTION

This chapter defines the STPC Consumer Strap Options and their location.

Memory Data Lines	Note	Designation	Location	Actual Settings	Set to '0'	Set to '1'
MD0	1		Index 4A, Bit 0	User defined	COLOR_SEL	SMEMW#
MD16		Reserved	Index 4C,bit 0	Pull up	-	-
MD17		PCI_CLKO Divisor	Index 4C,bit 1	User defined	HCLK / 2	HCLK / 3
MD18		Reserved	Index 4C,bit 2	Pull up	-	-
MD19		Reserved	Index 4C,bit 3	Pull up	-	-
MD20		Reserved	Index 4C, bit4	Pull up	-	-
MD21		Reserved	Index 5F, bit 0	Pull up	-	-
MD22		Reserved	Index 5F, bit 1	Pull up	-	-
MD23		Reserved	Index 5F,bit 2	Pull up	-	-
MD24		HCLK PLL Speed [26:24]	Index 5F,bit 3	User defined	see 3.1.4	
MD25			Index 5F,bit 4			
MD26			Index 5F,bit 5			
MD27		Reserved	-	Pull down	-	-
MD28		Reserved	-	Pull down	-	-
MD29		Reserved	-	Pull down	-	-
MD30		Reserved	-	Pull down	-	-
MD31		Reserved	-	Pull down	-	-
MD32		Reserved	-	Pull down	-	-
MD33		Reserved	-	Pull up	-	-
MD34		Reserved	-	Pull down	-	-
MD35		Reserved	-	Pull down	-	-
MD36		Reserved	-	Pull up	-	-
MD37		Reserved	-	Pull up	-	-
MD38		Reserved	-	Pull up	-	-
MD39		Reserved	-	Pull up	-	-
MD40		CPU Mode		User defined	DX1	DX2
MD41		Reserved	-	Pull down	-	-
MD42		Reserved	-	Pull up	-	-
MD43		Reserved	-	Pull down	-	-

Note 1: This Strap Option selects between two different functional blocks, the first is the ISA (SMEMW#) and the other is the VGA block (Color_Key).

3.1. STRAP REGISTER DESCRIPTION

3.1.1. STRAP REGISTER 0

This register reflect the status of pins MD[7:0] respectively. They are expected to be connected on the system board to the SIMM configuration pins as follows:

Strap0 Access = 0022h/0023h Regoffset = 04Ah

7	6	5	4	3	2	1	0
MD[7]	MD[6]	MD[5]	MD[4]	MD[3]	MD[2]	Rsv	
This register defaults to the values sampled on MD[7:0] pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-2	**MD[7:2]**	Available for user
Bits 1-0	**Rsv**	Reserved.

Note that the SIMM speed and type information read here is meant only for the software and is not used by the hardware. The software must program the Host and graphics DRAM controller configuration registers appropriately based on these bits.

3.1.2. STRAP REGISTER 1

This register reflect the status of pins MD[15:8] respectively. They are expected to be connected on the system board to the SIMM configuration pins as follows:

Strap1 Access = 0022h/0023h Regoffset = 04Bh

7	6	5	4	3	2	1	0
MD[15]	MD[14]	MD[13]	MD[12]	MD[11]	MD[10]	MD[9]	MD[8]
This register defaults to the values sampled on MD[15:8] pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-0	**MD[15:8]**	Available for user

Note that the SIMM speed and type information read here is meant only for the software and is not used by the hardware. The software must program the Host and graphics dram controller configuration registers appropriately based on these bits.

3.1.3. STRAP REGISTER 2

Bits 4-0 of this register reflect the status of pins MD[20:16] respectively. Bit 5 of this register reflect the status of pin MD[23]. Bit 4 is writeable, writes to other bits in this register have no effect.

Strap2 Access = 0022h/0023h Regoffset = 04Ch

7	6	5	4	3	2	1	0
Rsv						MD[17]	Rsv
This register defaults to the values sampled on MD[23] and MD[20:16] pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-2	**Rsv**	Reserved
Bit 1		This bit reflects the **value sampled on MD[17] pin** and controls the PCI clock output as follows: Setting to '0', the PCI clock output = HCLK / 2, Setting to '1', the PCI clock output = HCLK / 3.
Bit 0	**Rsv**	Reserved.

3.1.4. HCLK PLL STRAP REGISTER 0

Bits 5-0 of this register reflect the status of pins MD[26:21] respectively. They are use by the chip as follows:

HCLK_STRAP0 Access = 0022h/0023h Regoffset = 05Fh

7	6	5	4	3	2	1	0
Rsv		MD[26]	MD[25]	MD[24]	Rsv		
This register defaults to the values sampled on pins described below after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-6	**Rsv**	Reserved
Bits 5-3	**MD[26:24]**	These pins reflect the **value sampled on MD[26:24] pins** respectively and control the Host clock frequency synthesizer. 000: 25 MHz 001: 33 MHz 010: 40 MHz 011: 50 MHz 100: 60 MHz 101: 66 MHz 110: 75 MHz 111: 80 MHz
Bits 2-0	**Rsv**	Reserved.

Programming notes:

Strap Options [39:27] are reserved.

3.1.5. 486 CLOCK PROGRAMMING (486_CLK)

The bit MD[40] is used to set the clock multiplication factor of the 486 core. With the MD[40] pin pulled low the 486 will run in DX (x1) mode, while with the MD[40] pin pulled high the 486 will run in DX2 (x2) mode. The default value of the resistor on this strap input should be a resister to ground (DX mode).

Strap options MD[43:41] are reserved.

4. ELECTRICAL SPECIFICATIONS

4.1 Introduction

The electrical specifications in this chapter are valid for the STPC Consumer.

4.2 Electrical Connections

4.2.1 Power/Ground Connections/Decoupling

Due to the high frequency of operation of the STPC Consumer, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the STPC Consumer and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

4.2.2 Unused Input Pins

All inputs not used by the designer and not listed in the table of pin connections in Chapter 3 should be connected either to VDD or to VSS. Connect active-high inputs to VDD through a 20 kΩ (±10%) pull-down resistor and active-low inputs to VSS and connect active-low inputs to VCC through a 20 kΩ (±10%) pull-up resistor to prevent spurious operation.

4.2.3 Reserved Designated Pins

Pins designated reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.3 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the STPC Consumer device. Stresses beyond those listed under Table 4-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section "Operating Conditions".

Exposure to conditions beyond Table 4-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-1) may also result in reduced useful life and reliability.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DDx}	DC Supply Voltage	-0.3, 4.0	V
V_I, V_O	Digital Input and Output Voltage	-0.3, VDD + 0.3	V
T_{STG}	Storage Temperature	-40, +150	°C
T_{OPER}	Operating Temperature	0, +70	°C
P_{TOT}	Total Power Dissipation of the package	4.8	W

4.4 DC Characteristics

Table 4-2. DC Characteristics

Recommended Operating conditions : VDD = 3.3V ±0.3V, Tcase = 0 to 100°C unless otherwise specified

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
P_{DD}	Supply Power	V_{DD} = 3.3V, H_{CLK} = 66Mhz		3.2	3.9	W
V_{REF_DAC}	DAC Voltage Reference		1.215	1.235	1.255	V
V_{OL}	Output Low Voltage	I_{Load} =1.5 to 8mA depending of the pin			0.5	V
V_{OH}	Output High Voltage	I_{Load} =-0.5 to -8mA depending of the pin	2.4			V
V_{IL}	Input Low Voltage	Except XTALI	-0.3		0.8	V
		XTALI	-0.3		0.9	V
V_{IH}	Input High Voltage	Except XTALI	2.1		V_{DD}+0.3	V
		XTALI	2.35		V_{DD}+0.3	V
I_{LK}	Input Leakage Current	Input, I/O	-5		5	µA

4.5 AC Characteristics

Table 4-4 through Table 4-9 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 . The rising clock edge reference level VREF , and other reference levels are shown in Table 4-3 below for the STPC Consumer. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-3. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	3.0	V
V_{ILD}	0.0	V

Note: Refer to Figure 4-1.

Figure 4-1 Drive Level and Measurement Points for Switching Characteristics

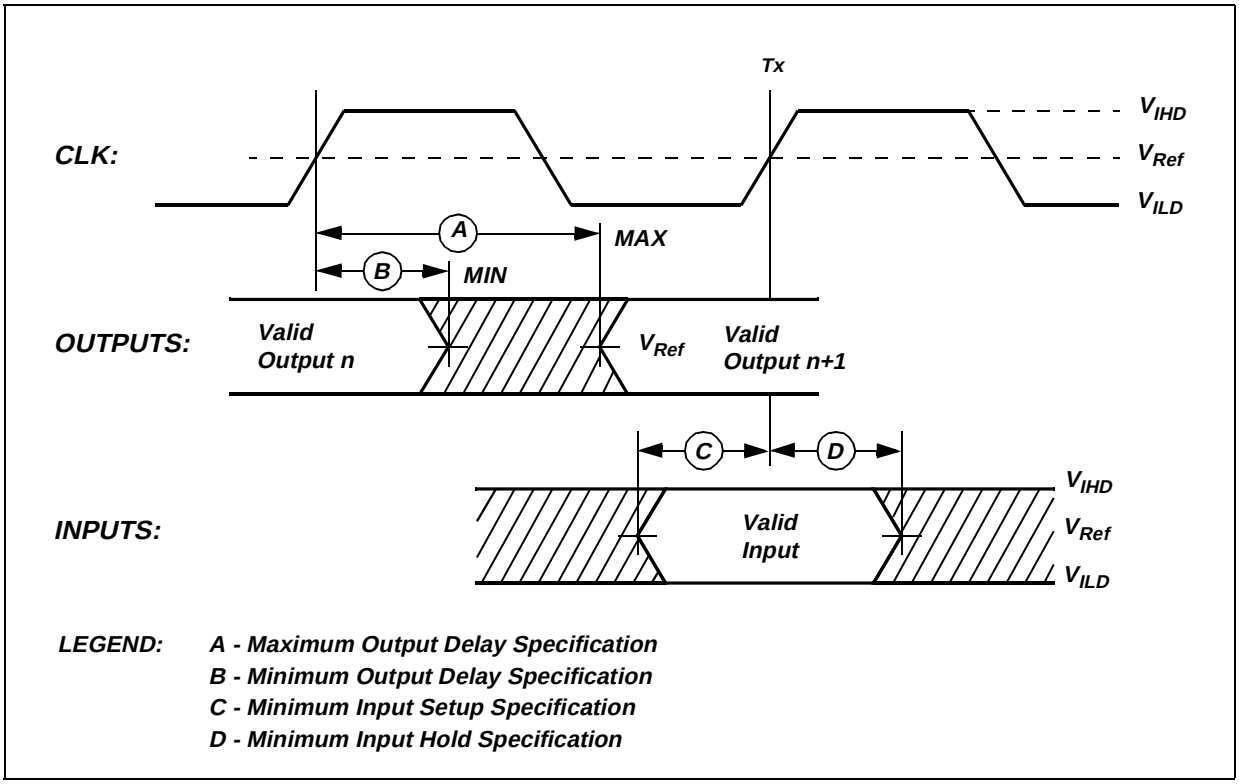
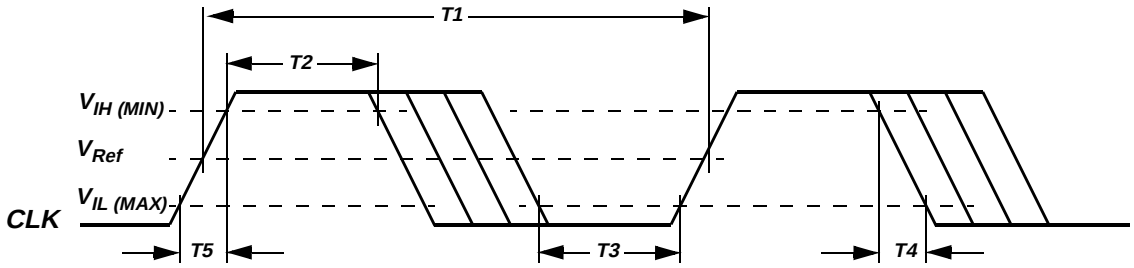


Figure 4-2 CLK Timing Measurement Points



LEGEND:

T1 - One Clock Cycle
T2 - Minimum Time at V_{IH}
T3 - Minimum Time at V_{IL}
T4 - Clock Fall Time
T5 - Clock Rise Time

NOTE; All sIgnals are sampled on the rising edge of the CLK.

Note; The above timings are generic timings and are not specific to the interfaces defined below

4.5.1 Power on sequence

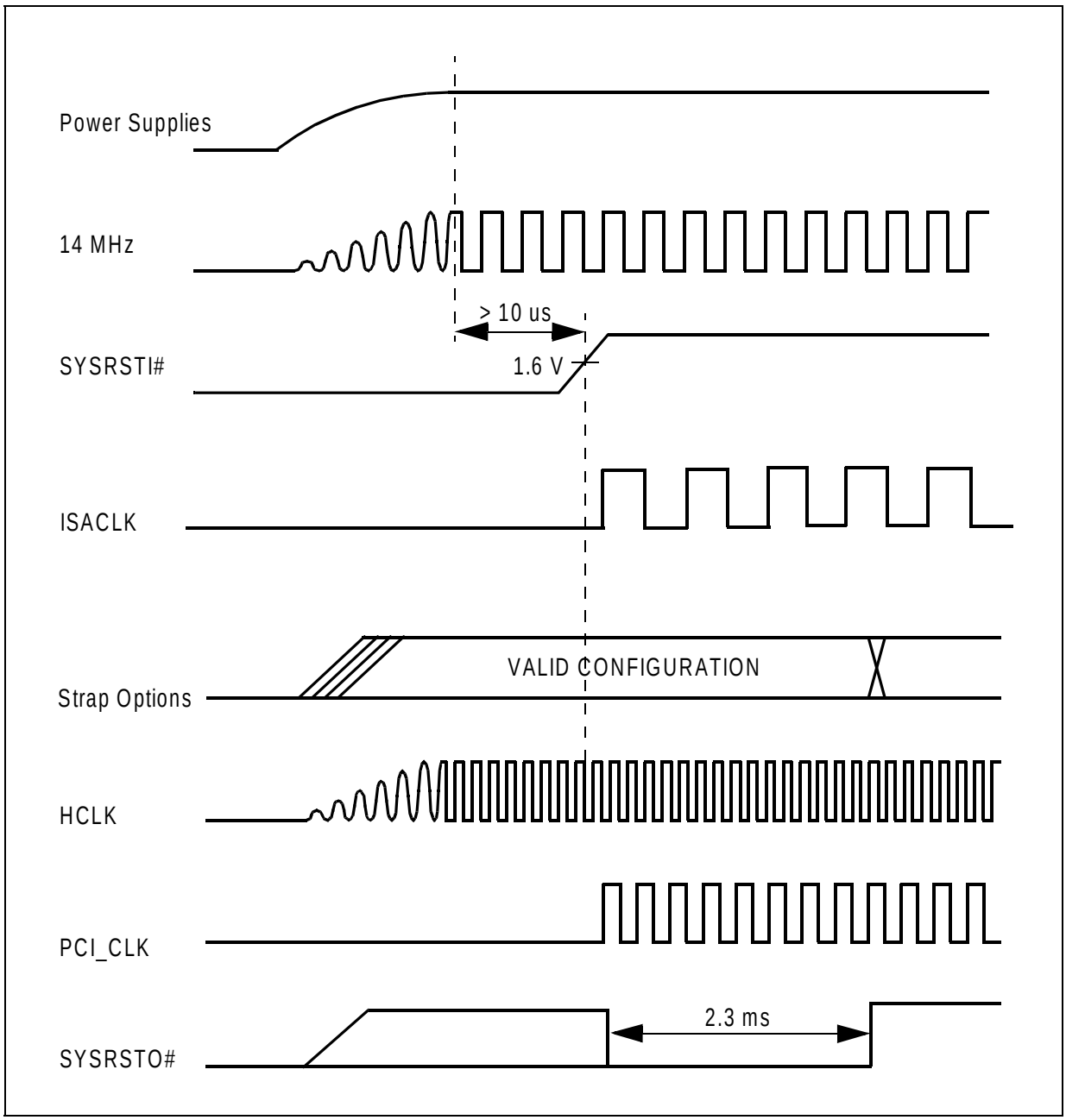
Figure 4-3 describes the power-on sequence of the STPC, also called cold reset.

There is no constraint on the rising edge of SYSRSTI#. It just needs to stay low at least 10µs after power supply is stable to let the STPC PLLs stabilize.

Strap Options are continuously sampled during SYSRSTI# low and must remain stable. Once SYSRSTI# is high, they MUST NOT CHANGE until SYSRSTO# goes high.

Bus activity starts only few clock cycles after the release of SYSRSTO#. The toggling signals depend on the STPC configuration.
In ISA mode, activity is visible on PCI prior to the ISA bus as the controller is part of the south bridge (CPC).
In Local Bus mode, the PCI bus is not accessed and the Flash Chip Select is the control signal to monitor.

Figure 4-3. Power-on timing diagram



4.5.2 RESET sequence

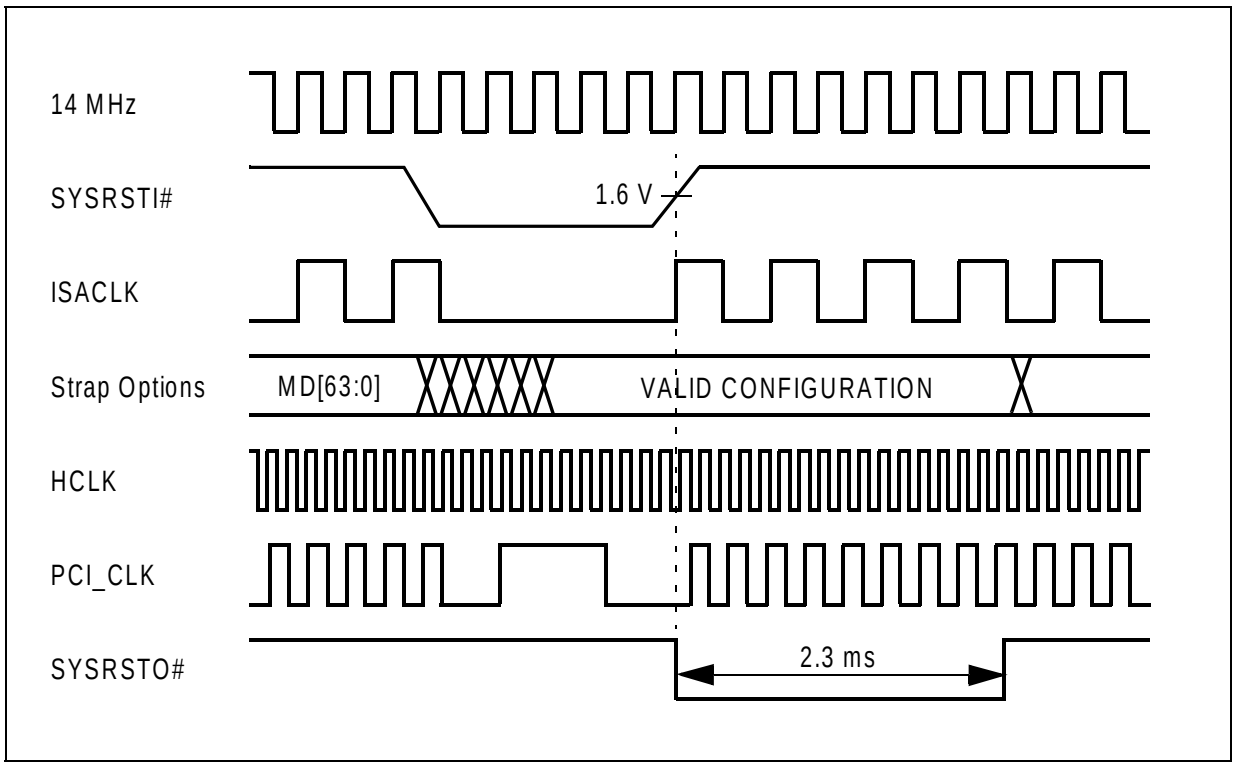
Figure 4-4 describes the reset sequence of the STPC, also called warm reset.

The constraints on the strap options and the bus activities are the same as for the cold reset.

It is mandatory to have a clean reset pulse without glitches as the STPC could then sample invalid strap option setting and enter into an unpredictable mode.

While SYSRSTI# is active, the PCI clock PLL runs in open loop mode at a speed of few 100's KHz.

Figure 4-4. Reset timing diagram



4.5.3 DRAM CONTROLLER AC TIMING CHARCTERISTICS

Figure 4-5 Read Mode (ref table Table 4-4)

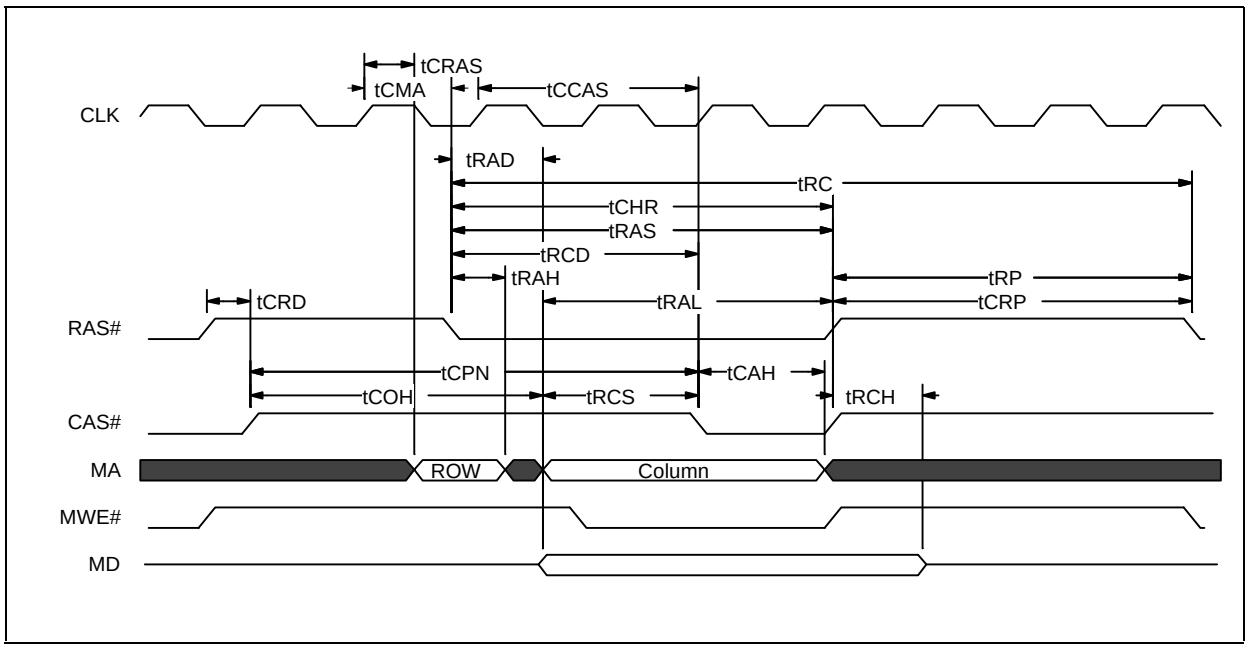


Figure 4-6 Memory Early Write Mode (ref table Table 4-4)

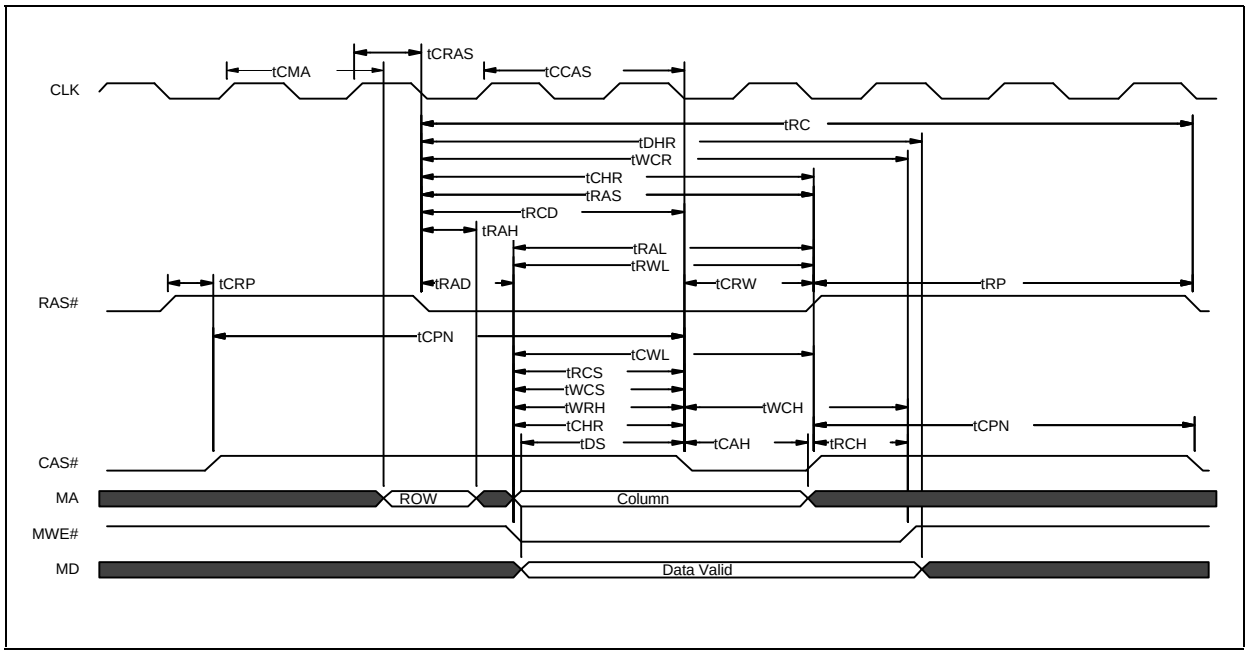


Figure 4-7 EDO Read Mode (ref table Table 4-4)

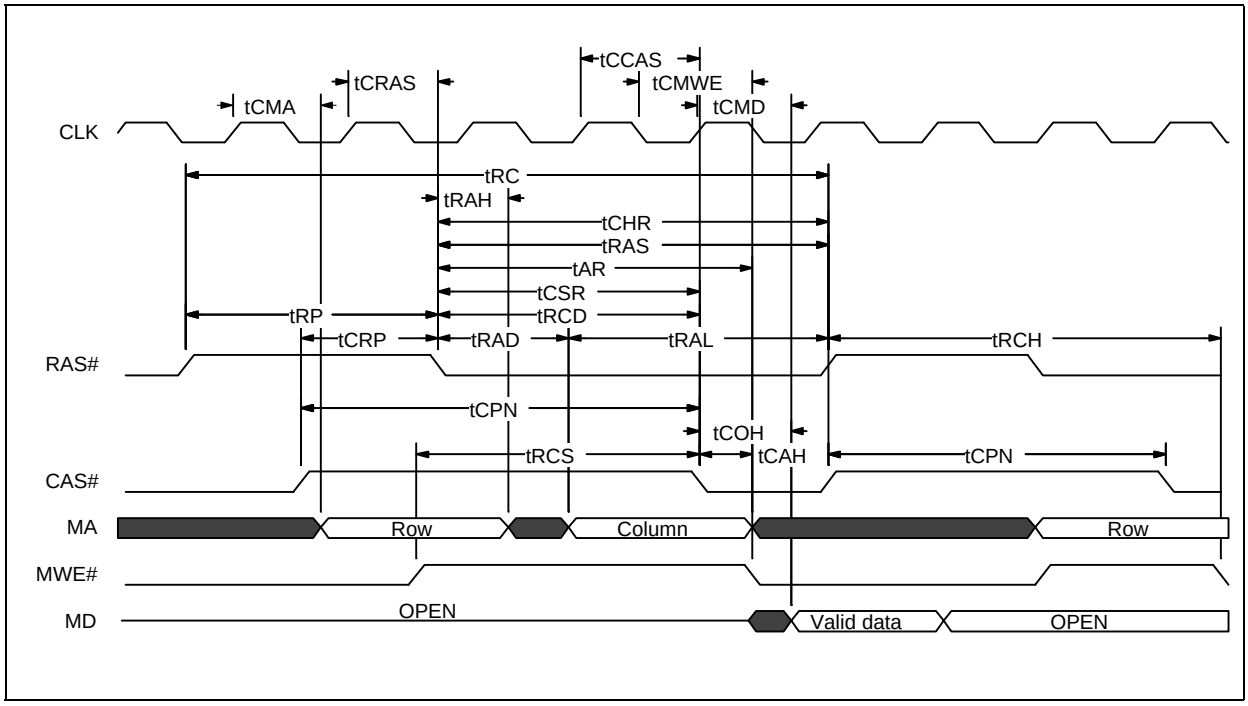


Figure 4-8 EDO Write Mode (ref table Table 4-4)

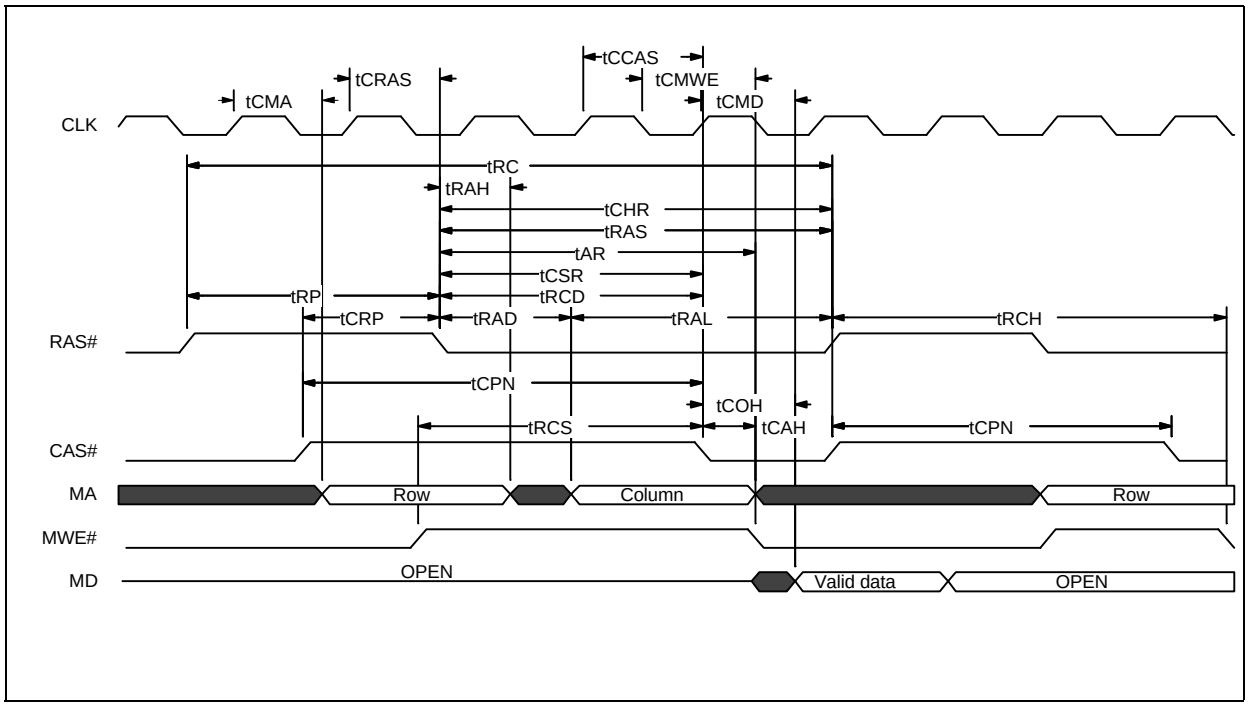


Figure 4-9 Fast Page Mode Read (ref table Table 4-4)

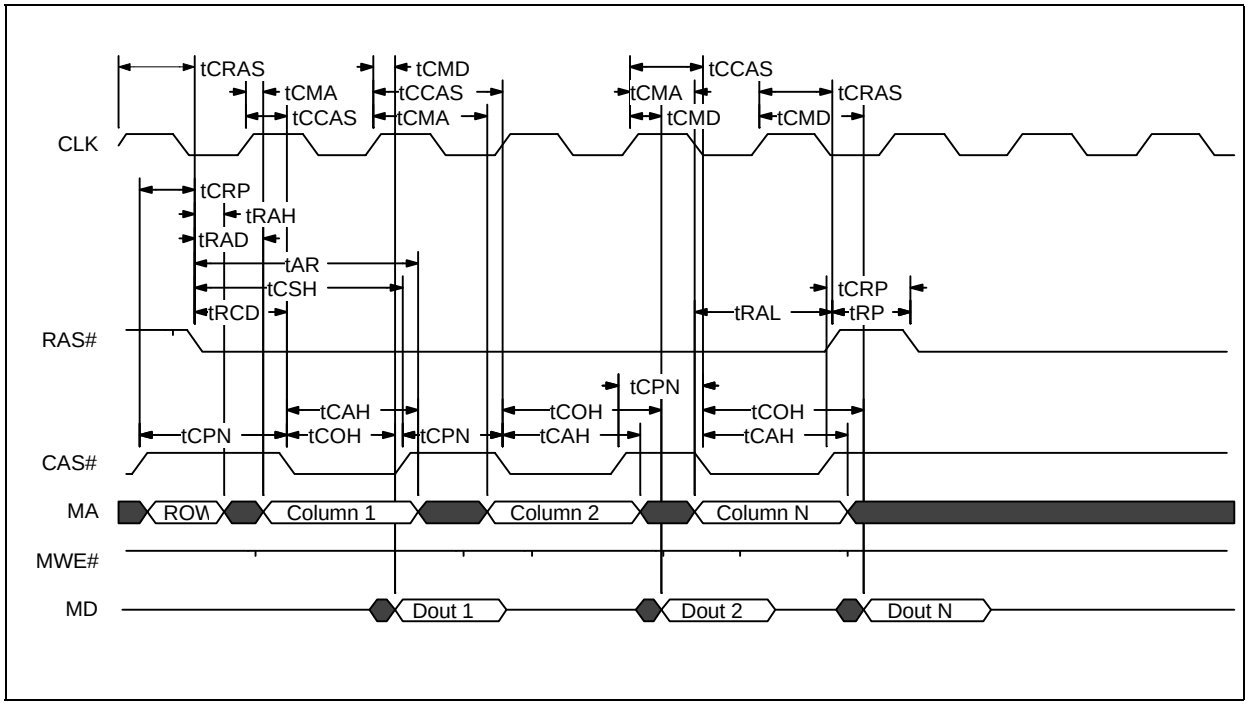


Figure 4-10 Fast Page Mode Write (ref table Table 4-4)

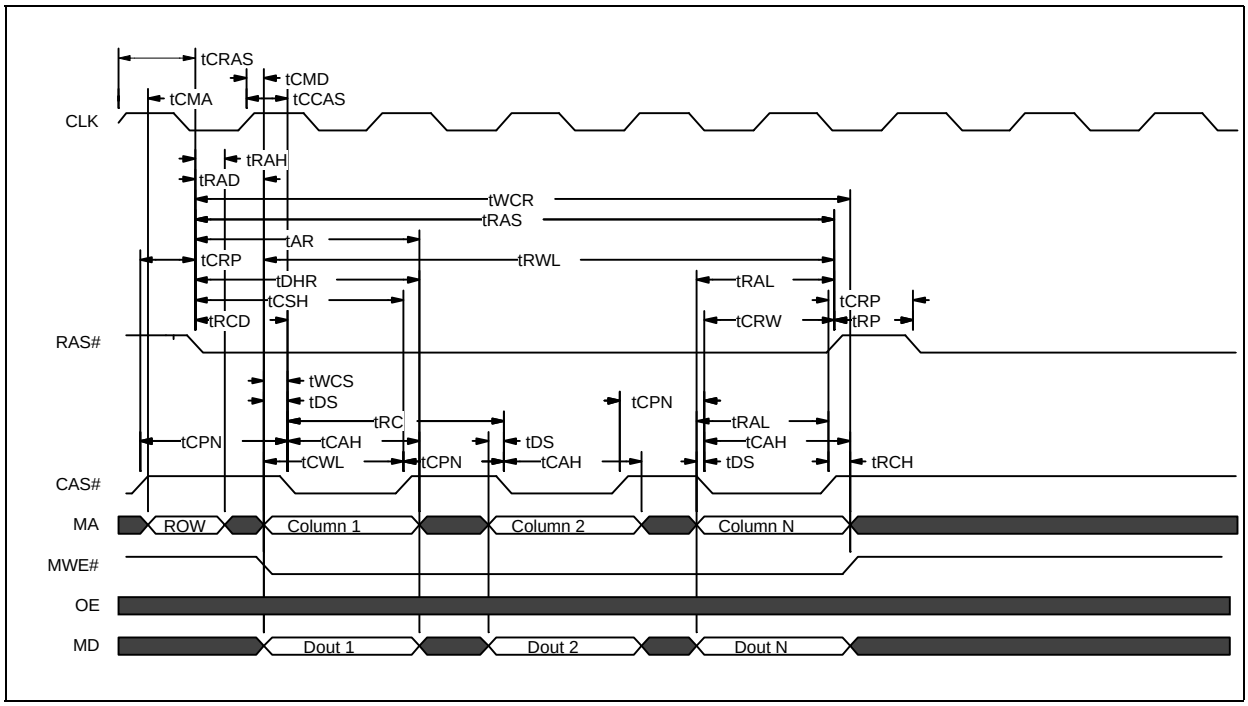


Figure 4-11 Refresh Cycle (ref table Table 4-4)

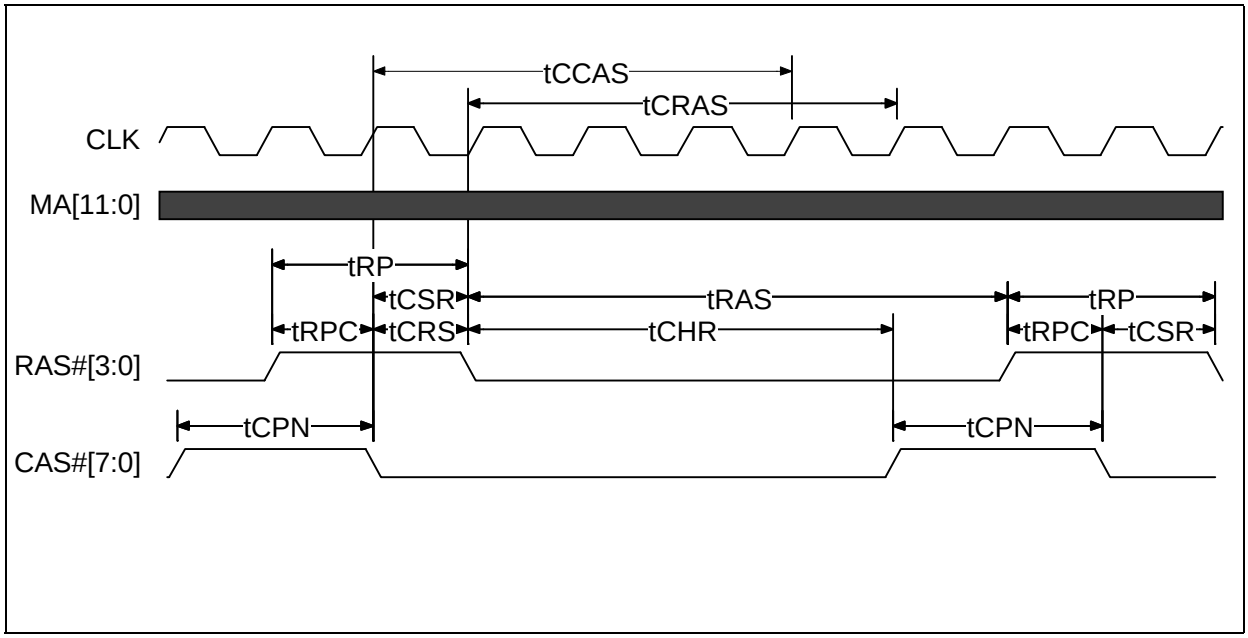


Table 4-4. AC Memory Timing Characteristics

	Parameter	Min	Max	Units
tCRAS	HCLK (or GCLK2X) to RAS#[3:0] valid (see Note 3)		17	ns
tCCAS	HCLK (or GCLK2X) to CAS#[7:0] bus valid (see Note 3)		17	ns
tCMA	HCLK (or GCLK2X) to MA[11:0] bus valid (see Note 3)		17	ns
tCMWE	HCLK (or GCLK2X) to MWE# valid (see Note 3)		17	ns
tCMD	HCLK to MD[63:0] bus valid (see Note 3)		25	ns
tGCMD	GCLK2X to MD[63:0] bus valid (see Note 3)		23	ns
tMDG	MD[63:0] Generic hold	0		ns
tCAH	Column Address Hold Time	$\geq 1T_{Cycles}$		ns
tCHR	CAS Hold Time	$\geq 1T_{Cycles}$		ns
tCOH	Data Hold TIme from CAS Low	Note 1		ns
tCPN	CAS Precharge Time	$1T_{Cycles}$		ns
tCRP	CAS to RAS Precharge Time		$\leq 1T_{Cycles}$	
tCRW	CAS Low to RAS HIGH (Write only)	$\geq 1T_{Cycles}$		ns
tCSR	CAS Setup Time	$\geq 1T_{Cycles}$		ns
tDS	Data In Setup Time	$\geq 1T_{Cycles}$		ns
tRAH	Row Address Hold Time	$\geq 1T_{Cycles}$		ns
tRAS	RAS Pulse Width	$\geq 3T_{Cycles}$		ns
tRC	Random Read or Write Time Cycle	$\geq 6T_{Cycles}$		ns
tRCD	RAS to CAS Delay Time	$\geq 1T_{Cycles}$		ns
tRCH	Read Command Hold Time	$\geq 1T_{Cycles}$		ns
tRCS	Read Command Setup Time	$\geq 1T_{Cycles}$		ns
tRP	RAS Precharge Time	$\geq 2T_{Cycles}$		ns
tWCH	Write Command Hold Time	$\geq 1T_{Cycles}$		ns
tWCS	WE Command Setup Time	$\geq 1T_{Cycles}$		ns
tWRH	WE Hold Time	Note 2		ns
tWRP	WE Setup Time	$\geq 1T_{Cycles}$		ns
tAR	Column Address Hold Time from RAS	$\geq 1T_{Cycles}$		ns
tRAD	RAS to valid Column Address Delay	$\geq 1T_{Cycles}$		ns
tRAL	Column Address to RAS Setup Time	$\geq 2T_{Cycles}$		ns
tWCR	Write Command Hold Reference to RAS	$\geq 1T_{Cycles}$		ns
tRWL	Write Command to RAS Setup Time (Note 2)	$\geq 1T_{Cycles}$		ns
tCWL	Write Command to CAS Setup Time (Note 2)	$\geq 1T_{Cycles}$		ns
tDHR	Data Hold Reference to RAS	$\geq 3T_{Cycles}$		ns
tRPC	RAS High to CAS Low Precharge	$\geq 1T_{Cycles}$		ns
tCRS	CAS Before RAS Setup Time	$\geq 1T_{Cycles}$		ns
tCHR	CAS Before RAS Hold Time	$\geq 1T_{Cycles}$		ns
tCSH	CAS Hold Time after RAS	$\geq 1T_{Cycles}$		ns

Note 1; $T_{Cycle} \times n_{CAS} + (t_{Data\ off} - t_{CAS\ out})$

Where T_{Cycle} is the the number of clock cycles.

n_{CAS} is the number of CAS Cycles (see section 6.7.)

$T_{Dataoff}$ is the Generic Datahold

$t_{CAS\ Out}$ the CLK (either HCLK or GCLK2X) to CAS Low.

$T_{Dataoff}$ and $t_{CAS\ Out}$ are used to refine the timing programming.

Note 2; Value to be derived from CAS pulse width which is programmable (see section 6.7.).

Note 3; for all chronograms, CLK refers to the clock signal that the program is using. It can be either HCLK or GCLK2X

4.5.4 PCI interface

Table 4-5 lists the AC characteristics of the PCI interface.

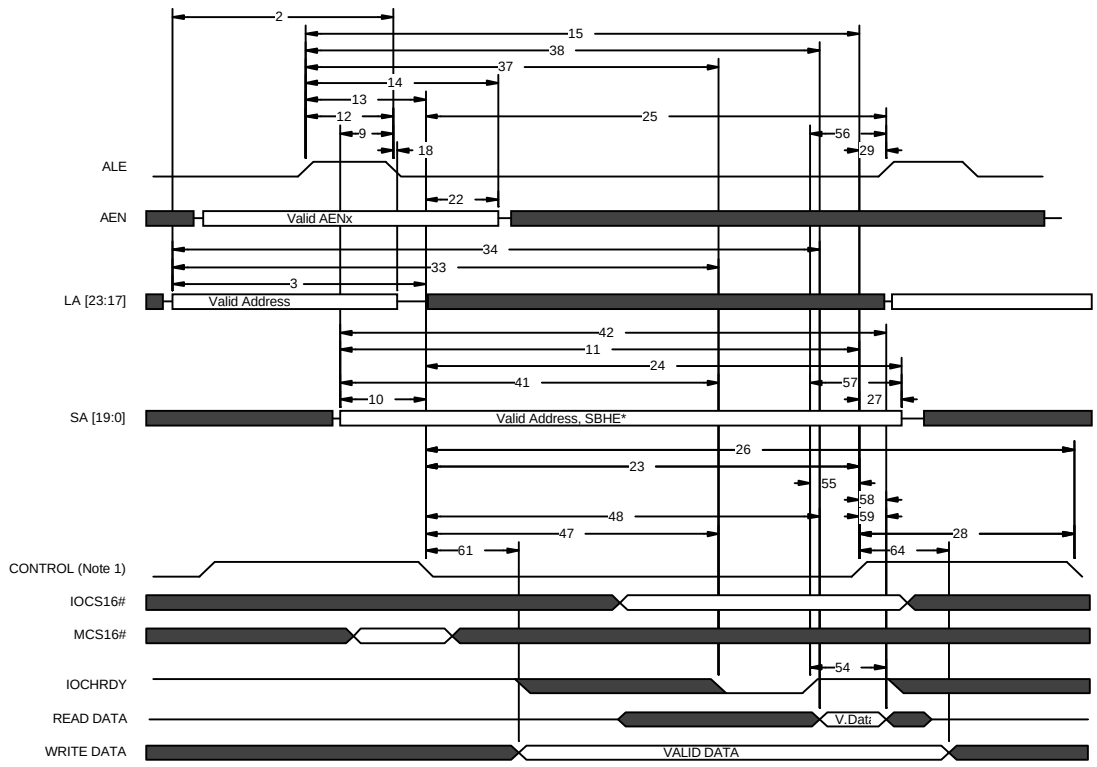
Table 4-5. PCI Bus AC Timing

Name	Parameter	Min	Max	Unit
t1	PCI_CLKI to AD[31:0] valid	2	11	ns
t2	PCI_CLKI to FRAME# valid	2	11	ns
t3	PCI_CLKI to CBE#[3:0] valid	2	11	ns
t4	PCI_CLKI to PAR valid	2	11	ns
t5	PCI_CLKI to TRDY# valid	2	11	ns
T6	PCI_CLKI to IRDY# valid	2	11	ns
T7	PCI_CLKI to STOP# valid	2	11	ns
T8	PCI_CLKI to DEVSEL# valid	2	11	ns
T9	PCI_CLKI to PCI_GNT# valid	2	12	ns
t10	AD[31:0] bus setup to PCI_CLKI	5		ns
t11	AD[31:0] bus hold from PCI_CLKI	0		ns
t12	PCI_REQ#[2:0] setup to PCI_CLKI	4		ns
t13	PCI_REQ#[2:0] hold from PCI_CLKI	4		ns
t14	CBE#[3:0] setup to PCI_CLKI	5		ns
t15	CBE#[3:0] hold to PCI_CLKI	0		ns
t16	IRDY# setup to PCI_CLKI	5		ns
t17	IRDY# hold to PCI_CLKI	0		ns
t18	FRAME# setup to PCI_CLKI	5		ns
t19	FRAME# hold from PCI_CLKI	0		ns

4.5.5 Isa interface AC Timing characteristics

Table 4-12 and Table 4-6 list the AC characteristics of the ISA interface.

Figure 4-12 ISA Cycle (ref Table 4-6)



Note 1: Stands for SMEMR#, SMEMW#, MEMR#, MEMW#, IOR# & IOW#.
The clock has not been represented as it is dependent on the ISA Slave mode.

Table 4-6. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
2	LA[23:17] valid before ALE# negated	5T		Cycles
3	**LA[23:17] valid before MEMR#, MEMW# asserted**			
3a	Memory access to 16-bit ISA Slave	5T		Cycles
3b	Memory access to 8-bit ISA Slave	5T		Cycles
9	SA[19:0] & SBHE valid before ALE# negated	1T		Cycles
10	**SA[19:0] & SBHE valid before MEMR#, MEMW# asserted**			
10a	Memory access to 16-bit ISA Slave	2T		Cycles
10b	Memory access to 8-bit ISA Slave	2T		Cycles
10	**SA[19:0] & SHBE valid before SMEMR#, SMEMW# asserted**			
Note: The signal numbering refers to Table 4-12				

Table 4-6. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	10c	Memory access to 16-bit ISA Slave	2T		Cycle
	10d	Memory access to 8-bit ISA Slave	2T		Cycle
10e	SA[19:0] & SBHE valid before IOR#, IOW# asserted		2T		Cycles
11	**ISACLK2X to IOW# valid**				
	11a	Memory access to 16-bit ISA Slave - 2BCLK	2T		Cycles
	11b	Memory access to 16-bit ISA Slave - Standard 3BCLK	2T		Cycles
	11c	Memory access to 16-bit ISA Slave - 4BCLK	2T		Cycles
	11d	Memory access to 8-bit ISA Slave - 2BCLK	2T		Cycles
11e		Memory access to 8-bit ISA Slave - Standard 3BCLK	2T		Cycles
12	ALE# asserted before ALE# negated		1T		Cycles
13	**ALE# asserted before MEMR#, MEMW# asserted**				
	13a	Memory Access to 16-bit ISA Slave	2T		Cycles
	13b	Memory Access to 8-bit ISA Slave	2T		Cycles
13	**ALE# asserted before SMEMR#, SMEMW# asserted**				
	13c	Memory Access to 16-bit ISA Slave	2T		Cycles
	13d	Memory Access to 8-bit ISA Slave	2T		Cycles
13e	ALE# asserted before IOR#, IOW# asserted		2T		Cycles
14	**ALE# asserted before AL[23:17]**				
	14a	Non compressed	15T		Cycles
	14b	Compressed	15T		Cycles
15	**ALE# asserted before MEMR#, MEMW#, SMEMR#, SMEMW# negated**				
	15a	Memory Access to 16-bit ISA Slave- 4 BCLK	11T		Cycles
	15e	Memory Access to 8-bit ISA Slave- Standard Cycle	11T		Cycles
18a	ALE# negated before LA[23:17] invalid (non compressed)		14T		Cycles
18a	ALE# negated before LA[23:17] invalid (compressed)		14T		Cycles
22	**MEMR#, MEMW# asserted before LA[23:17]**				
	22a	Memory access to 16-bit ISA Slave.	13T		Cycles
	22b	Memory access to 8-bit ISA Slave.	13T		Cycles
23	**MEMR#, MEMW# asserted before MEMR#, MEMW# negated**				
	23b	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
	23e	Memory access to 8-bit ISA Slave Standard cycle	9T		Cycles
23	**SMEMR#, SMEMW# asserted before SMEMR#, SMEMW# negated**				
	23h	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
	23l	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
23	**IOR#, IOW# asserted before IOR#, IOW# negated**				
	23o	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
	23r	Memory access to 8-bit ISA Slave Standard cycle	9T		Cycles
24	**MEMR#, MEMW# asserted before SA[19:0]**				
	24b	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	24d	Memory access to 8-bit ISA Slave - 3BLCK	10T		Cycles
	24e	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
	24f	Memory access to 8-bit ISA Slave - 7BCLK	10T		Cycles
24	**SMEMR#, SMEMW# asserted before SA[19:0]**				
	24h	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	24i	Memory access to 16-bit ISA Slave - 4BCLK	10T		Cycles
	24k	Memory access to 8-bit ISA Slave - 3BCLK	10T		Cycles
Note: The signal numbering refers to Table 4-12					

Table 4-6. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	24l	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
24	**IOR#, IOW# asserted before SA[19:0]**				
	24o	I/O access to 16-bit ISA Slave Standard cycle	19T		Cycles
	24r	I/O access to 16-bit ISA Slave Standard cycle	19T		Cycles
25	**MEMR#, MEMW# asserted before next ALE# asserted**				
	25b	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25d	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
25	**SMEMR#, SMEMW# asserted before next ALE# asserted**				
	25e	Memory access to 16-bit ISA Slave - 2BCLK	10T		Cycles
	25f	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25h	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
25	**IOR#, IOW# asserted before next ALE# asserted**				
	25i	I/O access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25k	I/O access to 16-bit ISA Slave Standard cycle	10T		Cycles
26	**MEMR#, MEMW# asserted before next MEMR#, MEMW# asserted**				
	26b	Memory access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26d	Memory access to 8-bit ISA Slave Standard cycle	12T		Cycles
26	**SMEMR#, SMEMW# asserted before next SMEMR#, SMEMW# asserted**				
	26f	Memory access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26h	Memory access to 8-bit ISA Slave Standard cycle	12T		Cycles
26	**IOR#, IOW# asserted before next IOR#, IOW# asserted**				
	26i	I/O access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26k	I/O access to 8-bit ISA Slave Standard cycle	12T		Cycles
28	**Any command negated to MEMR#, SMEMR#, MEMR#, SMEMW# asserted**				
	28a	Memory access to 16-bit ISA Slave	3T		Cycles
	28b	Memory access to 8-bit ISA Slave	3T		Cycles
28	**Any command negated to IOR#, IOW# asserted**				
	28c	I/O access to ISA Slave	3T		Cycles
29a	MEMR#, MEMW# negated before next ALE# asserted		1T		Cycles
29b	SMEMR#, SMEMW# negated before next ALE# asserted		1T		Cycles
29c	IOR#, IOW# negated before next ALE# asserted		1T		Cycles
33	**LA[23:17] valid to IOCHRDY negated**				
	33a	Memory access to 16-bit ISA Slave - 4 BCLK	8T		Cycles
	33b	Memory access to 8-bit ISA Slave - 7 BCLK	14T		Cycles
34	**LA[23:17] valid to read data valid**				
	34b	Memory access to 16-bit ISA Slave Standard cycle	8T		Cycles
	34e	Memory access to 8-bit ISA Slave Standard cycle	14T		Cycles
37	**ALE# asserted to IOCHRDY# negated**				
	37a	Memory access to 16-bit ISA Slave - 4 BCLK	6T		Cycles
	37b	Memory access to 8-bit ISA Slave - 7 BCLK	12T		Cycles
	37c	I/O access to 16-bit ISA Slave - 4 BCLK	6T		Cycles
	37d	I/O access to 8-bit ISA Slave - 7 BCLK	12T		Cycles
38	**ALE# asserted to read data valid**				
	38b	Memory access to 16-bit ISA Slave Standard Cycle	4T		Cycles
	38e	Memory access to 8-bit ISA Slave Standard Cycle	10T		Cycles
	38h	I/O access to 16-bit ISA Slave Standard Cycle	4T		Cycles
Note: The signal numbering refers to Table 4-12					

Table 4-6. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	38l	I/O access to 8-bit ISA Slave Standard Cycle	10T		Cycles
41	**SA[19:0] SBHE valid to IOCHRDY negated**				
	41a	Memory access to 16-bit ISA Slave	6T		Cycles
	41b	Memory access to 8-bit ISA Slave	12T		Cycles
	41c	I/O access to 16-bit ISA Slave	6T		Cycles
	41d	I/O access to 8-bit ISA Slave	12T		Cycles
42	**SA[19:0] SBHE valid to read data valid**				
	42b	Memory access to 16-bit ISA Slave Standard cycle	4T		Cycles
	42e	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
	42h	I/O access to 16-bit ISA Slave Standard cycle	4T		Cycles
	42l	I/O access to 8-bit ISA Slave Standard cycle	10T		Cycles
47	**MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# asserted to IOCHRDY negated**				
	47a	Memory access to 16-bit ISA Slave	2T		Cycles
	47b	Memory access to 8-bit ISA Slave	5T		Cycles
	47c	I/O access to 16-bit ISA Slave	2T		Cycles
	47d	I/O access to 8-bit ISA Slave	5T		Cycles
48	**MEMR#, SMEMR#, IOR# asserted to read data valid**				
	48b	Memory access to 16-bit ISA Slave Standard Cycle	2T		Cycles
	48e	Memory access to 8-bit ISA Slave Standard Cycle	5T		Cycles
	48h	I/O access to 16-bit ISA Slave Standard Cycle	2T		Cycles
	48l	I/O access to 8-bit ISA Slave Standard Cycle	5T		Cycles
54	**IOCHRDY asserted to read data valid**				
	54a	Memory access to 16-bit ISA Slave	1T(R)/2T(W)		Cycles
	54b	Memory access to 8-bit ISA Slave	1T(R)/2T(W)		Cycles
	54c	I/O access to 16-bit ISA Slave	1T(R)/2T(W)		Cycles
	54d	I/O access to 8-bit ISA Slave	1T(R)/2T(W)		Cycles
55a	IOCHRDY asserted to MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# negated		1T		Cycles
55b	IOCHRY asserted to MEMR#, SMEMR# negated (refresh)		1T		Cycles
56	IOCHRDY asserted to next ALE# asserted		2T		Cycles
57	IOCHRDY asserted to SA[19:0], SBHE invalid		2T		Cycles
58	MEMR#, IOR#, SMEMR# negated to read data invalid		0T		Cycles
59	MEMR#, IOR#, SMEMR# negated to data bus float		0T		Cycles
61	**Write data before MEMW# asserted**				
	61a	Memory access to 16-bit ISA Slave	2T		Cycles
	61b	Memory access to 8-bit ISA Slave (Byte copy at end of start)	2T		Cycles
61	**Write data before SMEMW# asserted**				
	61c	Memory access to 16-bit ISA Slave	2T		Cycles
	61d	Memory access to 8-bit ISA Slave	2T		Cycles
61	**Write Data valid before IOW# asserted**				
	61e	I/O access to 16-bit ISA Slave	2T		Cycles
	61f	I/O access to 8-bit ISA Slave	2T		Cycles
64a	MEMW# negated to write data invalid - 16-bit		1T		Cycles
64b	MEMW# negated to write data invalid - 8-bit		1T		Cycles
64c	SMEMW# negated to write data invalid - 16-bit		1T		Cycles
Note: The signal numbering refers to Table 4-12					

Table 4-6. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
64d	SMEMW# negated to write data invalid - 8-bit	1T		Cycles
64e	IOW# negated to write data invalid	1T		Cycles
64f	MEMW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master	1T		Cycles
64g	IOW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master	1T		Cycles
Note: The signal numbering refers to Table 4-12				

4.5.6 IDE INTERFACE

Table 4-7 lists the AC characteristics of the IDE interface.

Table 4-7. IDE Bus AC Timing

Name	Parameter	Min	Max	Unit
	DD[15:0] setup to PIOR#/SIOR# falling	15		ns
	DD[15:0} hold to PIOR#/SIOR# falling	0		ns

4.5.7 VGA INTERFACE

Table 4-8 lists the AC characteristics of the VGA interface.

Table 4-8. Graphics Adapter (VGA) AC Timing

Name	Parameter	Min	Max	Unit
	DCLK to VSYNC valid		30	ns
	DCLK to HSYNC valid		30	ns

4.5.8 VIDEO INPUT PORT

Table 4-9 lists the AC characteristics of the VIP interface.

Table 4-9. Video Input AC Timing

Name	Parameter	Min	Max	Unit
	VIN[7:0] setup to VCLK	5		ns
	VIN[7:0] hold from VCLK	4		ns
	VCLK to ODD_EVEN valid		15	ns
	VCLK to VCS valid		15	ns
	ODD_EVEN setup to VCLK	10		ns
	ODD_EVEN hold from VCLK	5		ns
	VCS setup to VCLK	10		ns
	VCS hold from VCLK	5		ns

5. MECHANICAL DATA

5.1. 388-PIN PACKAGE DIMENSION

The pin numbering for the STPC 388-pin Plastic BGA package is shown in Figure 5-1.

Dimensions are shown in Figure 5-2, Table 5-1 and Figure 5-3, Table 5-2.

Figure 5-1. 388-Pin PBGA Package - Top View

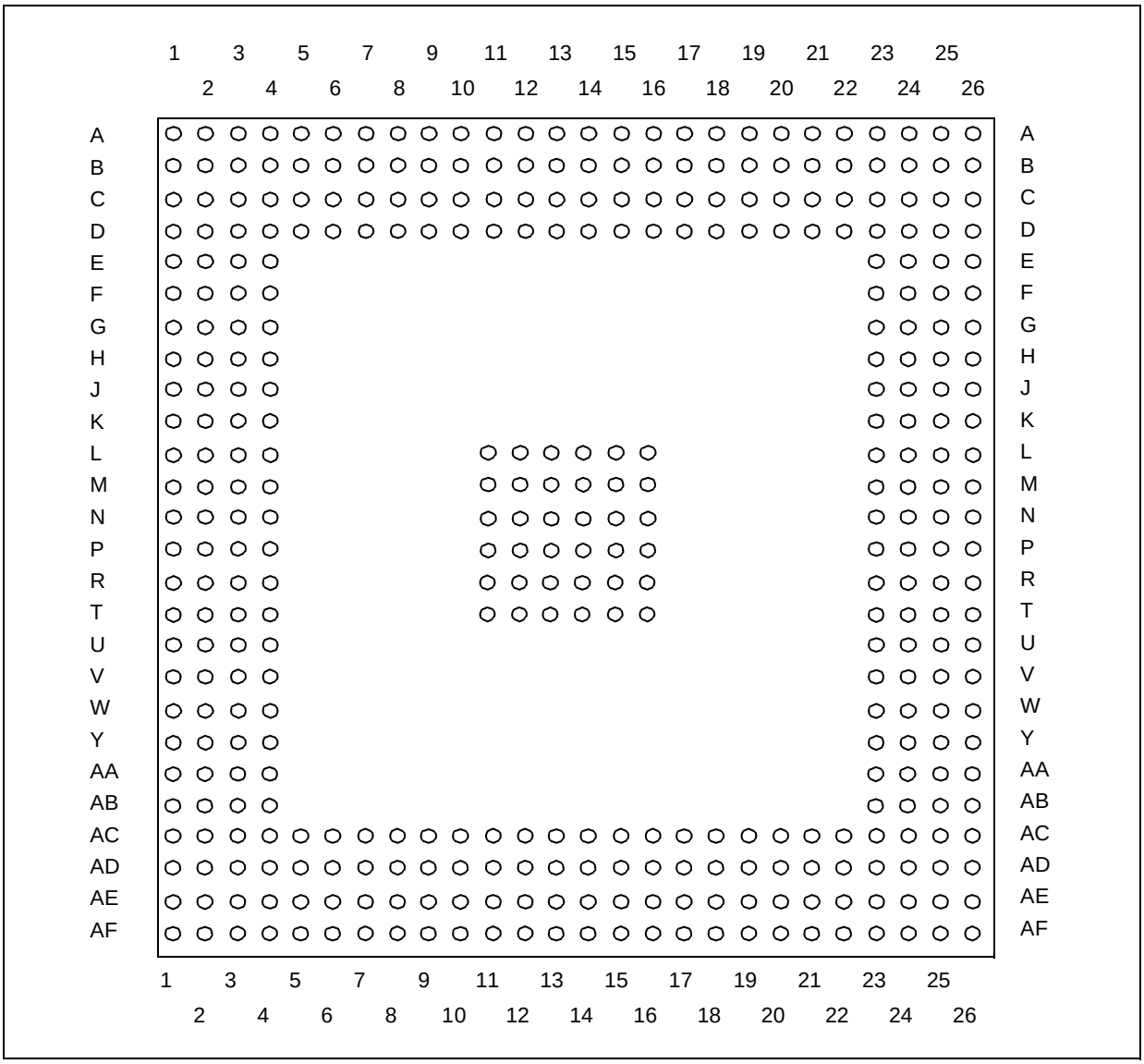


Figure 5-2. 388-pin PBGA Package - PCB Dimensions

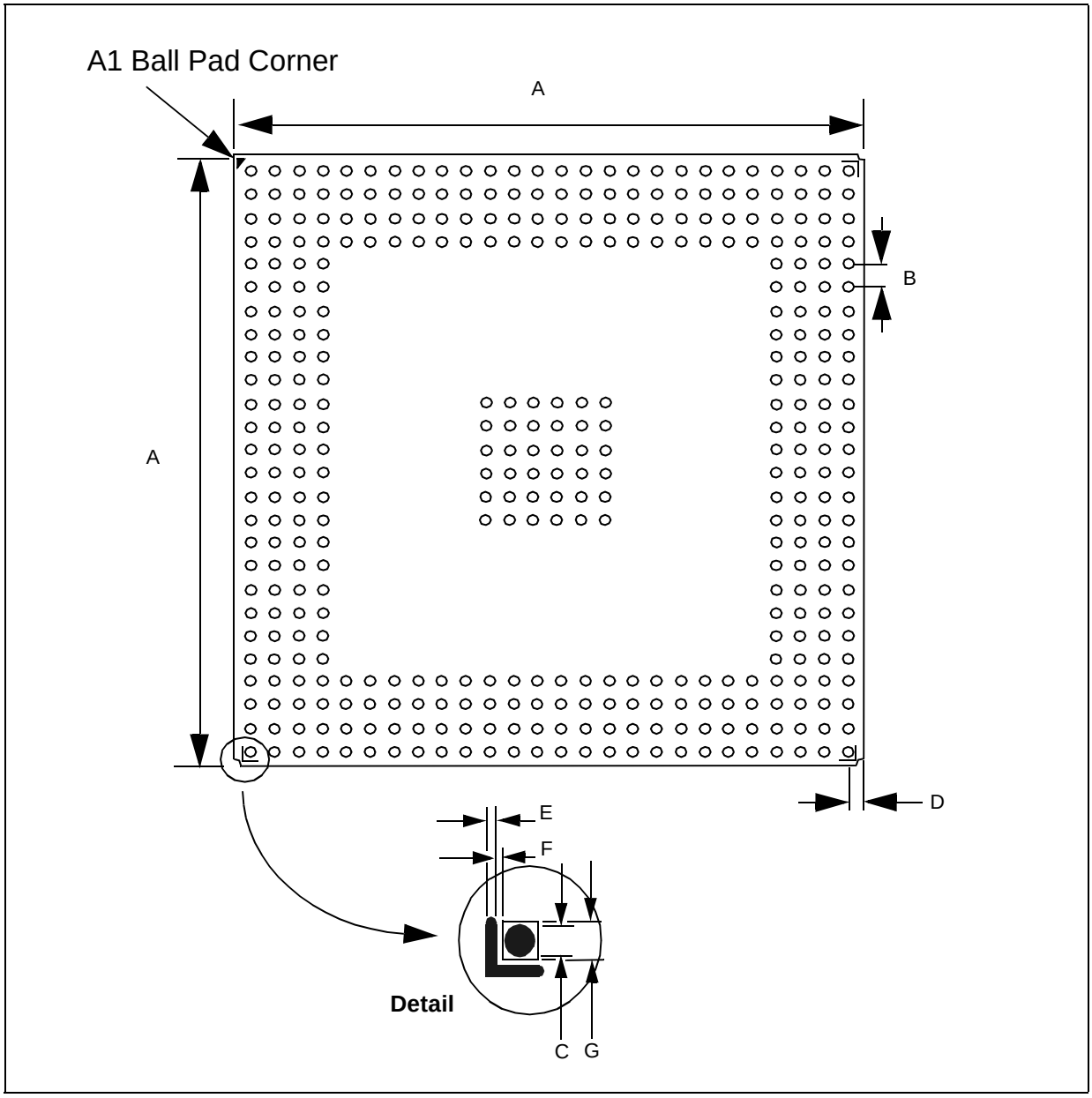


Table 5-1. 388-pin PBGA Package - PCB Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	34.95	35.00	35.05	1.375	1.378	1.380
B	1.22	1.27	1.32	0.048	0.050	0.052
C	0.58	0.63	0.68	0.023	0.025	0.027
D	1.57	1.62	1.67	0.062	0.064	0.066
E	0.15	0.20	0.25	0.006	0.008	0.001
F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 5-3. 388-pin PBGA Package - Dimensions

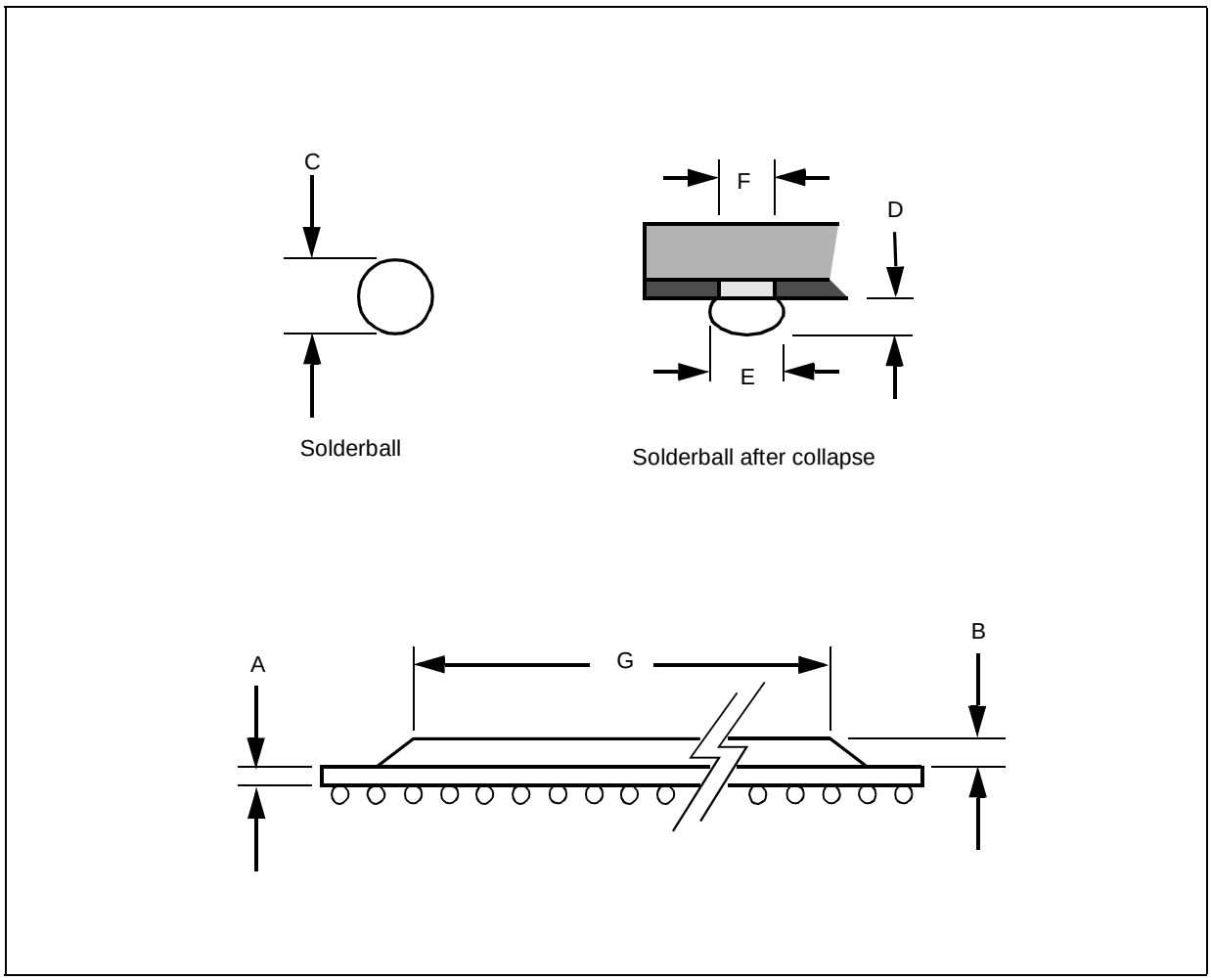


Table 5-2. 388-pin PBGA Package - Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

5.2. 388-PIN PACKAGE THERMAL DATA

The 388-pin PBGA package has a Power Dissipation Capability of 4.5W. This increases to 6W when used with a Heatsink.

The structure in shown in Figure 5-4.

Thermal dissipation options are illustrated in Figure 5-5 and Figure 5-6.

Figure 5-4. 388-Pin PBGA structure

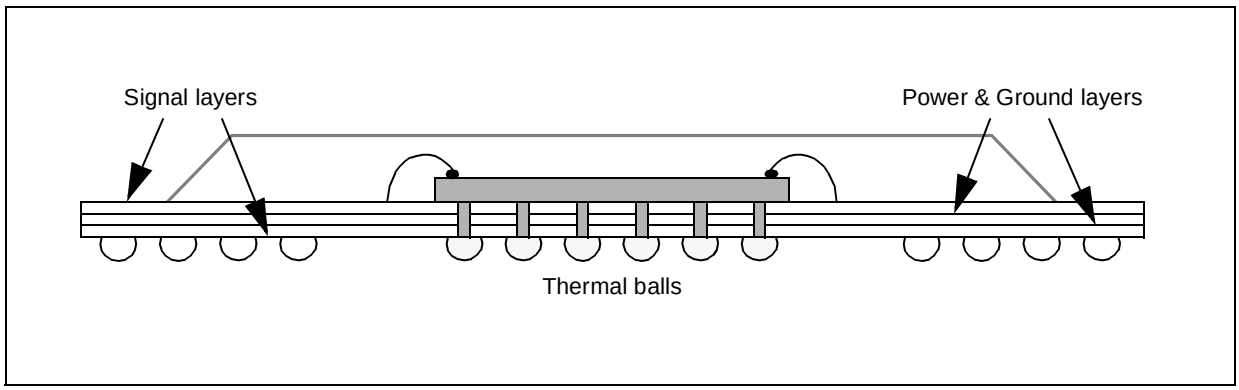


Figure 5-5. Thermal Dissipation Without Heatsink

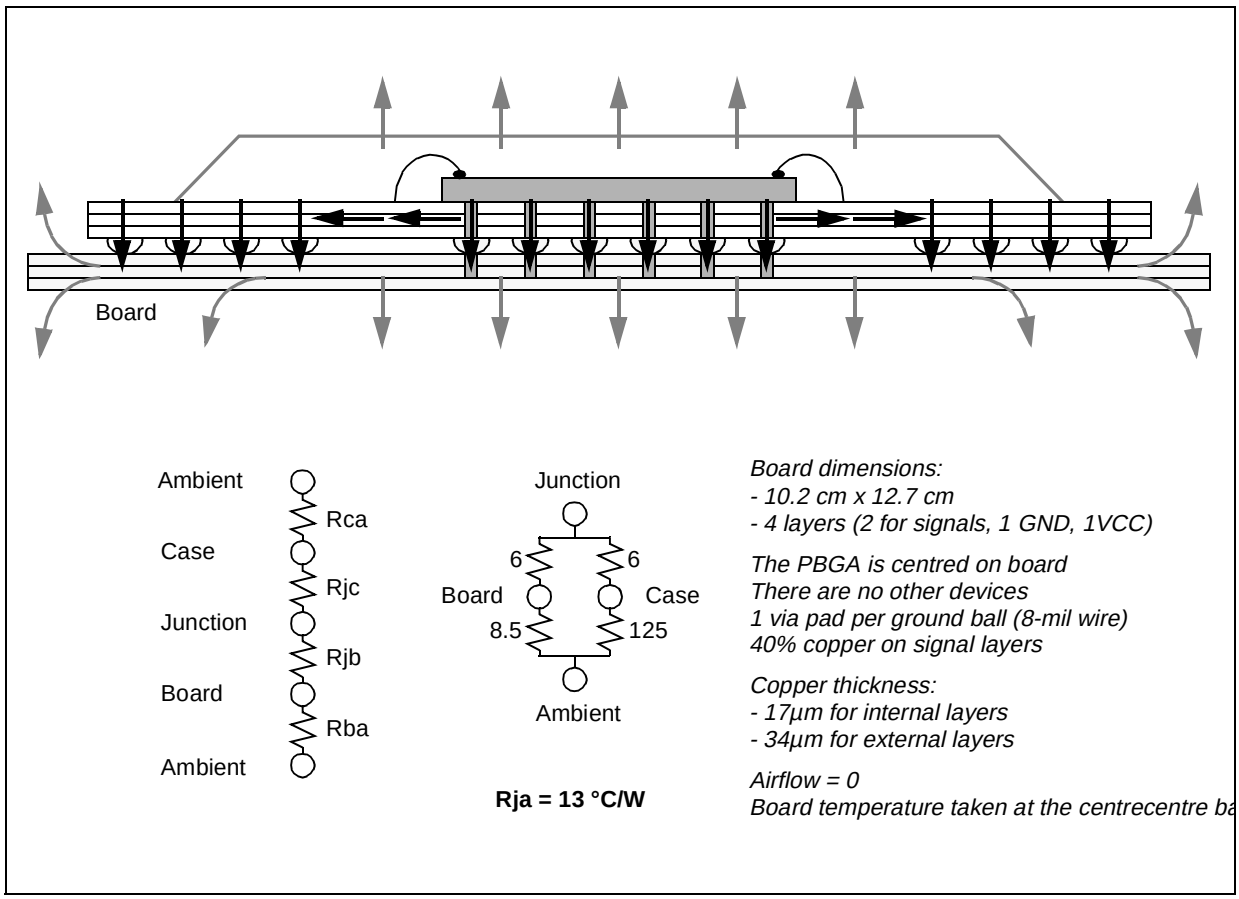
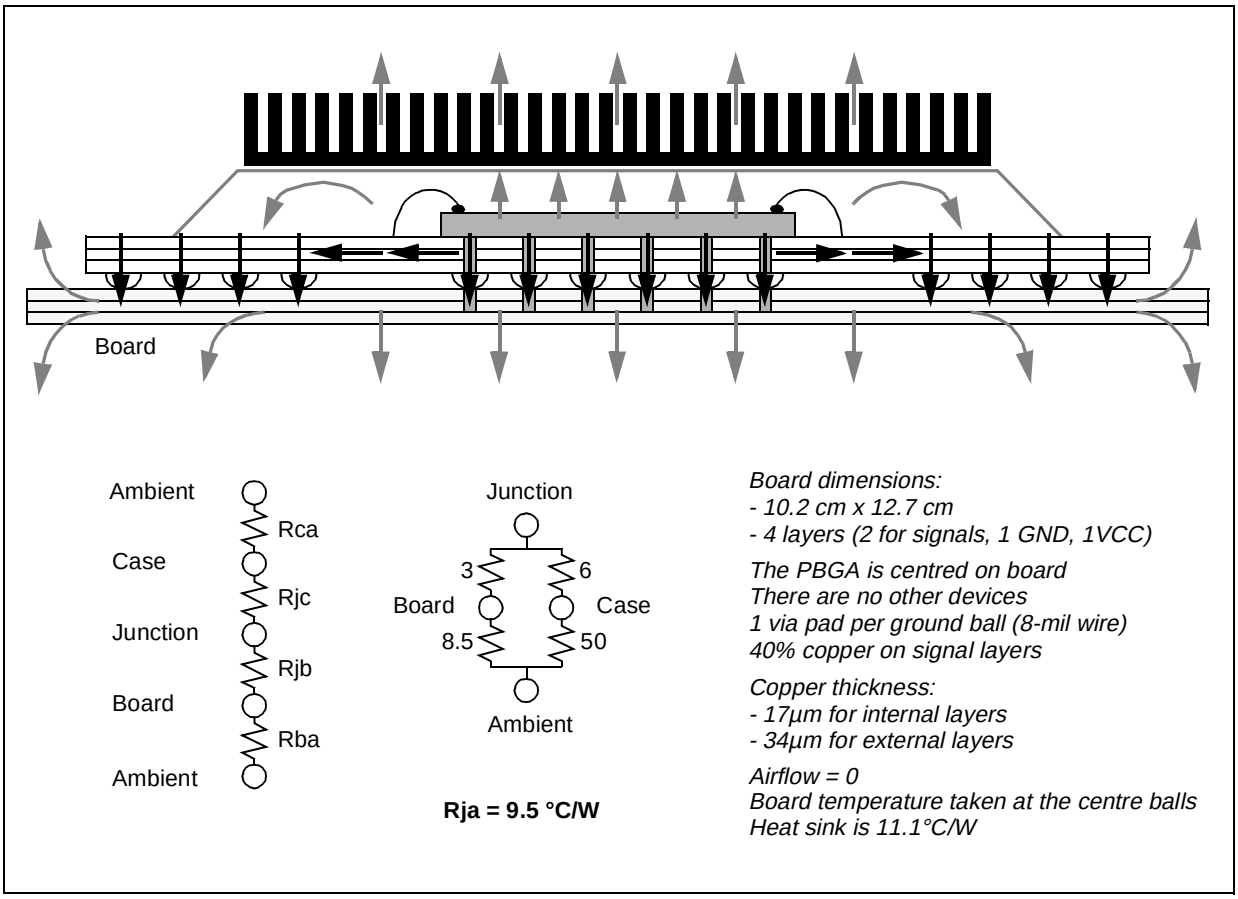


Figure 5-6. Thermal Dissipation With Heatsink



6. DESIGN GUIDELINES

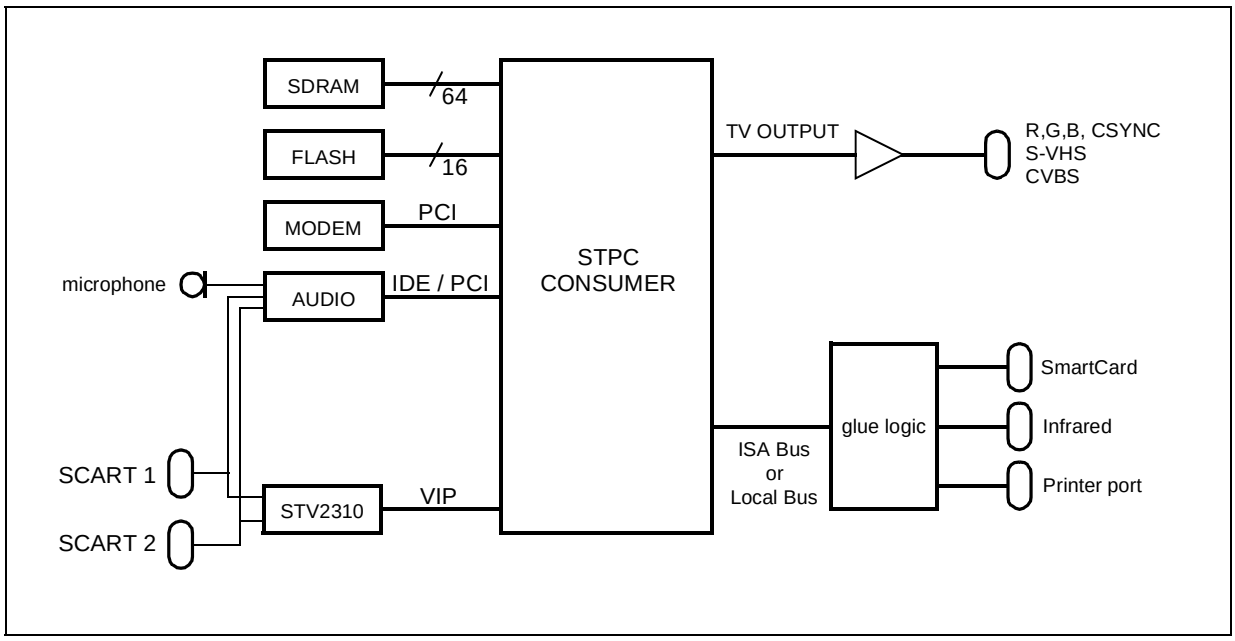
6.1 Typical Applications

The STPC Consumer is well suited for many applications. Some of the possible implementations are described below.

6.1.1 Web Box

A web box is an analog set top box providing internet browsing capability to a TV set. It has a TV output for connecting to the TV set, a modem for internet connection, a smartcard interface for the ISP access control, and an infrared interface for the remote control or the keyboard.

Figure 6-1. Web Box



6.2 Architecture recommendations

This section describes the recommend implementations for the STPC interfaces. For more details, download the "References Schematics" from the STPC web site.

6.2.1 14MHz oscillator stage

The 14.31818 MHz oscillator stage can be implemented using a quartz, which is the preferred and cheaper solution, or using an external 3.3V oscillator.

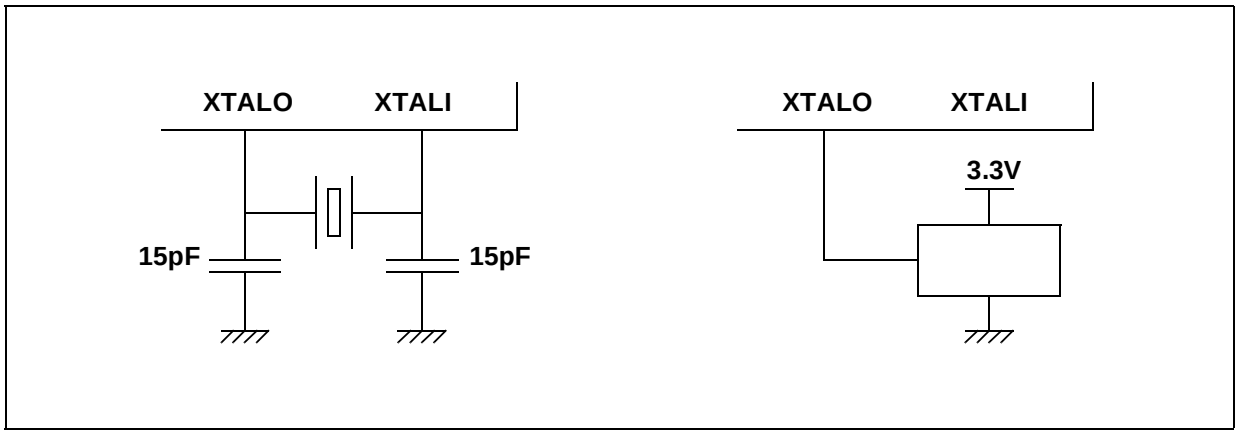
The crystal must be used in its series-cut fundamental mode and not in overtone mode. It must have an Equivalent Series Resistance (ESR, sometimes referred to as Rm) of less than 50 Ohms (typically 8 Ohms) and a shunt capacitance (Co) of less than 7 pF. The balance capacitors of 16 pF must be added, one connected to each pin, as described in Figure 6-2.

In the event of an external oscillator providing the master clock signal to the STPC Atlas device, the LVTTL signal should be connected to XTALO, as described in Figure 6-2.

As this clock is the reference for all the other on-chip generated clocks, it is **strongly recommended to shield this stage**, including the 2 wires go-

ing to the STPC balls, in order to reduce the jitter to the minimum and reach the optimum system stability.

Figure 6-2. 14.31818 MHz stage



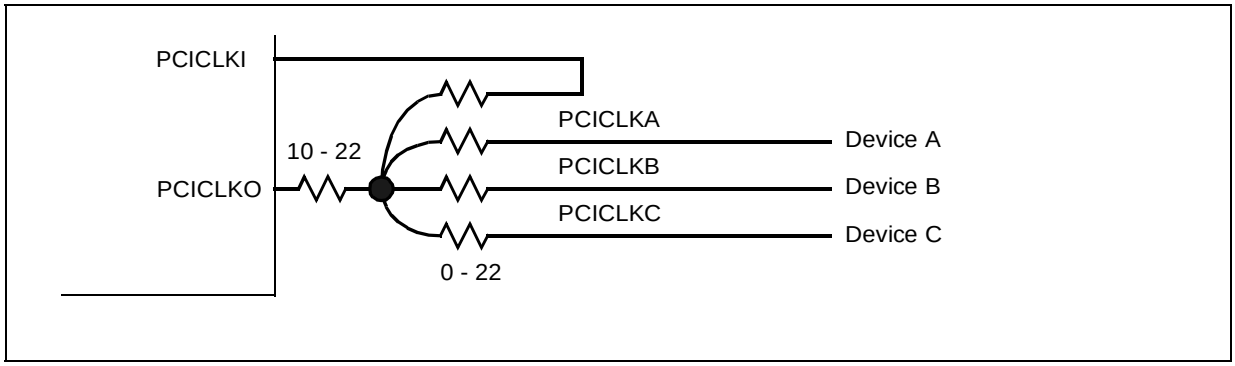
6.2.2 PCI bus

The PCI bus is always active and the following control signals must be pulled-up to 3.3V or 5V through 2K2 resistors even if this bus is not connected to an external device: FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, LOCK#, SERR#, PERR#, PCI_REQ#[2:0].

PCI_CLKO must be connected to PCI_CLKI through a 10 to 33 Ohms resistor. Figure 6-3 shows a typical implementation.

For more information on layout constraints, go to the **place and route recommendations** section.

Figure 6-3. Typical PCI clock routing

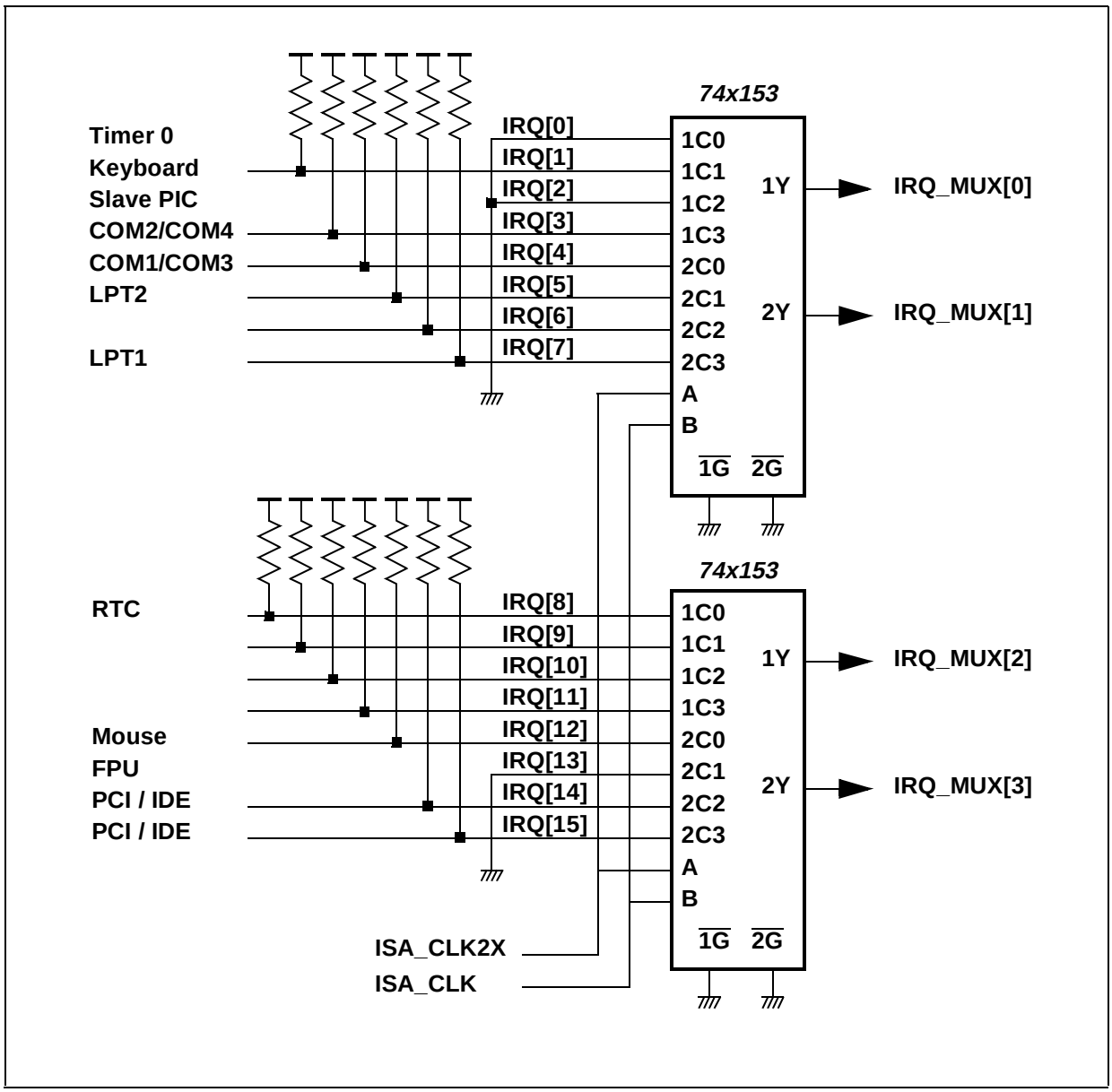


6.2.3 IPC

Most of the IPC signals are multiplexed: Interrupt inputs, DMA Request inputs, DMA Acknowledge outputs. Figure 6-4 describes a complete implementation of the IRQ[15:0] time-multiplexing.

When an interrupt line is used internally, the corresponding input can be grounded. In most of the embedded designs, only few interrupts lines are necessary and the glue logic can be simplified.

Figure 6-4. Typical IRQ multiplexing

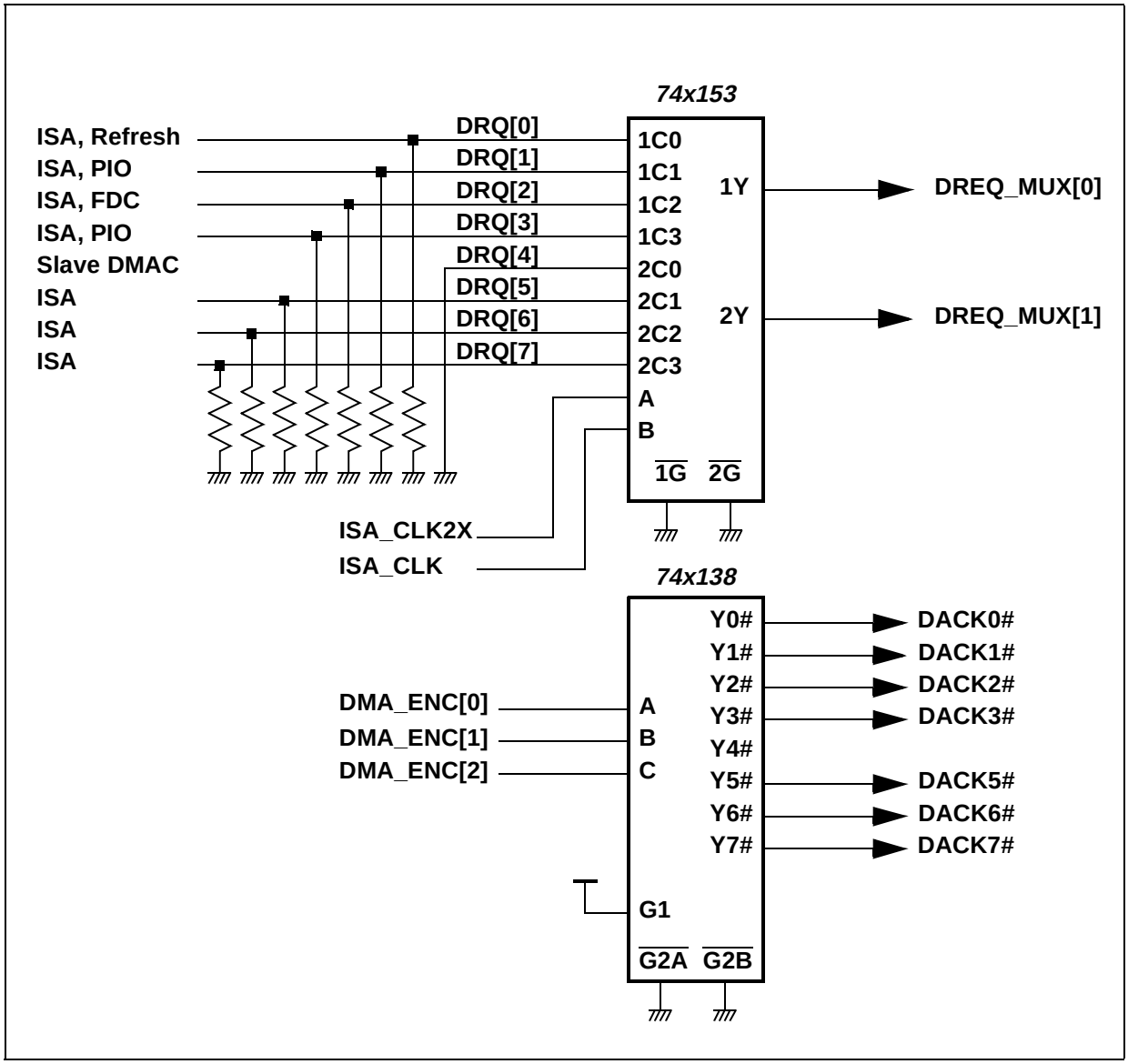


When the interface is integrated into the STPC, the corresponding interrupt line can be grounded as it is connected internally.

For example, if the integrated IDE controller is activated, the IRQ[14] and IRQ[15] inputs can be grounded.

Figure 6-5 describes a complete implementation of the external glue logic for DMA Request time-multiplexing and DMA Acknowledge demultiplexing. Like for the interrupt lines, this logic can be simplified when only few DMA channels are used in the application.
This glue logic is not needed in Local bus mode as it does not support DMA transfers.

Figure 6-5. Typical DMA multiplexing and demultiplexing



6.2.4 VGA interface

The STPC integrates a VGA DACs and video buffers. The amount of external devices is then limited to the minimum as described in the Figure 6-6.

All the resistors and capacitors have to be as close as possible to the STPC while the circuit protector DALC112S1 must be close to the VGA connector.

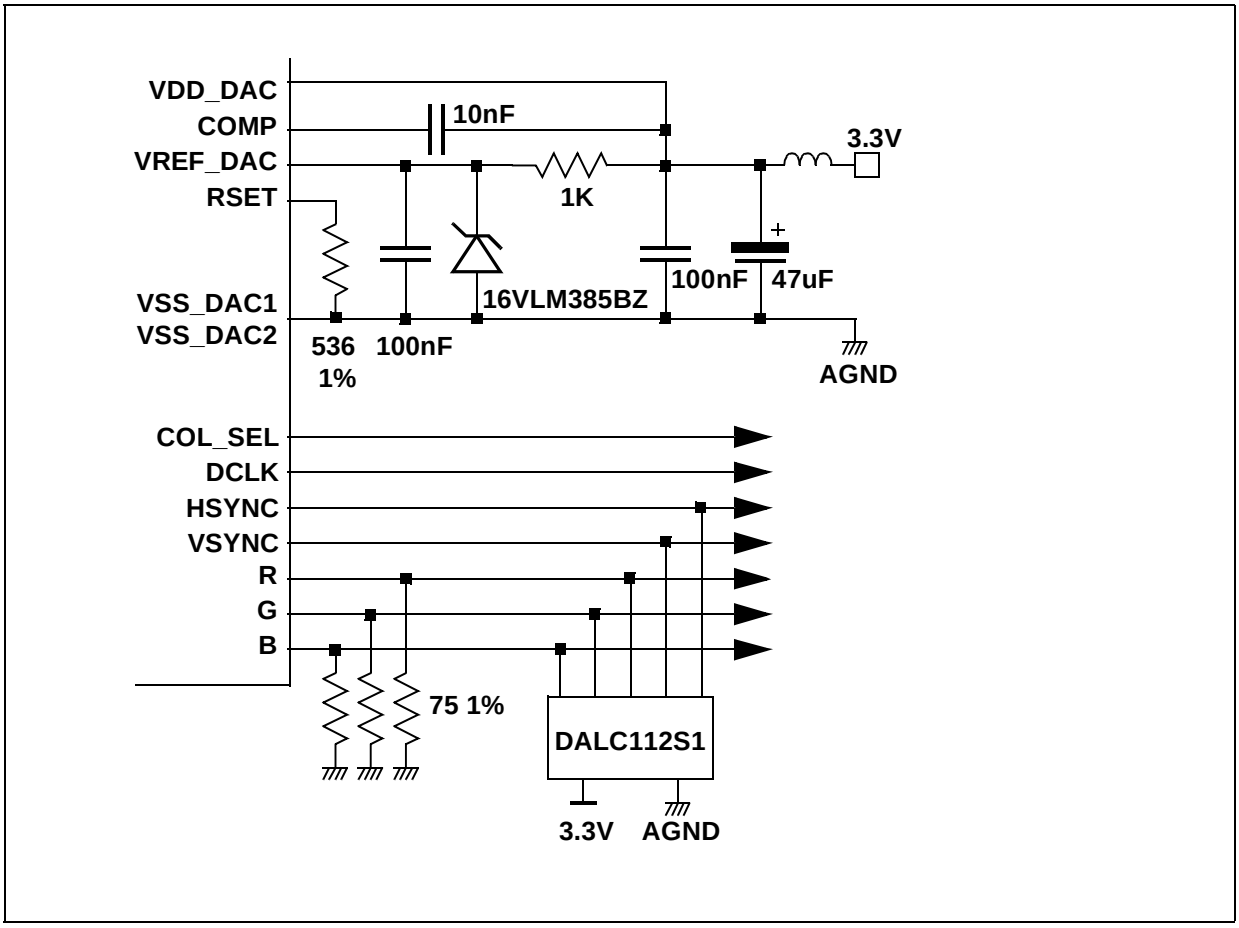
The DDC[1:0] lines, not represented here, have also to be protected when they are used on the VGA connector.

COL_SEL can be used when implementing the Picture-In-Picture function outside the STPC, for example when multiplexing an analog video source. In that case, the CRTC of the STPC has to be genlocked to this analog source.

DCLK is usually used by the TFT displays which have RGB inputs in order to synchronise the picture at the level of the pixel.

When the VGA interface is not needed, the signals R, G, B, HSYNC, VSYNC, COMP, RSET can be left unconnected, VSS_DAC[2:1] and VDD_DAC must then be connected to GND.

Figure 6-6. Typical VGA implementation



6.3 Place and route recommendations

6.3.1 General recommendations

Some STPC Interfaces run at high speed and need to be carefully routed or even shielded like:

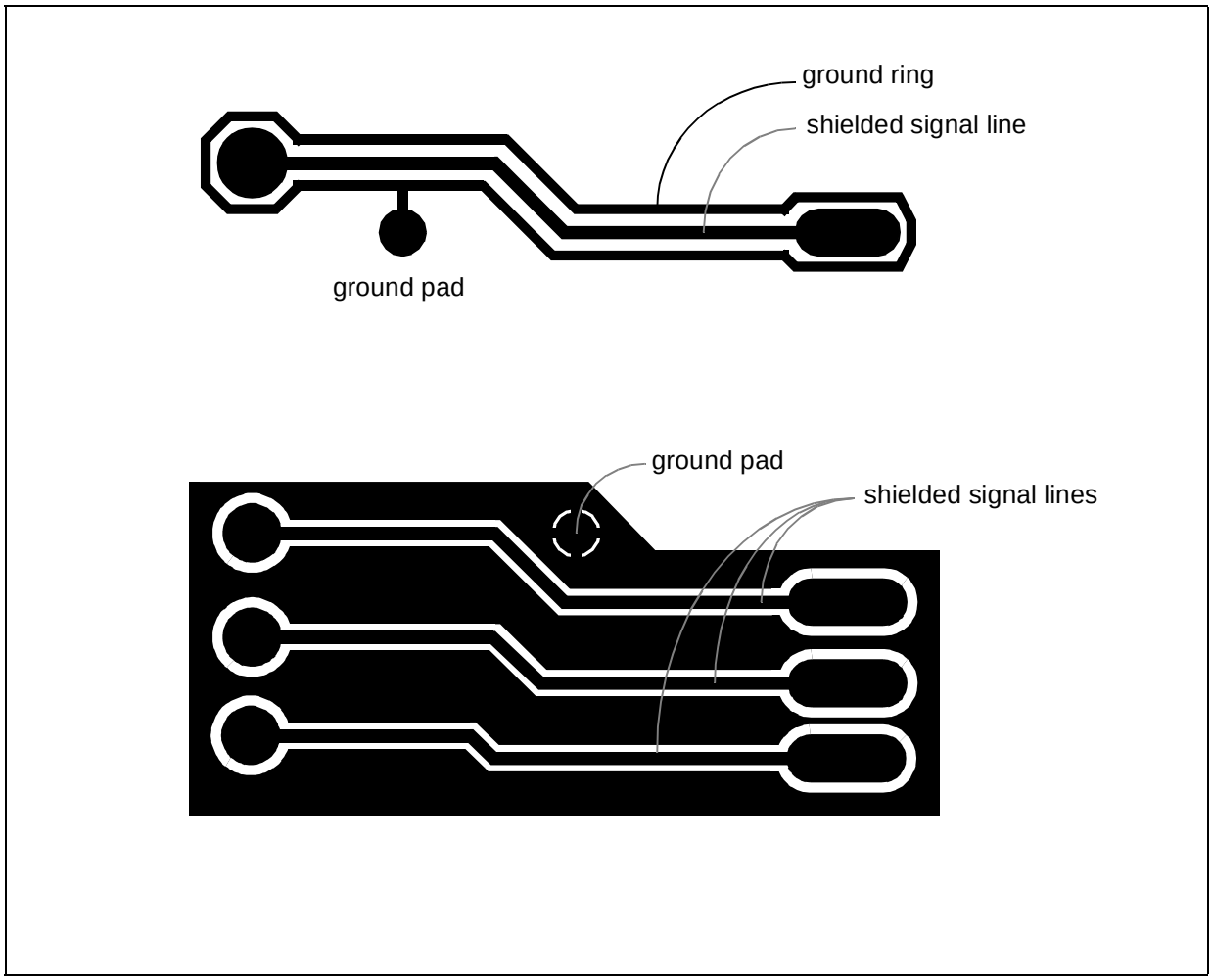
1) Memory Interface
2) PCI bus
3) Graphics and video interfaces
4) 14 MHz oscillator stage

All clock signals have to be routed first and shielded for speeds of 27MHz or higher. The high speed signals follow the same constraints, as for the memory and PCI control signals.

The next interfaces to be routed are Memory, PCI, and Video/graphics.

All the analog noise-sensitive signals have to be routed in a separate area and hence can be routed indepedently.

Figure 6-7. Shielding signals



6.3.2 Thermal dissipation

6.3.2.1 Power saving

Thermal dissipation of the STPC depends mainly on supply voltage. When the system does not need to work at the upper voltage limit, it may therefore be beneficial to reduce the voltage to the lower voltage limit, where possible. This could save a few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

6.3.2.2 Thermal balls

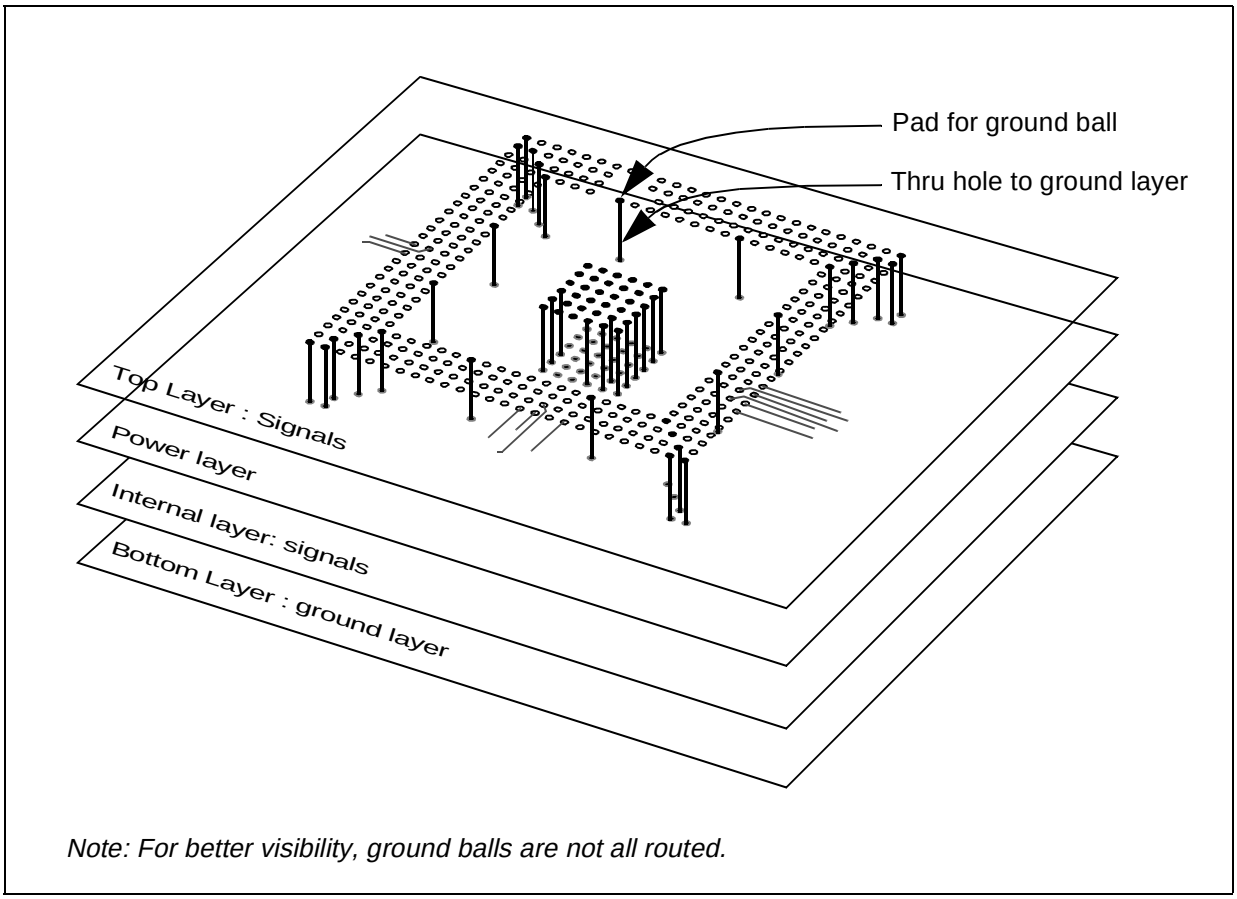
The standard way to route thermal balls to ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

With such configuration the Plastic BGA package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die. The remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules must be followed when routing the STPC in order to avoid thermal problems.

As the whole ground layer acts as a heat sink, the ground balls must be directly connected to it, as illustrated in Figure 6-8. If one ground layer is not enough, a second ground plane may be added.

Figure 6-8. Ground routing

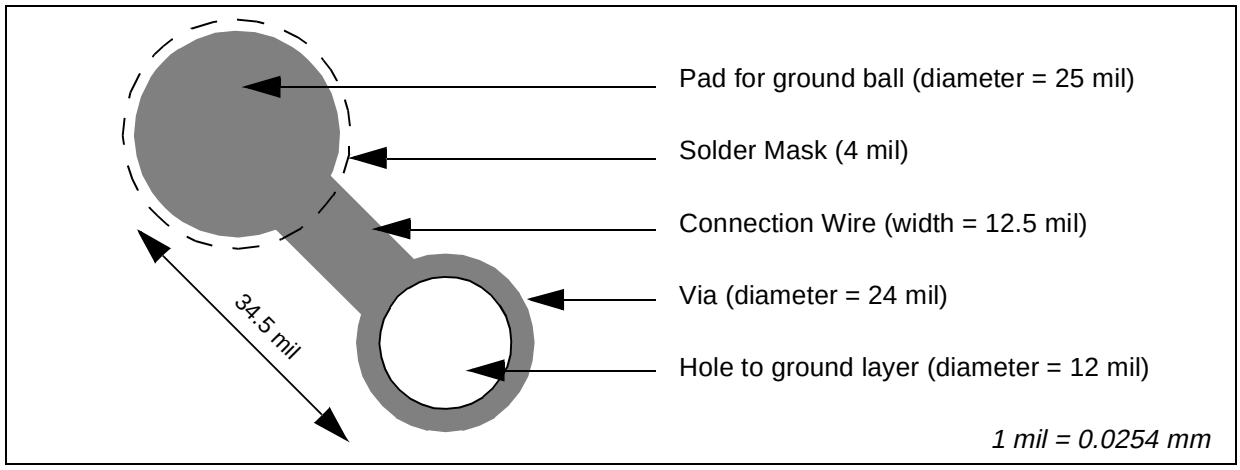


Note: For better visibility, ground balls are not all routed.

When considering thermal dissipation, one of the most important parts of the layout is the connection between the ground balls and the ground layer.

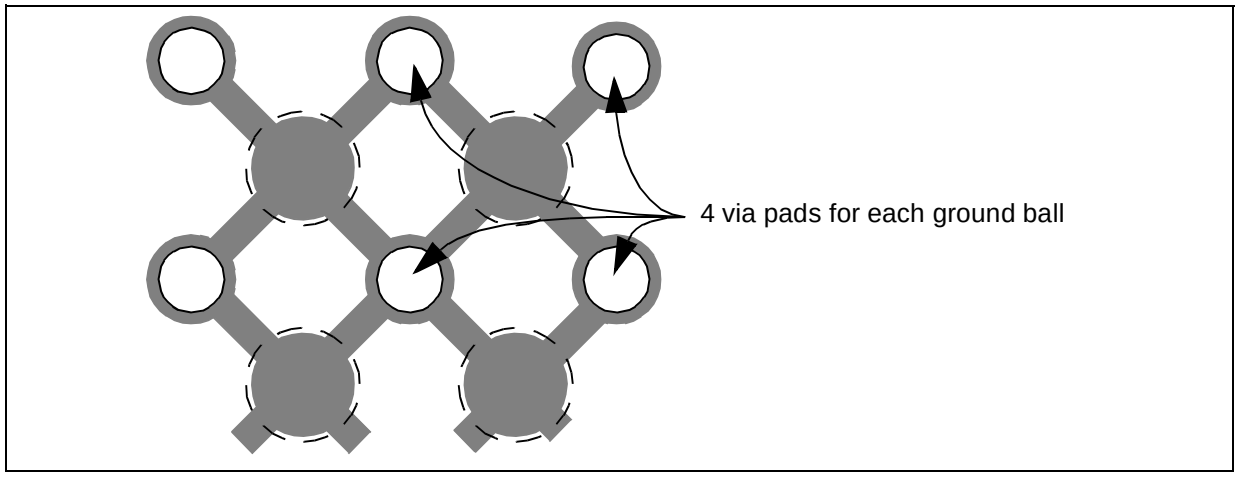
A 1-wire connection is shown in Figure 6-9. The use of a 8-mil wire results in a thermal resistance of 105°C/W assuming copper is used (418 W/m.°K). This high value is due to the thickness (34 µm) of the copper on the external side of the PCB.

Figure 6-9. Recommended 1-wire Power/Ground Pad Layout



Considering only the central matrix of 36 thermal balls and one via for each ball, the global thermal resistance is 2.9°C/W. This can be easily improved using four 12.5 mil wires to connect to the four vias around the ground pad link as in Figure 6-10. This gives a total of 49 vias and a global resistance for the 36 thermal balls of 0.5°C/W.

Figure 6-10. Recommended 4-wire Ground Pad Layout

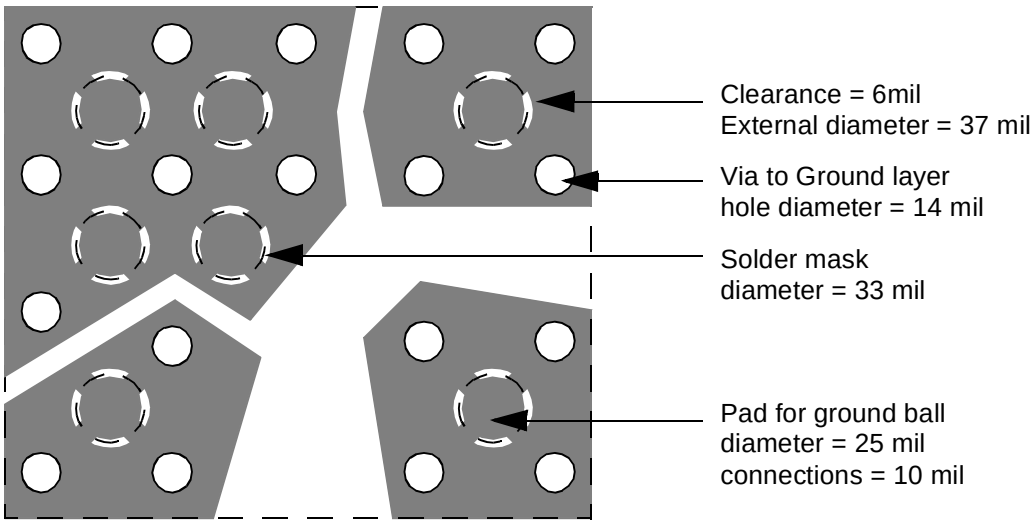


The use of a ground plane like in Figure 6-11 is even better.

To avoid solder wicking over to the via pads during soldering, it is important to have a solder mask of 4 mil around the pad (NSMD pad). This gives a diameter of 33 mil for a 25 mil ground pad.

To obtain the optimum ground layout, place the vias directly under the ball pads. In this case no local board distortion is tolerated.

Figure 6-11. Optimum Layout for Central Ground Ball - top layer



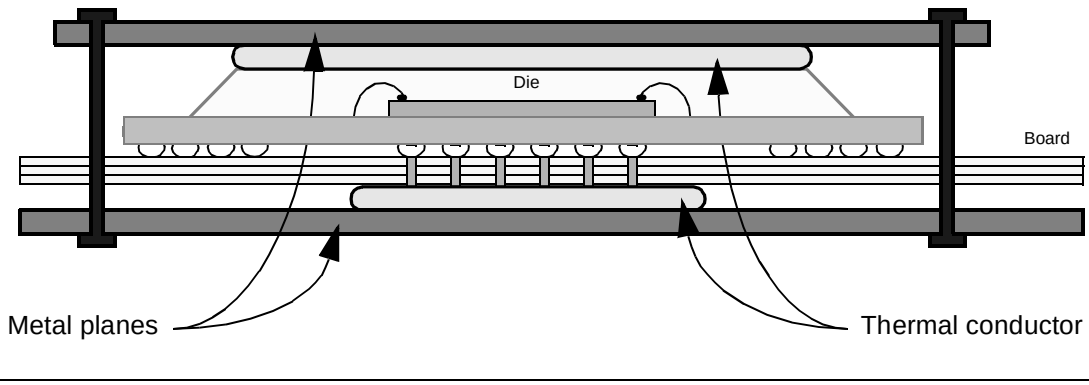
6.3.2.3 Heat dissipation

The thickness of the copper on PCB layers is typically 34 µm for external layers and 17 µm for internal layers. This means that thermal dissipation is not good; high board temperatures are concentrated around the devices and these fall quickly with increased distance.

Where possible, place a metal layer inside the PCB; this improves dramatically the spread of heat and hence the thermal dissipation of the board.

The possibility of using the whole system box for thermal dissipation is very useful in cases of high internal temperatures and low outside temperatures. Bottom side of the PBGA should be thermally connected to the metal chassis in order to propagate the heat flow through the metal. Thermally connecting also the top side will improve furthermore the heat dissipation. Figure 6-12 illustrates such an implementation.

Figure 6-12. Use of Metal Plate for Thermal Dissipation



As the PCB acts as a heat sink, the layout of top and ground layers must be done with care to maximize the board surface dissipating the heat. The only limitation is the risk of losing routing channels. Figure 6-13 and Figure 6-14 show a partial routing with a good thermal dissipation thanks to an optimized placement of power and signal vias. The ground plane should be on bottom layer for the best heat spreading (thicker layer than internal ones) and dissipation (direct contact with air). .

Figure 6-13. Layout for Good Thermal Dissipation - top layer

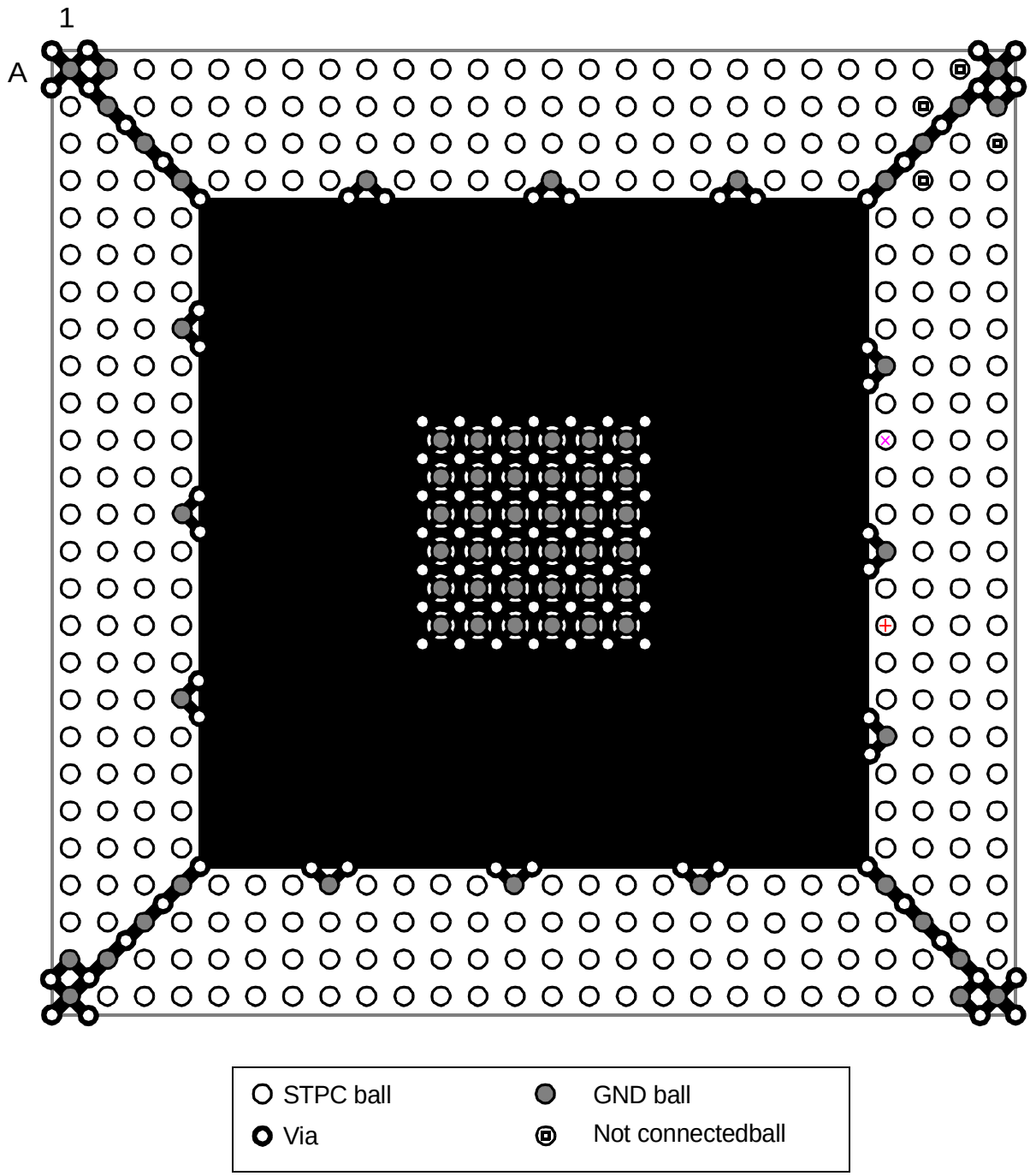
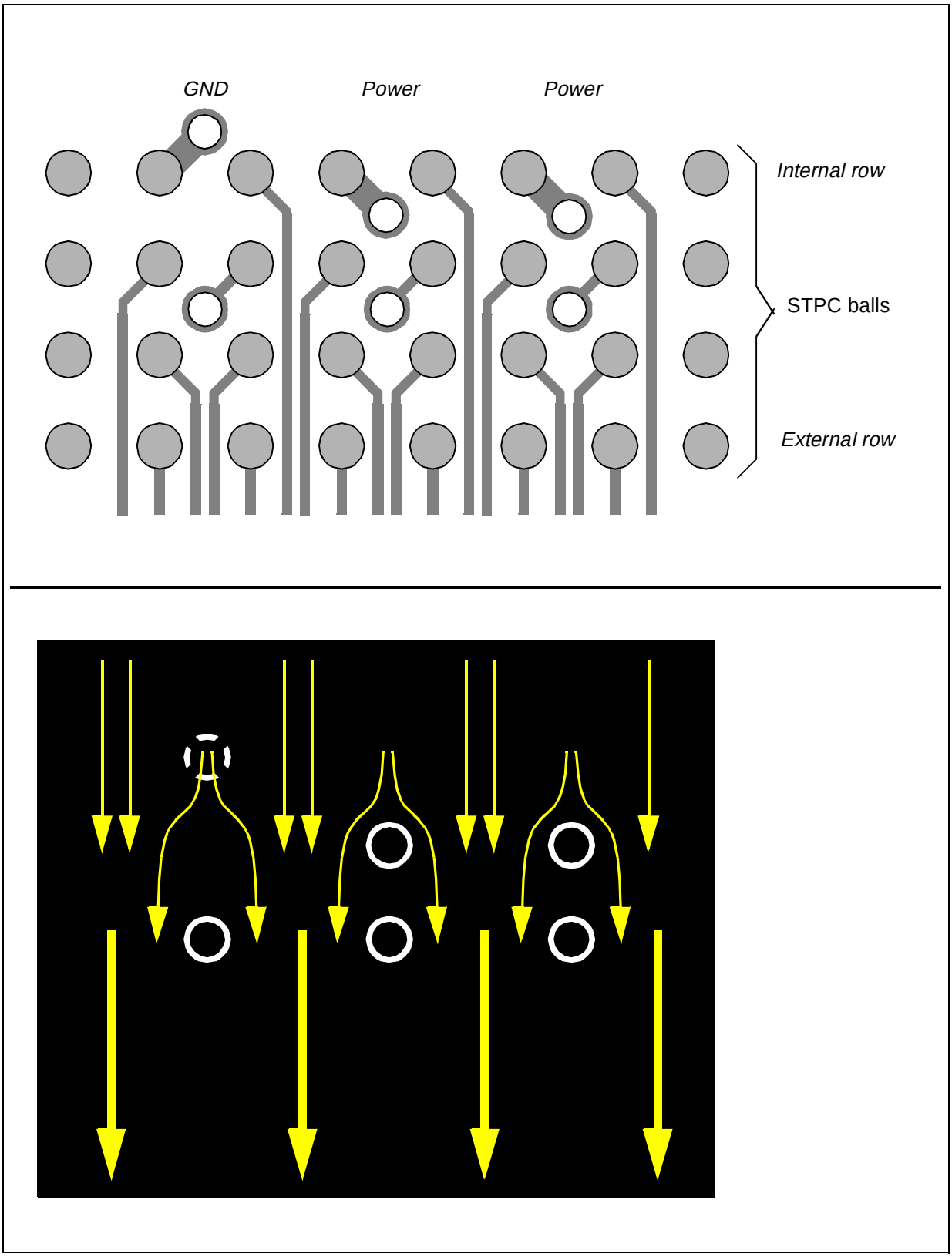
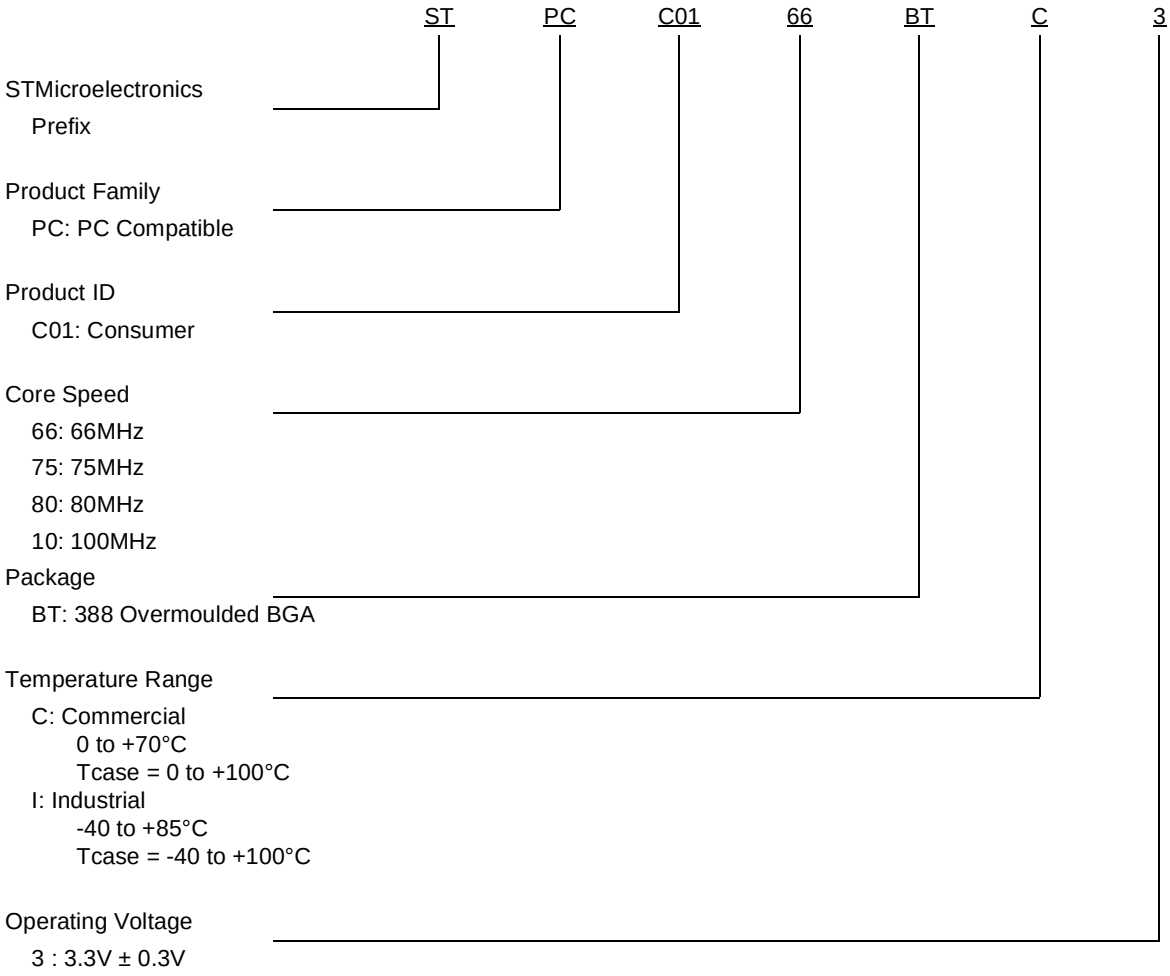


Figure 6-14. Recommend signal wiring (top & ground layers) with corresponding heat flow



7. ORDERING DATA

7.1 Ordering Codes



7.2 Available Part Numbers

Part Number	Core Frequency (MHz)	CPU Mode	Tcase Range (C)	Operating Voltage (V)
STPCC0166BTC3	66	DX	0°C to +100°C	3.3V ± 0.3V
STPCC0180BTC3	80	DX		
STPCC0166BTI3	66	DX	-40°C to +100°C	
STPCC0180BTI3	80	DX		