DS1MX7 Device
DS1 Mapper 7-Channel
TXC-04201B

DATA SHEET

FEATURES

- Seven independent 1.544 Mbit/s DS1 mappers
- Single byte-parallel Telecom Bus @ 6.48 MHz (28 Slots) or 19.44 MHz (84 Slots)
- Floating VT1.5 Byte Synchronous mapping for use with or without a slip buffer
- Asynchronous mapping for DS1
- SONET mapping (VT1.5) or SDH mapping (TU-11 in AU-3 or TU-11 in TUG-3)
- AMI, B8ZS or NRZ codec for DS1s
- Serial I/O for control of DS1 line interface transceivers or framers
- Telecom Bus and DS1 loopbacks with integral PRBS generator and analyzer
- VT1.5/TU-11 pointer tracking and insertion
- VT1.5/TU-11 overhead processing and insertion
- one-second latched performance registers and counters
- DS1 alarm detection and generation
- Auxiliary port for J2, V5, Z6/N2, Z7/K4 and O-bit access
- Ring port for USHR/P support
- Gapped clock option for Internet Applications without need for a framer
- Intel / Motorola-compatible microprocessor interface
- 3-bit RDI support
- Boundary Scan capability (IEEE 1149.1)
- Single +5 V, ±5 % power supply
- 208-pin plastic quad flat package

DESCRIPTION

The DS1MX7 is a seven-channel Byte Synchronous and Asynchronous DS1 mapper. Both SONET and SDH mappings are provided per Bellcore GR-253-CORE (VT1.5) and ITU G.709 (TU-11). A single add/drop Telecom Bus is provided that can operate at either 6.48 or 19.44 MHz, which is compatible with other TranSwitch devices. VT1.5/TU-11 pointer tracking and overhead extraction/processing with full error and alarm control is provided. VT1.5/TU-11 pointer calculation and overhead assembly is also provided. Alarm and error mappings from drop to add and SONET/SDH to/from DS1 are provided. Jitter performance is achieved with a fully digital threshold modulator and DPLL that meets GR-253-CORE MTIE requirements without external de-jitter buffers. For the DS1 line, AMI, B8ZS and NRZ line codes are supported with full alarm detection and generation per ANSI T1.231-1997 draft. Each channel is independently programmable for mixed service applications. Access to status and control bits is provided via an Intel/Motorola-compatible microprocessor interface. Diagnostic, test, and maintenance functions are provided, including boundary scan, PRBS generator/analyzer and loopbacks.

APPLICATIONS

- SONET/SDH terminal or add/drop multiplexers supporting both Asynchronous and Byte Synchronous modes
- Unidirectional or bidirectional ring applications
- SONET Remote Digital Terminal Equipment
- SONET CPE Equipment requiring access to DS0s
- SONET/SDH Test Equipment
- Internet Access Equipment

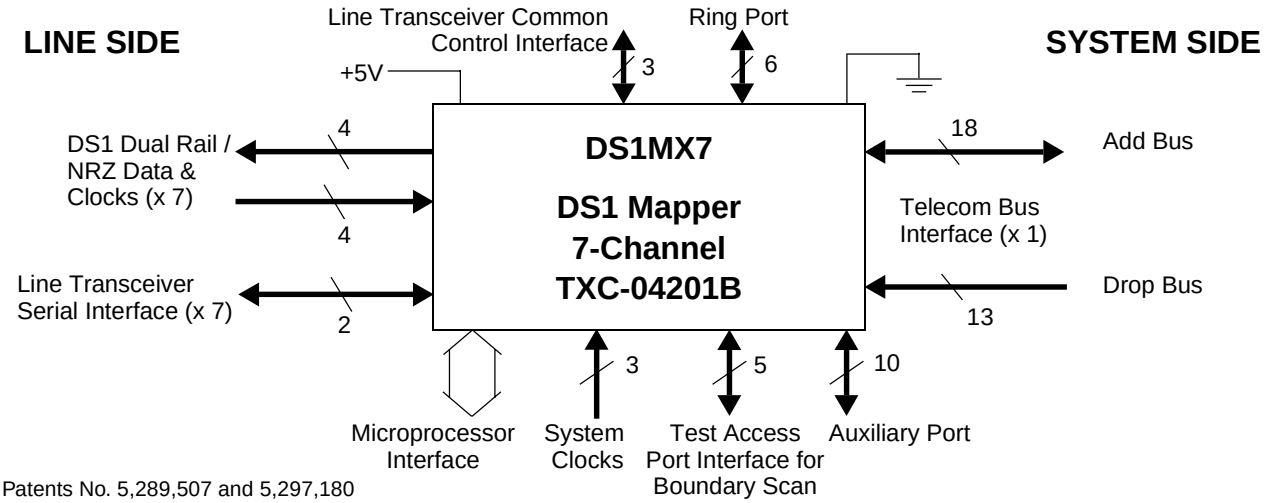

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TABLE OF CONTENTS

* Please note that TranSwitch provides documentation for all of its products. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

FEATURE LIST

The DS1MX7 device is a highly-featured seven-channel DS1 (T1) mapper for use in a wide variety of interface, transmission and switching applications. Seven independent DS1 Asynchronous / Byte Synchronous mappers are provided in a single monolithic VLSI device using sub-micron CMOS technology. Powered from a single +5.0 volt supply, the device dissipates less than one watt typically. The DS1MX7 is provided in a 208-pin plastic quad flat package. Its ambient operating temperature range extends from -40 ° C to 85 ° C with 0 ft/min airflow.

The DS1MX7 device has been designed to meet the latest industry standards, namely:

- ANSI T1.102- 1993
- ANSI T1.105- 1991
- ANSI T1.107- 1995
- ANSI T1.231 (1993 and 1997 draft)
- ANSI T1.403-1995
- AT&T Pub. 62411 (December 1990)
- Bellcore GR-253-CORE (Issue 2)
- Bellcore TR-NWT-000496 (Issue 3)
- Bellcore GR-499-CORE (Issue 1)
- IEEE 1149.1- 1990, -1994
- ITU G.708
- ITU G.709
- ITU G.782
- ITU G.783

FEATURES THAT ARE INDEPENDENTLY SELECTABLE FOR EACH OF THE MAPPERS

Line Interface Options

- Meets ANSI and Bellcore input jitter requirements
- Rail (for Asynchronous mapping only)
  B8ZS or AMI
  ANSI compliant LOS detector
  ANSI compliant AIS detector
  12-Bit BPV counters with excessive zeros option
- NRZ option (for Asynchronous and Byte Synchronous mapping)
  Clock polarity selection for clock in/out
  NRZ data inversion and clock edge options (separate transmit and receive control)
  For Asynchronous use, negative rail can be used to count externally detected code violations
- Programmable clock edges for transmit and receive data
- External pin per channel for status (may be programmed to combine with internal AIS and LOS to support external LOC detector)
- Clock slave for Asynchronous input; clock and multiframe synchronization (3 ms), master or slave, for Byte Synchronous input
- Separate signaling highway for Byte Synchronous, carries ABCD signaling bits and AIS / Yellow alarm information in and out of the DS1MX7
- External pin-controlled shut down of all DS1 line drive pins for card protection
- Gapped clock option in place of signaling for 1536 kHz datacom in Byte Synchronous operation
- CRC-6 generation (DS1 input) and error counting (DS1 output) in Byte Synchronous mapping

Mapping And Synchronizer Features

- Mapping to SONET or SDH columns according to GR-253-CORE or ITU G.709
- Per channel selectable Asynchronous and Byte Synchronous mapping to a floating VT1.5 or TU-11 for both mapping and demapping
- Overhead assembly with BIP-2 calculation, REI-FEBE (microprocessor or received BIP-2 error), signal label (microprocessor value), RDI (microprocessor value or via received signal label mismatch, VT AIS, VT LOP, or unequipped) and RFI (microprocessor value or DS1 Yellow from signaling highway)
- Pointer calculation (fixed at 78 for Asynchronous, calculated for Byte Synchronous) with generated pointer increment and decrement counters (4 bits each)
- In Byte Synchronous mode, line clock may be an input ('modified Byte Synchronous') or an output ('true Byte Synchronous')
- Multiplexing of signaling bits from the signaling highway with P0/P1 bit generation
- Unequipped and Unassigned VT payload generation
- VT AIS generation (microprocessor value, AIS from signaling highway, loss of frame on Byte Synchronous, or AIS / LOS / external pin from line decoder)
- Threshold modulator to reduce demapping jitter and wander
- Tracking of input multiframe pulses by pointer movements in Byte Synchronous mode

Demapping And Desynchronizer Features

- Asynchronous or Byte Synchronous per channel, programmable to match mapper mode
- Digital PLL with 2 Hz low pass filter to track up to $\pm$ 250 Hz nominal DS1 signal providing a smooth clock output with no need for an external de-jitter buffer
- Separate $\pm$5 byte pointer leak buffer with programmable dual slope leak rate (8 ms to 2048 ms per bit in 8 ms steps, automatically doubled to 16 ms to 4096 ms per bit in 16 ms steps within $\pm$12 bits of center of pointer leak buffer)
- Power down with all-zeros or all-ones sent to line interface
- Demapping of SONET or SDH columns according to GR-253-CORE or ITU G.709
- Asynchronous and Byte Synchronous demapping of a floating VT1.5 / TU-11
- Pointer tracking and extraction of overhead (V5 and Z7/K4), LOP, AIS, SS and NDF with received pointer increment and decrement counters (4 bits each)
- Overhead processing with BIP-2 calculation and error counting (12-bit, with overflow), REI (FEBE) counting (12-bit, with overflow), RDI (1- and 3-bit)/ RFI / signal label de-bouncing and detection, signal label mismatch / unequipped detection
- De-multiplexing of signaling bits to the signaling highway with multiframe generation for Byte Synchronous
- DS1 AIS from microprocessor value, VT AIS, VT LOP, signal label mismatch or unequipped
- DS1 Yellow to signaling highway from RFI

Fractional T1 For Frame Relay, ATM AAL1 Access

- Framer not required for many applications
- Receive and transmit gapped clock (1536 kbit/s) per mapper in Byte Synchronous mode
- CRC-6 generation and checking
- Direct connection to multichannel HDLC or ATM devices for N x 56 or N x 64 kbit/s service
- Internal DPLL to minimize received jitter

Signaling Support For Byte Synchronous Mapping

- Receive and transmit temporary buffers to align VT1.5/TU-11 payloads to signaling highway
- Signaling bits mapped to and demapped from specific locations per GR-253-CORE and G.709
- A, AB, ABCD signaling bit support
- Byte synchronous operation with TranSwitch QT1F-*Plus* VLSI device:
  Signaling bit positions in received DS0s optionally replaced with ones by QT1F-*Plus*
  VT AIS and VT RFI to DS1 AIS and DS1 RAI (Yellow) respectively
  DS1 AIS and DS1 RAI (Yellow) to VT AIS and VT RFI respectively
- Unicode support (DS0 alarms) for Byte Synchronous operation planned in future framers

Alarms And Errors

- Detection of VT AIS, VT RFI, unequipped, signal label mismatch, VT loss of pointer, single-bit RDI, 3-bit RDI, and demap error in the demap direction
- Detection of DS1 AIS, loss of signal, map error, and external pin alarm, in the mapping direction
- Counting of code violations (with or without excessive zeros) or CRC-6 errors, BIP-2, REI (FEBE), pointer generation and receive pointers with presets and overflow indications
- Microprocessor enable and insert of all alarms detected from line, calculated, or in overhead

Maintenance

- Loopbacks - DS1 line remote (toward DS1 line), DS1 line local (toward Telecom Bus), and Telecom Bus (toward DS1 line for all seven channels at once)
- PBRS generator in transmit framer and analyzer in receive path per T1 channel
  2^{15}-1 pattern
  Separate control bits with software indication
- Power-down modes force transmit leads to low, high or tri-state

Microprocessor Interface

- Nineteen-bit status register for VT AIS, VT RFI, unequipped, signal label mismatch, VT loss of pointer, single-bit RDI, 3-bit RDI, DS1 AIS, loss of signal, map error, demap error, external pin alarm, and counter overflow bits for code violation/CRC-6, BIP-2, REI (FEBE), pointer generation and receive pointers
- Latched event registers and interrupt mask registers to individually control each condition
- Twelve-bit CRC-6 (Byte Synchronous)/ code violation (Asynchronous), BIP-2, and REI (FEBE) error counters
- Four-bit increment and decrement pointer generation and receive pointer counters
- Shadow registers for all counters
- Full control of alarm mapping through enable bits
- Microprocessor forcing of alarm conditions
- Per channel reset and resynchronization
- Register access to J2, V5, Z6/N2, Z7/K4 bytes and O-bits for read and write

Performance and Fault Monitoring

- One second basis, via backplane one second clock
- Shadow registers for all 19 alarms and 7 counters
- Separate registers to indicate alarm changes (performance) and hard conditions (faults) are updated every second to simplify performance report generation

FEATURES THAT ARE ONLY SELECTABLE FOR THE SEVEN MAPPERS AS A GROUP

Telecom Bus Interface

- Single add bus and drop bus with individual timing
- Operation at 6.48 Mbyte/s or 19.44 Mbyte/s
- Compatible with TranSwitch SOT-1E and SOT-3 functional "B" version devices
- Parity generation and detection with device alarm (odd or even) on data and SPE / C1J1V1
- SONET mapping via VT1.5 at 6.48 and 19.44 Mbyte/s
- SDH mappings via TU-11 to AU-3 or to TUG-3 at 19.44 Mbyte/s
- Uses SPE and C1J1V1 to locate individual VTs
- Separate STS-1 phases permitted in an STS-3 for Asynchronous and modified Byte Synchronous operation
- Each transmit and receive time slot is programmable to one of 28 or 84 including internal and external add bus contention monitors with global alarm
- Add bus timing programmable to zero or one clock delay
- Drop or add bus clock edges programmable
- Add bus enable pin plus control pins for optional POH and/or TOH drive
- Per VT/ TU signal failure input via common pin
- Clock and SPE / C1J1V1 presence detectors on system in and system out buses, which generate device alarms on failure

External Line Interface Transceiver Support

- Three-wire serial port to read/write control up to seven line interface transceivers ('host mode')
- Designed to support integrated microprocessor control of loopbacks, alarms and line build out
- Per channel or broadcast for data out
- Internal registers to drive and read external devices

Common Microprocessor Support

- Microprocessor global reset, masks, polling registers, interrupt polarity and latch edge control
- Motorola split address/data or Intel split address/data
- Global alarm Indications ('or' of per channel alarms of the same type) with a channel pointer register indicating channels with any active alarms
- Global interrupt mask bits, one per alarm type
- Interrupt on alarm changes: on positive edge, negative edge or both edges
- Device level alarms for Telecom Bus signals and reference clocks using status and latched event registers with interrupt mask registers
- Device level alarms can be enabled to appear on separate interrupt line for card protection via hardware or software mechanisms
- Error insertion via the microprocessor for parity testing on the Telecom Bus
- Timed error insertion for REI (FEBE) and BIP-2 global value
- Hardware interrupt polarity selection
- Common hardware reset pin and global software reset register

Auxiliary Port Common

- Access to or from optional overhead bytes for special purposes with microprocessor enables
- Access to J2, V5, Z6/N2, Z7/K4 bytes and O-bits received via a shared serial port
- Insertion of J2, Z6/N2, Z7/K4 bytes and O-bits to mapping direction via a shared serial port

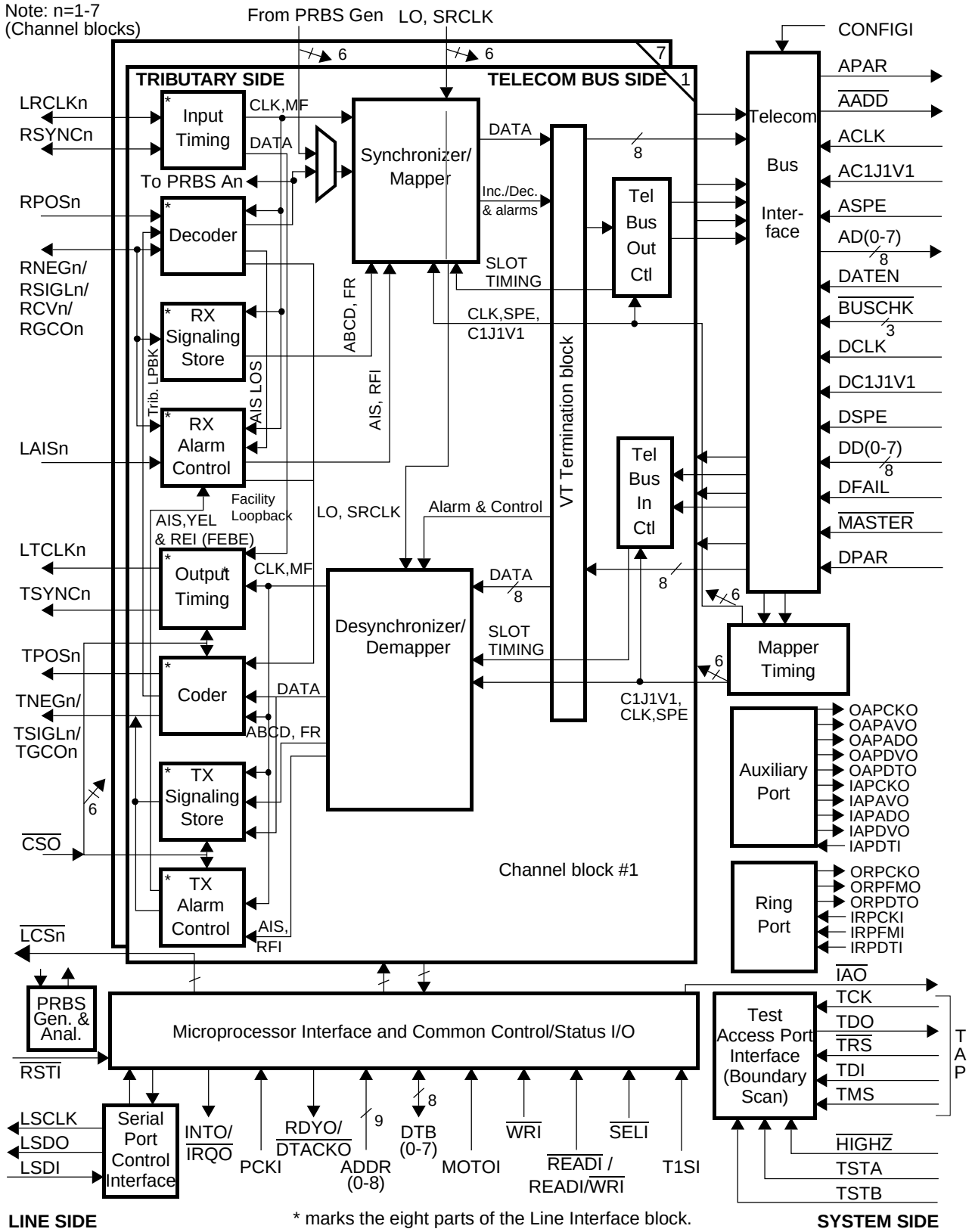
Ring Port Common

- Permits REI (FEBE) and single/three-bit RDI values to be sent from one DS1MX7 to another
- USHR/P support
- Shared serial port with clock and frame for transmit and receive
- Pair of DS1MX7s provides for dual Telecom Bus applications

Protection, Test and Maintenance Support

- IEEE 1149.1 boundary scan
- Ability to tri-state all outputs for in-circuit testing with a single control pin
- Loss of clock detectors and parity generator/error detector for add and drop Telecom Buses
- Internal alarm output programmable to a variety of bus fault and clock fault conditions and a card switch-off feature to assist in implementing protection switching
- External shadow register clock input (1Hz $\pm$ 32 ppm)
- PRBS generator and analyzer switchable to any of the seven mapper channels

BLOCK DIAGRAM



* marks the eight parts of the Line Interface block.

Figure 1. DS1MX7 TXC-04201B Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the DS1MX7 device is shown in Figure 1. The major blocks are the seven Channel blocks, the Microprocessor Interface, the Serial Port Control Interface, the Ring port, the Auxiliary port, the PRBS (Pseudo-Random Binary Sequence) Generator and Analyzer, the Test Access Port Interface, the Mapper Timing block and the Telecom Bus Interface.

Each of the seven Channel blocks consists of the following component blocks: Decoder/Coder and Input/Output Timing (for Receive and Transmit Line Interfaces), Receive and Transmit Alarm Control, Receive and Transmit Signaling Store, Synchronizer/ Mapper and Desynchronizer/ Demapper, VT Termination, and Telecom Bus Input and Output Control blocks.

The Receive and Transmit Line Interface blocks connect each of the seven mapper channels to an external line interface transceiver, which performs the LIU and clock recovery functions for the Asynchronous mode of operation. The interface to the transceiver can be configured for two interface modes: a dual unipolar (rail) interface or a NRZ interface. When the Byte Synchronous mode of operation is used, the clock and synchronization signals to and from an external DS1 framer are handled by these blocks; data is always in the NRZ mode.These blocks also provide a tributary (transmit to receive) loopback and a facility or remote (receive line to transmit line) loopback.

When the dual unipolar interface mode is selected, input data from the external line interface transceiver is clocked into the DS1MX7 on pins RPOSn and RNEGn using the recovered receive clock present on the LRCLKn input pins, where n=1-7 identifies one of the seven mappers (note: RNEGn is one of several pins that has multiple functions, with a signal symbol for each). In the transmit direction, unipolar data is clocked out of the DS1MX7 on pins TPOSn and TNEGn by the transmit line clock present on the LTCLKn output pins. Global control bits are provided in the memory map which enable the unipolar data to be clocked in and out of the DS1MX7 on either edge of the clocks. For the dual unipolar interface mode, the DS1MX7 provides either a Bipolar with Eight Zero Substitution (B8ZS), or an Alternate Mark Inversion (AMI), coder and decoder function, and Loss Of Signal detection. The Loss Of Signal detector meets the requirements specified in the ANSI T1.231 document listed above in the DS1MX7 Features section. An unframed AIS detector is also provided to assist in network fault isolation. A 12-bit performance counter is provided for each mapper, for counting B8ZS coding violation errors. An option is provided to also include excessive zeros in the coding violations counter.

When the NRZ interface mode is selected and the mapper channel is programmed for Asynchronous mapping, NRZ data is clocked in at the RPOSn pin by the recovered received clock input on the LRCLKn pin. The NRZ data is clocked out of the DS1MX7 on the TPOSn pins by the transmit system clock present on the LTCLKn pins. Global control bits are provided in the memory map which enable the NRZ data to be inverted or clocked in and out of the DS1MX7 on either edge of the clocks. Bipolar violations which are detected in the external line interface transceiver may be clocked into the DS1MX7 on the RNEGn/RCVn pins and counted in the associated 12-bit coding violation performance counter. The TNEGn output may be used in NRZ mode as a spare drive bit. The Remote Line Loopback function for each framer is also implemented in the Line Interface blocks.

When the NRZ interface mode is selected and the mapper channel is programmed for Byte Synchronous mapping, NRZ data is clocked in at the RPOSn pins by the clock present on pins LRCLKn. The DS1MX7 can generate a clock on LRCLKn and a 3.0 ms multiframe synchronization signal on pins RSYNCn if an external slip buffer is provided in the framer or if the source of the signal is a clock slaved to the DS1MX7. If LRCLKn and RSYNCn are inputs, the DS1MX7 translates any clock phase movements with respect to the SONET/SDH clock via VT/TU pointer movements. For applications that do not require a framer but where the DS1 ESF CRC-6 performance monitoring function is desired (true Byte Synchronous mode only), the DS1MX7 calculates and inserts CRC-6 into the defined frame bit positions in the VT1.5/ TU-11 structure in the mapping direction. After demapping, the CRC-6 is checked and any errors found are counted in the 12-bit counter shared for code violation counting.

Byte Synchronous mapping supports the independent transmission of signaling through defined nibbles in the VT1.5/ TU-11 structure, as shown in Figure 2. The DS1MX7 provides Receive and Transmit Signaling Stores to synchronize signaling and framing bits to and from a DS1 Framer or switching stage with the Mapper and

Demapper blocks. Signaling is received through the RNEGn/RSIGLn pins in Byte Synchronous mode, being clocked in with LRCLKn. Signaling is sent out on the TNEGn/TSIGLn pins in Byte Synchronous mode, using LTCLKn. TranSwitch framers like the QT1F-*Plus* (TXC-03103) can utilize the signaling bits on the signaling highways for automatic signaling propagation between SONET/SDH Byte Synchronous mapping and DS1 lines. For applications using the full DS1 payload in Byte Synchronous mode, the RNEGn/RSIGLn pins can be programmed to supply gapped clock (RGCOn), as can the TNEGn/TSIGLn pins (TGCOn).

The Receive and Transmit Alarm Control blocks work in conjunction with the Receive and Transmit Line Interface blocks as well as the Receive and Transmit Signaling Store blocks to move DS1 alarm signals in and out of the DS1MX7. The Receive Alarm Control block detects specific bits from the receive signaling highway, such as AIS or RAI (Yellow), for forwarding to the Mapper block as AIS and RFI. It also gathers LOS and AIS from the Receive Line Interface. The LAISn input pin may be used for forwarding an externally detected Loss of Signal or Loss of Clock, or as a general interrupt input. The Transmit Alarm Control block translates RFI and AIS from the Demapper block along with microprocessor controls to set specific bits on the transmit signaling highway. TranSwitch framers like the QT1F-*Plus* (TXC-03103) can utilize the control bits on the signaling highways for automatic alarm propagation between SONET/SDH and DS1 lines. For card protection schemes, control input pin $\overline{\text{CSO}}$, when driven low, causes all of the output pins for the seven Line Interfaces to go low.

The Synchronizer/ Mapper block takes the clock and data from the Receive Line Interface in Asynchronous mode, threshold modulates it with SRCLK, buffers it in a FIFO and inserts the data bits in the information bit positions of the Asynchronous VT1.5/ TU-11, and stuffs it using the two stuff opportunity bits with indication in the C1 and C2 bits, as shown in Figure 2. The stuffing matches the received DS1 clock to the bit positions available based on the SONET/SDH network clock supplied to the DS1MX7 in the Add Telecom Bus Clock, ACLK and the AC1J1V1 signal. Optional overhead bytes J2, Z6/N2, O and part of Z7 are taken from microprocessor-written values or the Auxiliary Port.

The Synchronizer/ Mapper block takes the clock, frame and data from the Receive Line Interface in Byte Synchronous mode, buffers it in a FIFO and writes it to defined byte positions in the Byte Synchronous VT1.5/ TU-11 along with the optional overhead bytes J2, Z6/N2 and part of Z7 which are taken from microprocessor-written values or the Auxiliary Port. For Byte Synchronous mode the signaling bits are taken from the Receive Signaling Store and mapped to the correct positions in the VT1.5/ TU-11. The 500-microsecond long VT superframe shown in Figure 2 is repeated six times, being synchronized to the RSYNCn 3.0 millisecond input. The P1P0 bits are generated to indicate which signaling bits are being carried in a specific VT superframe and are related to RSYNCn. FIFO conditions are monitored and can lead to increment or decrement requests of the VT Termination block. Synchronization changes in RSYNCn are monitored for possible NDF requests.

The VT Termination block takes the mapped data and optional overhead together with any frame, increment or decrement indications associated with Byte Synchronous mode from the Synchronizer/ Mapper block. The V5 and Z7 bytes are built from received DS1 alarms, demapped or Ring Port received error conditions, microprocessor-written values and parity calculated over the payload. V1 and V2 are set to 78, positioning V5 just after V1 for Asynchronous mode. For Byte Synchronous mode the V1 and V2 bytes are generated to track the phase of the incoming DS1 signal relative to ACLK; two four-bit counters are provided to keep track of pointer increments and pointer decrements generated. If a new position for the RSYNCn pulse is generated, this block will generate an NDF along with the new pointer. If the DS1MX7 acts as a clock source, the LO pin will be used to provide this clock and it must be frequency locked to the STS-1 or STM-1 clock, or pointer justifications and/ or mapping errors will result. If AIS is to be generated the entire payload is ones. If unassigned (Idle) is to be generated, an all-zeros payload with a valid V5 is generated. If an unequipped is to be generated, an all-zeros payload including V5 is generated.

The VT termination block also provides the pointer tracking, V5 and Z7 overhead location and VT1.5/ TU-11 alarm detection and de-bouncing functions. The alarms (RDI in four flavors, RFI, Unequipped, Signal Label Mismatch, LOP, AIS, REI, BIP-2 errors, etc.) are made available to the common microprocessor block for latching, shadowing, counting and interrupting purposes. Alarms are provided on the Ring Port for RDI and REI to support ring applications. It also identifies the payload for the Desynchronizer/ Demapper block as well as any pointer movements.

Byte Synchronous Floating VT Mode	Legend:	Asynchronous Floating VT Mode
V_1	C_n = Stuff Control	V_1
V_5	F = DS1 Frame Bit	V_5
P_1 P_0 S_1 S_2 S_3 S_4 F R	I = Information	R R R R R R I R
DS0 Channels 1 - 24	J_2 = VT Path Trace	24 Information Bytes
V_2	O = Overhead Bits	V_2
J_2	P_1P_0 = Signaling Phase	J_2
P_1 P_0 S_1 S_2 S_3 S_4 F R	R = Fixed Stuff	C_1 C_2 O O O O I R
DS0 Channels 1 - 24	S_n = Signaling	24 Information Bytes
V_3	St_n = Stuff Opportunity	V_3
Z_6	V_1 and V_2 = pointer	Z_6
P_1 P_0 S_1 S_2 S_3 S_4 F R	V_3 = Inc/Dec opportunity	C_1 C_2 O O O O I R
DS0 Channels 1 - 24		24 Information Bytes
V_4	V_4 = unused	V_4
Z_7	V_5 = VT Overhead	Z_7
P_1 P_0 S_1 S_2 S_3 S_4 F R	Z_6 = Reserved Byte	C_1 C_2 R R R St_1 St_2 R
DS0 Channels 1 - 24	Z_7 = Reserved and 3-bit RDI Byte	24 Information Bytes

V1 Byte						V2 Byte							
New Data Flag				Size		I	D	I	D	I	D	I	D	I	D
0	1	1	0	S1	S2	Pointer Range = 0 - 103 decimal							

A normal NDF is shown (new data flag = 1001); S1S2 = 11; Positive Justification = Invert the 5 I-bits; Negative Justification = Invert the 5 D-bits; shown MSB (bit 1) first.

1	V5 Byte			8
BIP-2	REI-V	RFI-V	Signal Label	RDI-V

Shown MSB (bit 1) first. REI-V is also known as FEBE. RDI-V set to a 1 for Unequipped, AIS-V and LOP-V.

1	Z7 Byte				8
R	R	R	R	3-bit RDI-V	R

3-bit RDI-V Codes: 001 = no defects; 010 = Signal label mismatch; 101 = AIS-V or LOP-V; 110 = Unequipped.

Figure 2. VT1.5/ TU-11 Asynchronous and Byte Synchronous Mappings

The Desynchronizer/ Demapper block takes the data and alarm information, along with pointer information, and extracts the DS1 signal. This block extracts the optional overhead bytes and sends V5, Z6/N2, O and Z7/ K4 to the Auxiliary Port for Asynchronous mode. For Byte Synchronous mode, the O bytes are omitted and the signaling bits are sent to the Transmit Signaling Store instead. In both modes the data is sent to a pointer leak buffer which is programmable for leak out rate. This is used to minimize jitter and wander on Asynchronously mapped signals as well as to smooth out Byte Synchronously mapped signals that utilize pointer movements for frequency adjustment. The Desynchronizer uses a DPLL operated from the signal on SRCLK (48.636 MHz) that smooths out the stuffing jitter and compensates for the demapping gapped positions used for all orders of overhead. The Desynchronizer outputs a DS1 clock along with the DS1 data to the Transmit Line Interface block ready for transmission or framing without additional de-jittering. In Byte Synchronous mode the Frame pulse (3.0 ms) is decoded from the P1P0 bits and is used to align the signaling highway to the Transmit Signaling Store, and it becomes the signal on TSYNCn. Alarm information (RFI and AIS) is sent to the Transmit Alarm block for forwarding on the signaling highway. AIS is used to cause the DPLL to output an in-frequency-range all-ones signal.

The Telecom Bus Input and Output Control blocks buffer the assembled VT1.5/ TU-11 bytes for insertion to or extraction from the Telecom Bus Interface. Each of the seven mapper channels can independently be placed on or independently taken from any one of three STS-1s or TUG-3s (19.44 MHz Telecom bus only), any one of seven VT groups or TUG-2s, and any one of four VT1.5 or TU-11s. Enable control bits allow a channel to be disconnected in transmit and/or receive from the Telecom Bus.

The Telecom Bus Interface block combines the signals from the seven mapper channels and synchronizes them to the Add Bus half of the Telecom Bus based on the ACLK, AC1J1V1 and ASPE signals. It can be configured as a single STS-1 (6.48 MHz), an STS-3 (19.44 MHz) or an STM-1 (19.44 MHz). Contention checks are made for the seven mapper channels; this feature is extended using the $\overline{\text{BUSCHK}}$ pins to up to 3 additional DS1MX7 devices sharing an Add Bus. Parity (pin APAR) and an add indication (pin $\overline{\text{AADD}}$) are included with the byte-wide data (pins AD(0-7)). The DATEN and $\overline{\text{MASTER}}$ pins allow optional drive of overhead and stuff columns. The Drop Bus part of the Telecom Bus provides DCLK, DC1J1V1 and DSPE signals along with a failure indication (pin DFAIL) to indicate to the seven mapper channels that the received data is errored due to higher order path, section or line failures. Parity (pin DPAR) is included with the data (pins DD(0-7)). Parity covers add and drop data and optionally SPE and C1J1V1 signals. All signals are monitored for failure and maskable interrupts may be generated both to the microprocessor interrupt pin and to a separate failure pin ($\overline{\text{IAO}}$).

The DS1MX7 has a PRBS Generator and Analyzer block. The Generator and Analyzer supports the 2^{15}-1 pattern. The Generator output may be substituted in place of the NRZ data stream output from each Receive Line Interface Decoder. The Analyzer monitors one of the NRZ data stream outputs from the seven Receive Line Interface Decoders. By setting the Telecom Bus Loopback (a function of the Telecom Bus Interface block) and a Tributary Loopback for one of the seven channels, the entire channel's transmit and receive path can be verified (Synchronizer/ Mapper, VT Termination, Telecom Bus Interface, Desynchronizer/ Demapper, Transmit Line Interface and Receive Line Interface). By moving the loopbacks to Framers, LIUs, VT Switches or remote end Mappers an entire path can be verified.

The Line Interface Control block is a common block to all seven mapper channels that provides a serial port for communicating with an external line interface transceiver that supports'Host Mode' operation. This allows the system microprocessor to control the transceiver through the DS1MX7. The interface consists of a data output pin (LSDO), clock output pin (LSCLK), and a data input pin (LSDI). These signals are shared between all of the transceivers. Each transceiver is selected by the DS1MX7, using chip select output signals ($\overline{\text{LCSn}}$). In addition, a general purpose input pin (LAISn) can be used in NRZ mode to generate a maskable interrupt.

The Test Access Port block is common to all seven mapper channels and includes a five-pin Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This block provides external boundary scan to read and write the DS1MX7 input and output pins from the TAP for board and component testing. In addition, a four-byte read only memory location is provided for reading the JEDEC manufacturer ID, DS1MX7 part number, and version number of the part. For non-boundary scan testing a $\overline{\text{HIGHZ}}$ pin is provided to tri-state all output pins.

The DS1MX7 provides a common six-wire Ring Port block. A pair of DS1MX7 devices can operate on a dual bus-based Add Drop Multiplexer. Since each DS1MX7 is configured to operate in a single one direction of the ring, RDI and REI (FEBE) values need to be sent to the mate DS1MX7 so that they are returned in the opposite direction. The Ring Port is shared among the seven mapper channels to facilitate the function of sending, receiving and buffering REI (FEBE) and RDI values from and for each of the seven mapper channels. The REI (FEBE) and RDI information used by the Mapper may either come from the demap direction within the DS1MX7 (non-ring mode), from a microprocessor-forced value, or from the Ring Port. The Ring Port outputs clock, data and frame (pins ORPCKO, ORPDTO and ORPFMO), and it expects clock, data and frame as inputs (pins IRPCKI, IRPDTI and IRPFMI).

A common Auxiliary Port block is provided that makes the optional and reserved overhead bytes to and from each of the seven mapper channels available on multiplexed DS1MX7 device pins. The Auxiliary Port outputs the V5, J2, Z6/N2, Z7/K4 and O bytes as they arrive, if enabled. When mapping opportunities for J2, Z6/N2, Z7/K4 and O bytes come up the Auxiliary Port requests and inputs these bytes, if enabled. Microprocessor read and write access of these bytes is also provided.

The DS1MX7 can be configured to operate with either Intel or Motorola-compatible microprocessors via the Microprocessor Input/Output Interface block. Separate address, data and control pins are provided. Interrupt capability is provided with global and individual framer mask bits as well as activity registers to guide software to the exact cause of an interrupt in the most expeditious manner. A wide variety of alarms is provided on a global level as well as on a per mapper channel level. Each alarm or error is reflected in a current status register or counter as well as a latched value register that may be set on the rising, falling or both edges of an alarm. Shadow registers for alarms and counters are provided, with the alarm shadow registers doubled to indicate either a change (performance item) or a persistent condition (fault). Any latched value may trigger an interrupt, unless it is masked to prevent it causing an interrupt. An option is provided in software which permits the interrupt polarity to be inverted. An external system clock provided at pin PCKI is used to run the internal state machines.

PIN DIAGRAM

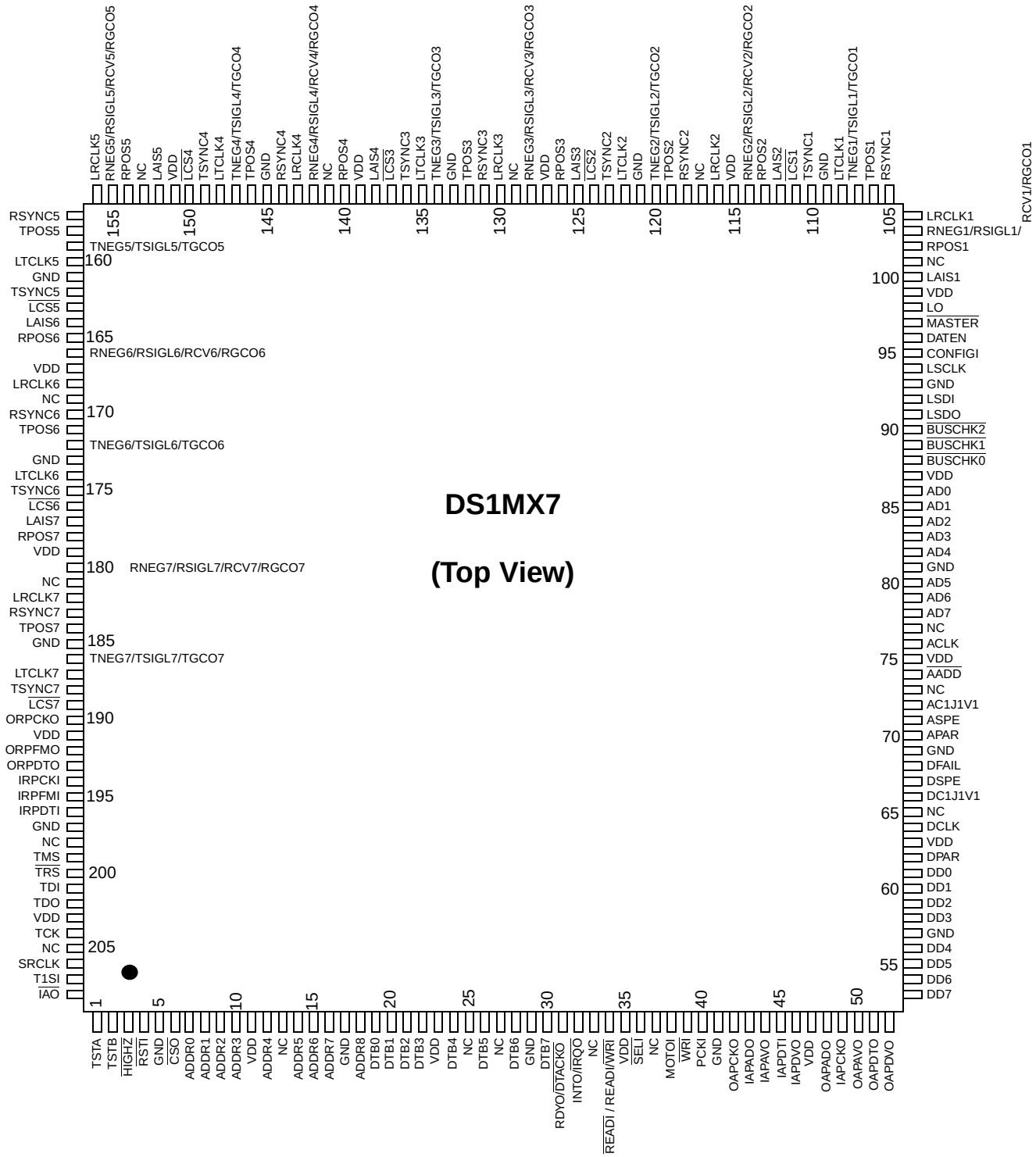


Figure 3. DS1MX7 TXC-04201B Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	11, 23, 35, 47, 63, 75, 87, 99, 115, 127, 139, 151, 167, 179, 191, 203	P		**VDD:** +5 volt supply, ± 5%
GND	5, 17, 29, 41, 57, 69, 81, 93, 109, 121, 133, 145, 161, 173, 185, 197	P		**GND:** Ground
NC	13, 25, 27, 33, 37, 65, 73, 77, 101, 117, 129, 141, 153, 169, 181, 198, 205			**NC**: Not Connected. Leave floating. Do not make any external connections to these pins or connect them to one another. Connection may impair performance or cause damage to the device.

*Note: I = Input; O = Output; P = Power

PER CHANNEL TRIBUTARY I/O (n = 1 TO 7)

Symbol	Pin No.	I/O/P	Type *	Name/Function
LRCLKn	104, 116, 130, 143, 156, 168, 182	I/O	CMOS	**Line Receive Clock Input:** 1.544 MHz ± 200 Hz clock from DSX-1 receiver for Asynchronous mapping mode; (tolerance is ± 50 Hz per ANSI and Bellcore for Byte Synchronous operation). Global control bit RCAE (bit 6) in register 007H determines the active edge of this clock. Input jitter tolerance is 5 UI peak to peak from 10 Hz to 500 Hz and 0.1 UI peak to peak from 8 kHz to 40 kHz. See Bellcore TR-TSY-000499. For Byte Synchronous operation with an external slip buffer for which control bits MODE1,0 (bits 1 and 0) in register X+00H are set to 10, LRCLKn is an output derived from pin LO.
RSYNCn	105, 118, 131, 144, 157, 170, 183	I/O	CMOS	**Receive Frame Sync.:** 3.0 millisecond multi-frame sync from framer, or to framer for Byte Synchronous mode. Sampled on LRCLKn falling edge if global control bit RCAE (bit 6) in register 007H is set to a 0. For Byte Synchronous operation with an external slip buffer for which control bits MODE1,0 (bits 1 and 0) in register X+00H are set to 10, RSYNCn is an output derived from pin LO.
RPOSn	102, 113, 126, 140, 154, 165, 178	I	CMOS	**Tributary Receive Data (Positive):** NRZ/Positive rail. DS1 data from framer or DSX-1 Receiver. RPOSn is sampled on LRCLKn falling edge if global control bit RCAE (bit 6) in register 007H is set to a 0. In NRZ mode, global control bit RXNRZP (bit 4) in register 007 selects the polarity (a 1 selects a low as a logical one).

*Note: See Input, Output and Input/Output Parameters section below for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
RNEGn/	103, 114, 128, 142, 155, 166, 180	I/O	CMOS	**Tributary Receive Data (Negative):** Negative rail DS1 data from DSX-1 receiver. This pin is sampled on LRCLKn falling edge if global control bit RCAE (bit 6) in register 007H is set to a 0.
RSIGLn/				**Receive Signaling Highway Input:** Signaling Highway from framer. Sampled on LRCLKn falling edge if global control bit RCAE (bit 6) in register 007H is set to a 0.
RCVn				**Tributary Receive Code Violations:** Code violation counter input. Sampled on LRCLKn falling edge if global control bit RCAE(bit 6) in register 007H is set to a 0.
RGCOn				**Receive Gapped Clock Output:** When the datacom mode is selected (only available for Byte Synchronous operation) via control bit DATACOM (bit 5) in per channel register X+00H being set to a 1, this pin provides a gapped clock output in which the gap appears at the Frame bit times on RPOSn.
LAISn	100, 112, 125, 138, 152, 164, 177	I	CMOS	**Line Alarm Input:** Line transceiver interrupt, AIS or Loss of Signal / Clock from DSX-1 receiver.The active level is determined by global control bit RXNRZP (bit 4) in register 007, which selects the polarity (a 1 selects a low as a logical one). A per channel control bit EXPLOS (bit 6) in register X+00H enables this pin to act as LOS if set to a 1. Control bit LOS2AIS (bit 6) in register X+01H, when set to a 1, causes this signal to propagate VT AIS upstream. When EXPLOS is set to a 0, status bit XPS (bit 7) in register X+10H becomes a separate status indication with latched, mask, performance and fault registers plus global mask and status capability
LTCLKn	108, 122, 135, 148, 160, 174, 187	O	CMOS	**Line Transmit Clock Output:** 1.544 MHz ± 200 Hz clock to DSX-1 line driver or framer. Global control bit TCAE (bit 7) in register 007H determines the active edge of this clock. See $\overline{\text{CSO}}$ below. The output frequency tracks the input frequency as defined by the synchronized payload. Output jitter caused by desynchronization and single pointer movements is 0.4 UI or less peak to peak at 10 Hz and above (0.075 UI peak to peak or less from 8 kHz to 40 kHz).
TPOSn	106, 119, 132, 146, 158, 171, 184	O	CMOS	**Tributary Transmit Data (Positive):** NRZ/Positive DS1 data to DSX-1 line driver or framer. Output on LTCLKn rising edge if global control bit TCAE (bit 7) in register 007H is set to a 1. In NRZ mode, global control bit TXNRZP (bit 0) in register 007H selects the polarity (a 1 selects a low as a logical one). Also see $\overline{\text{CSO}}$ below.

Symbol	Pin No.	I/O/P	Type	Name/Function
TNEGn/	107, 120, 134, 147, 159, 172, 186	O	CMOS	**Tributary Transmit Data (Negative):** Negative rail DS1 data to DSX-1 line driver output on LTCLKn rising edge if global control bit TCAE (bit 7) in register 007H is set to a 1. When NRZ mode is used in Asynchronous mode this pin can be used as a spare output (e.g., select B8ZS/AMI in line I/F transceiver). Also see $\overline{\text{CSO}}$ below.
TSIGLn				**Transmit Signaling Highway Output:** Signaling highway to framer. Output on LTCLKn rising edge if global control bit TCAE (bit 7) in register 007H is set to a 1. Also see $\overline{\text{CSO}}$ below.
TGCOn				**Transmit Gapped Clock Output:** When the Datacom mode is selected (only available for Byte Synchronous operation) via control bit DATACOM (bit 5) in per channel register X+00H being set o a 1, this pin provides a gapped clock output in which the gap appears at the frame bit times on TPOSn.
TSYNCn	110, 123, 136, 149, 162, 175, 188	O	CMOS	**Transmit Frame Sync:** 3.0 millisecond multi-frame sync to framer. Output on LTCLKn rising edge if global control bit TCAE (bit 7) in register 007H is set to a 1. Also see $\overline{\text{CSO}}$ below.
$\overline{\text{LCSn}}$	111, 124, 137, 150, 163, 176, 189	O	CMOS	**Line Interface Transceiver Chip Select:** An active low signal that enables communications in both directions between the external line interface transceiver for channel n and the DS1MX7. This pin is under control of global register 01AH where ENSRP (bit 4) enables transmission to channel n, which is selected by BDCST (bit 7) to select all channels or the channel selection controls (bits 2-0) which select one of the 7 channels.

TRIBUTARY COMMON CONTROL

Symbol	Pin No.	I/O/P	Type	Name/Function
LO	98	I	CMOS	**Local Oscillator:** 1.544 MHz ± 32 ppm system clock input used for Byte Synchronous mode. 1.544 MHz synchronized to system (ASPE, ACLK and a specific J1 of AC1J1V1) for Byte Synchronous operation where LRCLKn and RSYNCn are outputs. This signal is also used to generate the serial port clock output LSCLK.
SRCLK	206	I	CMOS	**System Reference Clock:** 48.636 MHz ± 32 ppm (31.5 times 1.544 MHz) system clock input used to operate the synchronizer, desynchronizer, PRBS generator/ analyzer, and to generate DS1 AIS.

Symbol	Pin No.	I/O/P	Type	Name/Function
LSDO	91	O	CMOS	**Line Interface Transceiver Data Output Signal:** Common serial control data bus output shared by the seven channels. A command byte followed by a data byte, as stored in control registers 017H and 018H respectively, is transmitted to the line interface transceiver selected by $\overline{\text{LCS}}$n.
LSDI	92	I	CMOS	**Line Interface Transceiver Data Input Signal:** Common serial control data bus input. A data byte coincident with the data byte on LSDO is clocked into the DS1MX7 and stored in register 019H from the line interface transceiver selected by $\overline{\text{LCS}}$n.
LSCLK	94	O	CMOS	**Line Interface Transceiver Clock Signal:** Common serial control bus clock output. A 1.544 MHz clock derived from LO. LSDO is clocked out of the DS1MX7 on the falling edge of LSCLK and LSDI is clocked into the DS1MX7 on the rising edge of LSCLK.
T1SI	207	I	TTL	**One Second Performance Clock Input:** Shadow register latch. This input operates the latched counters and PM/FM registers. The following parameter value limits are suggested to prevent counters from overflowing when operating in noisy environments or other unfavorable conditions: min. high time 0.50 ms; min. low time 3.0 ms; max. low time 1.5 s. Operation at 1.0 Hz $\pm$ 32 ppm, 1.0 ms high time, is recommended. This clock is used in conjunction with global control bit ENPMFM (bit 3) in register 006H to clear per channel event registers (not device event registers) after the PM and FM registers have been updated.
$\overline{\text{IAO}}$	208	O	CMOS open drain (4mA)	**Internal Alarm Output:** Internal Alarm detected, active low output. Control bits in registers 01BH and 01CH, if set to a 1, enable Telecom Bus clock, payload and synch. failures, as well as parity errors and PRBS out of lock, to generate an alarm or interrupt on this pin,
$\overline{\text{CSO}}$	6	I	TTL	**Card Switch Off:** When driven low, LTCLKn, TPOSn, TNEGn/TSIGLn and TSYNCn are driven to a logic low level.

SYSTEM INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
DCLK	64	I	TTL	**Drop Bus Clock:** Telecom Bus clock for data from system; 6.48 MHz for pin CONFIGI tied high or 19.44 MHz for pin CONFIGI tied low. Control bit TBRCI (bit 4) in register 01EH set to a 0 selects the rising edge of DCLK as the active edge.
DC1J1V1	66	I	TTL	**Drop Bus C1J1V1 Indicator:** Telecom Bus C1#1, J1#1, or V1#1 valid from system. Valid on the rising edge of DCLK when control bit TBRCI (bit 4) in register 01EH is set to a 0. Used with DSPE to identify the start of the payload.
DSPE	67	I	TTL	**Drop Bus SPE Indicator:** Telecom Bus SPE valid from system. Valid on rising edge of DCLK when control bit TBRCI (bit 4) in register 01EH is set to a 0. This signal is high during all VT1.5 or TU-11 bytes from the system.
DD(0-7)	61, 60, 59, 58, 56, 55, 54, 53	I	TTL	**Drop Bus Data:** Telecom Bus data from system; DD0 is LSB. Valid on rising edge of DCLK when control bit TBRCI (bit 4) in register 01EH is set to a 0
DPAR	62	I	TTL	**Drop Bus Parity Bit:** Telecom Bus parity received over DD(0-7), DSPE and DC1J1V1. Valid on rising edge of DCLK when control bit TBRCI (bit 4) in register 01EH is set to a 0; odd/even selectable by control bit TBPE (bit 2) in register 007H; when set to a 1, even parity is selected. When control bit TBPIS (bit 3) in register 007H is set to a 0 only DD(0-7) is checked for parity.
DFAIL	68	I	TTL	**Drop Bus Signal Fail:** Signal fail indication valid on the rising edge of DCLK when control bit TBRCI (bit 4) in register 01EH is set to a 0. If DFAIL is high the specific VT slot contains invalid data (DD(0-7)); the per VT alarms are invalid and are masked; DS1 AIS is generated.
ACLK	76	I	TTL	**Add Bus Clock:** Telecom Bus clock for data to system; 19.44 MHz for pin CONFIGI tied high or 6.48 MHz for pin CONFIGI tied low. Control bit TBTCI (bit 5) in register 01EH set to a 0 selects the falling edge of ACLK as the active edge. From the system it is used to clock out AD(0-7) and APAR on its falling edge (control bit TBTCI = 0) so that these signals are readable by the system on the rising edge.
AC1J1V1	72	I	TTL	**Add Bus C1J1V1 Indicator:** Telecom Bus C1#1, J1#1, V1#1 valid for data to system. Valid on the falling edge of ACLK when control bit TBTCI (bit 5) in register 01EH is set to a 0. Used with ASPE to indicate the start of the payload to the system.

Symbol	Pin No.	I/O/P	Type	Name/Function
ASPE	71	I	TTL	**Add Bus SPE Indicator:** Telecom Bus SPE valid for data to system. Valid on the falling edge of ACLK when control bit TBTCI (bit 5) in register 01EH is set to a 0. This signal is high during all VT1.5 or TU-11 bytes to the system.
AD(0-7)	86, 85, 84, 83, 82, 80, 79, 78	O(T)	TTL 4mA	**Add Bus Data:** Telecom Bus data to system; AD0 is LSB. Valid on the falling edge of ACLK when control bit TBTCI (bit 5) in register 01EH is set to a 0. Control bit TBDD (bit 3) in register 01EH selects zero ACLK clock period delay if set to a 0 and a single ACLK clock period delay if set to a 1.
APAR	70	O(T)	TTL 4mA	**Add Bus Parity Bit:** Telecom Bus parity generated for any AD(0-7), ASPE and AC1J1V1 placed on the Telecom Bus. Valid on the falling edge of ACLK when control bit TBTCI (bit 5) in register 01EH is set to a 0; odd/even selectable by control bit TBPE (bit 2) in register 007H; when set to a 1 even parity is selected. When control bit TBPIS (bit 3) in register 007H is set to a 0 only AD(0-7) is included in the parity calculation. Control bit TBDD (bit 3) in register 01EH selects zero ACLK clock period delay if set to a 0 and a single ACLK clock period delay if set to a 1.
$\overline{\text{AADD}}$	74	O(T)	TTL 4mA	**Add Bus Add Data Present Indicator:** Telecom Bus device outputs valid. This signal goes low on the falling edge of ACLK when control bit TBTCI (bit 5) in register 01EH is set to a 0 if the DS1MX7 writes to the Telecom Bus, allowing for external drivers to be used. Control bit TBDD (bit 3) in register 01EH selects zero ACLK clock period delay if set to a 0 and a single ACLK clock period delay if set to a 1.
$\overline{\text{BUSCHK(0-2)}}$	88, 89, 90	I	TTL	**Add Bus Check:** Used to determine if another DS1MX7 on the same Telecom Bus is driving in the same slot. Each $\overline{\text{BUSCHK}}$ input is connected to the $\overline{\text{AADD}}$ of another DS1MX7. If a collision is detected, status bit TBXES (bit 0) in register 00BH is set to a 1. Latched value, mask PM, and FM register bits are also supplied.
$\overline{\text{MASTER}}$	97	I	TTLp	**Add Bus Master:** When tied to ground, POH and stuff columns are driven to zero on AD(0-7) with correct parity. See the Telecom Bus Operations subsection.
DATEN	96	I	TTL	**Add Bus Data Enable:** When high, AD(0-7), APAR and $\overline{\text{AADD}}$ are enabled. It is normally tied to ASPE to float the Telecom Bus during TOH.
CONFIGI	95	I	TTL	**Add/Drop Bus Configuration Input:** Configuration of the Telecom Bus. For CONFIGI high, Telecom Bus is 28 slot/6.48 MHz. For CONFIGI low, Telecom Bus is 84 slot/ 19.44 MHz.

AUXILIARY PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
OAPCKO	42	O	CMOS	**Output Auxiliary Port Clock:** DCLK divided by 2 when CONFIGI is high. DCLK divided by 4 when CONFIGI is low.
OAPAVO	50	O	CMOS	**Output Auxiliary Port Address Valid:** OAPAVO is High during the 12 AddreSS-bits of OAPADO. Information is clocked out on the falling edge of OAPCKO.
OAPADO	48	O	CMOS	**Output Auxiliary Port Address:** Address information identifying O-bits, V5, J2, Z6/N2, or Z7/K4 information that will be output on OAPDTO. Information is clocked out on the falling edge of OAPCKO.
OAPDVO	52	O	CMOS	**Output Auxiliary Port Data Valid:** OAPDVO is High during the eight Data Bits of OAPDTO. Information is clocked out on the falling edge of OAPCKO.
OAPDTO	51	O	CMOS	**Output Auxiliary Port Data:** This pin provides the data byte specified in the preceding OAPADO Address. Information is clocked out on the falling edge of OAPCKO.
IAPCKO	49	O	CMOS	**Input Auxiliary Port Clock:** ACLK divided by 2 when CONFIGI is high. ACLK divided by 4 when CONFIGI is low.
IAPAVO	44	O	CMOS	**Input Auxiliary Port Address Valid:** IAPAVO is High during the 12 Address Bits of IAPADO. Information is clocked out on the falling edge of IAPCKO.
IAPADO	43	O	CMOS	**Input Auxiliary Port Address:** Address information identifying O-bits, J2, Z6/N2, or Z7/K4 information that will be input on IAPDTI. Information is clocked out on the falling edge of IAPCKO.
IAPDVO	46	O	CMOS	**Input Auxiliary Port Data Valid:** IAPDVO is High during the eight Data Bits of IAPDTI. Information is clocked out on the falling edge of OAPCKO.
IAPDTI	45	I	TTL	**Input Auxiliary Port Data:** This pin accepts the data byte specified in the preceding IAPADO Address. Information is clocked in on the second rising edge of IAPCKO after the rising edge of IAPDVO.

RING PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
ORPCKO	190	O	CMOS	**Output Ring Port Clock:** Burst of 56 clock pulses at 1.944 Mbit/s.
ORPFMO	192	O	CMOS	**Output Ring Port Frame:** Active High signal during Bit 0 of Channel 1. ORPFMO is clocked out on the falling edge of ORPCKO.
ORPDTO	193	O	CMOS	**Output Ring Port Data:** REI-V (FEBE), RDI-VPD, RDI-VSD, and RDI-VCD data from all seven channels for use in PPS Ring applications. Information is clocked out on the falling edge of ORPCKO.
IRPCKI	194	I	TTL	**Input Ring Port Clock:** Burst of 56 clock pulses at 1.944 Mbit/s.
IRPFMI	195	I	TTL	**Input Ring Port Frame:** Active High signal during Bit 0 of Channel 1. IRPFMI is clocked on the rising edge of IRPCKI.
IRPDTI	196	I	TTL	**Input Ring Port Data:** REI-V (FEBE), RDI-VPD, RDI-VSD, and RDI-VCD data for all seven channels for use in PPS Ring applications. Information is clocked in on the rising edge of IRPCKI.

MICROPROCESSOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RSTI}}$	4	I	TTLp	**Hardware Reset:** Device reset. This active low signal will reset all seven DS1 mappers. It should be held low for a minimum of 4 clock periods of PCKI.
MOTOI	38	I	TTL	**Motorola Mode:** Motorola - Intel microprocessor mode select. High selects Motorola. Low selects Intel.
DTB(0-7)	19, 20, 21, 22, 24, 26, 28, 30	I/O	TTL 8mA	**Data:** Microprocessor bidirectional, tri-state data bus; DTB0 is LSB.
ADDR(0-8)	7, 8, 9, 10, 12, 14, 15, 16, 18	I	TTL	**Address Bus:** Microprocessor address bus; ADDR0 is LSB.
$\overline{\text{SELI}}$	36	I	TTLp	**Select:** Microprocessor Interface select. A low selects the interface and allows the transfer of information between the DS1MX7 and the microprocessor.
$\overline{\text{READI}}$ / READI/$\overline{\text{WRI}}$	34	I	TTL	**Read:** Read or Read/Write. Intel: low to read DS1MX7. Motorola: high to read/low to write.
$\overline{\text{WRI}}$	39	I	TTL	**Write:** Intel mode only; low to write to DS1MX7.

Symbol	Pin No.	I/O/P	Type	Name/Function
RDYO/	31	O(T)	TTL 8mA	**Ready:** Intel mode: A high acknowledges that data transfer can take place this cycle. A low indicates wait states.
$\overline{\text{DTACKO}}$				**Data Transfer Acknowledge:** Motorola mode: A low during read indicates data bus is valid. A low during write indicates data is accepted.
INTO/	32	O	TTL 4mA	**Interrupt:** Intel mode: If control bit IPOL (bit 4) in register 006H is set to a 0, a high indicates an interrupt request to the microprocessor.
$\overline{\text{IRQO}}$				**Interrupt Request:** Motorola mode: If control bit IPOL (bit 4) in register 006H is set to a 0, a low indicates an interrupt request to the microprocessor.
PCKI	40	I	TTL	**Processor Clock:** Processor Clock Input. Required for device operation; 8 to 20 MHz. DS1MX7 will continue to pass data on loss of PCKI, but microprocessor access will be blocked.

TEST ACCESS PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	204	I	TTL	**Test Clock:** IEEE 1149.1 Boundary Scan Clock input. This clock is used to shift data into TDI on the rising edge and out of TDO on the falling edge.
TDI	201	I	TTLp	**Test Data Input:** Boundary Scan Data input. Serial test instructions and data are clocked into this pin on the rising edge of TCK.
TDO	202	O(T)	TTL4mA	**Test Data Output:** Boundary Scan Data output. Serial data and test instructions are clocked out of this pin on the falling edge of TCK.
TMS	199	I	TTLp	**Test Mode Select:** Boundary Scan Test Mode Select input; sampled by TCK rising edge to put DS1MX7 into test mode.
$\overline{\text{TRS}}$	200	I	TTLp	**Test Reset:** Boundary Scan Reset input. This pin will asynchronously reset the Test Access Port (TAP) controller if held low for a minimum duration of 300 ns. This pin is to be held low, asserted low or pulsed low to reset the TAP controller on DS1MX7 power-up.
$\overline{\text{HIGHZ}}$	3	I	CMOS	**High Impedance Select:** Grounding this pin causes all outputs except TDO to go high impedance but alters no internal registers.
TSTA	1	I	CMOS	**Test A:** Device test pin. Must be connected to ground.
TSTB	2	I	CMOS	**Test B:** Device test pin. Must be connected to ground.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		$\pm$2000	V	per MIL-STD-833D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance from junction to ambient, θ_{JA}			30	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD} supply voltage	4.75	5.0	5.25	V	
I_{DD} supply current		180		mA	Asynchronous mapping; CONFIGI = High. V_{DD} = 5.0 V. T_A = 25 ^oC
P_{DD} supply power		900		mW	Asynchronous mapping; CONFIGI = High. V_{DD} = 5.0 V. T_A = 25 ^oC
I_{DD} supply current			280	mA	Byte Synchronous mapping; CONFIGI = Low. V_{DD} = 5.25V. T_A = 85 ^oC.
P_{DD} supply power			1500	mW	Byte Synchronous mapping; CONFIGI = Low. V_{DD} = 5.25V. T_A = 85 ^oC.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 x V_{DD}			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.3 x V_{DD}	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		2.5		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	
Input capacitance		2.5		pF	

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current		0.5	1.4	mA	V_{DD} = 5.25; Input = 0 volts
Input capacitance		2.5		pF	

Note: Input has a 9K (nominal) internal pull-up resistor.

OUTPUT PARAMETERS FOR CMOS/TTL 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			11	ns	C_{LOAD} = 50 pF
t_{FALL}			7.0	ns	C_{LOAD} = 50 pF
Leakage Tri-state			±10	µA	0 to 5.25 V input

OUTPUT PARAMETERS FOR CMOS OPEN DRAIN (4mA)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
t_{FALL}			7.0	ns	C_{LOAD} = 50 pF
High Z leakage current			10	µA	V_{DD} = 5.25

Note: Open Drain requires use of 4.7 kOhm external pull-up resistor. If this resistor is not provided the output behaves as tri-state.

OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			6.0	ns	C_{LOAD} = 50 pF
t_{FALL}			4.0	ns	C_{LOAD} = 50 pF

INPUT/OUTPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 x V_{DD}		V_{DD} + 0.5	V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.3 x V_{DD}	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance			2.5	pF	
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			6.0	ns	C_{LOAD} = 50 pF
t_{FALL}			4.0	ns	C_{LOAD} = 50 pF

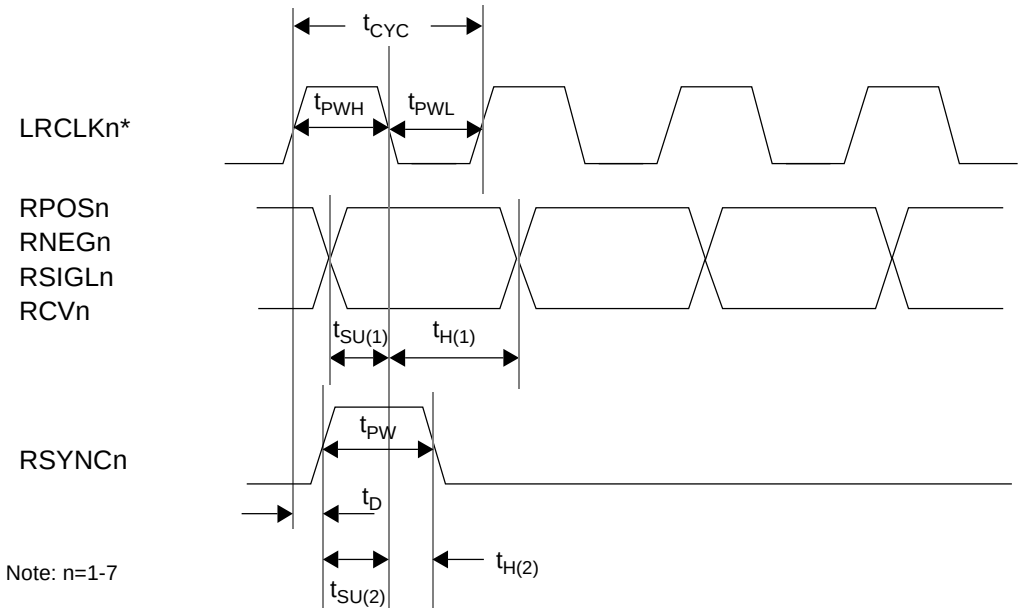
INPUT/OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance			2.5	pF	
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			6.0	ns	$C_{LOAD} = 50$ pF
t_{FALL}			4.0	ns	$C_{LOAD} = 50$ pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the DS1MX7 are illustrated in Figures 4 through 18, with values of the timing intervals tabulated below each diagram. All output times are measured with a maximum 25 pF load capacitance, unless otherwise indicated. Timing parameters are measured at voltage levels of $(V_{OH} + V_{OL})/2$ for output signals or $(V_{IH} + V_{IL})/2$ for input signals.

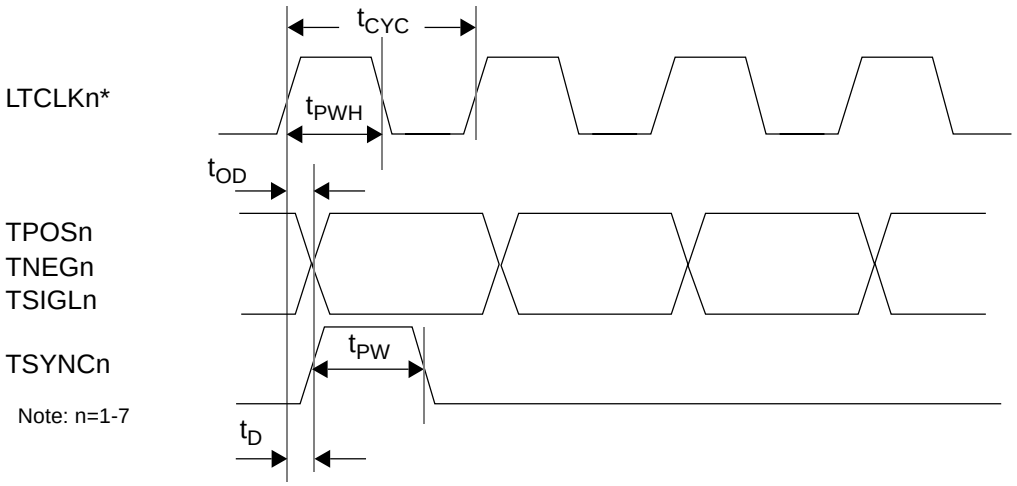
Figure 4. Tributary Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn clock period	t_{CYC}	560	648		ns
LRCLKn high time	t_{PWH}	240			ns
LRCLKn low time	t_{PWL}	240			ns
RPOS/RNEG/RSIGL/RCV set-up time to LRCLK↓	$t_{SU(1)}$	50			ns
RPOS/RNEG/RSIGL/RCV hold time after LRCLK↓	$t_{H(1)}$	50			ns
RSYNC pulse width as input	t_{PW}	500		750	ns
RSYNC pulse width as output	t_{PW}	560	648		ns
RSYNC setup as input before LRCLK↓	$t_{SU(2)}$	50			ns
RSYNC hold as an input after LRCLK↓	$t_{H(2)}$	50			ns
RSYNC delay as output after LRCLK↑	t_D			50	ns

* LRCLKn may be inverted via control bit RCAE (bit 6) in register 007H; as shown RCAE = 0.

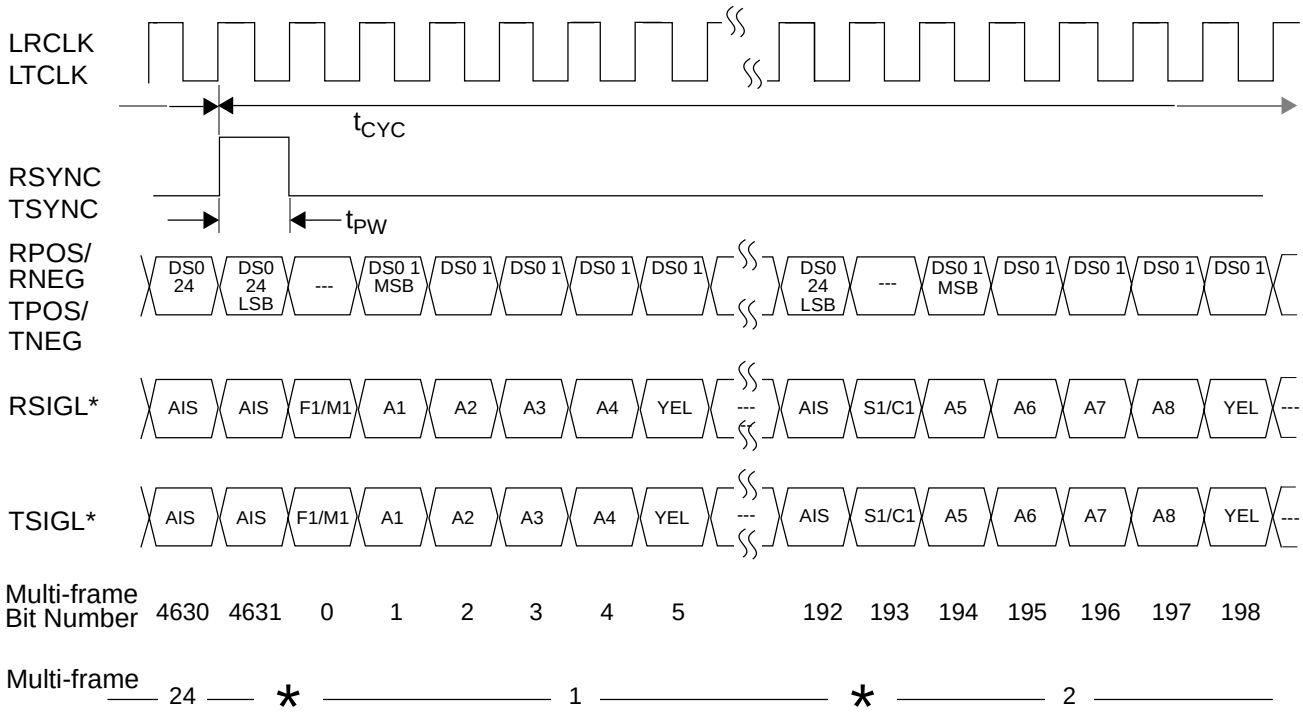
Figure 5. Tributary Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn clock period	t_{CYC}	637	648	656	ns
LTCLKn duty cycle, t_{PWH}/t_{CYC}	--	45		55	%
TPOS/TNEG/TSIGL output delay after LTCLK↑	t_{OD}	-5.0		50	ns
TSYNC delay after LTCLK↑	t_D	-5.0		50	ns
TSYNC pulse width	t_{PW}	637	648	656	ns

* LTCLKn may be inverted via control bit TCAE (bit 7) in register 007H; as shown TCAE = 1.

Figure 6. Signaling Highway Structure



Note: n=1-7

Note 1: * shown for 16-state signaling. See Operation section.

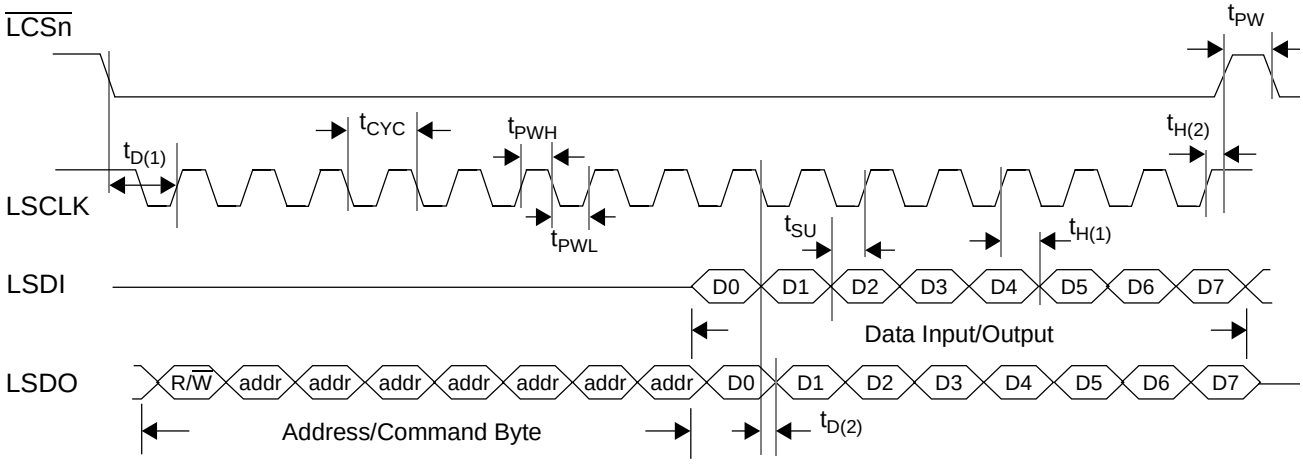
Note 2: "---" in TPOS, TNEG, RPOS, RNEG, RSIGL, and TSIGL are unused bits (see Operation section).

Note 3: AIS is present in DS0 bit positions 16 through 192 (DS0 3 - DS0 24); bits 6 through 15 are unused.

Parameter	Symbol	Min	Typ	Max	Unit
TSYNCn/RSYNCn clock period (n=1-7)	t_{CYC}		3.000		ms
TSYNCn/RSYNCn pulse width (n=1-7)	t_{PW}		One clock period of LTCLK or LRCLK*		ns

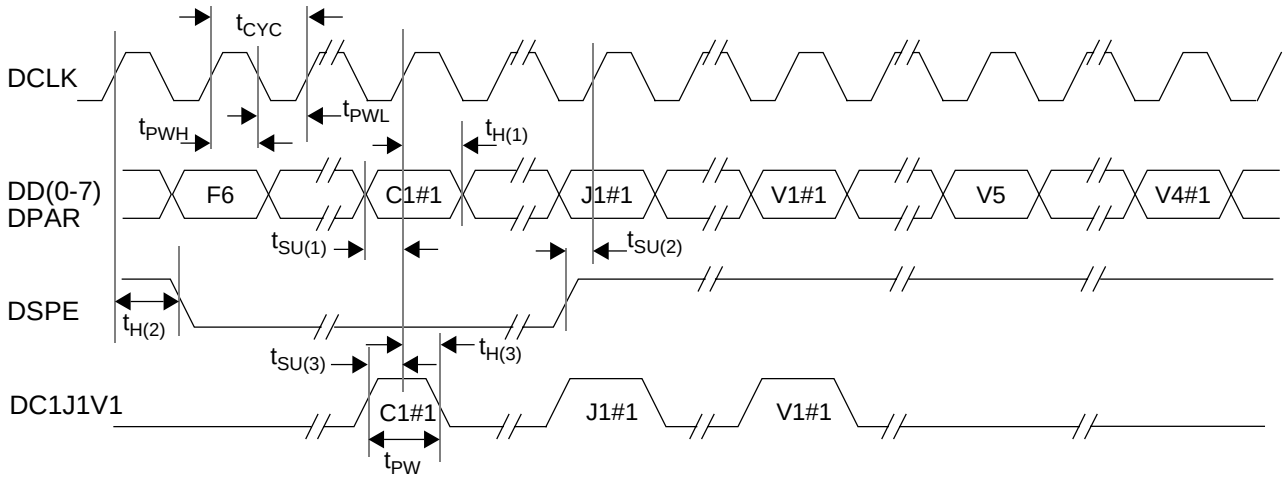
* TSYNC or RSYNC should be valid on the active edge of LTCLK or LRCLK, respectively.

Figure 7. Serial Control Port Structure and Timing



Parameter	Symbol	Min	Typ	Max	Unit
LSCLK clock period	t_{CYC}	560	648		ns
LSCLK high time	t_{PWH}	280			ns
LSCLK low time	t_{PWL}	280			ns
$\overline{LCSn}$ delay time to LSCLK↑	$t_{D(1)}$	100	324	350	ns
$\overline{LCSn}$ inactive pulse width	t_{PW}	300			ns
LSDI set-up time to LSCLK↑	t_{SU}	100			ns
LSDI hold time after LSCLK↑	$t_{H(1)}$	100			ns
LSCLK↑ to LCSn inactive	$t_{H(2)}$	100			ns
LSDO delay after LSCLK↓	$t_{D(2)}$			100	ns
LSCLK rise and fall times (10% - 90%)	t_r, t_f			50	ns

Figure 8. Telecom Bus Input Timing

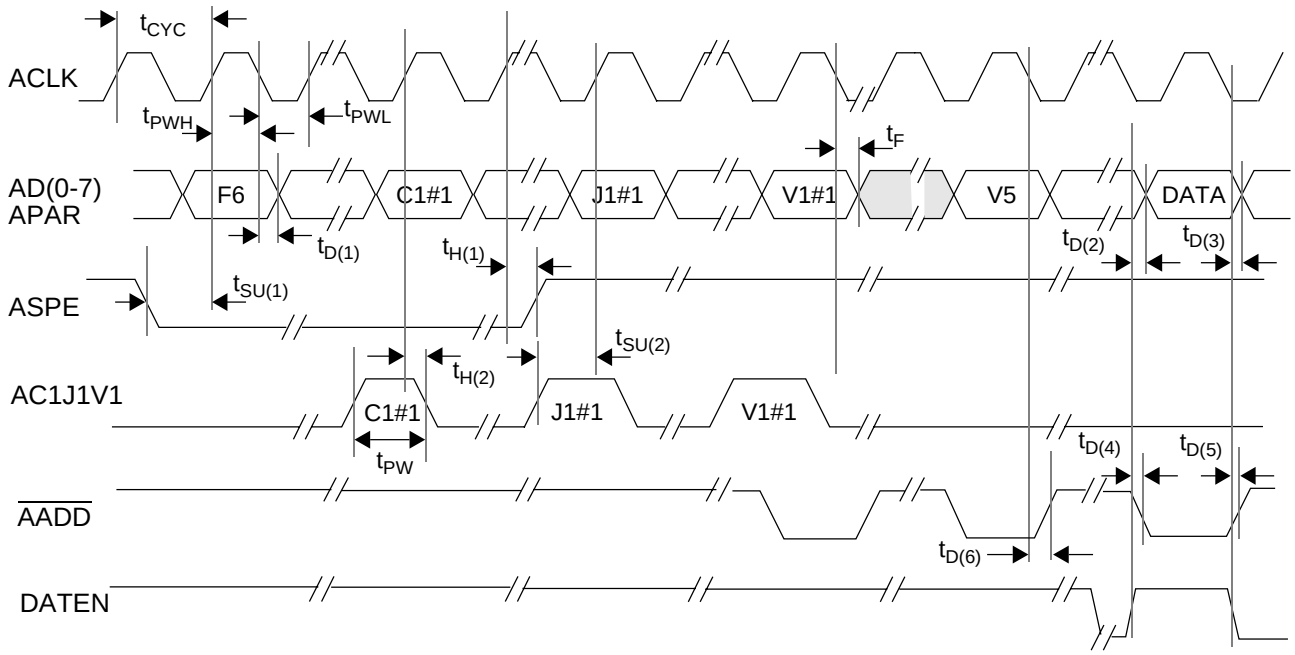


Parameter	Symbol	Min*	Typ*	Max*	Unit
DCLK clock period	t_{CYC}	150/50	154.32/51.44		ns
DCLK high time	t_{PWH}	38/23		116/29	ns
DCLK low time	t_{PWL}	38/23		116/29**	ns
DD(0-7)/DPAR set-up time to DCLK↑	$t_{SU(1)}$	7.0			ns
DD(0-7)/DPAR hold time after DCLK↑	$t_{H(1)}$	3.0			ns
DSPE set-up time to DCLK↑	$t_{SU(2)}$	7.0			ns
DSPE hold time after DCLK↑	$t_{H(2)}$	3.0			ns
DC1J1V1 set-up time to DCLK↑	$t_{SU(3)}$	7.0			ns
DC1J1V1 hold time after DCLK↑	$t_{H(3)}$	3.0			ns
DC1J1V1 pulse width	t_{PW}	40			ns

* The first number is for 6.48 MHz operation; the second is for 19.44 MHz operation (shown in timing diagram).

** For gapped clock applications, skipping a rising (and next falling) edge of DCLK will extend the current low time to twice the listed value. All data is clocked in on the rising clock edge unless control bit TBRCI (bit 4) in register 01EH is set to a 1, in which case all data is clocked in on the falling clock edge.

Figure 9. Telecom Bus Output Timing

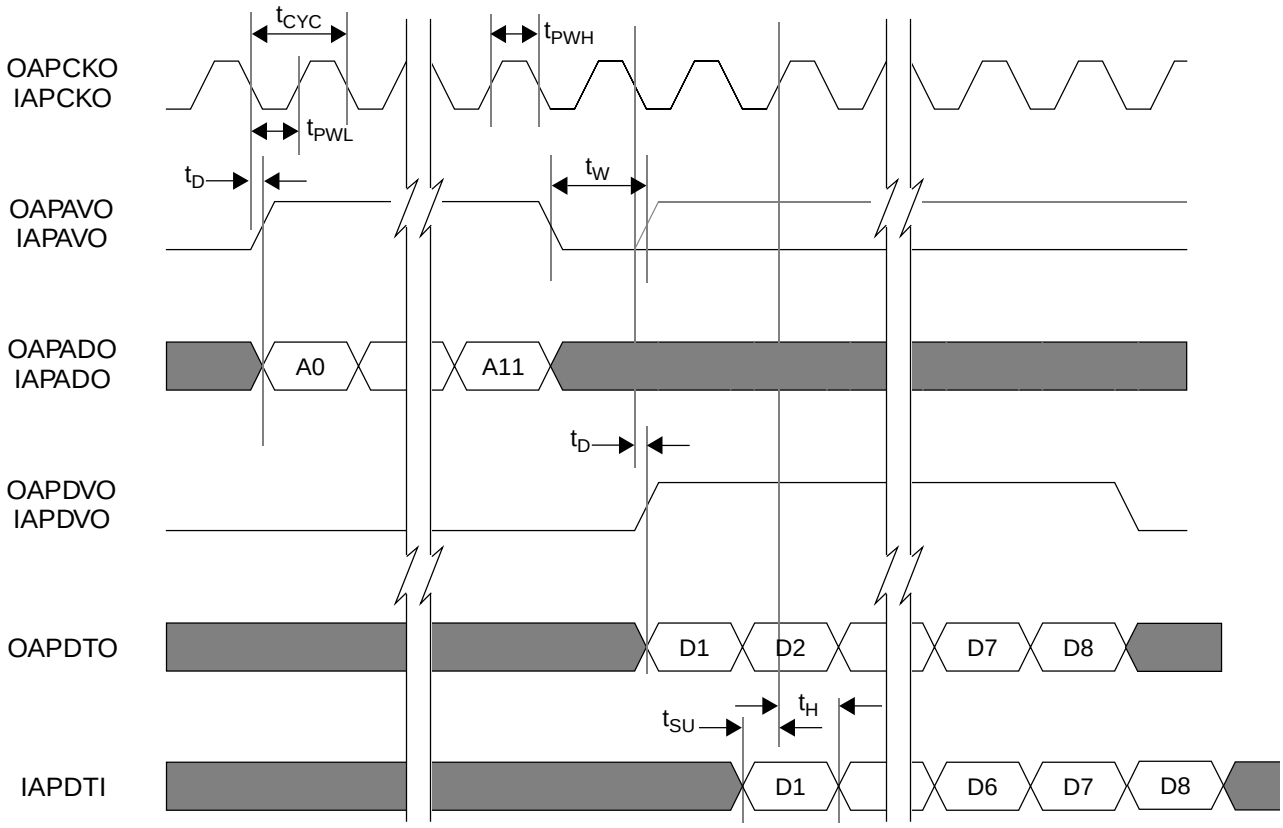


Parameter	Symbol	Min*	Typ*	Max*	Unit
ACLK clock period	t_{CYC}	150/50	154.32/51.44		ns
ACLK high time	t_{PWH}	38/23		116/29	ns
ACLK low time	t_{PWL}	38/23		116/29**	ns
AD(0-7)/APAR delay time after ACLK↓	$t_{D(1)}$	3.0		20	ns
AD(0-7)/APAR float time after ACLK↓	t_F	3.0		20	ns
ASPE set-up time to ACLK↑	$t_{SU(1)}$	7.0			ns
ASPE hold time after ACLK↑	$t_{H(1)}$	3.0			ns
AC1J1V1 set-up time to ACLK↑	$t_{SU(2)}$	7.0			ns
AC1J1V1 hold time after ACLK↑	$t_{H(2)}$	3.0			ns
AD(0-7)/APAR delay time after DATEN↑	$t_{D(2)}$			15.9	ns
AD(0-7)/APAR delay time after DATEN↓	$t_{D(3)}$			13.6	ns
$\overline{\text{AADD}}$ delay time after DATEN↑	$t_{D(4)}$			13.1	ns
$\overline{\text{AADD}}$ delay time after DATEN↓	$t_{D(5)}$			13.2	ns
$\overline{\text{AADD}}$ delay time after ACLK↓	$t_{D(6)}$	0.0		16.8	ns
AC1J1V1 pulse width	t_{PW}	120/40			ns
AD(0-7)/APAR rise/fall times (10% - 90%)	t_r, t_f			10.9	ns

* The first number is for 6.48 MHz operation; the second is for 19.44 MHz operation (shown in timing diagram).

** For gapped clock applications, skipping a rising (and next falling) edge of ACLK will extend the current low time to twice the listed value. If control bit TBTCI (bit 5) in register 01EH is set to a 0, all data is clocked in on the rising ACLK clock edge and out on the falling ACLK clock edge, as is shown in the timing diagram. If control bit TBTCI = 1, all data is clocked in on the falling clock edge and out on the rising clock edge of ACLK. If control bit TBDD = 1, AD(0-7), APAR and $\overline{\text{AADD}}$ are delayed one clock period from what is shown in the timing diagram with reference to ASPE and AC1J1V1.

Figure 10. Auxiliary Port Timing



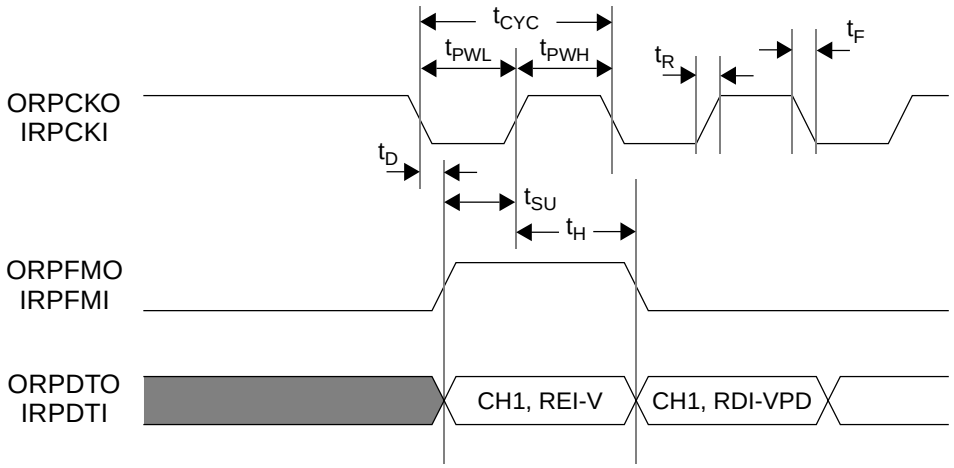
Parameter	Symbol	Min	Typ	Max	Unit
OAPCKO or IAPCKO period (2 times DCLK or ACLK clock period)	t_{CYC}		308.64/ 102.88*		ns
Delay - ↓OAPCKO to OAPAVO, OAPADO, OAPDVO or OAPDTO - ↓IAPCKO to IAPAVO, IAPADO, IAPDVO	t_D	-2.0		5.0	ns
Fall Time (90% - 10%)**–OAPAVO, OAPADO, OAPDVO, OAPDTO,IAPAVO, IAPADO, IAPDVO	t_F			6.0	ns
Hold - IAPDTI after ↑IAPCKO	t_H	3.0			ns
OAPCKO or IAPCKO High time	t_{PWH}	40	50	60	% t_{CYC}
OAPCKO or IAPCKO Low time	t_{PWL}	40	50	60	% t_{CYC}
Rise Time (10% - 90%)**- OAPAVO, OAPADO, OAPDVO, OAPDTO, IAPAVO, IAPADO, IAPDVO	t_R			6.0	ns
Setup - IAPDTI to ↑IAPCKO	t_{SU}	7.0			ns
Wait - OAPAVO or IAPAVO Low time	t_W	1.0			t_{CYC}

Notes: * The first number is for 6.48 MHz operation; the second is for 19.44 MHz operation.

1. ** 25 pF load

2. Auxiliary port transfers depend on the Telecom Bus add and drop assignments as controlled by registers X+04H and X+05H being valid, with control bit TBTVAL (bit 7) in register X+05H set to a 1 for auxiliary input timing (IAPAVO, IAPADO, and IAPADO) and control bit TBRVAL (bit 7) in register X+04H set to a 1 for auxiliary output timing (OAPAVO, OAPADO, OAPDVO, and OAPDTO). Also, for an input byte to be fetched, the related control bits OBAPEN, J2APEN, Z6APEN and Z7APEN (bits 3-0) in register X+0BH must be set to a 1.

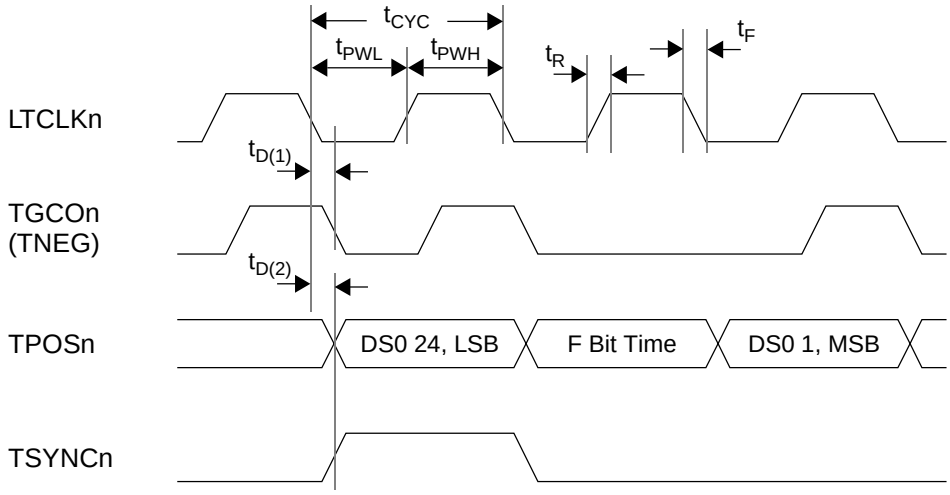
Figure 11. Ring Port Timing



Parameter	Symbol	Min	Typ	Max	Unit
ORPCKO or IRPCKI period	t_{CYC}		514.4		ns
Delay - ↓ORPCKO to ORPFMO or ORPDTO	t_D			5.0	ns
Fall Time (90% - 10%)* – OPRCKO, ORPFMO or ORPDTO	t_F			6.0	ns
Hold - IRPFMI or IRPDTI after ↑IRPCKI	t_H	3.0			ns
Rise Time (10% - 90%)* - ORPCKO, ORPFMO or ORPDTO	t_R			6.0	ns
ORPCKO or IRPCKI High time	t_{PWH}	40	50	60	% t_{CYC}
ORPCKO or IRPCKI Low time	t_{PWL}	40	50	60	% t_{CYC}
Setup - IRPFMI or IRPDTI to ↑IRPCKI	t_{SU}	7.0			ns

*Note: 25 pF load

Figure 12. Datacom Mode Output Timing



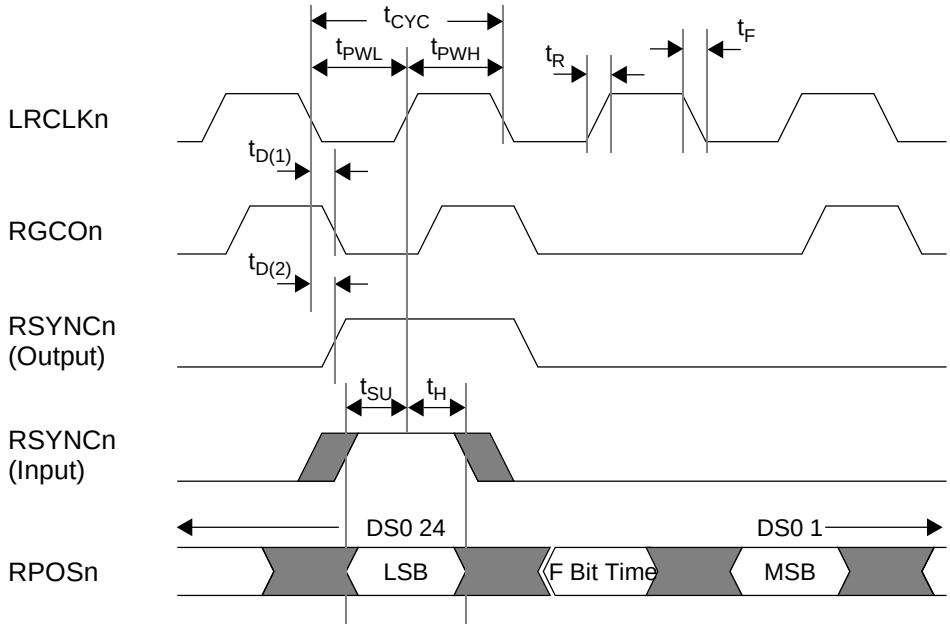
Note: n = 1 - 7

Parameter	Symbol	Min	Typ	Max	Unit
LTCLKn period	t_{CYC}	637	648	656	ns
Delay - LTCLKn[1,2] to TGCOn	$t_{D(1)}$	0.0		10	ns
Delay - ↓LTCLKn to TPOSn or TSYNCn	$t_{D(2)}$	-5.0		50	ns
Fall Time (90% - 10%)[3]– LTCLKn, TGCOn, TPOSn or TSYNCn	t_F			6.0	ns
LTCLKn or TGCOn High time	t_{PWH}	40%	50%	55%	t_{CYC}
LTCLKn or TGCOn Low time	t_{PWL}	40%	50%	55%	t_{CYC}
Rise Time (10% - 90%)[3]- LTCLKn, TGCOn, TPOSn or TSYNCn	t_R			6.0	ns

Notes:

1. LTCLKn can be inverted with the control bit TCAE (bit 7) in register 007H.
2. LTCLKn shown with TCAE set to a 0.
3. 25 pF load

Figure 13. Datacom Mode Input Timing



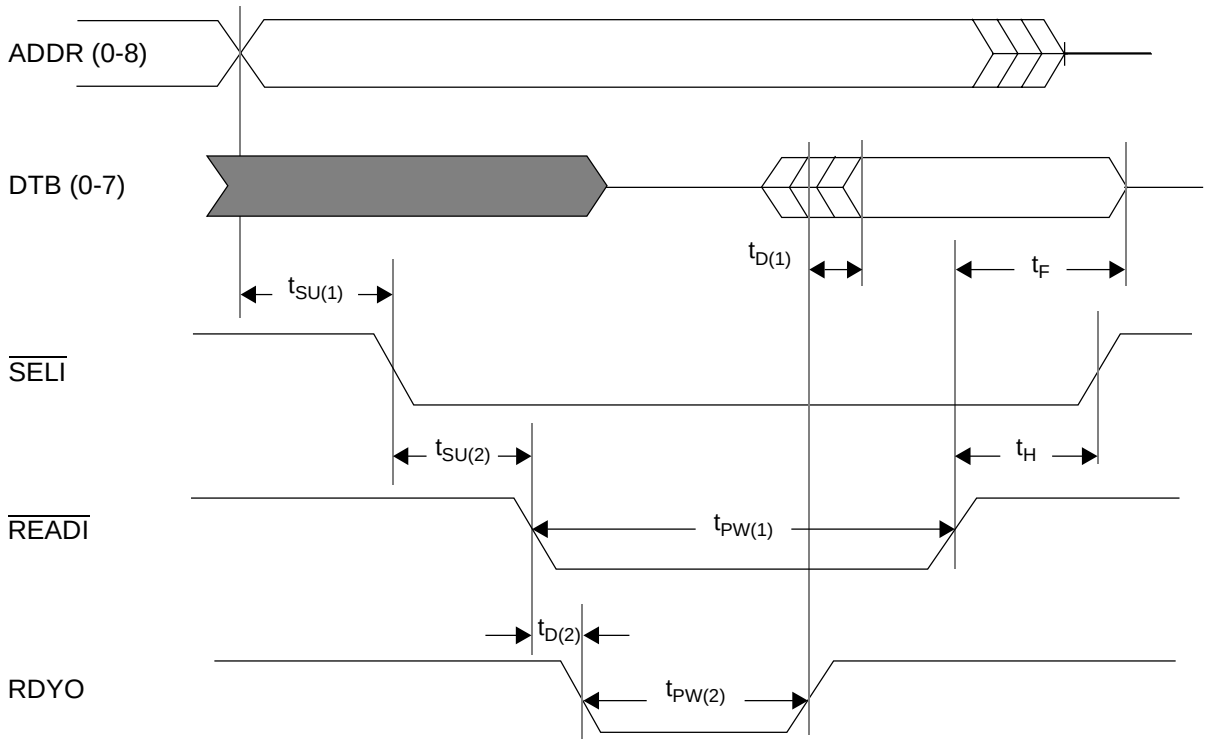
Note: n = 1 - 7

Parameter	Symbol	Min	Typ	Max	Unit
LRCLKn period	t_{CYC}	560	648		ns
Delay - LRCLKn[1,2] to RGCOn	$t_{D(1)}$	0.0		10	ns
Delay - ↓LRCLKn[1,2] to RSYNCn if Output	$t_{D(2)}$			50	ns
Fall Time (90% - 10%)[3]– RGCOn, and LRCLKn or RSYNCn if Outputs	t_F			6.0	ns
Hold - RPOSn or RSYNCn if input after ↑LRCLKn[1,2]	t_H	50			ns
LRCLKn or RGCO High time	t_{PWH}	240			ns
LRCLKn or RGCO Low time	t_{PWL}	240			ns
Rise Time (10% - 90%)[3]- RGCOn, and LRCLKn or RSYNCn if Outputs	t_R			6.0	ns
Set-up - RPOSn or RSYNCn if input to ↑LRCLKn[1,2]	t_{SU}	50			ns

Notes:

1. LRCLKn can be inverted with the control bit RCAE (bit 6) in register 007H.
2. LRCLKn shown with RCAE set to a 1.
3. 25 pF load

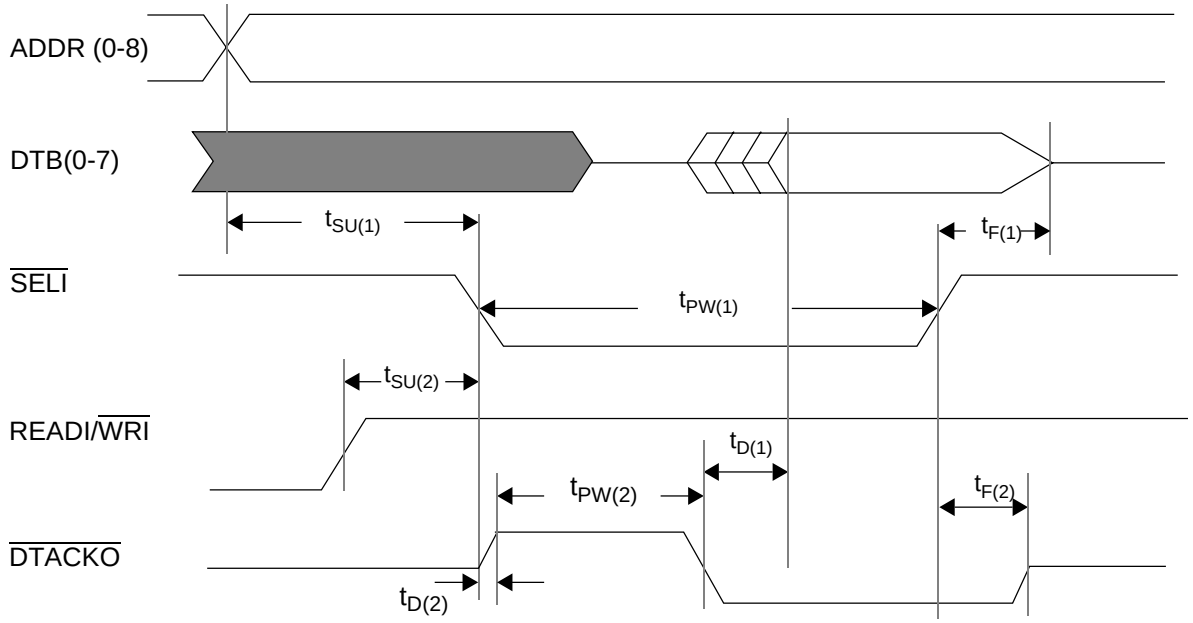
Figure 14. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR(0-8) set-up time to $\overline{SELI}\downarrow$	$t_{SU(1)}$	0.0			ns
DTB(0-7) valid delay after RDYO$\uparrow$	$t_{D(1)}$		-1/2 cycle PCKI*	-10	ns
DTB(0-7) float time after $\overline{READI}\uparrow$	t_F	1.0	3.0	5.0	ns
$\overline{SELI}$ set-up time to $\overline{READI}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{READI}$ pulse width	$t_{PW(1)}$	50			ns
$\overline{SELI}$ hold time after $\overline{READI}\uparrow$	t_H	0.0			ns
RDYO delay after $\overline{READI}\downarrow$	$t_{D(2)}$	0.0		12	ns
RDYO pulse width	$t_{PW(2)}$	2 cycles of PCKI*		6 cycles of PCKI*	ns

*Note: PCKI (not shown) is Processor Clock Input, 8 to 20 MHz, which is required for device operation.

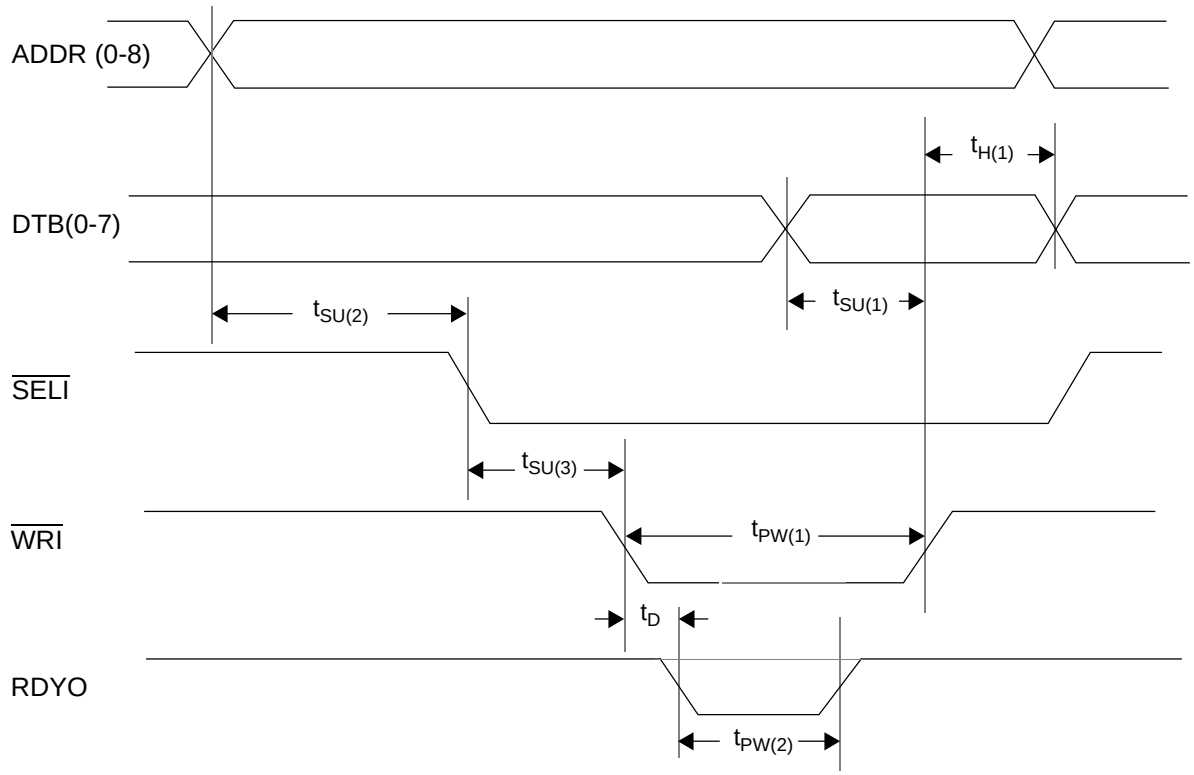
Figure 15. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
DTB(0-7) float time after $\overline{SELI}\uparrow$	$t_{F(1)}$	1.0		10	ns
ADDR(0-8) valid set-up time to $\overline{SELI}\downarrow$	$t_{SU(1)}$	0.0			ns
READI/$\overline{WRI}$ set-up time to $\overline{SELI}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{SELI}$ pulse width	$t_{PW(1)}$	50			ns
$\overline{DTACKO}$ pulse width	$t_{PW(2)}$	2 cycles of PCKI*		6 cycles of PCKI*	ns
DTB(0-7) output delay after $\overline{DTACKO}\downarrow$	$t_{D(1)}$		-1/2 cycle PCKI*	-10	ns
$\overline{DTACKO}$ float time after $\overline{SELI}\uparrow$	$t_{F(2)}$	1.0		10	ns
$\overline{DTACKO}$ delay after $\overline{SELI}\downarrow$	$t_{D(2)}$	0.0		12	ns

*Note: PCKI (not shown) is Processor Clock Input, 8 to 20 MHz, which is required for device operation.

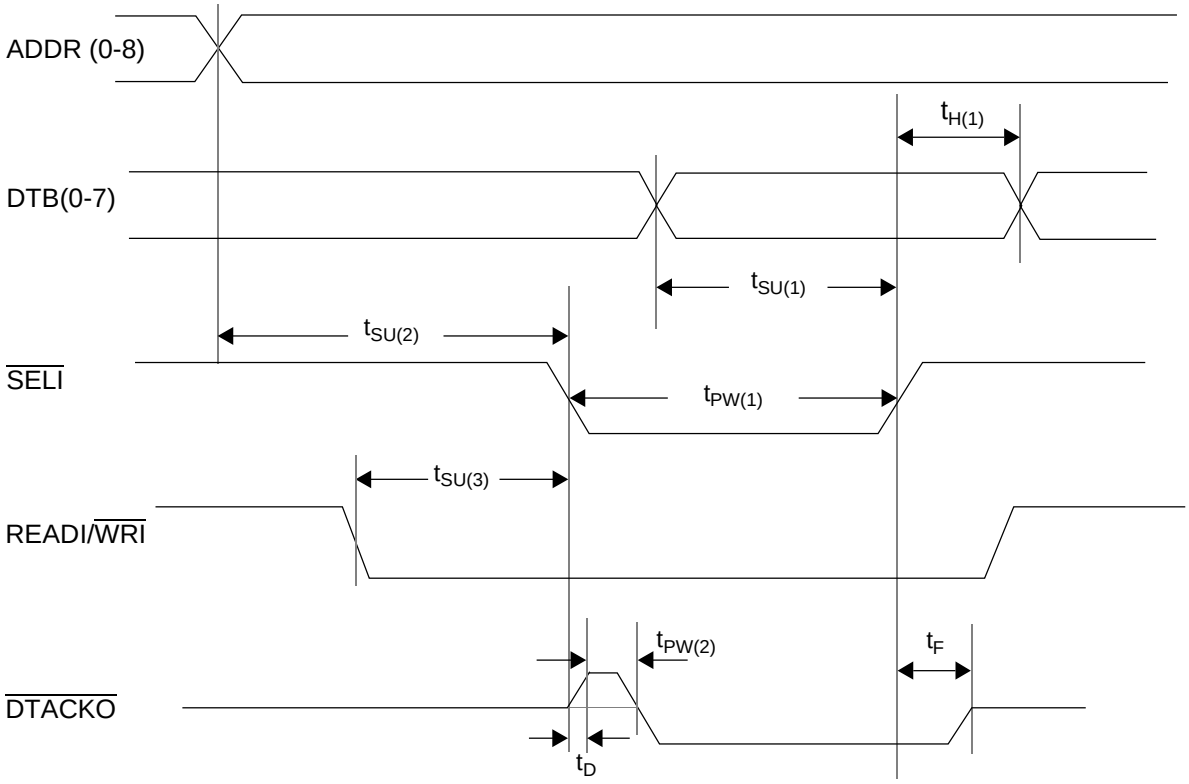
Figure 16. Intel Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
DTB(0-7) valid set-up time to $\overline{WRI}\uparrow$	$t_{SU(1)}$	20			ns
DTB(0-7) hold time after $\overline{WRI}\uparrow$	$t_{H(1)}$	5.0			ns
ADDR(0-8) set-up time to $\overline{SELI}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{SELI}$ set-up time to $\overline{WRI}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{WRI}$ pulse width	$t_{PW(1)}$	50			ns
RDYO delay after $\overline{WRI}\downarrow$	t_D	0.0		12	ns
RDYO pulse width	$t_{PW(2)}$	0.0		6 cycles of PCKI*	ns

*Note: PCKI (not shown) is Processor Clock Input, 8 to 20 MHz, which is required for device operation. Wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g.'read modify write' or word-wide write).

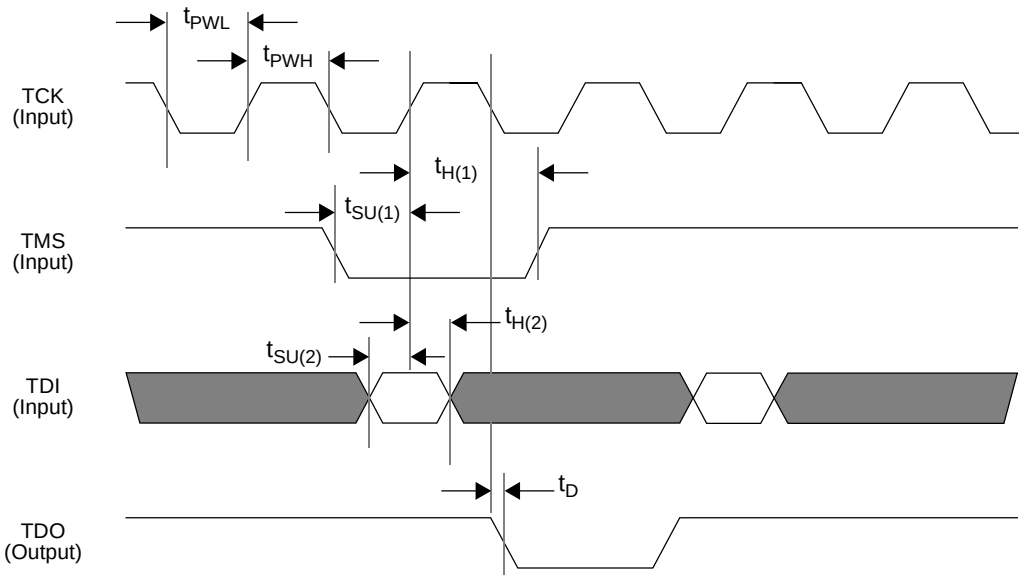
Figure 17. Motorola Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
DTB(0-7) valid set-up time to $\overline{SELI}\uparrow$	$t_{SU(1)}$	20			ns
DTB(0-7) valid hold time after $\overline{SELI}\uparrow$	$t_{H(1)}$	5.0			ns
ADDR(0-8) valid set-up time to $\overline{SELI}\downarrow$	$t_{SU(2)}$	0.0			ns
READI/$\overline{WRI}$ set-up time to $\overline{SELI}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{SELI}$ pulse width	$t_{PW(1)}$	50			ns
$\overline{DTACKO}$ pulse width	$t_{PW(2)}$	0.0		6 cycles of PCKI*	ns
$\overline{DTACKO}$ float time after $\overline{SELI}\uparrow$	t_F	1.0		10	ns
$\overline{DTACKO}$ delay after $\overline{SELI}\downarrow$	t_D	0.0		12	ns

*Note: PCKI (not shown) is Processor Clock Input, 8 to 20 MHz, which is required for device operation. Wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g.'read modify write' or word-wide write).

Figure 18. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time to TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time to TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	2.0	-	ns
TDO delay from TCK↓	t_D	-	7.0	ns

OPERATION

GENERAL MAPPER APPLICATION OVERVIEW

The DS1MX7 can be used in a wide variety of applications (see Figures 40 through 42) that require either an Asynchronous mapping of a DS1 signal into and out of a SONET or SDH payload in which the input clock and data are replicated at the output, or a Byte Synchronous mapping of a DS1 signal into or out of a SONET or SDH payload in which not only is the input clock and data replicated at the output, but DS0 visibility and signaling information is replicated at the output. When used in an Asynchronous application the DS1 side of the mapper connects to the line through DS1 Line Interface Units (LIUs) that recover the 1.544 MHz from the data, provide clock and data to the DS1MX7, input clock and data from the DS1MX7 and format a line signal for transmission. A port is provided to control up to 7 LIUs from the DS1MX7. When used in Byte Synchronous applications, DS1 framers may be inserted between the LIUs and the DS1MX7 to delineate the DS0s, extract and insert signaling, process DS0 and DS1 alarms, etc. The Byte Synchronous applications may also be used for direct interface to sources of DS0s (e.g., time slot interchangers, PCM codecs) or to data sources like fractional T1 with HDLC protocol on N x DS0 channels. The DS1MX7 provides complete clock recovery of DS1 signals through a two stage digital filter, eliminating the need for special external de-jitter buffers. The DS1MX7 provides complete SONET or SDH low order path termination and origination functions (VT1.5/ TU-11) with alarm mapping to and from the DS1 line. On the system side, all that is required is a high order section, line and path termination/ origination function. The Telecom Bus provided in the DS1MX7 allows for multiple devices to be connected seamlessly to a TranSwitch SOT-1E or SOT-3 device, both of which supply these high order functions. A separate port is provided for access to optional overhead bytes. For redundant and ring applications a ring I/O port is provided as well as special alarm output and DS1 isolation input. A microprocessor port is provided to configure the DS1MX7 as well as to provide interrupts for device wide/ Telecom Bus alarms as well as VT1.5/ TU-11 or DS1 alarms. One second shadow registers are provided to assist in the preparation of performance monitoring information. An IEEE 1149.1 boundary scan function and an internal PRBS generator/ analyzer are provided for manufacturing support,

LINE INTERFACE SELECTION

Each of the seven DS1MX7 channels can be individually programmed for Asynchronous mode, Byte Synchronous mode as clock master, or a modified Byte Synchronous mode where the DS1MX7 channel is a clock slave in which pointer movements are generated as needed to map the incoming DS1 signal to the SONET/ SDH payload. The table below details the options present at the Line Interface.

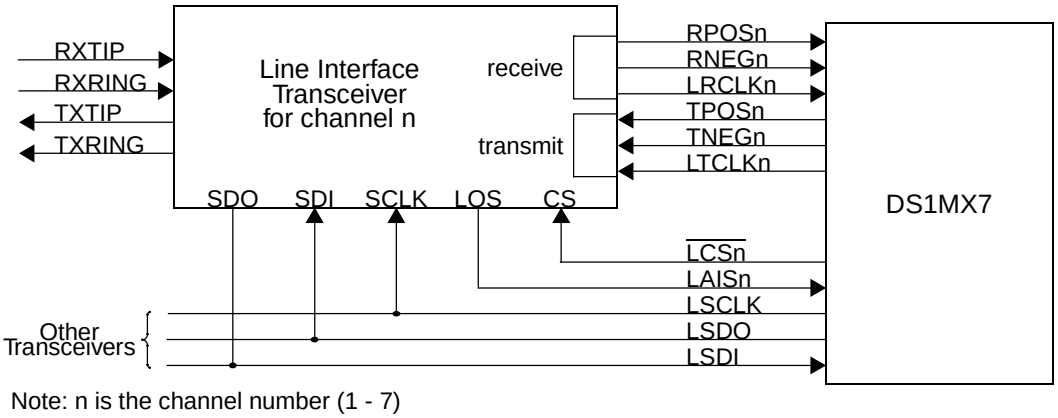
Mode of Operation	Line Code	RNEGn	TNEGn	MODE1	MODE0	LCODE	ENCOD	DATACOM
				X+00 bit 1	X+00 bit 0	X+00 bit 3	X+00 bit 2	X+00 bit 5
Asynchronous	AMI	Data	Data	0	X	0	1	X
Asynchronous	B8ZS	Data	Data	0	X	1	1	X
Asynchronous	NRZ	RCVn	Low	0	X	0	0	X
Asynchronous	NRZ	RCVn	High	0	X	1	0	X
Byte Synchronous LRCLK/RSYNCn out	NRZ	RSIGLn input	TSIGLn input	1	0	X	X	0
Byte Synchronous LRCLK/RSYNCn out	NRZ	RGCOn	TGCOn	1	0	X	X	1
Byte Synchronous LRCLK/RSYNCn in	NRZ	RSIGLn input	TSIGLn input	1	1	X	X	0
Byte Synchronous LRCLK/RSYNCn out	NRZ	RGCOn	TGCOn	1	1	X	X	1

Asynchronous Operation with the Line Interface

Each of the seven mappers in the DS1MX7 can be programmed to provide either a dual unipolar interface or a NRZ interface. The dual unipolar interface is selected when a 1 is written into control bit ENCOD (bit 2) in the control register located at address X+00H in the memory map. The X is (n x 040H), where n is the number of the mapper selected (1-7), as explained in the Memory Map section. The B8ZS line or AMI coder/decoder (CODEC) feature can be selected for the dual unipolar interface. The B8ZS CODEC is selected by writing a 1 to control bit LCODE (bit 3) in the register X+00H. A 0 will select an AMI CODEC. The B8ZS stands for Bipolar with Eight Zero Substitution, which is described in ANSI Document ANSI T1.102-1993 and other Bellcore documents.

The clock polarity of the input and output line clocks is selectable by writing the sense required to global control bits TCAE and RCAE (bits 7 and 6) in register 007H. When a mapper is configured for the dual unipolar mode, the line signal is monitored for loss of signal (LOS). LOS is detected if no transitions are present for 175 ± 75 pulse positions. Recovery occurs when a ones density of 12.5% or more is detected in 175 ± 75 pulse positions. A status bit LOSS (bit 5) in register X+10H indicates this condition. A mask, LOSM, a latched value, LOSE, a PM value, LOSPM and a FM value, LOSFM are available (bit 5) at register locations X+08H, X+14H, X+18H and X+1CH respectively. Coding violations are counted in a 12-bit performance counter located at register locations X+22H and X+23H with shadow value in registers X+2AH and X+2BH. A counter overflow bit CVOS (bit 0) in register X+10H is provided. A mask, CVOM, a latched value, CVOE, a PM value, CVOPM and a FM value, CVOFM are available (bit 0) at register locations X+08H, X+14H, X+18H and X+1CH respectively. Excessive zeros (8 or more for B8ZS or 16 or more for AMI) are included if control bit ENZC (bit 4) in register X+00H is set to a 1. An AIS indication is provided which checks to see if more than 99.9% ones occur in a 3 to 75 millisecond period or if less than 99.9% ones occur in a 3 to 75 millisecond period. Status bit DAISS (bit 3) in register X+10H indicates the AIS condition. A mask, DAISM, a latched value, DAISE, a PM value, DAISPM and a FM value, DAISFM are available (bit 3) at register locations X+08H, X+14H, X+18H and X+1CH respectively. The LOS condition can also be used to generate an AIS (DS1 payload all-ones will be mapped in place of the received signal) if control bit LOS2AIS (bit 6) in register X+01H is set to a 1.

The Coder block provides an AMI/B8ZS encoder. This block provides AIS generation either from the Microprocessor Interface by control bit SDAISL (bit 3) in register X+03H when set to a 1 or optionally from various system conditions (VT AIS/LOP, Signal Label Mismatch or Unequipped) all of which are individually enabled by control bits VAIS2AIS (bit 3 at X+01H), SLM2AIS (bit 2 at X+02H) and UNE2AIS (bit 0 at X+02H) being set to a 1. A high level signal failure input on pin DFAIL will cause DS1 AIS for all seven mappers. A 'transmit all-zeros' capability is provided to conserve power in an external Line Transceiver when AIS is not required by setting control bit SDAISL (bit 3) in register X+03H to a 0 when control bit TBRVAL (bit 7) in register X+04H is also set to a 0 (Drop slot not assigned). The connections between a DS1MX7 mapper and external line interface transceivers are shown in Figure 19 below for dual unipolar mode.

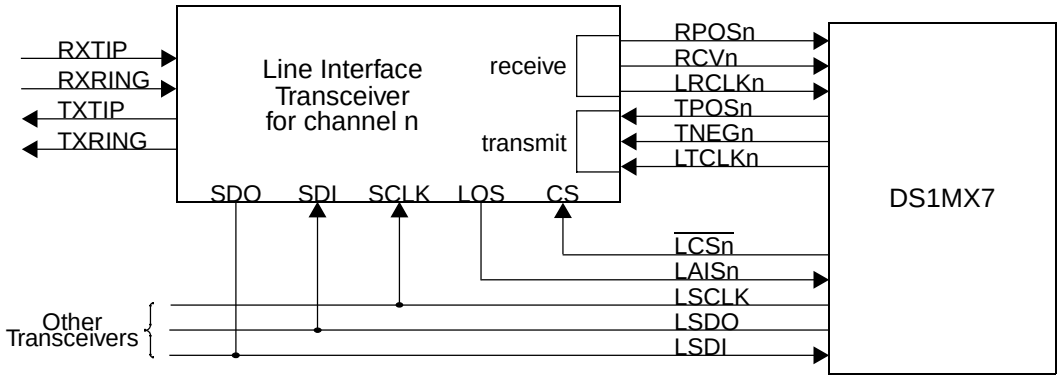


Note: n is the channel number (1 - 7)

Figure 19. Line Interface for Dual Unipolar Mode

The NRZ interface is selected when a 0 is written into control bit ENCOD (bit 2) in register X+00H. The clock polarity of the line input and output clocks is selectable by writing to global control bits TCAE and RCAE (bits 7 and 6) in register 007H. Options are provided for inverting the polarity of the transmit and receive data pins. A 1 written to control bit TXNRZP (bit 0) in global register 007H inverts the polarity of the transmit data signal, TPOSn, while a 1 written to control bit RXNRZP (bit 4) in the same register inverts the polarity of the receive data signal RPOSn. In NRZ mode, the RNEGn pin may be used to input an external indication of coding violations (RCVn). External coding violations are counted in the same 12-bit performance counter as described above. Coding violations are counted when the input is high for rising edges of the line clock LRCLKn. The same AIS detector as described above for bipolar is available in NRZ mode. LOS can be detected only externally and input on pin LAISn. By setting control bit EXPLOS (bit 6) in register X+00H to a 1, LOSS status plus latched event, mask, PM and FM functions are provided as described above.

In the transmit direction, when the NRZ mode is selected, the TNEGn pin becomes a spare drive pin. When control bit ENCOD (bit 2) in register X+00H is a 0, the output state of TNEGn is defined by the value written to bit LCODE (bit 3) in register X+00H (LCODE set to a 0 is a low on TNEGn and LCODE set to a 1 is a high on TNEGn). A typical interface between a mapper in the DS1MX7 and an external line transceiver is shown in Figure 20 below for the NRZ mode. TNEGn, for example, may be used to select the encoding mode for the LIU.



Note: n is the channel number (1 - 7)

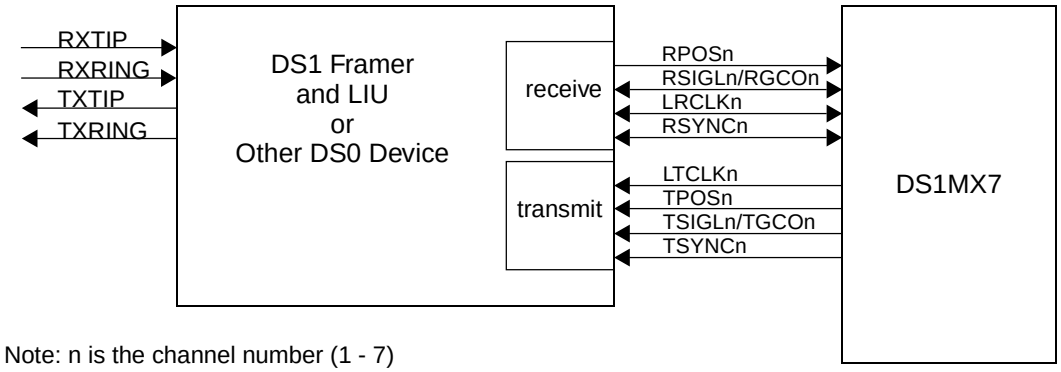
Figure 20. Line Interface for NRZ Mode

Byte Synchronous Operation with the Line Interface

For Byte Synchronous operation the line interface operates in the NRZ mode with RSIGLn and TSIGLn carrying the signaling information from/to an external framer using the negative polarity input and output pins. Figure 21 is the basic Byte Synchronous setup. Typical applications are shown in Figures 40 and 42. In Byte Synchronous applications where signaling is not used, a Datacom option is provided for connections to HDLC controllers or other devices that operate over the DS1 payload only. TGCO and RGCO are gapped clock outputs for clocking out or in data on TPOSn and RPOSn. The clock is gapped during the frame bit time every 125 µs. This option is available by setting control bit DATACOM (bit 5) in register X+00H to a 1.

For Byte Synchronous applications that require DS1-based performance monitoring (control bits MODE1, 0 =10 in register X+00H bits 1 and 0 only), CRC-6 is generated optionally for each superframe of data presented on RPOSn and inserted in the Cn frame bit locations of the following superframe to be mapped. When control bit CRC6 (bit 4) in register X+01H is set to a 1 CRC-6 is both inserted and checked. After demapping CRC-6 is checked. CRC-6 errors share the 12-bit line code violation counter shadow register and overflow indications to support performance monitoring. CRC-6 errors are counted in the 12-bit performance counter located at register locations X+22H and X+23H with shadow value in registers X+2AH and X+2BH. Each ESF superframe in which a calculated CRC-6 value does not match the received CRC-6 value increments the counter by one. A

counter overflow bit CVOS (bit 0) in register X+10H is provided. A mask, CVOM, a latched value, CVOE, a PM value, CVOPM and a FM value, CVOFM are available (bit 0) at register locations X+08H, X+14H, X+18H and X+1CH respectively.



Note: n is the channel number (1 - 7)

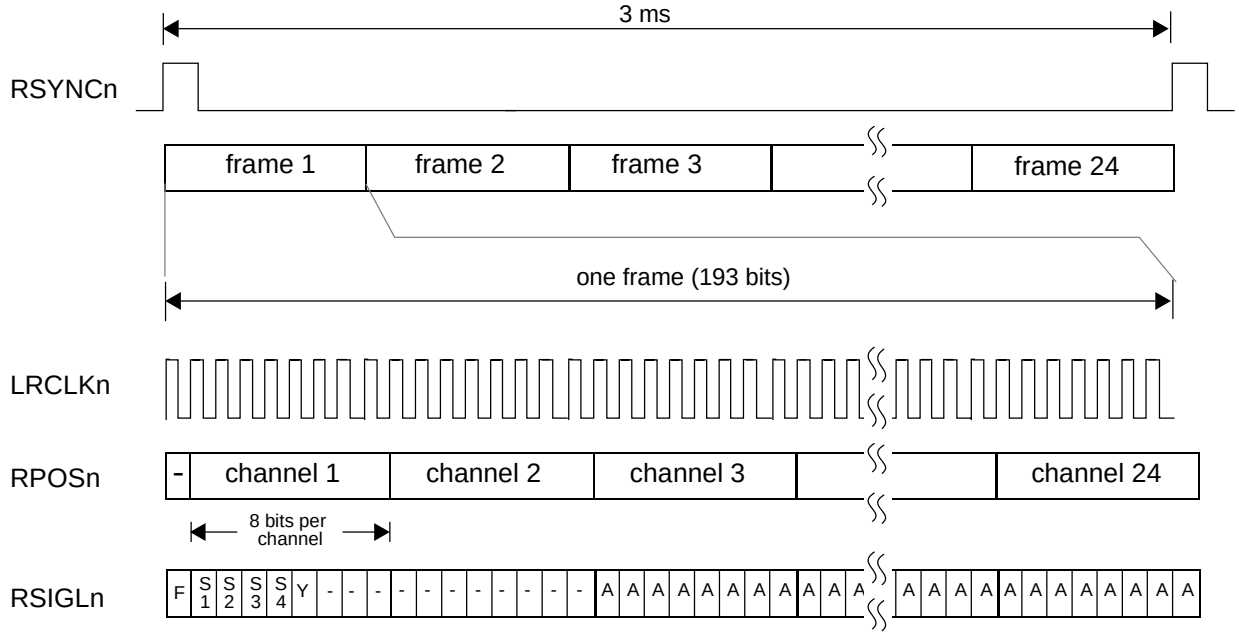
Figure 21. Byte Synchronous Interface to a DS1 Framer

Receive Data and Signaling Highway Operation

The receive highway carries information from the framer to the DS1MX7. The highway is sub-divided into two time division multiplexed buses, one for the data (RPOSn), and one for signaling, frame bit and alarms (RSIGLn). These two buses are synchronous with the signals LRCLKn and RSYNCn, a 1.544 MHz clock and a 3 millisecond synchronization signal driven from the framer or the DS1MX7 depending on the mode of Byte Synchronous operation. If the DS1MX7 operates in the modified Byte Synchronous mode, receive clock and synchronization are inputs to the DS1MX7; if the DS1MX7 operates in true Byte Synchronous mode, receive clock and synchronization are outputs of the DS1MX7. The data highway is a single-bit serial bus organized into 193-bit groups called frames. Each frame consists of a spare bit position followed by twenty-four 8-bit data samples representing the 24 DS0s. 24 frames form a multiframe, the beginning of which is identified by a synchronization pulse, RSYNCn. The RSYNCn high pulse occurs one bit time before the first frame of the multiframe and every 24 frames after that. The signaling highway, RSIGLn, is also divided into 193-bit frames. Each frame consists of a frame bit followed by 192 bits of signaling and alarm information for the 24 data channels on the data highway. The frame bit pattern tracks the signaling bit pattern received from the system. The alarm bits in the signaling highway follow the signaling bits. In each frame of 193 bits, four signaling bits are transmitted followed by a RAI (Yellow) alarm bit position. The bit positions coincident with DS0 3 through DS0 24 are all used for the AIS alarm bit. Signaling bits A1 through A4 occur in frame number one, followed by A5 through A8 in frame number two, and so on, ending with D21 through D24 in frame number 24, corresponding to the ESF mode with 16-state signaling. For two-state or four-state signaling the B, C and D bits or the C and D bits are replaced by A bits or A and B bits respectively, as shown in the following table. The receive framing format and signaling format are shown in Figures 22 and 23. The signaling information is stored in the RX Signaling Store block for mapping. The alarm information (DS1 AIS and DS1 RAI-Yellow) is stored in the RX Alarm Control block and can be enabled to generate VT AIS or RFI automatically. Control bit SH2VAIS (bit 7) in register X+01H, when set to a 1, causes the AIS alarm bits on the signaling highway to activate VT AIS generation for the affected channel. When control bit YEL2RFI (bit 1) in register X+01H is set to a 1, the RAI-Yellow alarm bit on the signaling highway causes the DS1MX7 mapper channel to send a VT RFI in the V5 byte. The status of these two signaling highway alarm bits is available as SHDAIS and SHYEL (bits 7 and 6) in register X+20H as status only. When control bit AIS2VAIS (bit 0) in register X+01H is set to a 1, the DS1MX7 will cause VT AIS to be generated if the DS1 AIS condition as defined above for the Asynchronous Mode of operation is detected. When control bit DATACOM (bit 5) in register X+00H is set to a 1, RSIGLn input becomes RGCOn output, which is a gapped LRCLKn clock with a gap of one LRCLKn cycle wide occurring at the frame bit time of RPOSn every 125 microseconds.

Signaling bit positions on RSIGLn and TSIGLn

Frame	SF/ESF	16-St. RSIGL; S_1-S_4	TSIGL; S_1-S_4	4-State; S_1-S_4	2-State; S_1-S_4
1	F1/M1	A01, A02, A03, A04	A01, A02, A03, A04	A01, A02, A03, A04	A01, A02, A03, A04
2	S1/C1	A05, A06, A07, A08	A05, A06, A07, A08	A05, A06, A07, A08	A05, A06, A07, A08
3	F2/M2	A09, A10, A11, A12	A09, A10, A11, A12	A09, A10, A11, A12	A09, A10, A11, A12
4	S2/F1	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16
5	F3/M3	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20
6	S3/C2	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24
7	F4/M4	B01, B02, B03, B04	B01, B02, B03, B04	B01, B02, B03, B04	A01, A02, A03, A04
8	S4/F2	B05, B06, B07, B08	B05, B06, B07, B08	B05, B06, B07, B08	A05, A06, A07, A08
9	F5/M5	B09, B10, B11, B12	B09, B10, B11, B12	B09, B10, B11, B12	A09, A10, A11, A12
10	S5/C3	B13, B14, B15, B16	B13, B14, B15, B16	B13, B14, B15, B16	A13, A14, A15, A16
11	F6/M6	B17, B18, B19, B20	B17, B18, B19, B20	B17, B18, B19, B20	A17, A18, A19, A20
12	S6/F3	B21, B22, B23, B24	B21, B22, B23, B24	B21, B22, B23, B24	A21, A22, A23, A24
13	F1/M7	C01, C02, C03, C04	C01, C02, C03, C04	A01, A02, A03, A04	A01, A02, A03, A04
14	S1/C4	C05, C06, C07, C08	C05, C06, C07, C08	A05, A06, A07, A08	A05, A06, A07, A08
15	F2/M8	C09, C10, C11, C12	C09, C10, C11, C12	A09, A10, A11, A12	A09, A10, A11, A12
16	S2/F4	C13, C14, C15, C16	C13, C14, C15, C16	A13, A14, A15, A16	A13, A14, A15, A16
17	F3/M9	C17, C18, C19, C20	C17, C18, C19, C20	A17, A18, A19, A20	A17, A18, A19, A20
18	S3/C5	C21, C22, C23, C24	C21, C22, C23, C24	A21, A22, A23, A24	A21, A22, A23, A24
19	F4/M10	D01, D02, D03, D04	D01, D02, D03, D04	B01, B02, B03, B04	A01, A02, A03, A04
20	S4/F5	D05, D06, D07, D08	D05, D06, D07, D08	B05, B06, B07, B08	A05, A06, A07, A08
21	F5/M11	D09, D10, D11, D12	D09, D10, D11, D12	B09, B10, B11, B12	A09, A10, A11, A12
22	S5/C6	D13, D14, D15, D16	D13, D14, D15, D16	B13, B14, B15, B16	A13, A14, A15, A16
23	F6/M12	D17, D18, D19, D20	D17, D18, D19, D20	B17, B18, B19, B20	A17, A18, A19, A20
24	S6/F6	D21, D22, D23, D24	D21, D22, D23, D24	B21, B22, B23, B24	A21, A22, A23, A24



F = frame bit; A = AIS; Y = RAI-Yellow alarm; S1, S2, S3, S4 = signaling bits; - = not assigned

Figure 22. System Interface Receive Framing Format

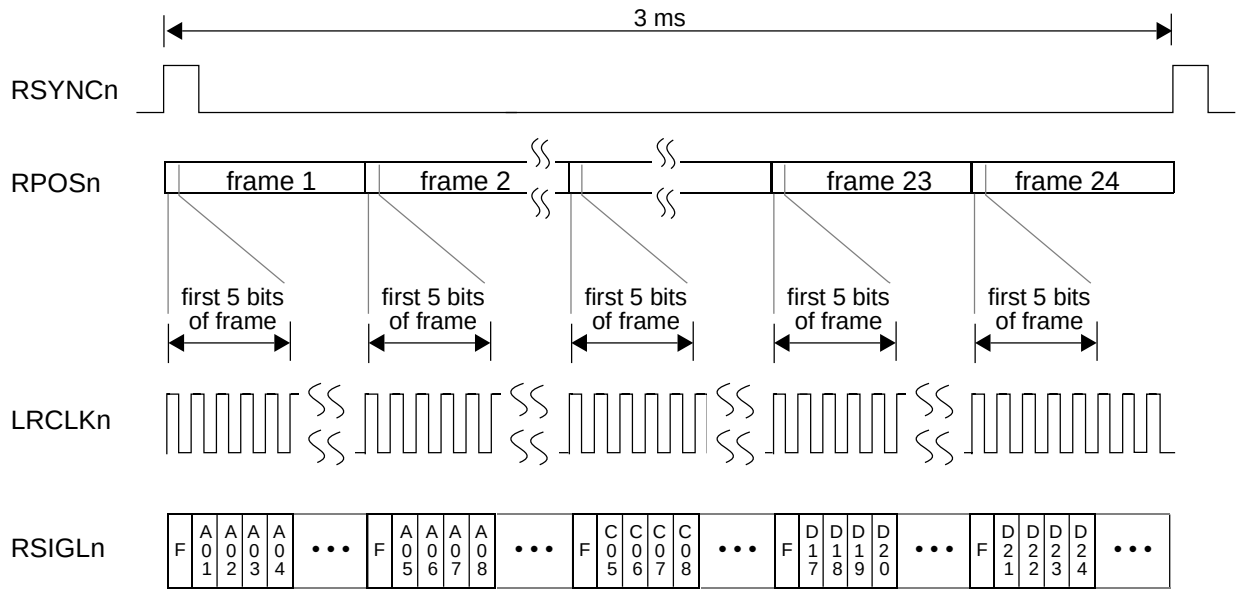


Figure 23. System Interface Receive Signaling Format

Transmit Data and Signaling Highway Operation

The transmit highway carries information from the DS1MX7 to the framer. The highway is sub-divided into two time division multiplexed buses, one for the data (TPOSn) and one for signaling, frame bits and alarms (TSIGLn). These two buses are synchronous with the signal LTCLKn, a 1.544 MHz clock that is driven from the DS1MX7. The data highway is a single bit-serial bus that is organized into 193-bit groups called frames. Each frame consists of a frame bit followed by twenty-four 8-bit data samples. Each of the 8-bit data samples represents a single DS0 on the receive highway. The 193-bit frames are grouped into a 24-frame multiframe. In order to help locate the beginning of a frame and extract signaling information, the DS1MX7 sources a synchronization signal, TSYNCn. The TSYNCn high pulse occurs one bit time before the first frame in the multiframe and every 24 frames after that. The signaling highway, TSIGLn, is also divided into 193-bit frames and is organized in an identical fashion to RSIGLn (see the table above for signaling bit assignments). The alarm bits in the signaling highway follow the signaling bits. In each frame of 193 bits, four signaling bits are transmitted followed by a RAI (Yellow) alarm bit position. The bit positions coincident with DS0 3 through DS0 24 are all used for the AIS alarm bit. Signaling bits A1 through A4 occur in frame number one followed by A5 through A8 in frame number two ending with D21 through D24 in frame number 24, corresponding to the ESF mode with 16-state signaling. For two-state or four-state signaling the B, C and D bits or the C and D bits are replaced by A bits or A and B bits respectively, as shown in the table above. AIS or Yellow alarm sourced by the DS1MX7 are output in the same positions as on RSIGLn. These alarm bits may be used to force DS1 Yellow or DS1 AIS automatically in the QT1F-*Plus*. Control bit VAIS2AIS (bit 3) in register X+01H, when set to a 1, causes the detection of VT-LOP or VT AIS to set the AIS bits on TSIGLn unless control bit DATACOM (bit 5) in register X+00H is set to a 1. Similarly, if control bits SLM2AIS (bit 2) and UNE2AIS (bit 0) in register X+02H are set to a 1, and if either a Signal Label Mismatch or Unequipped condition exists, the AIS bits on the signaling highway are set to a 1 unless control bit DATACOM is set to a 1. Setting control bit SDAISL (bit 3) in register X+03H to a 1 will also set the AIS bits in TSIGLn unless control bit DATACOM is set to a 1. Control bit SDAISL set to a 1 or control bits VAIS2AIS, SLM2AIS or UNE2AIS set to a 1 and the condition VT LOP/AIS, Signal Label Mismatch or Unequipped occurs will cause an all-ones signal to be generated on TPOSn without regard for control bits DATACOM or MODE1. Likewise, the Yellow alarm bit on the signaling highway may be set if control bit

RFI2YEL (bit 2) in register X+01H and an RFI alarm is detected, or if control bit SYELL (bit 2) in register X+03H is set to a 1 when control bit MODE1 (bit 1) in register X+00H is set to a 1 indicating Byte Synchronous operation and DATACOM (bit 5) in the same register is set to a 0 indicating TSIGLn is not used for gapped clock output. The frame bits received from the VT1.5/ TU-11 are available on TSIGLn as well; they track the signaling bits and may be used for FDL extraction.

When control bit DATACOM (bit 5) in register X+00H is set to a 1, TSIGLn output becomes TGCOn output, which is a gapped LTCLKn clock with a gap one LTCLKn cycle wide occurring at the frame bit time of TPOSn every 125 microseconds. System interface transmit framing format and signaling format are shown as Figures 24 and 25.

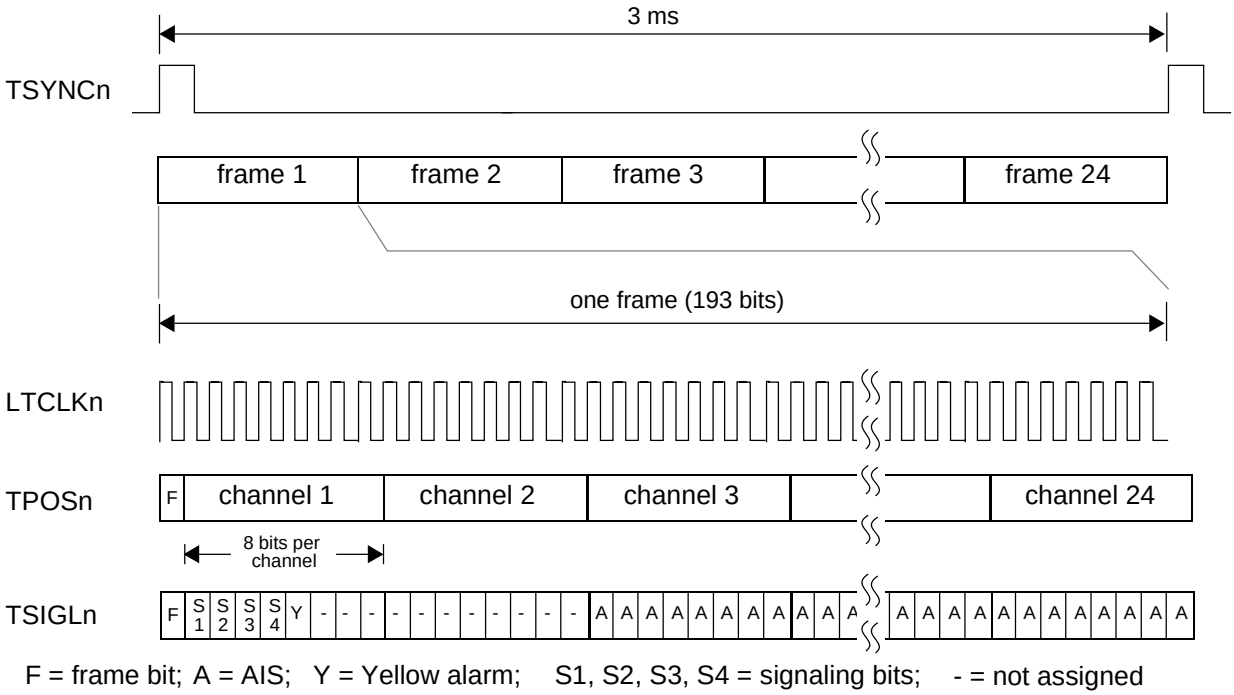


Figure 24. System Interface Transmit Framing Format

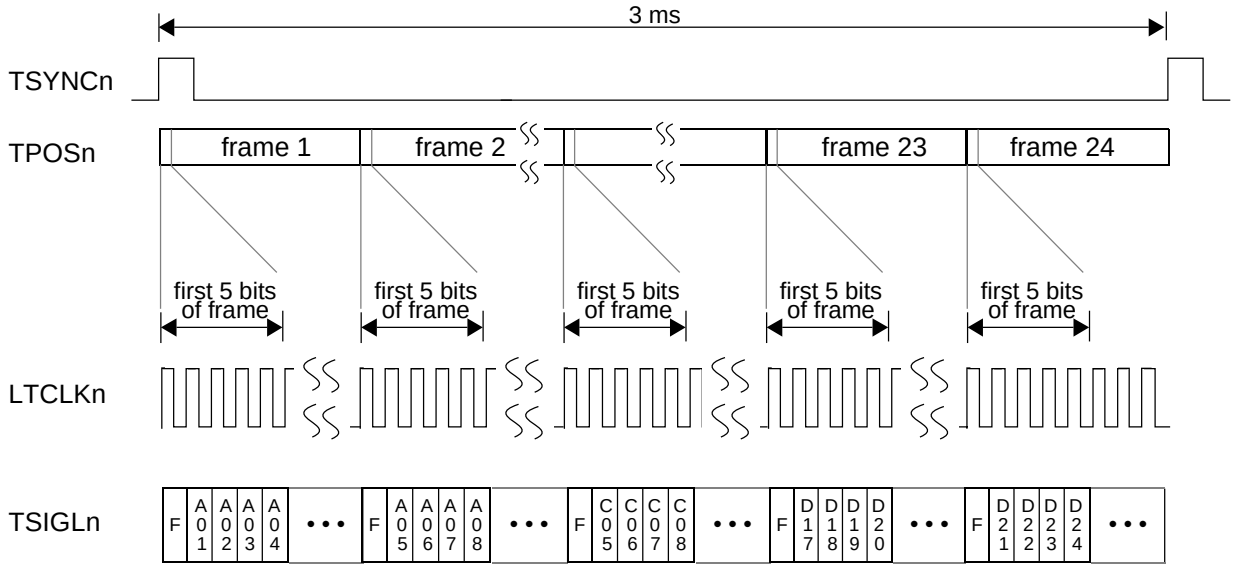


Figure 25. System Interface Transmit Signaling Format

The TX Signaling Store and the TX Alarm Control blocks buffer the signaling and alarm information to be sent on the signaling highway. The signaling bits are output as shown in the table above as well as in Figure 25. To support certain protection schemes, pin $\overline{CSO}$ when tied low will cause the transmit line interface leads (LTCLKn, TNEGn/TSIGLn/TGCOn, TPOSn, and TSYNCn) to be driven to a logic low.

The Synchronizer, Mapper and Overhead Generator

The Synchronizer/Mapper block operates in three different modes, programmable on a per channel basis as described above in the Line Interface Section. The Synchronizer/Mapper is the heart of the mapping side of the device. It synchronizes the 1.544 Mb/s data stream to the SONET/SDH clock domain, it maps the data stream to the virtual tributary (VT1.5/ TU-11) and it inserts the low order path overhead for performance monitoring and administrative purposes. Figure 2 shows the result of the synchronization, mapping and overhead insertion functions to form a VT1.5/ TU-11 for Asynchronous or Byte Synchronous mode.

The synchronization function adjusts approximately 772 DS1 bits so that they fit into a VT1.5 / TU-11 which is 500 microseconds long. The DS1 signal, whether framed to SF or ESF formats or framed to another format, generates 193 bits every 125 microseconds. As shown in Figure 2, three opportunities are provided for 193 bits (I plus 24 bytes) and one opportunity for 192 (no St bits used for information), 193 (one St bit used for information) or 194 bits (both St bits used for information) in the VT1.5/ TU-11 for the Asynchronous mode. Two stuffing control bits (C_1 and C_2) repeated twice are provided in every VT1.5/ TU-11 to indicate if a stuffing bit opportunity is to be used for information or stuff; for $C_1C_1C_1 = 000$ indicates that S_{T1} is used for an information bit and $C_1C_1C_1 = 111$ indicates that S_{T1} is used for a stuff bit. C_2 is treated likewise.This mechanism allows majority voting to be used at the desynchronizer, providing a robust solution at high bit error rates. The DS1MX7 has an input buffer that is written by the DS1 line clock and read by the SONET/ SDH clock. The stuffing control in the DS1MX7 uses the depth of this input buffer to set the value of C_1 and C_2. Buffer overflow/ underflow is a fault condition of the input caused by the input frequency being outside the stuffing range for Asynchronous mapping (approximately $\pm$ 230 Hz). This condition will be passed to the Microprocessor Interface as an alarm (Map Error). Status bit MPS (bit 4) in register X+10H indicates the Map Error status; mask MPM, latched event MPE, performance value MPPM and hard fault value MPFM are all bit 4 of registers X+08H, X+14H, X+18H and X+1CH respectively. The stuffing mechanism in the DS1MX7 employs threshold

modulation such that a desynchronizer will meet GR-253-CORE category I jitter requirements. This is done by using SRCLK to vary the input DS1 clock's phase for every sequential VT1.5/ TU-11 such that the stuffing pattern varies at a frequency high enough to be filtered easily by the desynchronizer. This prevents a DS1 clock that is a few Hz different from a SONET/SDH derived 1.544 MHz reference clock from generating jitter spikes when desynchronized. This feature can be turned off for testing purposes by setting global control bit TMDIS (bit 2) in register 03DH to a 1.

Byte Synchronous mapping permits full DS0 and signaling visibility as is shown in Figure 2. The 24 bytes every 125 microseconds are now 24 DS0s; the stuffing mechanism is replaced by a P_1/P_0 pattern that is used to identify different SF and ESF frame bits as well as which signaling bits are being sent and which go to what DS0s. Byte Synchronous mapping performs synchronization in two different ways. When LRCLKn and RSYNCn are outputs they are derived from signal LO, which must be sourced from the SONET/SDH payload timing (ACLK, ASPE and AC1J1V1). As such, exactly 24 DS0s, one frame bit and four signaling bits are mapped every 125 microseconds. RSYNCn output defines the start of the first of six VT superframes (the P_1/P_0 pattern goes from 11 to 00) that form a 3.0 ms multiframe. If the source of the DS1 has a different clock than at pin LO, an external slip buffer must be provided; the TranSwitch QT1F-*Plus* (TXC-03103) provides this function.

Since some applications do not want to have the added delay of up to two DS1 frames for slip buffering (e.g. TR-496 Objective 3-6)), a modified version of Byte Synchronous mapping is provided where LRCLKn and RSYNCn are inputs for floating VT1.5/ TU-11 mode. On the tributary or DS1 line side it operates from the input timing block, where data is fed into the block. On the system side it operates off of Telecom Bus SONET/SDH drop timing. DS1 line side clock and multi-frame synchronization uses the buffering supplied by this block. If the input buffer becomes too full the synchronizer requests a pointer decrement to be generated by the VT Termination block which aligns the virtual container to the virtual tributary; this will cause an extra byte of data to be read out of the input buffer in a 500 microsecond period. In Figure 2 the V3 byte will be skipped and everything will shift up one byte. Likewise, if the input buffer is too empty the synchronizer requests a pointer increment causing the V3 position to be repeated and one less byte of data will be read out of the input buffer in a 500 microsecond period. Buffer overflow/underflow is a fault condition of the input caused by the loss of frame synchronization (if control bit LOF2VAIS (bit 5) in register X+01H is set to a 1) for this mode. This condition will be passed to the Microprocessor Interface as an alarm (Map Error). Status bit MPS (bit 4) in register X+10H indicates the Map Error status; mask MPM, latched event MPE, performance value MPPM and hard fault value MPFM are all bit 4 of registers X+08H, X+14H, X+18H and X+1CH respectively. RSYNCn input defines the start of the first of six VT superframes (the P_1/P_0 pattern goes from 11 to 00), as shown in the table below.

The Mapper takes the output of the synchronizer and adds the overhead bits and bytes to it. The O, J2, Z6 and Z7 positions are driven with the values stored in registers X+36H (O-bits), X+37H (J2 byte), X+38H (Z6/N2 byte) and X+39H (Z7/K4 byte) unless the Auxiliary Port is used. If the Auxiliary Port is used and the enable bit (OBAPEN, J2APEN, Z6APEN or Z7APEN, bits 3 - 0 in register X+0BH) for the specific byte is set to a 1, the byte is brought in from the Auxiliary Port and inserted into the overhead byte position as well as in the above register locations. For Asynchronous operation only, the eight O-bits and six C_1 and C_2 bits are included as shown in Figure 2. For Byte Synchronous operation the mapper also multiplexes into the payload the data from the RX Signaling Store, which contains both the ABCD signaling bits for each DS0 and also the DS1 SF or ESF frame bits. Since the signaling and framing bits in a framed DS1 take 3.0 milliseconds for a single ESF superframe, six 500-microsecond VT superframes are required to define it. The P_1/P_0 bits for the Byte Synchronous mapping are coded to identify the signaling and framing bits as shown in the table below. Refer to Figure 2 for the signaling and P_1/P_0 bit positions. The signaling bits are shown for ESF; for SF or ESF with four-state signaling the CnDn bits are the AnBn bits repeated; for two-state signaling AnBnCnDn becomes AnAnAnAn in the table below. Whether the frame bits are provided or not, the DS1MX7 can be set to calculate CRC-6 over the DS0s only, inserting them in the CRC positions in the table below if control bit CRC6 (bit 4) in register X+01H is set to a 1. The TranSwitch QT1F-*Plus* (TXC-03103) supports the insertion of specific ABCD signaling codes for DS0 AIS and DS0 RAI via its signaling buffer write capability and it optionally forces the robbed bit positions to all 1 to support Byte Synchronous GR-253-CORE signaling conditional requirements.

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Signaling and Frame Bit Assignments for Byte Synchronous Modes

P_1	P_0	S_1	S_2	S_3	S_4	F for SF	F for ESF	Time (ms)
0	0	A1	A2	A3	A4	F_{T1}	M_1	0.125
0	0	A5	A6	A7	A8	F_{S1}	CRC_1	0.250
0	0	A9	A10	A11	A12	F_{T2}	M_2	0.375
0	0	A13	A14	A15	A16	F_{S2}	FPS_1	0.500
0	0	A17	A18	A19	A20	F_{T3}	M_3	
0	0	A21	A22	A23	A24	F_{S3}	CRC_2	
0	1	B1	B2	B3	B4	F_{T4}	M_4	
0	1	B5	B6	B7	B8	F_{S4}	FPS_2	1.000
0	1	B9	B10	B11	B12	F_{T5}	M_5	
0	1	B13	B14	B15	B16	F_{S5}	CRC_3	
0	1	B17	B18	B19	B20	F_{T6}	M_6	
0	1	B21	B22	B23	B24	F_{S6}	FPS_3	1.500
1	0	C1	C2	C3	C4	F_{T1}	M_7	
1	0	C5	C6	C7	C8	F_{S1}	CRC_4	
1	0	C9	C10	C11	C12	F_{T2}	M_8	
1	0	C13	C14	C15	C16	F_{S2}	FPS_4	2.000
1	0	C17	C18	C19	C20	F_{T3}	M_9	
1	0	C21	C22	C23	C24	F_{S3}	CRC_5	
1	1	D1	D2	D3	D4	F_{T4}	M_{10}	
1	1	D5	D6	D7	D8	F_{S4}	FPS_5	2.500
1	1	D9	D10	D11	D12	F_{T5}	M_{11}	
1	1	D13	D14	D15	D16	F_{S5}	CRC_6	
1	1	D17	D18	D19	D20	F_{T6}	M_{12}	
1	1	D21	D22	D23	D24	F_{S6}	FPS_5	3.000

Legend:

An, Bn, Cn, and Dn are the signaling bits for 16-state signaling in ESF format and represent the bits robbed from DS0 'n' in frames 6, 12, 18 and 24. For4-state signaling Cn and Dn are interpreted as An and Bn. For 2-state signaling Bn, Cn and Dn are interpreted as An.

F_{Tn} are the frame alignment bits for SF; F_{Sn} are the signaling framing bits for SF.

FPS_n are the ESF frame alignment bits; CRC_n are the CRC-6 bits in ESF;

M_n are the Facility Data Link bits in ESF.

Pointer Generation and Telecom Bus Slot Selection

In the DS1MX7 device only the VT1.5/TU-11 termination is provided. The VT Termination block accepts data, alarms and timing information from the Synchronizer/Mapper block and completes the generation of the VT1.5/ TU-11 started in the Synchronizer/Mapper block.

Each mapper can add its VT1.5/ TU-11 to any one of 28 or 84 slots as shown in Figure 31 and Figure 32 below. Control bit TBTVAL (bit 7) in register X+05H must be set to a 1 for the VT1.5/ TU-11 to be added to the Telecom Bus. Bits 6-5 of the same register determine the STS-1, AU3 or TUG-3 number (one of three). Bits 4-2 in this same register determine the VT Group or TUG-2 number (one of seven) and bits 1 and 0 determine the VT1.5 or TU-11 number (one of four).

For Asynchronous operation a fixed position for V5 is generated (offset of 78 with a valid V1 and V2; next VT/ TU byte after V1) as shown in Figure 2 above. For the modified version of Byte Synchronous operation, the VT synchronous payload envelope or virtual container (VT-SPE/ VC) moves to accommodate frequency differences as described above. The VT Termination block provides a pointer generation state machine that follows the Bellcore, ANSI and ITU rules in T1.105, GR-253-CORE and G.709 by generating no more than a single movement every four VT superframes (2.0 ms). Loss of frame or signal will cause a new start of VT superframe position when the signal recovers; this will force a New Data Flag (NDF) request of the VT Termination block. On exiting AIS the synchronizer block will re-center its buffer and request an NDF. The synchronizer block will also look for a change in the expected position of RSYNCn and indicate an NDF request upstream. Valid V1 and V2 bytes are always generated. V3 is used as a stuff opportunity when pointer decrements are done and V4 is unused. For Byte Synchronous operation a fixed position for V5 results from the fact that clock and frame synchronization are outputs which are synchronous with the SONET/SDH structure even though the pointer generation state machine is enabled. Two four-bit counters (one to count increments generated and one to count decrements generated) are provided to track frequency deviations. These counters are located at X+25H (bits 7-4 for increment and bits 3-0 for decrement) with latched shadow values located in the same bits at X+2DH. If an overflow of either counter occurs, status bit PGOS (bit 1) in register X+10H is set to a 1 and an interrupt can be generated; one second polling/clearing of this counter is recommended. A mask PGOM, latched event PGOE, performance value PGOPM and hard fault value PGOFM are all bit 1 of registers X+08H, X+14H, X+18H and X+1CH respectively.

The V5 byte is generated for all modes. V5 is formed from a bit-interleaved parity calculation, a signal label stored in register X+07H bits 2-0, and three alarm bits, REI-V, RFI-V and RDI-V. Now that the entire virtual container is formed, the BIP-2 bits are calculated and inserted in the V5 byte as shown in Figure 2 based on the previous VT-SPE/ VC; the MSB is chosen to make the sum of the odd bits of every byte in the VT-SPE even parity and the second bit is chosen to make the sum of all the even bits of every byte in the VT-SPE even. The alarm bits are mapped based on the results of demapping, DS1 Line conditions or via the Ring Port as shown in the table below. When the Ring Port is enabled, V5 only gets REI-V and RDI-V from this port. RFI-V is used in Byte Synchronous modes only and comes from a microprocessor-forced value as the result of software-based failure detection (usually in the 2 to 3 second range) of a persisting line, section or high or low order path defect or via the signaling highway as the result of a DS1 RAI or Yellow alarm.

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V5 Generation Alarm Sources and Controls

Alarm	Microproc. Force	Demap Conditions	DS1 Line Conditions	Enable Controls	Ring Bit	Ring Enable
BIP-2	SBIPE = 1, reg. X+03H, bit 5. ECTL(7-0) in reg. 01DH sets number of times	none	none	FEBEIS = 1, reg. X+02H, bit 1, enables microproc. forcing. FEBEIS = 0 for normal calculation.	none	none
REI-V = 1	SFEBE = 1, reg. X+03H, bit 5. ECTL(7-0) in reg. 01DH sets number of times	One or two BIP-2 errors	none	FEBEIS = 1, reg. X+02H, bit 1, enables microproc. forcing. FEBEIS = 0 for normal calculation.	REI-V = 1	RINGEN = 1, reg. X+0BH, bit 4
RFI-V = 1	SRFI = 1, reg. X+03H, bit 1.	Software integrated failure state from LOS, LOF, AIS-L/P/V, LOP-P/V, UNEQ-P/V, & PLM-P/V	Yellow via signaling highway; Y-bit = 1	YEL2RFI = 1, reg. X+01H, bit 1.	none	none
RDI-V = 1	SRDI-VSD = 1, reg. X+02H, bit 6.	AIS-V, LOP-V	none	RDIIS = 1 reg. X+02H, bit 3 enables microproc. forcing. RDIIS = 0 for normal insertion from demap	RDI-VSD = 1	RINGEN = 1 reg. X+0BH, bit 4
	SRDI-VCD = 1, reg. X+02H, bit 5.	UNEQ-V			RDI-VCD = 1	

To support three-bit RDI, the Z7 byte is also encoded based on different demap conditions or on the three-bit RDI values supplied by the Ring Port. The unused bits in Z7/K4 are supplied from the Auxiliary Port or the internal register at X+39H; Figure 2 shows the Z7 byte usage for three-bit RDI. The table below defines the conditions that generate three-bit RDI. When the alarms occur in the Demap side of the DS1MX7 and are supplied internally or via the Ring Port, the higher priority code always replaces the lower priority code.

Z7 Three-bit RDI Generation Sources and Controls

Alarm	Microproc. Force	Demap Conditions	Z7 Code bits 5, 6, 7	Priority	Enable Controls	Ring Bit	Ring Enable
RDI-VSD = 1	SRDI-VSD = 1, reg. X+02H, bit 6.	AIS-V, LOP-V	101	1	RDIIS = 1, reg. X+02H, bit 3 enables microproc. forcing. RDIIS = 0 for normal insertion from demap	RDI-VSD = 1	RINGEN = 1, reg. X+0BH, bit 4
RDI-VCD = 1	SRDI-VCD = 1, reg. X+02H, bit 5.	UNEQ-V	110	2		RDI-VCD = 1	
RDI-VPD = 1	SRDI-VPD = 1, reg. X+02H, bit 7.	PLM-V	010	3		RDI-VPD = 1	
none	none	No defects	001	4		all 0	

VT/TU Idle and AIS Insertion are performed at this point. Microprocessor Interface controls for V5 allow either a valid V5 with an all-zeros payload to be generated for idle or an all-zeros V5 for unequipped. Control bit IDLE (bit 7) in register X+00H, when set to a 0, powers down the channel. Control bits RDIIS, FEBEIS, SBIPE, SFEBE, Transmit Signal Label, SRDI-VPD, SRDI-VSD, SRDI-VCD and Tx Z7 all have an effect on the idle sig-

nal sent. The table below provides recommended settings for idle and unassigned (but still monitored) and idle but unequipped (not monitored).

Idle Control of DS1MX7

Control Bit	Valid V5 & Z7 Payload = 0	Payload Z7 & V5 = 0
IDLE; reg. X+00H, bit 7	0	0
RDIIS; reg. X+02H, bit 3	0	1
SRDI-VPD; reg. X+02H, bit 7	X	0
SRDI-VSD; reg. X+02H, bit 6	X	0
SRDI-VCD; reg. X+02H, bit 5	X	0
FEBEIS; reg. X+02H, bit 1	0	1
SFEBE; reg. X+03H, bit 7	0	0
SBIPE; reg. X+03H, bit 5	0	0
Tx Z7; reg. X+39H, bits 7-0	00H	00H
RINGEN (if Ring Port used); reg. X+0BH, bit 4	1	0

Note: X = Don't Care

Control bits SH2VAIS, LOS2AIS, LOF2VAIS, AIS2VAIS, SDAISS and SVTAIS, together with the mapping mode control bits (MODE1, MODE0 and DATACOM) and the line decoder controls (ENCOD and EXPLOS) determine whether AIS or VT AIS is mapped. The AIS alarm bits on the signaling highway, Loss of Frame in modified Byte Synchronous mode, microprocessor command, an all-ones detected in the decoder, a LOS condition detected in the decoder and the LOS condition via a signal on the LAIS pin can be used to generate an AIS (DS1 payload all-ones will be mapped in place of the received signal) or VT AIS (payload, overhead and V1 plus V2 bytes all-ones). The table below details the feature.

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AIS and VT-AIS Generation Sources and Controls

Alarm Generated	Microproc. Force	DS1Line Conditions	MODE1 reg. X+00H, bit 1	MODE0 reg. X+00H, bit 0	DATACOM reg. X+00H, bit 5	Enable Controls
DS1 AIS	SDAISS = 1, reg. X+03H, bit 6	All-ones	X	X	X	none (passes through)
		any	X	X	X	none
		LAIS pin high	0	X	X	EXPLOS =1, reg. X+00H, bit 6 & LOS2AIS = 1, reg. X+01H, bit 6
		LOS detected	0	X	X	ENCOD = 1, reg. X+00H, bit 2 & LOS2AIS = 1, reg. X+01H, bit 6
VT AIS	SVTAIS = 1, reg. X+03H, bit 0	any	X	X	X	none
		LAIS pin high	1	X	X	EXPLOS =1, reg. X+00H, bit 6 & LOS2AIS = 1, reg. X+01H, bit 6
		TSIGLn A-bits = 1	1	X	0	SH2VAIS = 1, reg. X+01H, bit 7
		>99.9% ones detected in decoder	1	X	0	AIS2VAIS = 1, reg. X+01H, bit 0
		Loss of signal on RSYNCn	1	1	X	LOF2VAIS = 1, reg. X+01H, bit 5

Note: X = Don't Care

VT/TU Pointer Tracking and Telecom Bus Slot Selection

In the DS1MX7 device only the VT1.5/TU-11 termination is provided. The VT Termination block accepts data, high order alarms and timing information from the Telecom Bus Interface block, tracks the VT1.5/ TUI-11 pointer and extracts the alarms. The VT Termination block also provides data, alarms and control to the Desynchronizer/Demapper block. All operations (pointer interpretation, pointer generation, VT/TU LOP detection, VT/TU AIS detection, etc.) are performed in accordance with GR-253-CORE, G.709, and G.783.

Each mapper can drop its VT1.5/ TU-11 from any one of 28 or 84 slots as shown in Figure 31 and Figure 32 below. Control bit TBRVAL (bit 7) in register X+04H must be set to a 1 for the VT1.5/ TU-11 to be dropped from the Telecom Bus. Bits 6-5 of the same register determine the STS-1, AU3 or TUG-3 number (one of three). Bits 4-2 in this same register determine the VT Group or TUG-2 number (one of seven) and bits 1 and 0 determine the VT1.5 or TU-11 number (one of four). The values chosen may be the same or different from the add bus values.

The starting location of the V1 byte is determined by the V1 pulses in the DC1J1V1 signals. The VT/TU pointer bit assignment for the V1 and V2 bytes is shown below. The alignment is necessary to determine the starting locations of the V5 byte and the other bytes that are carrying the 1544 kbit/s format.

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V1 Byte								V2 Byte							
1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
N	N	N	N	SS-bits		I	D	I	D	I	D	I	D	I	D

I = Increment Bit
D = Decrement Bit
N = New Data Flag Bit
(enabled = 1001 or 0001/1101/1011/1000, normal or disabled = 0110 or 1110/0010/0100/0111)
Negative Justification: Inverted 5 D-bits and accept 8 out of 10 rule
Positive Justification: Inverted 5 I-bits and accept 8 out of 10 rule
SS-bits (VT Size) = 11 for 1544 kbit/s,

Pointer Bytes Bit Assignment

The pointer value is a binary number with a range of 0 to 103 for the 1544 kbit/s format. It indicates the offset from the V2 byte to the first byte in the VT1.5 mapping. The pointer bytes are not counted in the offset calculation. The pointer offset arrangement for this format is shown below.

1544 kbit/s TU-11/VT1.5

V1
78
79-102
103
V2
0
1-24
25
V3
26
27-50
51
V4
52
53-76
77

VT/TU Pointer Offset Locations

Seven independent pointer tracking state machines are used in the DS1MX7. The pointer tracking algorithm is illustrated in Figure 26. The pointer tracking state machine is based on the pointer tracking machine found in the latest ETSI requirements, and is also valid for both Bellcore and ANSI. See GR-253-CORE and G.709 for pointer processing rules. Where differences occur the GR-253-CORE rules are used; in particular, the AIS state is not exited to LOP state on invalid pointers; receipt of all-ones for a pointer is considered an invalid pointer until 3 consecutive all-ones pointers are received (considered as AIS); new pointers without NDF count toward the 3 consecutive new pointers even though an INC/DEC action is taken as the result of the new pointer mimicking an INC/DEC; the INC/DEC decision is 8 out of 10 bits. When control bit SDH (bit 5) in register 007H is set to a 1, the transition from AIS to LOP is enabled (shown dotted), which is required in ITU recommendations. Increments and decrements are forwarded to the desynchronizer for counting and use in pointer leak controls as described below.

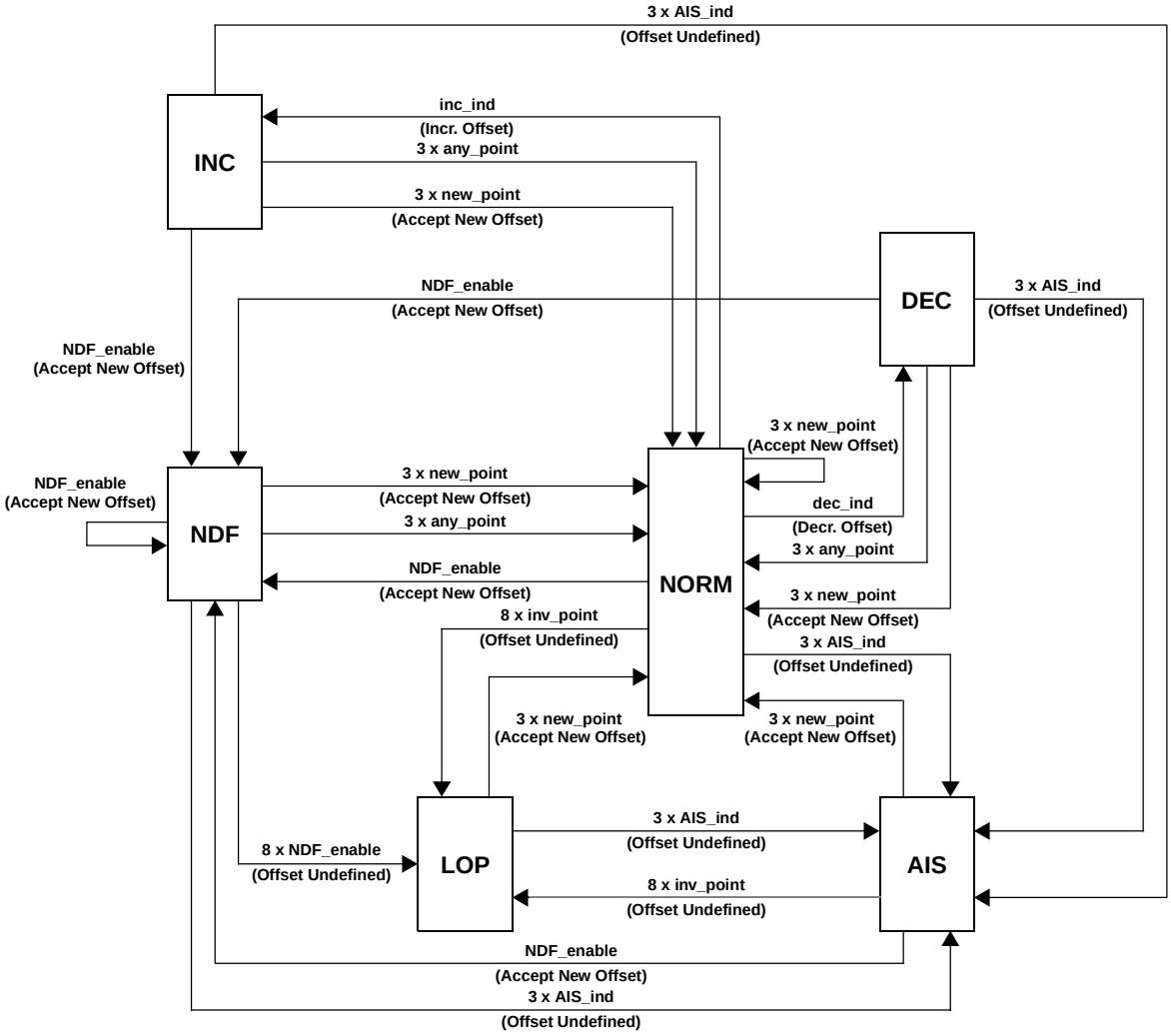


Figure 26. VT/TU Pointer Tracking State Machine

From the Telecom Bus input, V1 and V2 are extracted by means of DC1J1V1 and DSPE. VT/TU LOP and VT/TU AIS are individually made available to the Microprocessor Interface as status bits VAISS and LOPS (bits 5 and 4) in register X+11H. Masks VAISM and LOPM, latched events VAISE and LOPE, performance values VAISPM and LOPPM and hard fault values VAISFM and LOPFM are all bits 5 and 4 of registers X+09H, X+15H, X+19H and X+1DH respectively.The logical 'OR' of these two alarms is handled as AIS for the demapped DS1 as described above in the Transmit Data and Signaling Highway section. The 'SS' bits are compared to the expected value of '11' for a VT1.5/TU-11 and are interpreted as LOP (high level signal failure input at pin DFAIL masks VTAIS, VTLOP and Signal Label Mismatch). The SS-bits are available as status only bits RXSS1 and RXSS0 (bits 4 and 3) in register X+20H.

The Demapper

The Signal Label received in the V5 Byte is extracted and sent to the Microprocessor Interface. It is stored in bits 2-0 of register X+20H. Additional processing is performed to detect a Signal Label Mismatch (compare with Expected Signal Label) and the Unequipped Code. Both conditions are reported to the Microprocessor Interface and notification of an Unequipped or Signal Label Mismatch Condition (also known as VT Path Label Mismatch or PLM-V) is handled as described herein for the mapping direction. Status bits UNES and SLMS (bits 2 and 1) in register X+11 indicate the current condition. Masks UNEM and SLMM, latched events UNEE and SLME, performance values UNEPM and SLMPM and hard fault values UNEFM and SLMFM are all bits 2 and 1 of registers X+09H, X+15H, X+19H and X+1DH respectively. A mismatch alarm is considered as 5 consecutive Signal Labels of a different condition; 5 consecutive matches will clear the alarm. The Signal Label 'Equipped - Nonspecific' (001) received is not considered a mismatch to any non-zero expected value. Also, if the Expected Signal Label is set to 'Equipped-Nonspecific' (001) any non-zero value received for the Signal Label will not cause an alarm. If an unequipped signal label is received, the DS1MX7 will generate an alarm regardless of the setting of the expected signal label (including 000). The alarm should be masked when both ends of a connection are programmed unequipped but a path exists. The table below shows the alarms based on the received versus expected value, per GR-253-CORE.

Signal Label Mismatch and Unequipped Alarms

	Expected Signal Label Stored in reg. X+07H, bits 6-4							
Received Signal Label	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
000	*	UNEQ						
001	M	M	M	PLM				
010			PLM	M	PLM			
011			PLM	PLM	M	PLM		
100			PLM		PLM	M	PLM	
101			PLM			PLM	M	PLM
110			PLM				M	PLM
111			PLM					M

Legend: M = match found and no alarm
PLM = Path label mismatch and alarm, PLM-V
UNEQ = Unequipped alarm (* DS1MX7 will generate an alarm for RX/EXP=000/000)

The V5 and Z7/K4 Bytes are further processed to extract BIP-2 Errors, VT/TU REI (FEBE) Events, and VT/TU RDI-V and VT/TU RFI Alarms. VT/TU RDI-V is de-bounced for 5 (default) or 10 (selectable) consecutive VT superframes before an alarm is declared; 5 (default) or 10 (selectable) consecutive RDI-V = 0 will clear the alarm. De-bounce control is through global register RDID10 (bit 0) in register 01EH which, when set to a 1, causes the DS1MX7 to de-bounce all RDI bits over 10 VT superframes. RFI is de-bounced for 10 consecutive VT superframes before an alarm is declared; 10 consecutive RFI = 0 will clear the alarm. V5 byte RDI and RFI

alarms are sent to the Microprocessor Interface once de-bounced, with status bits RFIS and RDI-VS (bits 3 and 0) in register X+11H. Masks RFIM and RDI-VM, latched events RFIE and RDI-VE, performance values RFIPM and RDI-VPM and hard fault values RFIFM and RDI-VFM are all bits 3 and 0 of registers X+09H, X+15H, X+19H and X+1DH respectively. The VT/TU RFI Alarm can be sent to the signaling highway as a DS1 Yellow for Byte Synchronous modes only, as was described in the Transmit Data and Signaling Highway section.

BIP-2 Errors and VT/TU REI (FEBE) events are accumulated in 12-bit overflow indicating counters. Control bit SDH (bit 5) in register 007H, when set to a 1, will cause BIP-2 errors to count in blocks (count 1 error if one or both BIP-2 bits received is different than calculated). When SDH is set to a 0 each different bit counts as an error. The BIP-2 Error counter is located at location X+26H and X+27H with a shadow value located at X+2EH and X+2FH. An overflow bit BIPOS (bit 6) in register X+11H is set to a 1 if an overflow occurs. The REI (FEBE) Error counter is located at location X+28H and X+29H with a shadow value located at X+30H and X+31H. An overflow bit FEOS (bit 7) in register X+11H is set to a 1 if an overflow occurs. Masks BIPOM and FEOM, latched events BIPOE and FEOE, performance values BIPOPM and FEOPM and hard fault values BIPOFM and FEOFM are all bits 6 and 7 of registers X+09H, X+15H, X+19H and X+1DH respectively.

The DS1MX7 supports three-bit RDI using the Z7/K4 byte. Three-bit RDI is an enhanced Remote Defect Indication that provides three classes of defects: Payload Defect (Path Label Mismatch), Server Defects (Loss of Pointer or AIS) and Connectivity Defects (Unequipped). The mechanism uses a combination of V5 Bit 0, and Z7/K4 Bits 3, 2 and 1 to implement an algorithm that is compatible with the existing RDI-V (V5 Bit 0) and the new indications. When Z7/R4 Bits 2 and 1 = 00 or 11, the RDI is from old equipment. When Z7/K4 Bits 2 and 1 = 01 or 10, the RDI is from enhanced equipment. Enhanced RDI is checked for persistency for either 5 or 10 consecutive VT superframes, the same as for RDI-V. Alarms are available to the Microprocessor Interface. Status bits RDI-VPDS, RDI-VSDS and RDI-VCDS (bits 2-0) of register X+12H indicate the signals received in Z7/K4. Masks RDI-VPDM, RDI-VSDM and RDI-VCDM, latched events RDI-VPDE, RDI-VSDE and RDI-VCDE, performance values RDI-VPDPM, RDI-VSDPM and RDI-VCDPM and hard fault values RDI-VPDFM, RDI-VSDFM and RDI-VCDFM are all bits 2 through 0 of registers X+0AH, X+16H, X+1AH and X+1EH respectively.

The table below indicates the V5 and Z7/K4 bit settings the DS1MX7 uses to support both old equipment and enhanced equipment. Higher priority events (e.g., AIS) cause RDI codes to be sent that override lower priority RDI codes when both conditions occur simultaneously. The signal failure input pin, DFAIL, blocks all RDI-V detection. The DS1MX7 will automatically switch between single-bit and three-bit RDI based on the received Z7/K4 bits 2 and 1.

RDI-V Bit Settings and Interpretation

Z7/K4 Bits 5, 6 and 7	V5 Bit 8	Priority of Enhanced RDI-V Codes	Trigger	Interpretation
yxx[a]	0	Not Applicable	No defects	No RDI-V defect
yxx[a]	1	Not Applicable	AIS-V, LOP-V, UNEQ-V[b]	RDI-V defect (one-bit RDI-V)
001[c]	0[d]	4	No defects	No RDI-V defect
010[c]	0[d]	3	PLM-V	RDI-V Payload defect
101[c]	1[d]	1	AIS-V, LOP-V	RDI-V Server defect
110[c]	1[d]	2	UNEQ-V	RDI-V Connectivity defect

Notes: a. These codes are transmitted by equipment that does not support enhanced RDI-V. If enhanced RDI-V is not supported, Z7 Bits 6 and 7 must be set to the same value.
b. A signal label mismatch (PLM-V) does not cause a one-bit RDI-V
c. This code is transmitted by equipment that supports enhanced RDI-V.
d. V5 Bit 8 is set to the same value as Z7/K4 Bit 5 by the equipment that supports enhanced RDI-V. At the receiving equipment, V5 Bit 8 is ignored unless Z7 Bits 6 and 7 are both set to '0' or both set to '1'

The Signal Label expected and the Signal Label to be sent in the V5 by the DS1MX7 are stored separately in register X+07H. Acceptable values for the Signal Label are as shown in the following table:

VT/TU Assignment	V5 Signal Label (Bits 5-7)
Idle/Unequipped	000
Equipped - Nonspecific	001
Asynchronous Mapping	010
Byte Synchronous Mapping	100

Desynchronization and Pointer Leak Rate Calculations

Desynchronization is performed in two stages, a pointer leak buffer and a DPLL/FIFO. Thus the DS1MX7 removes jitter from the demapped and destuffed VT1.5 or TU-11 in two steps. First the payload is sent to a pointer leak buffer which is a 10-byte deep FIFO centered at 5 bytes, allowing for up to 5 VT pointer increments or decrements in a row to be absorbed when a change in a network condition or rate adjustment for Byte Synchronous mappings are translated into VT pointer movements. The pointer leak buffer converts VT pointer movements (± 8 bits) into slowly leaked single ±1 bit adjustments to the DPLL/FIFO. The pointer leak buffer can be programmed to leak in steps of 8 milliseconds per bit. For test purposes, the pointer leak buffer may be bypassed by setting control bit BYPLB (bit 4) in register 03DH to a 1. STS-1 pointer movements have approximately one twenty-eighth of the effect of a VT pointer movement; STS-1 pointer movements, in effect, represent about one half of a stuffing bit and are handled by the DPLL in the same way as a stuffing bit.

The second filtering stage is provided by the DPLL, which operates from the '31.5 times 1.544 MHz' clock (48.636 MHz) supplied to pin SRCLK. The DPLL controls a FIFO whose depth measurement is made once every VT superframe. From the depth measurement the DPLL adjusts its output frequency to match the effects of stuffing performed for Asynchronous mapping and pointer movements which have been converted to stuffing by the pointer leak buffer. The DPLL provides rate adjustments for Byte Synchronous mappings as well as rate adjustments affecting both mappings in addition to Asynchronous rate tracking. The DPLL has a single pole low pass filter characteristic with a 1.8 Hz corner frequency. Residual jitter without pointer movement of the demapper is approximately 0.20 UI peak to peak (p-p). Mapping and demapping jitter combined with VT pointer movements is under 1.20 UI p-p. Through delay (DA1 to or from Telecom Bus) is under 65 µs.

For testing purposes the DPLL can have its output frequency locked by setting control bit DPLLK (bit 7) in global register 03CH to a 1; control bits DPLL6- DPLL0 in the same global register are used to adjust the output frequency; this affects all seven channels. When control bit DPLLK is set to a 0, control bits DPLL6- DPLL0 can be used to change the DPLL bias offset which changes the DPLL FIFO's residual depth. Control register 03CH must be set to 00H for normal desynchronizer operation.

Since a wide range of VT pointer increment and decrement rates can occur, the DS1MX7 provides a wide range of leak rates. As was mentioned above, the pointer increments and decrements received represent a variety of sources of frequency correction relative to the SONET or SDH clock rates that can occur after a DS1 signal is mapped asynchronously (e.g., due to synchronization failures or clock noise) as well as part of the mapping function for a byte synchronously mapped DS1. A VT pointer movement represents an 8-bit instantaneous frequency correction (an 8 UI jitter spike). Such adjustments are not palatable to most traditional DS1 network equipment and may cause slips or bit errors. The DS1MX7 has a programmable pointer leak buffer that can be set to convert the received VT pointer movements to a rate that can match the actual DS1 payload frequency. For example, if a pointer decrement is being received once every second, the DS1 payload signal needs to be adjusted 8 HZ higher. By programming the pointer leak buffer to leak one bit every 125 milliseconds, the DPLL will automatically run 8 Hz faster continuously by receiving an extra bit in its FIFO every 125 milliseconds. If the pointer leak rate is set too slow the pointers will build up in the pointer leak buffer; at a ±12 bit (one and a half pointers) level the pointer leak rate automatically doubles to compensate. If the pointer leak

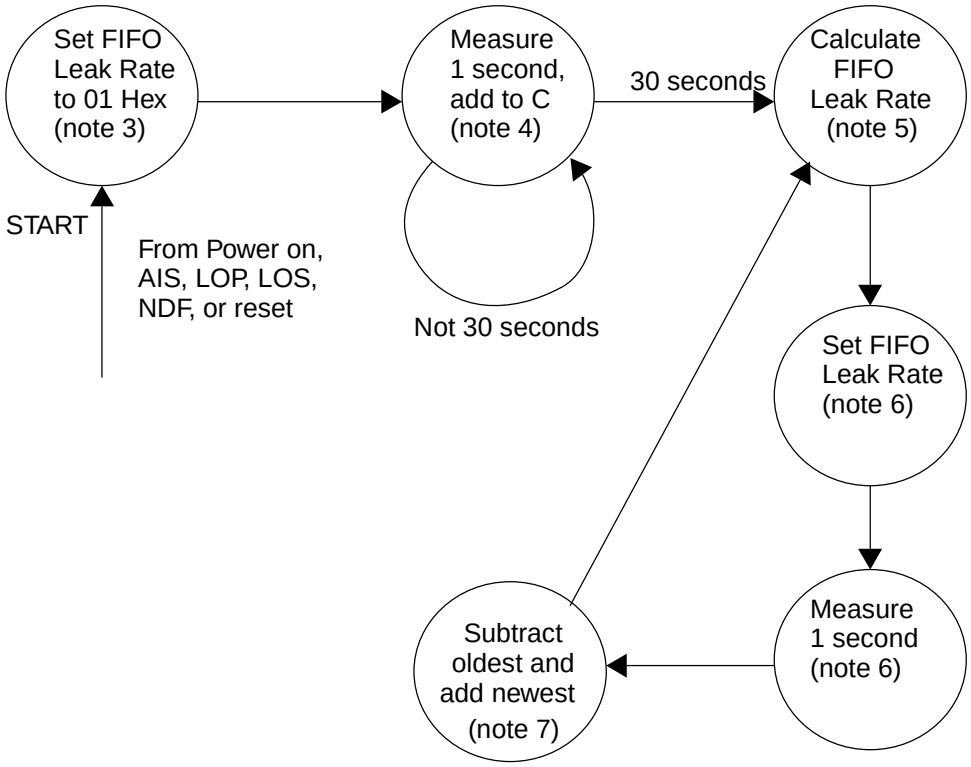
rate is set too fast the frequency will be over-corrected for a period and then return to nominal. For example, if the pointer leak rate were set to once every 63 milliseconds for the 'pointer decrement per second' case, the output frequency would run 16 Hz faster (8 Hz too high) for one half second and return to nominal (8 Hz too low) for one half second. This would cause a frequency modulation of the DS1 output signal that would result in jitter and wander. The Mean Time Interval Error (MTIE) would build up to an undesirable level relative to GR-253-CORE objectives and requirements. The table below indicates the pointer leak rate range available by setting per channel control bits PL8 - PL1 in register X+06H.

PL8 - PL1	Time between bits leaked from Pointer Leak Buffer when less than 12 bits from center	Time between bits leaked from Pointer Leak Buffer when equal to or more than 12 bits from center
00H	16 ms	8 ms
01H	32 ms	16 ms
02H ↓	48 ms ↓	24 ms ↓
FDH	4,064 ms	2,032 ms
FEH	4,080 ms	2,040 ms
FFH	4,096 ms	2,048 ms

A software-based control loop is required to program the DS1MX7 to meet MTIE requirements. The control loop is required to read the received pointer increment and decrement counters, bits 7-4 in register X+24H and bits 3-0 in register X+24H respectively for unlatched values; if the one second performance feature is used by setting control bit ENPMFM (bit 3) in register 006H to a 1 and supplying a 1 Hz ±32 ppm clock on pin T1SI, latch pointer increment and decrement values are preferably used from bits 7-4 in register X+2CH and bits 3-0 in register X+2CH respectively. Measuring the 4-bit counters every one second is sufficient for up to 15 increments or decrements, representing up to ± 120 Hz, which is beyond the range of a Byte Synchronous DS1 used as a clock source (LRCLKn as an input) handled between two add drop multiplexers experiencing a synchronization failure. To initialize the pointer leak buffer, set it to the maximum expected or possible leak rate required from the application (Asynchronous, Byte Synchronous, network clock stratum references along the path, etc.). The table below provides some typical settings.

Mapping	Application	Clock difference	PL8 - PL1
Asynchronous	Add Drop Mux to DCS	38 Hz [20 ppm +4.6 ppm]	01H
Byte Synchronous: LRCLKn an output	Add Drop Mux to DCS	38 Hz [20 ppm +4.6 ppm]	01H
Byte Synchronous: LRCLKn an input	Add Drop Mux to DCS with customer DS1	87 Hz [20 ppm +4.6 ppm + 32 ppm (DS1 @ Stratum 4)]	00H
Asynchronous	DCS to DCS, one stratum 2	7.1 Hz [4.6 ppm]	08H
Asynchronous	DCS to DCS, both stratum 3	14.2 Hz [9.2 ppm]	04H

From the values that are read, use the net value (increment less decrement) to form a running average over a 30 second period. This value is used to calculate the nearest applicable pointer leak rate for within 12 bits of center and written to the DS1MX7 PL8-PL1 per channel control bits. At each subsequent one-second period, the oldest value is discarded and the newest value is added; the pointer leak rate is again calculated and written to the DS1MX7 PL8-PL1 control bits. For a constant stream of pointer increments or decrements, the last pointer should be leaked out just before the next pointer arrives. Missing or additional pointer increments or decrements in the stream will alter the average only slightly. Figure 27 below shows the general algorithm. Each time a DS1MX7 is reset, or the channel experiences an AIS, LOP, NDF or LOS, the algorithm needs to be restarted. The algorithm is independent for all seven channels and must be performed as such. The maximum range of adjustment due to pointers is when PL8 - PL1 is set to 00H. With at least one and a half residual increments or decrements, one additional or less than normal bit per 8 milliseconds will be sent to the DPLL representing, ±125 Hz. This range supports Byte Synchronous mapping for DS1 signals which are ± 50 Hz.



NOTES:

1. The procedure described must be performed independently for each of the seven channels.
2. The procedure shown uses a 30-second sliding window with a 1-second resolution.
3. The initial leak rate is application dependent; however setting the PL8 - PL1 value in register X+06H to 01H will cover all Asynchronous applications and setting it to 00H will cover all Byte Synchronous applications where the DS1 line supplies clock (pleisiochronous).
4. Measure 30 consecutive one-second samples from the Receive Pointer Increment and Decrement Counters. If the counters overflow use a value of 16 for the overflowed counter:
   S_1 = Pointer Increment Value - Pointer Decrement Value for first one-second sample.
   S_2 = Pointer Increment Value - Pointer Decrement Value for second one-second sample, and so on.
   S_{30} = Pointer Increment Value - Pointer Decrement Value for thirtieth one-second sample.
5. Calculate the Leak Rate:
   Leak Rate = Hex [Integer {232/C - 1}] where
   C = Absolute Value [sum(S_i to S_{30+i})] and i represents the number of times through the loop above (notes 5, 6 and 7).
   If the C is 0 set the Leak Rate to FFH; if C exceeds 463 set the Leak Rate to 00H.
   A pointer will be leaked before another arrives for uniform pointer arrivals for $0 \leq C \leq 234$ arrival rates.
6. Set the leak rate register between 0 and 255 per note 5, and take another measurement (e.g., S_{31}).
7. Recalculate the value of 'C' in note 5 by discarding the oldest value and adding the newest value; (i = i + 1).
8. Continue the loop in notes 5, 6 and 7 until AIS, LOP, LOS, NDF or reset.

Figure 27. Pointer Leak Rate Algorithm

In general, the receive DPLL/FIFO in the desynchronizer should never overflow or underflow. If it does it will set status bit DMPS (bit 6) in register X+10H and recenter the FIFO. Mask DMPM, latched event DMPE, performance value DMPPM and hard fault value DMPFM are all bit 6 of registers X+08H, X+14H, X+18H and X+1CH respectively.

MICROPROCESSOR INTERFACE AND COMMON CONTROL/STATUS I/O

The Microprocessor Interface and Common Control/Status I/O block allows access and control for each of the seven DS1 mappers. It also provides common control and status of the entire DS1MX7. Alarm information detected by the mappers can be read as current status and is also latched in event registers which are write to clear. Either the arrival or the departure of a condition can be individually enabled to set the event register. To facilitate either interrupt or polled systems, global interrupt masks, per channel interrupt masks, global event and global polling registers are provided. To assist in the collection of performance parameters, shadow registers and counter latching are provided in addition to latched value and raw value registers. Two forms of shadow registers (performance-PM and fault logic-FM) and counter latching are provided at separate locations and are triggered by an external one second clock input pin (T1SI), as is described below. The configuration of each mapper is provided by this interface. The Serial Port Control block is also controlled by the Microprocessor Interface and Common Control/Status I/O. The microprocessor bus supports both Intel and Motorola style processors with a minimum amount of interface logic. An external pin (MOTOI) configures the type of bus supported. The data bus is an 8-bit, bidirectional, 3-state port. The internal control and status registers are accessed through this port. When not accessed, this port is in a high impedance state. The address bus is a 9-bit input port. These address pins select individual control and status registers within the mapper. $\overline{\text{SELI}}$ is the microprocessor port select signal. $\overline{\text{WRI}}$ and $\overline{\text{READI}}$ / READI/$\overline{\text{WRI}}$ are the microprocessor port write and read/write input pins (only the latter is used for the Motorola interface). The RDYO/$\overline{\text{DTACKO}}$ output is used to delay microprocessor access, if required to access internal registers. The INTO/$\overline{\text{IRQO}}$ output is the microprocessor port interrupt line. The $\overline{\text{RSTI}}$ input is the overall device reset line that resets all counters, state machines and the configuration. PCKI is a high speed processor clock input signal that is used by all blocks.

Alarms

The nineteen per channel alarms have been covered in the above sections. To facilitate a quick microprocessor location of an alarm that has been programmed to generate an interrupt, global event and mask registers are provided as well as an activity register. Global masks are provided at register locations 015H and 016H. Setting any of these to a 1 will prevent that condition from generating an interrupt; for example, if the DS1MX7 is programmed for Asynchronous operation, setting GRFIM (bit 3) in register 016H to a 1 would prevent RFI alarms (used in Byte Synchronous mappings) from causing spurious interrupts. Global event registers are provided at locations 013H and 014H. These registers are the logical 'or' of all seven like per channel registers; for example, GLOSE (bit 5) in register 013H is the logical 'or' of all seven LOSE per channel event registers. Note that GRDIE and GRDIM provide a global event indication and mask for all RDI conditions (RDI-VE; V5 bit 8 and RDI-VPDE, RDI-VSDE, RDI-VCDE; Z7 bits 5, 6 and 7). To facilitate polling, an activity register is provided at location 011H; each bit CH1 to CH7 (bits 0 to 6) represents a mapper channel (1 to 7). Each bit CHn is the logical 'or' of all 19 event bits for mapper channel 'n'. To disable all interrupts to pin INTO/$\overline{\text{IRQO}}$, control bit GIM (bit 7) in register 006H can be set to a 1; polling may be done instead to detect alarm events. The interrupt polarity may be inverted by setting control bit IPOL (bit 4) in register 006H to a 1.

Events may be latched into the event registers (global registers 00CH and 00DH or per channel registers X+14H, X+15H and X+16H) either on the onset of the condition, the exit of the condition or both. Control bit RISE (bit 6) in register 006H, when set to a 1, will cause the associated event bit to be set when a status bit changes from 0 to 1. Likewise, control bit FALL (bit 5) in register 006H, when set to a 1, will cause the associated event bit to be set when a status bit changes from 1 to 0. By setting both RISE and FALL to a 1, both the onset of an alarm and the clearing of an alarm will cause an interrupt if the event register is cleared after the onset of the alarm.

Assuming all mask bits are set to a 0, Asynchronous mode is used, and both RISE and FALL are set to a 1, the following scenario would apply if mapper channel 2 (X=080H) detected a LOS condition for 2 seconds at its line decoder. First, bit 5 of register 090H (LOSS) would be set to a 1. Bit 5 of register 094H (LOSE) would be set to a 1 on the rising edge of LOSS. This would set bit 5 of register 013H (GLOSE) to a 1, set bit 1 of register 011H (CH2) to a 1 and cause an interrupt to be asserted on pin INTO/$\overline{\text{IRQO}}$. The software in the attached microprocessor would respond by reading registers 011H, 013H and 014H. Analysis would indicate an LOS change at channel 2. The software in the attached microprocessor would then respond by reading registers

090H and 094H, followed by clearing register 094H by writing 00H to it. This writing to clear will automatically clear the interrupt, bit 5 of register 013H (GLOSE) and bit 1 of register 011H (CH2). At the end of 2 seconds, bit 5 of register 090H (LOSS) will clear. Bit 5 of register 094H (LOSE) would be set on the falling edge of LOSS. This would set bit 5 of register 013H (GLOSE) to a 1, set bit 1 of register 011H (CH2) to a 1 and cause an interrupt to be asserted on pin INTO/$\overline{\text{IRQO}}$. The software in the attached microprocessor would respond by reading registers 011H, 013H and 014H. Analysis would indicate an LOS change at channel 2. The software in the attached microprocessor would then respond by reading registers 090H and 094H followed by clearing register 094H by writing 00H to it. This writing to clear will automatically clear the interrupt, bit 5 of register 013H (GLOSE) and bit 1 of register 011H (CH2).

To provide for operational security and fault localization, system clocks and reference signals are optionally monitored for lack of transitions and alarmed to the Microprocessor Interface and the internal alarm output in $\overline{\text{IAO}}$. Status bits TBRCKS, TBRSNS and TBRPAS (bits 7 through 5) in register 00AH indicate a failure of DCLK, DC1J1V1 or DSPE, if set to a 1, respectively. Mask bits MTBRCF, MTBRSF and MTBRPF, latched event bits TBRCKE, TBRSNE and TBRPAE, performance values TBRCKPM, TBRSNPM and TBRPAPM, and fault values TBRCKFM, TBRSNFM and TBRPAFM are all bits 7, 6 and 5 of registers 008H, 00CH, 00EH and 03EH respectively. Status bits TBTCKS, TBTSNS and TBTPAS (bits 2 through 0) in register 00AH indicate a failure of ACLK, AC1J1V1 or ASPE, if set to a 1, respectively. Mask bits MTBTCF, MTBTSF and MTBTPF, latched event bits TBTCKE, TBTSNE and TBTPAE, performance values TBTCKPM, TBTSNPM and TBTPAPM, and fault values TBTCKFM, TBTSNFM and TBTPAFM are all bits 2 through 0 of registers 008H, 00CH, 00EH and 03EH respectively. Status bit MCKS (bit 3) in register 00AH indicates a failure of SRCLK if set to a 1. Mask bit MMCKF, latched event bit MCKE, performance value MCKPM, and fault value MCKFM are all bit 3 of registers 008H, 00CH, 00EH and 03EH respectively.

In addition, internal checks are made in the Telecom Bus Interface block to determine if two or more channels of a DS1MX7 device attempt to drive the same bus slot; if multiple channel drive attempts are detected an internal alarm event is indicated by status bit TBIES (bit 1) in register 00BH being set to a 1. Mask bit MTBIE, latched event bit TBIEE, performance value TBIEPM, and fault value TBIEFM are all bit 1 of registers 009H, 00DH, 00FH and 03FH respectively. Similarly, if two or more DS1MX7s attempt to drive the Telecom Bus simultaneously, an external alarm is declared by status bit TBXES (bit 0) in register 00BH being set to a 1; this is implemented by connecting the $\overline{\text{AADD}}$ output of each DS1MX7 to one of the three $\overline{\text{BUSCHK}}$ inputs of the other DS1MX7s (up to 4 DS1MX7s are supported without external logic). Mask bit MTBXE, latched event bit TBXEE, performance value TBXEPM, and fault value TBXEFM are all bit 0 of registers 009H, 00DH, 00FH and 03FH respectively. Parity errors are monitored on the Drop Telecom Bus for all active slots from which signals are dropped. Control bit TBPIS (bit 3) in register 007H includes DC1J1V1 and DSPE in the parity check if set to a 1. Control bit TBPE (bit 2) in the same register selects even parity if set to a 1. Status bit TBRPYS (bit 3) in register 00BH is set to a 1 whenever a parity error is detected. Mask bit MTBRPY, latched event bit TBRPYE, performance value TBRPYPM, and fault value TBRPYFM are all bit 3 of registers 009H, 00DH, 00FH and 03FH respectively. Bad parity may be forced onto the Add Telecom bus by setting control bit FTBTPE (bit 6) in register 01EH to a 1.

Device alarms can also be enabled to a separate alarm output pin $\overline{\text{IAO}}$, which can be used as an interrupt or a board failure lead when wire "or'ed" with other DS1MX7s. Control bits ETBRCF, ETBRSF, ETBRPF (bits 7 through 5) in register 01BH, when set to a 1, enable the DCLK, DC1J1V1 and DSPE failures to drive pin $\overline{\text{IAO}}$ low. Control bits ETBTCF, ETBTSF, ETBTPF (bits 2 through 0) in register 01BH, when set to a 1, enable the ACLK, AC1J1V1 and ASPE failures to drive pin $\overline{\text{IAO}}$ low. Likewise, EMCKF (bit 3) in register 01BH, when set to a 1, enables the SRCLK failure to drive pin $\overline{\text{IAO}}$ low. Control bits ETBRPY, ETBIE, ETBXE (bits 3, 1 and 0) in register 01CH, when set to a 1, enable the Parity error, internal Telecom Bus collision and external Telecom Bus collision to drive pin $\overline{\text{IAO}}$ low. The alarm output $\overline{\text{IAO}}$ is enabled by control bit ENHWM (bit 2) in register 006H being set to a 1.

To provide for masking alarms on a particular assigned VT/TU, the DFAIL input pin signal, which indicates a general signal failure, is sampled on the rising edge of DCLK and latched for the particular channel assigned to that VT/TU column. If it is high, the data on DD(0-7) is invalid (e.g., STS-1 AIS), and any alarms generated as

a result will not interrupt the microprocessor. However, some consequent actions on the data should still be properly handled (e.g., generate DS1 AIS); other actions (e.g., RDI) will not occur. DFAIL is not included in bus parity. The following tables show the masking of lower order alarms by higher order alarms provided in the DS1MX7 in both the mapping and demapping directions.

DS1MX7 Demapper Alarm Masking

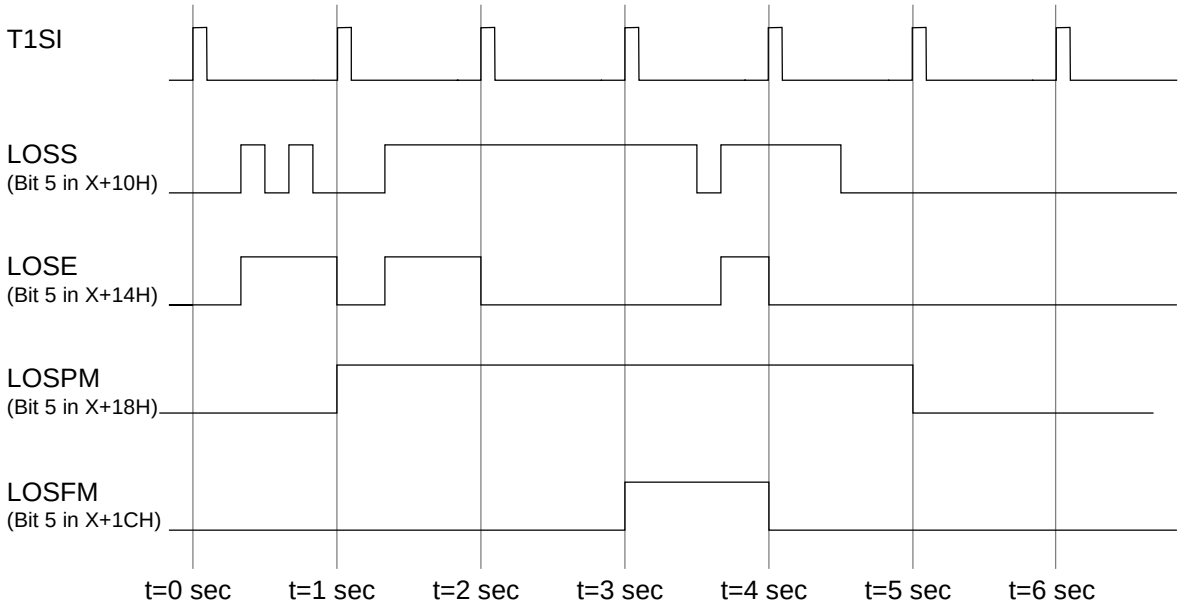
Condition Reported	Signal Fail	VT AIS detected	VT LOP detected	VT Unequipped detected	Signal Label Mismatch detected	VT RDI detected	VT RFI detected	Demap Error
Signal Failure	X							
VT AIS		X						
VT LOP			X					
VT Uneq.				X				
Sig Label Mismatch					X			
VT RDI						X		
VT RFI							X	
Demap Error								X

The shaded area indicates which detectors are blocked for which condition. For example, VT AIS blocks VT LOP, VT Unequipped, Signal Label Mismatch, VT RDI, VT RFI and Demap errors.

DS1MX7 Demapper Alarm Masking

Condition	LOS	AIS	OOF	Yellow	Map error
LOS	x				
DS1 AIS		x			
OOF			x		
Other					

Figure 28 illustrates the operation of the shadow registers for a loss of signal (LOSS) alarm for any one of the seven mappers. The behavior shown in the diagram also applies to the other alarms in the same registers (AIS, LOP, RDI, etc.) for per channel alarms. Global control bit ENPMFM (bit 3) in register 006H is assumed to be set to a 1. Global alarms (e.g. Master Clock Fail - MCKS, MCKE, etc.) are handled slightly differently in that the T1SI pulse does not clear the event value as it does for per channel alarms. This figure assumes that control bits RISE and FALL (bits 6 and 5) in the Global Configuration Register 006H are set to 10 (latched event set on a positive transition only). Please note that the LOS alarm causes a latched status indication LOSE (bit 5) in register X+14H, and that the latched bit is reset by the rising edge of the T1SI pulse. The LOSPM status bit (bit 5) in register X+18H is a 1 whenever there is a transition to LOS during the last one-second interval or LOS is present at the end of the last one-second interval. The LOSFM status bit (bit 5) in register X+1CH is a 1 if the LOS alarm is active but did not become active during the previous one-second interval.



Note 1: For this example, latched events are set only on positive event transitions.

Note 2: LOSPM = LOSS + LOSE evaluated at one-second boundaries (where '+' is a logical or).

Note 3: LOSFM = LOSS & $\overline{\text{LOSE}}$ evaluated at one-second boundaries (where '&' is a logical and, and $\overline{X}$ is a logical inversion).

Figure 28. Shadow Register Operation

SERIAL PORT CONTROL INTERFACE

The Serial Port Control Interface block is a serial interface that can be used to control and manage the external analog line transceivers operating in the 'host mode'. This allows the system processor to have complete co n-trol of the line transceivers through the DS1MX7 Microprocessor Interface. The interface consists of a data input pin (LSDI), a data output pin (LSDO), and a serial clock output pin (LSCLK) that are shared among all the transceivers. The source of LSCLK is the signal present on input pin LO. In addition, there is an individual chip select ($\overline{\text{LCSn}}$) for each transceiver, and an individual input (LAISn) from each transceiver that may be used to generate a maskable interrupt; status bit XPS (bit 7) in register X+10H indicates the signal on this pin. A mask XPM, a latched event value XPE, a PM value XPPM and a FM value XPFM are available (bit 7) at register locations X+08H, X+14H, X+18H and X+1CH respectively. If desired, the signal at this pin may be used to indicate a Loss of Signal, which can be used to generate AIS (see the Line Interface section for details).

Data to be written to the external transceiver is formatted as a two-byte message. The first byte is an address/ command byte and the second byte contains the data to be written or read. Figure 29 illustrates the message and control formats associated with the transceiver serial I/O timing. The format of the address/command byte depends upon the external transceiver being controlled. Please refer to the transceiver's data sheet for the command/data formats. The interface for controlling the external transceiver operates in the following way. The external transceiver selection (via $\overline{\text{LCSn}}$) is determined by the value written to three bits (bits 2, 1 and 0) in register 01AH. For example, a 000 value selects the transceiver for mapper 1. The microprocessor writes the com-

mand byte to the Line Interface Control register 017H. This is followed by writing the data byte to be written to the selected transceiver in Line Interface Control register 018H. The serial message is sent on LSDO when a 1 is written to replace the 0 in the ENSRP bit (bit 4) in register 01AH. The ENSRP bit must be first written with a 0, followed by a 1, before another transfer can take place between the DS1MX7 and the external transceiver selected. Broadcast capability to all transceivers is enabled when the control bit BDCST (bit 7) in register 01AH is written with a 1. Eight clock cycles later, the selected transceiver will respond by sending serial data on the LSDI input pin. The data is shifted in to the Serial Port Data Input Register 019H, LSB first.

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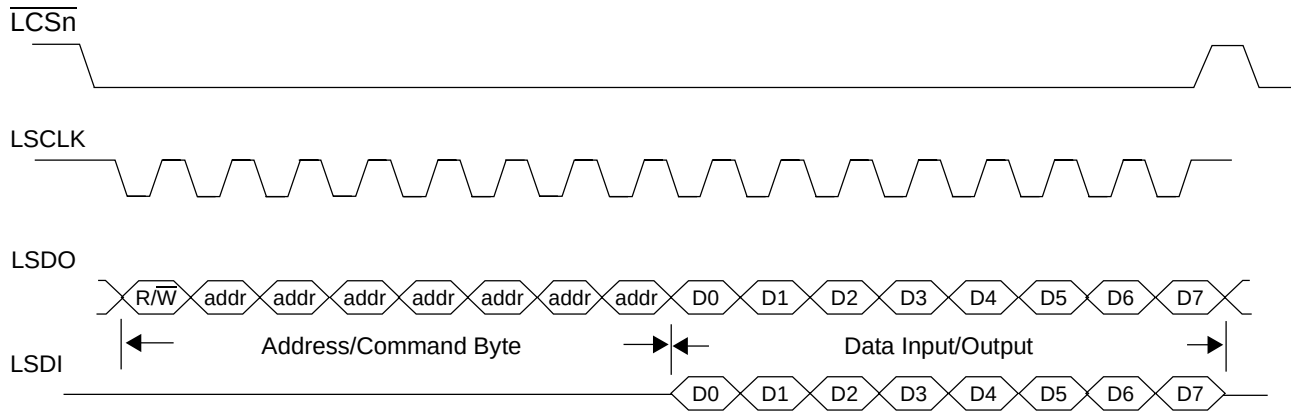
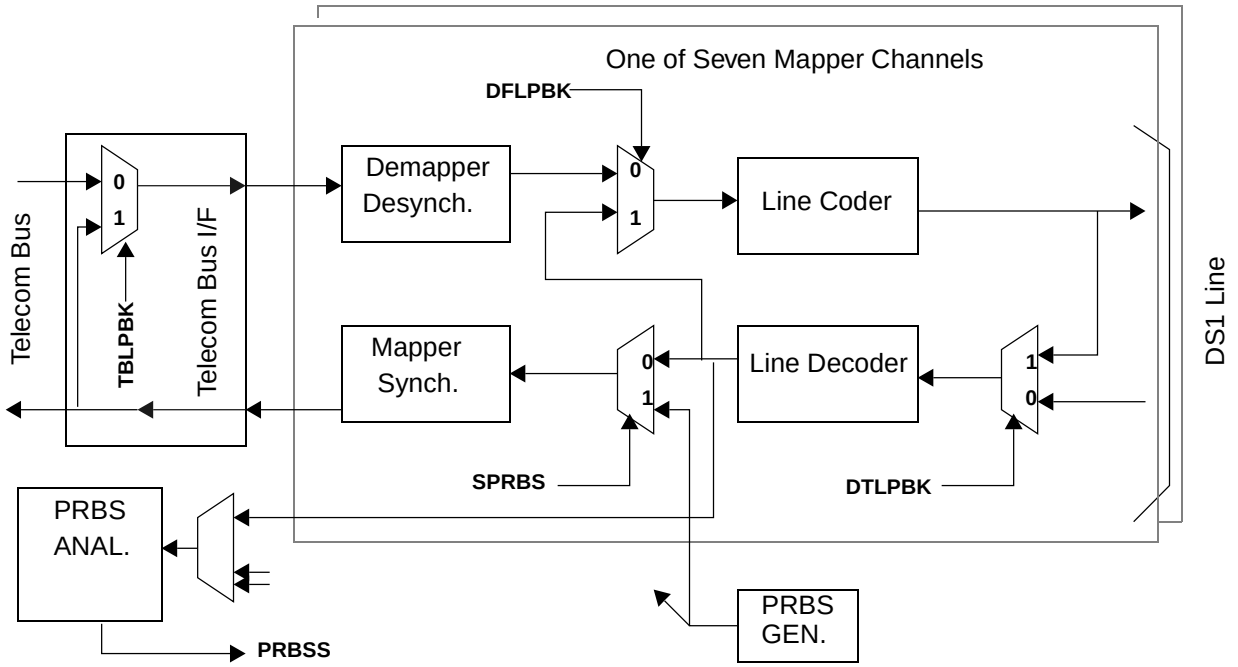


Figure 29. Serial Interface Operation

DS1MX7 Channel Testing using the PRBS Generator and Analyzer

The PRBS Generator and Analyzer block provides the ability to test each channel using the tributary and/or Telecom Bus loopback features provided. Figure 30 below shows the general configuration used for testing any one of the seven channels. Control bit TBLPBK (bit 7) in register 01EH, when set to a 1, loops back the Telecom Bus. Setting TBLPBK to a 1 should only be done if all seven channels are off line, because normal operation for the channels not under test is suspended. For the Telecom Bus loopback to function, control bits in registers X+04H and X+05H also need to be set to enable the VT1.5/ TU-11 to and from the same Telecom Bus slot. Control bit DTLPBK (bit 7) in register X+0CH, when set to a 1, loops the encoder output clock, signaling, synchronization pulse and data back to the decoder input, providing a local loopback. The local loopback can be moved to the Line Interface Transceiver or as a distant end remote loop back. If the distant end is a DS1MX7, control bit DFLPBK (bit 6) in register X+0CH may be set to a 1 to loop the received DS1 clock, signaling, synchronization and data to the transmit clock, signaling, synchronization and data. The PRBS pattern may be inserted into any one or more mappers in place of the line decoder output by setting control bit SPRBS (bit 4) in register X+0CH to a 1 when control bit EPRBSA (bit 5) in global register 01AH is also set to a 1. The PRBS Analyzer is assigned to a mapper channel by the same control bits used to select an LIU for the serial port, bits 2- 0 in register 01AH. The analyzer monitors any one of the seven line decoder outputs. The output of the analyzer is readable by the Microprocessor Interface as status bit PRBSS (bit 2) in register 00BH with a mask MPRBSE, a latched value PRBSE, a performance value PRBSPM and a hard fault value PRBSFM, all bit 2 in registers 009H, 00DH, 00FH and 03FH respectively. The pattern is a 2^{15}-1 bit pseudo-random binary sequence that follows the ITU O.151 recommendations, but is inverted. Control bit TXNRZP (bit 0) in register 007H, when set to a 1, will make the internal PRBS signal readable by standard test equipment connected to the DS1 line side of the DS1MX7 mapper channel. The Out Of Lock alarm can be made to go to an external pin $\overline{\text{IAO}}$, if desired, by setting control bit EPRBSE, bit 2 in register 01CH, to a 1.



Note: Control and status bits are shown in bold font

Figure 30. Loopbacks and Built-in PRBS Testing of the DS1MX7

TELECOM BUS INTERFACE

The Telecom Bus Interface contains the drivers and receivers for all the Telecom Bus signals. It multiplexes and demultiplexes all the data flowing from/to the Telecom Bus Output and Input Control blocks. It also calculates the parity for APAR and checks the parity against DPAR for any driven slot used by this DS1MX7 (both odd and even parity are selectable, and APAR may be calculated on AD(0-7) only or on the combination of AD(0-7), ASPE and AC1J1V1); slots that are not selected are skipped. Telecom Bus assignments can be used to localize parity errors. This block generates the $\overline{\text{AADD}}$ signal for any active slot driven by this DS1MX7, to permit using external buffers. $\overline{\text{AADD}}$ is generally not required as the DS1MX7 outputs are tri-stated; however, if an application requires bus drivers with different characteristics or with additional drive this signal is available. SPE is valid during the STS-1 or STS-3 synchronous payload. C1J1V1 defines the starting position of the VT/TUs on the bus. Note that AD(0-7) data is pre-fetched to be ready to be clocked into an external device on the rising edge of ACLK; if the column or byte is a stuff position in the STS-1 the data remains present until the slot is a valid SPE (ASPE active). For systems that use the Telecom Bus to multiplex in transport or path overhead information (e.g., H4 via the TranSwitch SOT-1E), the DATEN pin should be tied externally to ASPE so that SPE inactive bytes are not driven during the rising edge of ACLK. If required, the $\overline{\text{MASTER}}$ input pin may be grounded so that the STS-1 POH and stuff columns or bytes may be driven with idle (all-zeros with valid parity) or an assigned VT value such that bus parity errors are prevented. The following table shows which bytes are driven on the Telecom Bus in various modes; note that each STS-1 or TUG-3 is treated separately. Under Microprocessor Interface control the data, AD(0-7), may be delayed one clock period by control bit TBDD (bit 3) in register 01EH, and the active clock edges of DCLK and ACLK may be inverted by control bits TBRCI (bit 4) and TBTCI (bit 5) in the same register being set to a 1.

.

DATEN and $\overline{\text{MASTER}}$ Pins	Assigned VT	Unassigned VT	POH and Stuff	TOH	TOH
Condition				Followed by assigned VT	Followed by POH or Stuff
DATEN high; $\overline{\text{MASTER}}$ high	driven $\overline{\text{AADD}}$ low	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high	driven to VT value that follows $\overline{\text{AADD}}$ low	float $\overline{\text{AADD}}$ high
DATEN high; $\overline{\text{MASTER}}$ low	driven $\overline{\text{AADD}}$ low	float $\overline{\text{AADD}}$ high	driven to zero $\overline{\text{AADD}}$ high	driven to VT value that follows $\overline{\text{AADD}}$ low	driven to zero $\overline{\text{AADD}}$ high
DATEN = ASPE; MASTER high	driven $\overline{\text{AADD}}$ low	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high
DATEN = ASPE; MASTER low	driven $\overline{\text{AADD}}$ low	float $\overline{\text{AADD}}$ high	driven to zero $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high
DATEN low	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high	float $\overline{\text{AADD}}$ high

The Telecom Bus Interface also provides a loopback mode for device testing. Internally, the entire Telecom Bus is looped. Individual channels are tested by enabling them through the serial port select byte for the PRBS Analyzer and the per channel select bit for the PRBS Generator, as described above.

The Mapper Timing block supplies overall mapper timing to both the Synchronizer/Mapper and the Desynchronizer/Demapper blocks based on the Telecom Bus clocks, C1J1V1 and SPE signals received. SONET and SDH have different stuff column positions. In SONET format V1 is coincident with V1 #1; in SDH format for TUG-3, V1 starts six TUG-3 clock pulses early. A bit in the Common Control register is used to select this. The external clock, LO, is an independent 1.544 MHz clock for the purpose of generating a system-synchronized clock for clocking in data and signaling for Byte Synchronous operation.

The DS1MX7 can operate at 6.48 MHz or 19.44 MHz, as shown in Figures 31 and 32. The bus speed is determined by the CONFIGI pin; if tied low, the DS1MX7 operates in 19.44 MHz mode with 84 VT1.5/ TU-11 slots; if tied high, the DS1MX7 operates in 6.48 MHz mode with 28 VT1.5/ TU-11 slots. For gapped clock situations an allowance for up to 10% higher speed needs to be made. The DS1MX7 cannot account for extra columns, so SPE being inactive for extra columns must be used.

For 19.44 MHz operation in SONET or SDH AU-3 mapping, the three J1 signals can be anywhere in the STS-1 or AU-3 for both DC1J1V1 and AC1J1V1; hence separate tracking is provided for each. Control bit VC3VC4 (bit 1) in register 007H must be set to a 1. In this mode of operation there are no restrictions on the three J1 positions in AC1J1V1 for Asynchronous or modified Byte Synchronous applications. However, if Byte Synchronous modes are used, the three J1s in AC1J1V1 cannot move with respect to each other, since LO must be locked to ACLK and AC1J1V1. If all channels are mapped to a specific STS-1, the restriction does not apply as long as the J1 reference for LO is the same STS-1.

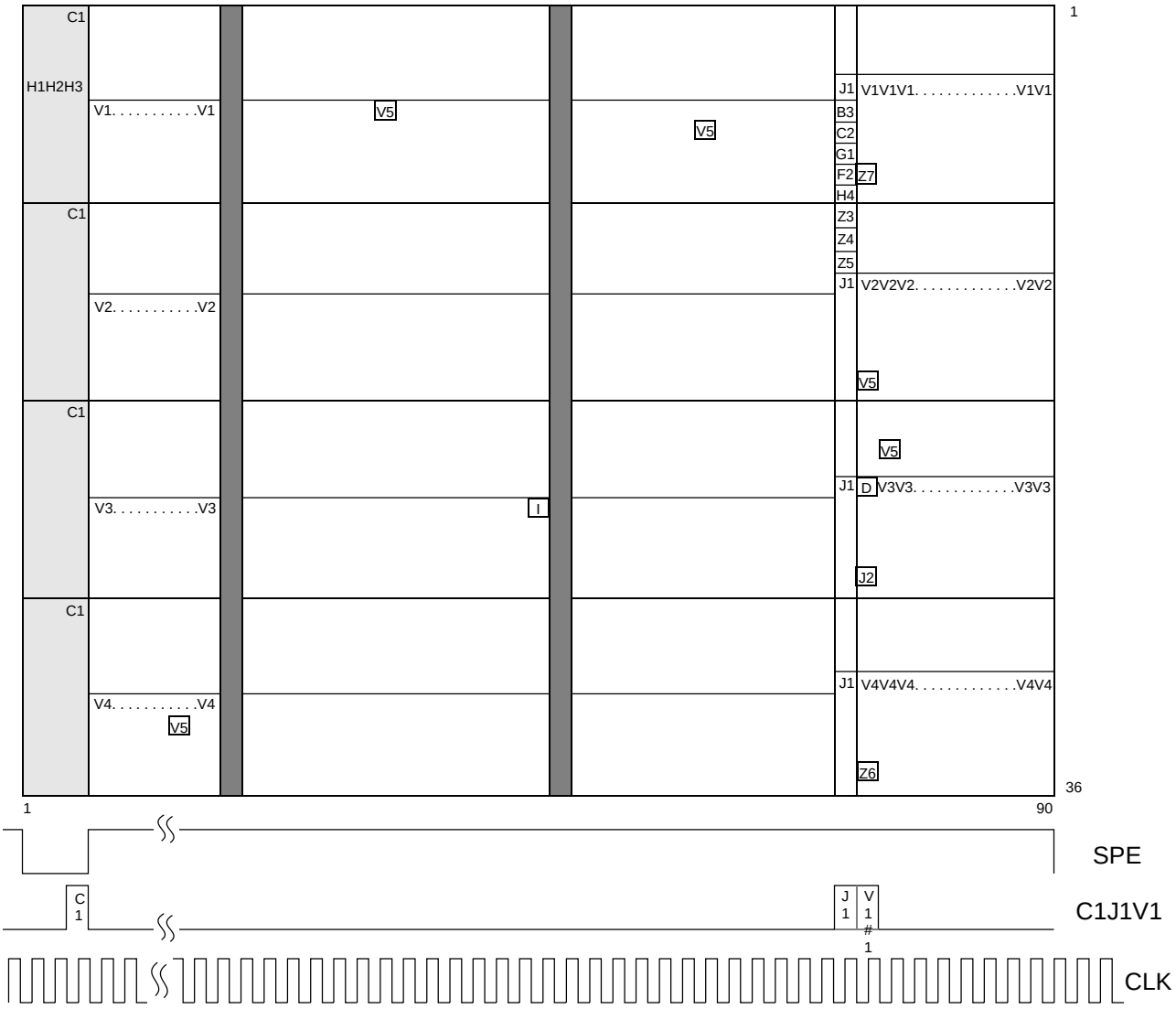


Figure 31. Telecom Bus Structure; SONET or VC-3 SDH; Telecom Bus @ 6.48 MHz

The signals shown in Figure 31 are valid for the entire STS-1 signal, representing an overlay of all 36 rows of 90 bytes each. Each of the 28 VT1.5s occupy 3 columns (counted from the STS-1 path overhead and with the two stuff columns the same) with transport overhead (TOH) taking 3 columns (shaded), the STS-1 path overhead taking a column (J1, B3.Z5) and 2 columns of fixed stuff (crosshatched). SPE is only low during TOH. C1J1V1 is high during the 4 C1 bytes shown, the 4 J1 bytes shown and the one V1 #1 byte shown. For VT#1 of VTG#1, J2, Z6 and Z7 are also shown. Figure 33 below provides the column assignments for an STS-1 system bus. The STS-3 case is as depicted in Figure 32, with the columns of the three STS-1s byte-interleaved; in this case, the three C1 bytes occur together, but the individual J1 bytes can occur in any of the 87 columns of the STS-1 or VC-3. Fixed offset places V5s after V1s. Figure 34 below provides the column assignments for the STS-3.

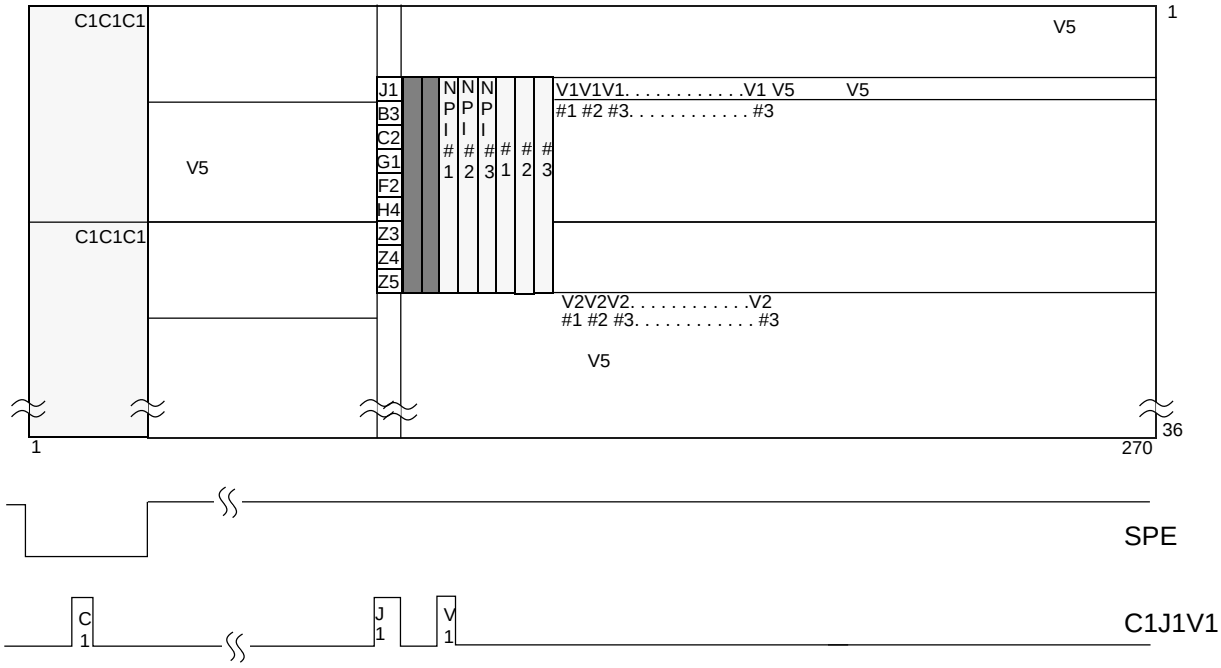


Figure 32. Telecom Bus Structure; TUG-3 SDH; Telecom Bus @ 19.44 MHz

Figure 32 above shows the SDH format for three TUG-3s in a VC-4. Control bit VC3VC4 (bit 1) in register 007H must be set to a 0. Figure 35 below provides the column assignments for an STM-1. Each TUG-3 contains seven TUG-2s and each TUG-2 contains four TU-11s. The signals shown are an overlay of all 36 rows of 270 bytes each. SPE is low only for the STM-1 transport overhead (TOH), which is the first 9 columns (shaded). C1J1V1 is high for the first C1 byte of the TOH, the J1 byte of the VC-4 path overhead (POH) and the first column of each TUG-3 (null pointer indications). Fixed offset for V5 generation of 78 places system-bound V5 bytes after V1 bytes for Asynchronous and Byte Synchronous modes only.

MULTIPLEX FORMAT AND MAPPING INFORMATION

STS-1 VT1.5 (1.544 Mbit/s) Multiplex Format

The following diagram and table illustrate the mapping of the 28 VT1.5s into a STS-1 SPE. Column 1 is assigned to carry the path overhead bytes.

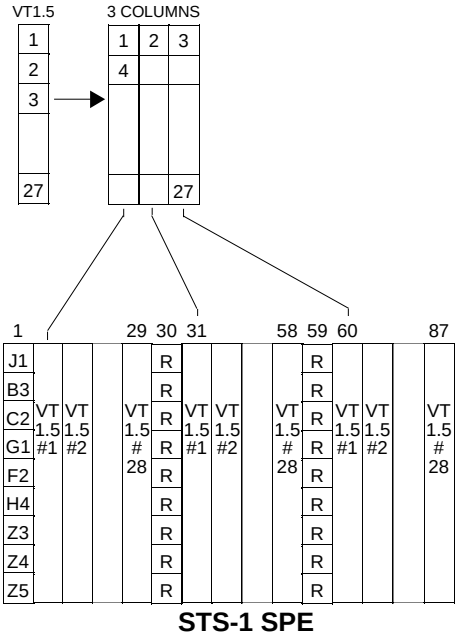


Figure 33. STS-1 SPE Mapping

STS-1 Mapping

VT#	Registers X+04H for Drop and X+05H for Add								VT1.5 Column Numbers*
	7	6	5	4	3	2	1	0	
	0	X	X	X	X	X	X	X	No VT Selected
1	1	0	0	0	0	0	0	0	2, 31, 60
2	1	0	0	0	0	1	0	0	3, 32, 61
3	1	0	0	0	1	0	0	0	4, 33, 62
4	1	0	0	0	1	1	0	0	5, 34, 63
5	1	0	0	1	0	0	0	0	6, 35, 64
6	1	0	0	1	0	1	0	0	7, 36, 65
7	1	0	0	1	1	0	0	0	8, 37, 66
8	1	0	0	0	0	0	0	1	9, 38, 67
9	1	0	0	0	0	1	0	1	10, 39, 68
10	1	0	0	0	1	0	0	1	11, 40, 69
11	1	0	0	0	1	1	0	1	12, 41, 70
12	1	0	0	1	0	0	0	1	13, 42, 71
13	1	0	0	1	0	1	0	1	14, 43, 72
14	1	0	0	1	1	0	0	1	15, 44, 73
15	1	0	0	0	0	0	1	0	16, 45, 74
16	1	0	0	0	0	1	1	0	17, 46, 75
17	1	0	0	0	1	0	1	0	18, 47, 76
18	1	0	0	0	1	1	1	0	19, 48, 77
19	1	0	0	1	0	0	1	0	20, 49, 78
20	1	0	0	1	0	1	1	0	21, 50, 79
21	1	0	0	1	1	0	1	0	22, 51, 80
22	1	0	0	0	0	0	1	1	23, 52, 81
23	1	0	0	0	0	1	1	1	24, 53, 82
24	1	0	0	0	1	0	1	1	25, 54, 83
25	1	0	0	0	1	1	1	1	26, 55, 84
26	1	0	0	1	0	0	1	1	27, 56, 85
27	1	0	0	1	0	1	1	1	28, 57, 86
28	1	0	0	1	1	0	1	1	29, 58, 87

* Note: Columns 30 and 59 carry fixed stuff bytes. Column 1 is assigned for the POH bytes.

STS-3/AU-3 VT1.5/TU-11 (1.544 Mbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the VT1.5/TU-11s into a STS-3/AU-3 SPE. Each STS-3 carries three STS-1s. Column 1 in each STS-1/AU-3 is assigned to carry the path overhead bytes.

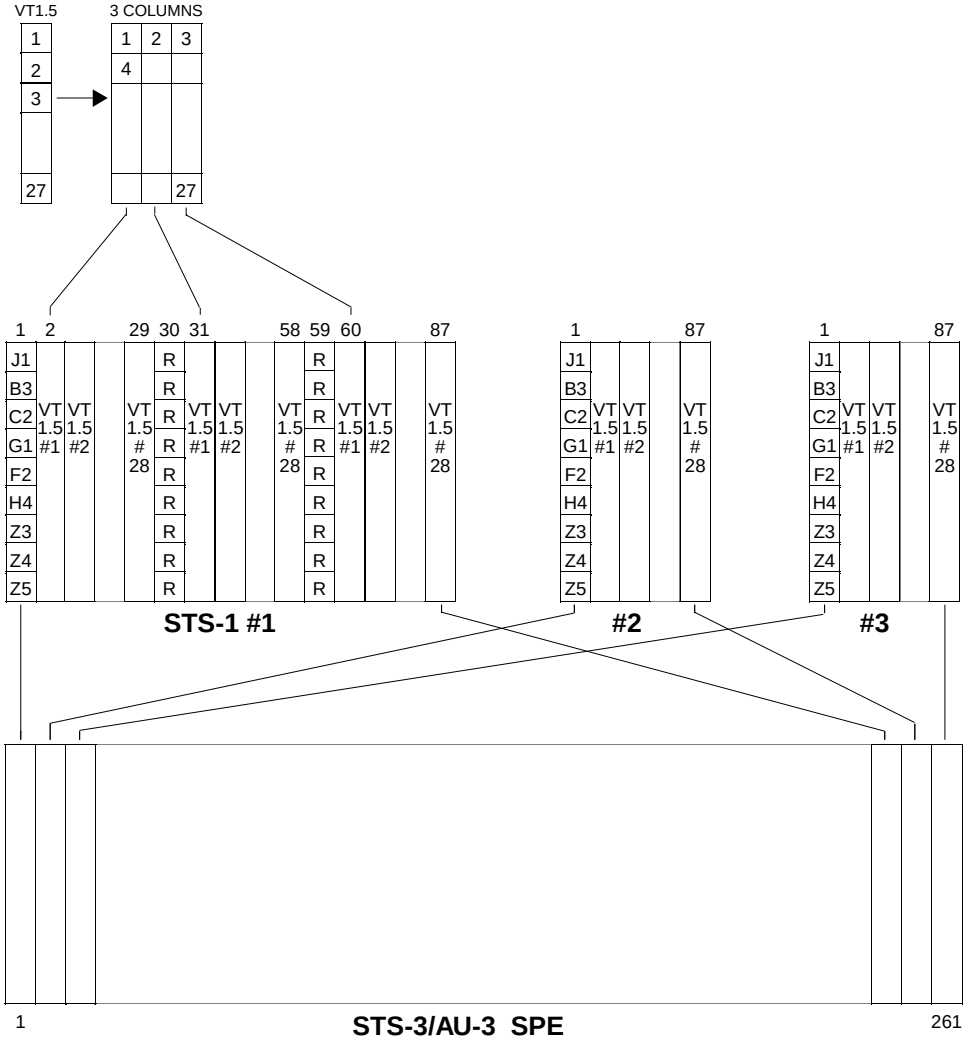


Figure 34. STS-3/AU-3 Mapping

STS-3 AU-3 Mapping

VT TU #	Registers X+04H or X+05H 6 5 4 3 2 1 0	VT/TU Column Numbers	VT TU #	Registers X+04H or X+05H 6 5 4 3 2 1 0	VT/TU Column Numbers	VT TU #	Registers X+04H or X+05H 6 5 4 3 2 1 0	VT/TU Column Numbers*
	TBTVAL or TBRVAL = 0	No TU Selected						
1	0 0 0 0 0 0 0	4 91 178	29	0 1 0 0 0 0 0	5 92 179	57	1 0 0 0 0 0 0	6 93 180
2	0 0 0 0 1 0 0	7 94 181	30	0 1 0 0 1 0 0	8 95 182	58	1 0 0 0 1 0 0	9 96 183
3	0 0 0 1 0 0 0	10 97 184	31	0 1 0 1 0 0 0	11 98 185	59	1 0 0 1 0 0 0	12 99 186
4	0 0 0 1 1 0 0	13 100 187	32	0 1 0 1 1 0 0	14 101 188	60	1 0 0 1 1 0 0	15 102 189
5	0 0 1 0 0 0 0	16 103 190	33	0 1 1 0 0 0 0	17 104 191	61	1 0 1 0 0 0 0	18 105 192
6	0 0 1 0 1 0 0	19 106 193	34	0 1 1 0 1 0 0	20 107 194	62	1 0 1 0 1 0 0	21 108 195
7	0 0 1 1 0 0 0	22 109 196	35	0 1 1 1 0 0 0	23 110 197	63	1 0 1 1 0 0 0	24 111 198
8	0 0 0 0 0 0 1	25 112 199	36	0 1 0 0 0 0 1	26 113 200	64	1 0 0 0 0 0 1	27 114 201
9	0 0 0 0 1 0 1	28 115 202	37	0 1 0 0 1 0 1	29 116 203	65	1 0 0 0 1 0 1	30 117 204
10	0 0 0 1 0 0 1	31 118 205	38	0 1 0 1 0 0 1	32 119 206	66	1 0 0 1 0 0 1	33 120 207
11	0 0 0 1 1 0 1	34 121 208	39	0 1 0 1 1 0 1	35 122 209	67	1 0 0 1 1 0 1	36 123 210
12	0 0 1 0 0 0 1	37 124 211	40	0 1 1 0 0 0 1	38 125 212	68	1 0 1 0 0 0 1	39 126 213
13	0 0 1 0 1 0 1	40 127 214	41	0 1 1 0 1 0 1	41 128 215	69	1 0 1 0 1 0 1	42 129 216
14	0 0 1 1 0 0 1	43 130 217	42	0 1 1 1 0 0 1	44 131 218	70	1 0 1 1 0 0 1	45 132 219
15	0 0 0 0 0 1 0	46 133 220	43	0 1 0 0 0 1 0	47 134 221	71	1 0 0 0 0 1 0	48 135 222
16	0 0 0 0 1 1 0	49 136 223	44	0 1 0 0 1 1 0	50 137 224	72	1 0 0 0 1 1 0	51 138 225
17	0 0 0 1 0 1 0	52 139 226	45	0 1 0 1 0 1 0	53 140 227	73	1 0 0 1 0 1 0	54 141 228
18	0 0 0 1 1 1 0	55 142 229	46	0 1 0 1 1 1 0	56 143 230	74	1 0 0 1 1 1 0	57 144 231
19	0 0 1 0 0 1 0	58 145 232	47	0 1 1 0 0 1 0	59 146 233	75	1 0 1 0 0 1 0	60 147 234
20	0 0 1 0 1 1 0	61 148 235	48	0 1 1 0 1 1 0	62 149 236	76	1 0 1 0 1 1 0	63 150 237
21	0 0 1 1 0 1 0	64 151 238	49	0 1 1 1 0 1 0	65 152 239	77	1 0 1 1 0 1 0	66 153 240
22	0 0 0 0 0 1 1	67 154 241	50	0 1 0 0 0 1 1	68 155 242	78	1 0 0 0 0 1 1	69 156 243
23	0 0 0 0 1 1 1	70 157 244	51	0 1 0 0 1 1 1	71 158 245	79	1 0 0 0 1 1 1	72 159 246
24	0 0 0 1 0 1 1	73 160 247	52	0 1 0 1 0 1 1	74 161 248	80	1 0 0 1 0 1 1	75 162 249
25	0 0 0 1 1 1 1	76 163 250	53	0 1 0 1 1 1 1	77 164 251	81	1 0 0 1 1 1 1	78 165 252
26	0 0 1 0 0 1 1	79 166 253	54	0 1 1 0 0 1 1	80 167 254	82	1 0 1 0 0 1 1	81 168 255
27	0 0 1 0 1 1 1	82 169 256	55	0 1 1 0 1 1 1	83 170 257	83	1 0 1 0 1 1 1	84 171 258
28	0 0 1 1 0 1 1	85 172 259	56	0 1 1 1 0 1 1	86 173 260	84	1 0 1 1 0 1 1	87 174 261
	STS-1 #1, AU-3 A			STS-1 #2, AU-3 B			STS-1 #3, AU-3 C	

* Note: Columns 88, 89, 90, 175, 176, 177 are fixed stuff.

TU-11 - VC-4 Multiplex Format Mapping

The following Figure 35 and table illustrate the mapping of TU-11s into a VC-4.

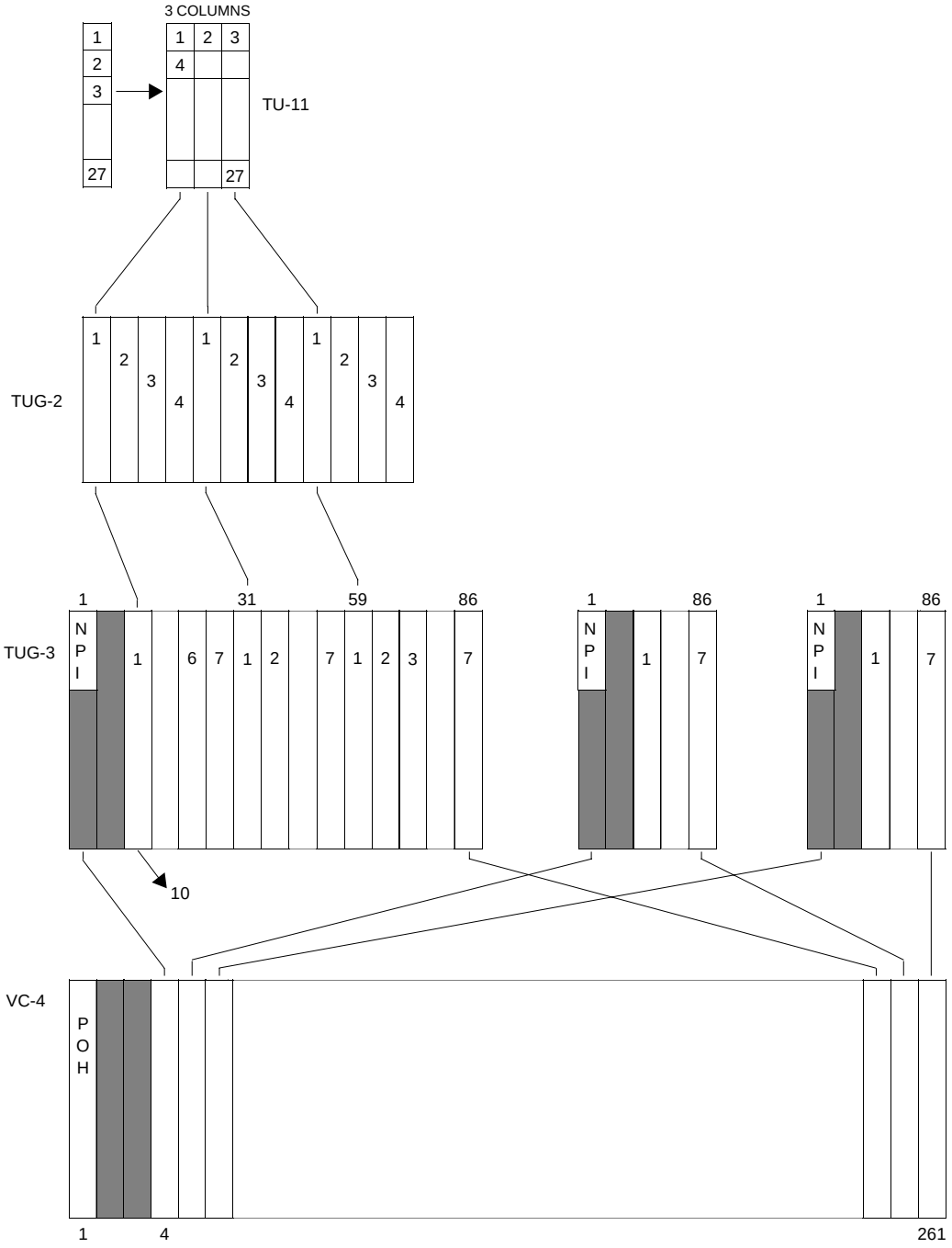


Figure 35. STM-1/VC-4 Mapping

TU-11 - VC-4 Multiplex Format Mapping

TU #	Registers X+04H or X+05H 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	Registers X+04H or X+05H 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	Registers X+04H or X+05H 6 5 4 3 2 1 0	VC-4 Column Numbers
	TBTVAL or TBRVAL = 0	No TU Selected						
1	0 0 0 0 0 0 0	10 94 178	29	0 1 0 0 0 0 0	11 95 179	57	1 0 0 0 0 0 0	12 96 180
2	0 0 0 0 1 0 0	13 97 181	30	0 1 0 0 1 0 0	14 98 182	58	1 0 0 0 1 0 0	15 99 183
3	0 0 0 1 0 0 0	16 100 184	31	0 1 0 1 0 0 0	17 101 185	59	1 0 0 1 0 0 0	18 102 186
4	0 0 0 1 1 0 0	19 103 187	32	0 1 0 1 1 0 0	20 104 188	60	1 0 0 1 1 0 0	21 105 189
5	0 0 1 0 0 0 0	22 106 190	33	0 1 1 0 0 0 0	23 107 191	61	1 0 1 0 0 0 0	24 108 192
6	0 0 1 0 1 0 0	25 109 193	34	0 1 1 0 1 0 0	26 110 194	62	1 0 1 0 1 0 0	27 111 195
7	0 0 1 1 0 0 0	28 112 196	35	0 1 1 1 0 0 0	29 113 197	63	1 0 1 1 0 0 0	30 114 198
8	0 0 0 0 0 0 1	31 115 199	36	0 1 0 0 0 0 1	32 116 200	64	1 0 0 0 0 0 1	33 117 201
9	0 0 0 0 1 0 1	34 118 202	37	0 1 0 0 1 0 1	35 119 203	65	1 0 0 0 1 0 1	36 120 204
10	0 0 0 1 0 0 1	37 121 205	38	0 1 0 1 0 0 1	38 122 206	66	1 0 0 1 0 0 1	39 123 207
11	0 0 0 1 1 0 1	40 124 208	39	0 1 0 1 1 0 1	41 125 209	67	1 0 0 1 1 0 1	42 126 210
12	0 0 1 0 0 0 1	43 127 211	40	0 1 1 0 0 0 1	44 128 212	68	1 0 1 0 0 0 1	45 129 213
13	0 0 1 0 1 0 1	46 130 214	41	0 1 1 0 1 0 1	47 131 215	69	1 0 1 0 1 0 1	48 132 216
14	0 0 1 1 0 0 1	49 133 217	42	0 1 1 1 0 0 1	50 134 218	70	1 0 1 1 0 0 1	51 135 219
15	0 0 0 0 0 1 0	52 136 220	43	0 1 0 0 0 1 0	53 137 221	71	1 0 0 0 0 1 0	54 138 222
16	0 0 0 0 1 1 0	55 139 223	44	0 1 0 0 1 1 0	56 140 224	72	1 0 0 0 1 1 0	57 141 225
17	0 0 0 1 0 1 0	58 142 226	45	0 1 0 1 0 1 0	59 143 227	73	1 0 0 1 0 1 0	60 144 228
18	0 0 0 1 1 1 0	61 145 229	46	0 1 0 1 1 1 0	62 146 230	74	1 0 0 1 1 1 0	63 147 231
19	0 0 1 0 0 1 0	64 148 232	47	0 1 1 0 0 1 0	65 149 233	75	1 0 1 0 0 1 0	66 150 234
20	0 0 1 0 1 1 0	67 151 235	48	0 1 1 0 1 1 0	68 152 236	76	1 0 1 0 1 1 0	69 153 237
21	0 0 1 1 0 1 0	70 154 238	49	0 1 1 1 0 1 0	71 155 239	77	1 0 1 1 0 1 0	72 156 240
22	0 0 0 0 0 1 1	73 157 241	50	0 1 0 0 0 1 1	74 158 242	78	1 0 0 0 0 1 1	75 159 243
23	0 0 0 0 1 1 1	76 160 244	51	0 1 0 0 1 1 1	77 161 245	79	1 0 0 0 1 1 1	78 162 246
24	0 0 0 1 0 1 1	79 163 247	52	0 1 0 1 0 1 1	80 164 248	80	1 0 0 1 0 1 1	81 165 249
25	0 0 0 1 1 1 1	82 166 250	53	0 1 0 1 1 1 1	83 167 251	81	1 0 0 1 1 1 1	84 168 252
26	0 0 1 0 0 1 1	85 169 253	54	0 1 1 0 0 1 1	86 170 254	82	1 0 1 0 0 1 1	87 171 255
27	0 0 1 0 1 1 1	89 172 256	55	0 1 1 0 1 1 1	89 173 257	83	1 0 1 0 1 1 1	90 174 258
28	0 0 1 1 0 1 1	91 175 259	56	0 1 1 1 0 1 1	92 176 260	84	1 0 1 1 0 1 1	93 177 261
	TUG-3 A			TUG-3 B			TUG-3 C	

AUXILIARY PORT

The Auxiliary Port is used to access the J2, Z6/N2, Z7/K4 bytes, and the O-bit information, contained in the VT1.5 Overhead. The Auxiliary Port consists of ten pins. The five output port pins are Output Port Clock (OAPCKO), Output Port Address Valid (OAPAVO), Output Port Address (OAPADO), Output Port Data Valid (OAPDVO), and Output Port Data (OAPDTO), all of which are output signals. The five input port pins are Input Port Clock (IAPCKO, an output), Input Port Address Valid (IAPAVO, an output), Input Port Address (IAPADO, an output), Input Port Data Valid (IAPDVO, an output), Input Port Data (IAPDTI, an input).

Figure 36 shows the Auxiliary Port operation. All signals are outputs except for IAPDTI, as noted above. Input and output operations are identical. (O/I)APCKO are continuous. An Input or Output Transfer Cycle requires 21 clock times. The cycle begins with (O/I)APAVO transitioning High. Input and Output Transfer Cycles are asynchronous to each other. As indicated by the dotted lines, Transfer Cycles may overlap, i.e., Address information can be output while data is being output or input. The minimum time between Transfer Cycles is one clock time. OAPCKO and IAPCKO are 'divide by 2' derivatives of DCLK and ACLK, respectively. Data bytes are formatted with MSB first.

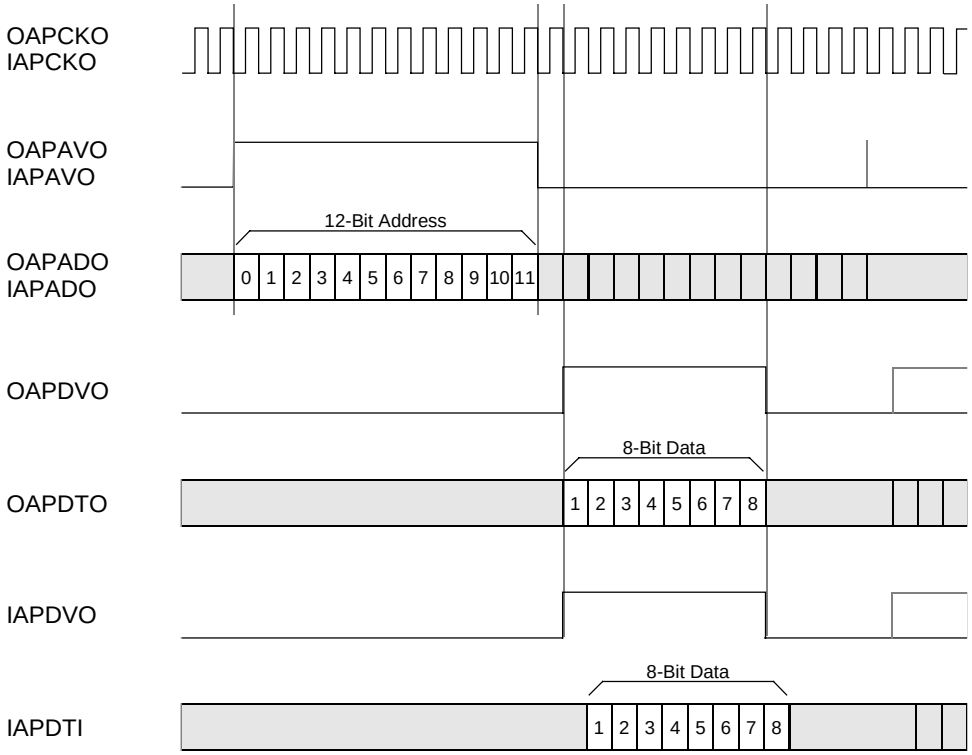


Figure 36. Auxiliary Port Operation

Input and output accesses require that Telecom Bus slots have been assigned to a specific channel; TBTVAL (bit 7) in control register X+05H and TBRVAL (bit 7) in control register X+04H are set to 1, and that the appropriate control bits in register X+0BH for the overhead bytes are enabled.

The 12-bit address identifies the information that will be output or input during the Transfer Cycle. Figure 37 details the address fields. The O-bits are output or input eight bits at a time (per VT Super frame basis) where:

1. the first four O-bits (Byte following J2, Bits 3, 4, 5 and 6) are placed in Bits 3, 2, 1 and 0
2. the second four O-bits (Byte following Z6/N2, Bits 3, 4, 5 and 6) are placed in Bits 7, 6, 5 and 4

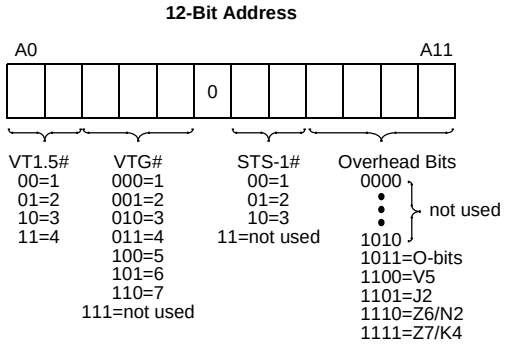


Figure 37. Auxiliary Port Address Designation

The remaining bytes are mapped to the Auxiliary Port on a bit-for-bit basis.

All five indicated bytes are output from information input on DD(0-7). In addition, the O-bits, J2, Z6/N2, and Z7/K4 information will be written in the Per Channel Memory Map, for access by the microprocessor. Register X+32H stores the received O-bits, X+33H is used to store the last received J2 byte, X+34H is used to store the last received Z6/N2 byte and X+35H is used to store the last received Z7/K4 byte.

The Input Port will accept the O-bits, J2, Z6/N2, and Z7/K4 Bytes. The V5 Byte will not be requested. Four Per Channel Memory Locations will be used for storage of outgoing O-bit, J2, Z6/N2 and Z7/K4 information. These locations will be available to the microprocessor to read the data collected by the Auxiliary Port. If an overhead byte is not to be input to the Auxiliary Port, these same memory locations can be used by the microprocessor to write a desired value which will be transmitted in the overhead byte location. Control bit OBAPEN (bit 3) in register X+0BH, when set to a 0, enables the O-bits for mapper channel n to be accessed from register X+36H and input to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11; when OBAPEN is set to a 1, the O-bits for mapper channel n are requested at the Auxiliary Port input, written to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11, and also stored in register X+36H. Control bit J2APEN (bit 2) in register X+0BH, when set to a 0, enables the J2 byte for mapper channel n to be accessed from register X+37H and input to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11; when J2APEN is set to a 1, the J2 byte for mapper channel n is requested at the Auxiliary Port input, written to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11, and also stored in register X+37H. Control bit Z6APEN (bit 1) in register X+0BH, when set to a 0, enables the Z6/N2 byte for mapper channel n to be accessed from register X+38H and input to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11; when Z6APEN is set to a 1, the Z6/N2 byte for mapper channel n is requested at the Auxiliary Port input, written to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11, and also stored in register X+38H. Control bit Z7APEN (bit 0) in register X+0BH, when set to a 0, enables the Z7/K4 byte for mapper channel n to be accessed from register X+39H and input to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11; when Z7APEN is set to a 1, the Z7/K4 byte for mapper channel n is requested at the Auxiliary Port input, written to the correct position per Figure 2 for inclusion in the VT1.5/ TU-11, and also stored in register X+39H. It should be noted that bits 3, 2 and 1 of Z7/K4 are used for 3-bit RDI and will be overwritten with the appropriate values prior to transmission to the Telecom Bus.

RING PORT

The Ring Port is used in USHR/P Ring applications to communicate REI (FEBE) and RDI Information between mated DS1MX7s. The Ring Port consists of six pins, three outputs and three inputs. The output port pins are Output Port Clock (ORPCKO), Output Port Frame (ORPFMO), Output Port Data (ORPDTO) and the input port pins are Input Port Clock (IRPCKI), Input Port Frame (IRPFMI), Input Port Data (IRPDTI).

Figure 38 shows the ring port operation and Figure 42 shows an application. The information consists of seven eight-bit fields, one for each channel. The first four bits are REI-V (FEBE), RDI-VPD, RDI-VSD, and RDI-VCD. The last four bits are not used. The information is accumulated for all seven channels and sent as a burst of 56 bits. The ORPCKO is a 'divide by ten' derivative of DCLK. Ring operation is enabled with the control bit RI N-GEN (bit 4) in register X+0BH. When set to zero, normal operations are performed. When set to one, Ring Mode is enabled. The information incoming on IRPDTI is stored in register X+3AH, Bits 3-0 for access by the microprocessor. The designation for these bits is RGFEBE-V (bit 3), RGRDI-VPD (bit 2), RGRDI-VSD (bit 1), and RGRDI-VCD (bit 0). The four remaining bits will be designated "Unused".

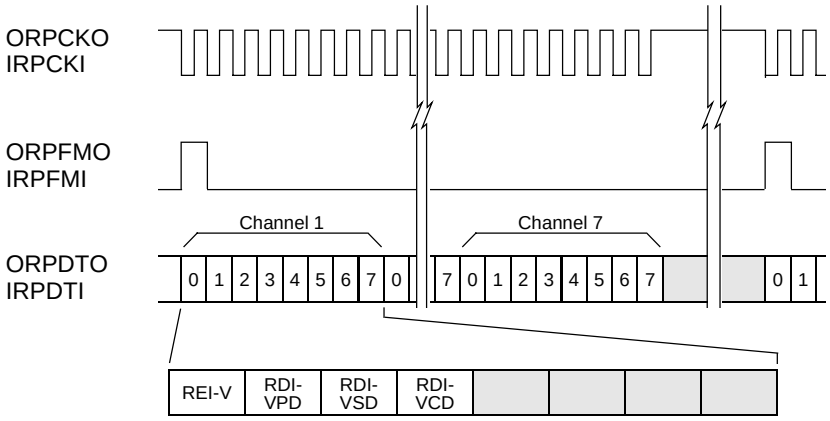


Figure 38. Ring Port Operation

TEST ACCESS PORT

Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and test data registers, and a boundary scan register path bordering the input and output pins, as illustrated in Figure 39. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{TRS}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a three-bit serial instruction register and two or more serial test data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and test data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device pins to pass to and from the DS1MX7 device's internal logic, as illustrated in Figure 39. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 18.

Boundary Scan Support

The maximum frequency the DS1MX7 device will support for boundary scan is 10 MHz. The DS1MX7 device performs the following boundary scan test instructions:

- EXTEST (000)
- SAMPLE/PRELOAD (010)
- BYPASS (111)

It should be noted that the Capture - IR State (INSTRUCTION_CAPTURE attribute of BSDL) is 011.

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the DS1MX7 device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external DS1MX7 input and output leads.

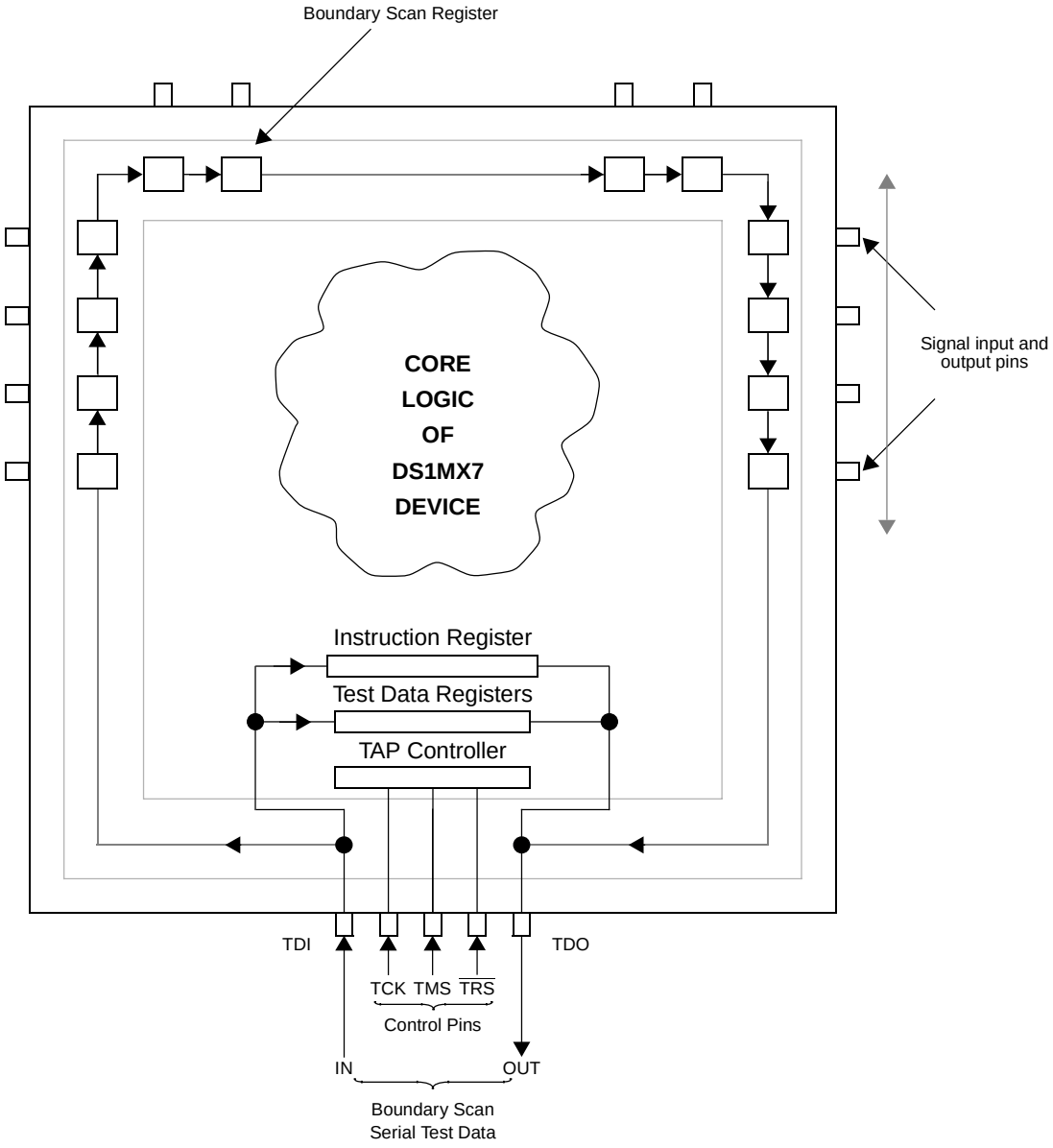
SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the DS1MX7 device remains fully operational. While in this test mode, DS1MX7 input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the DS1MX7 device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

Figure 39. Boundary Scan Schematic



Note: Pin locations are shown for illustration only, and do not correspond to the physical device pins.

Boundary Scan Chain

There are 200 boundary scan register cells in the boundary scan chain. Scan cell number 0 is defined as the cell nearest the TDO pin and is therefore the first to be shifted out. The last scan cell to be shifted out is number 199. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their functions.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
199	INPUT	196	IRPDTI	
198	INPUT	195	IRPFMI	
197	INPUT	194	IRPCKI	
196	OUTPUT	193	ORPDTO	
195	OUTPUT	192	ORPFMO	
194	OUTPUT	190	ORPCKO	
193	OUTPUT	189	$\overline{\text{LCS7}}$	
192	OUTPUT	188	TSYNC7	
191	OUTPUT	187	LTCLK7	
190	OUTPUT	186	TNEG7	
189	OUTPUT	184	TPOS7	
188	CONTROL	NA	DEN_7	A one makes pins 182 and 183 outputs.
187	BIDIR_IN	183	RSYNC7	
186	BIDIR_OUT	183	RSYNC7	
185	BIDIR_IN	182	LRCLK7	
184	BIDIR_OUT	182	LRCLK7	
183	CONTROL	NA	RNEG7_EN	A one makes pin 180 an output.
182	BIDIR_IN	180	RNEG7	
181	BIDIR_OUT	180	RNEG7	
180	INPUT	178	RPOS7	
179	INPUT	177	LAIS7	
178	OUTPUT	176	$\overline{\text{LCS6}}$	
177	OUTPUT	175	TSYNC6	
176	OUTPUT	174	LTCLK6	
175	OUTPUT	172	TNEG6	
174	OUTPUT	171	TPOS6	
173	CONTROL	NA	DEN_6	A one makes pins 168 and 170 outputs.
172	BIDIR_IN	170	RSYNC6	
171	BIDIR_OUT	170	RSYNC6	
170	BIDIR_IN	168	LRCLK6	
169	BIDIR_OUT	168	LRCLK6	
168	CONTROL	NA	RNEG6_EN	A one makes pin 166 an output.

Scan Cell No.	I/O	Pin No.	Symbol	Comments
167	BIDIR_IN	166	RNEG6	
166	BIDIR_OUT	166	RNEG6	
165	INPUT	165	RPOS6	
164	INPUT	164	LAIS6	
163	OUTPUT	163	$\overline{\text{LCS5}}$	
162	OUTPUT	162	TSYNC5	
161	OUTPUT	160	LTCLK5	
160	OUTPUT	159	TNEG5	
159	OUTPUT	158	TPOS5	
158	CONTROL	NA	DEN_5	A one makes pins 156 and 157 outputs.
157	BIDIR_IN	157	RSYNC5	
156	BIDIR_OUT	157	RSYNC5	
155	BIDIR_IN	156	LRCLK5	
154	BIDIR_OUT	156	LRCLK5	
153	CONTROL	NA	RNEG5_EN	A one makes pin 155 an output.
152	BIDIR_IN	155	RNEG5	
151	BIDIR_OUT	155	RNEG5	
150	INPUT	154	RPOS5	
149	INPUT	152	LAIS5	
148	OUTPUT	150	$\overline{\text{LCS4}}$	
147	OUTPUT	149	TSYNC4	
146	OUTPUT	148	LTCLK4	
145	OUTPUT	147	TNEG4	
144	OUTPUT	146	TPOS4	
143	CONTROL	NA	DEN_4	A one makes pins 143 and 144 outputs.
142	BIDIR_IN	144	RSYNC4	
141	BIDIR_OUT	144	RSYNC4	
140	BIDIR_IN	143	LRCLK4	
139	BIDIR_OUT	143	LRCLK4	
138	CONTROL	NA	RNEG4_OUT	A one makes pin 142 an output.
137	BIDIR_IN	142	RNEG4	
136	BIDIR_OUT	142	RNEG4	
135	INPUT	140	RPOS4	
134	INPUT	138	LAIS4	
133	OUTPUT	137	$\overline{\text{LCS3}}$	
132	OUTPUT	136	TSYNC3	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
131	OUTPUT	135	LTCLK3	
130	OUTPUT	134	TNEG3	
129	OUTPUT	132	TPOS3	
128	CONTROL	NA	DEN_3	A one makes pins 130 and 131 outputs.
127	BIDIR_IN	131	RSYNC3	
126	BIDIR_OUT	131	RSYNC3	
125	BIDIR_IN	130	LRCLK3	
124	BIDIR_OUT	130	LRCLK3	
123	CONTROL	NA	RNEG3_EN	A one makes pin 128 an output.
122	BIDIR_IN	128	RNEG3	
121	BIDIR_OUT	128	RNEG3	
120	INPUT	126	RPOS3	
119	INPUT	125	LAIS3	
118	OUTPUT	124	$\overline{\text{LCS2}}$	
117	OUTPUT	123	TSYNC2	
116	OUTPUT	122	LTCLK2	
115	OUTPUT	120	TNEG2	
114	OUTPUT	119	TPOS2	
113	CONTROL	NA	DEN_2	A one makes pins 116 and 118 outputs.
112	BIDIR_OUT	118	RSYNC2	
111	BIDIR_IN	118	RSYNC2	
110	BIDIR_OUT	116	LRCLK2	
109	BIDIR_IN	116	LRCLK2	
108	CONTROL	NA	RNEG2_EN	A one makes pin 114 an output.
107	BIDIR_IN	114	RNEG2	
106	BIDIR_OUT	114	RNEG2	
105	INPUT	113	RPOS2	
104	INPUT	112	LAIS2	
103	OUTPUT	111	$\overline{\text{LCS1}}$	
102	OUTPUT	110	TSYNC1	
101	OUTPUT	108	LTCLK1	
100	OUTPUT	107	TNEG1	
99	OUTPUT	106	TPOS1	
98	CONTROL	NA	DEN_1	A one makes pins 104 and 105 outputs.
97	BIDIR_IN	105	RSYNC1	
96	BIDIR_OUT	105	RSYNC1	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
95	BIDIR_IN	104	LRCLK1	
94	BIDIR_OUT	104	LRCLK1	
93	CONTROL	NA	RNEG1_EN	A one makes pin 103 an output.
92	BIDIR_IN	103	RNEG1	
91	BIDIR_OUT	103	RNEG1	
90	INPUT	102	RPOS1	
89	INPUT	100	LAIS1	
88	INPUT	98	LO	
87	INPUT	97	$\overline{\text{MASTER}}$	
86	INPUT	96	DATEN	
85	INPUT	95	CONFIGI	
84	OUTPUT	94	LSCLK	
83	INPUT	92	LSDI	
82	OUTPUT	91	LSDO	
81	INPUT	90	$\overline{\text{BUSCHK2}}$	
80	INPUT	89	$\overline{\text{BUSCHK1}}$	
79	INPUT	88	$\overline{\text{BUSCHK0}}$	
78	CONTROL	NA	DATA_EN_DRIVE	A one enables OUTPUT1.
77	OUTPUT1	86	AD0	
76	OUTPUT1	85	AD1	
75	OUTPUT1	84	AD2	
74	OUTPUT1	83	AD3	
73	OUTPUT1	82	AD4	
72	OUTPUT1	80	AD5	
71	OUTPUT1	79	AD6	
70	OUTPUT1	78	AD7	
69	INPUT	76	ACLK	
68	OUTPUT1	74	$\overline{\text{AADD}}$	
67	INPUT	72	AC1J1V1	
66	INPUT	71	ASPE	
65	OUTPUT1	70	APAR	
64	INPUT	68	DFAIL	
63	INPUT	67	DSPE	
62	INPUT	66	DC1J1V1	
61	INPUT	64	DCLK	
60	INPUT	62	DPAR	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
59	INPUT	61	DD0	
58	INPUT	60	DD1	
57	INPUT	59	DD2	
56	INPUT	58	DD3	
55	INPUT	56	DD4	
54	INPUT	55	DD5	
53	INPUT	54	DD6	
52	INPUT	53	DD7	
51	OUTPUT	52	OAPDVO	
50	OUTPUT	51	OAPDTO	
49	OUTPUT	50	OAPAVO	
48	OUTPUT	49	IAPCKO	
47	OUTPUT	48	OAPADO	
46	OUTPUT	46	IAPDVO	
45	INPUT	45	IAPDTI	
44	OUTPUT	44	IAPAVO	
43	OUTPUT	43	IAPADO	
42	OUTPUT	42	OAPCKO	
41	OUTPUT	40	PCKI	
40	INPUT	39	$\overline{\text{WRI}}$	
39	INPUT	38	MOTOI	
38	INPUT	36	$\overline{\text{SELI}}$	
37	INPUT	34	$\overline{\text{READI}}$/ READI/$\overline{\text{WRI}}$	
36	OUTPUT	32	INTO	
35	CONTROL	NA	RDY_EN	A one enables pin 31; a zero tri-states pin 31.
34	OUTPUT2	31	RDYO	
33	CONTROL	NA	DATA_EN	A one makes pins 19 through 30 outputs.
32	BIDIR_IN	30	DTB7	
31	BIDIR_OUT	30	DTB7	
30	BDIR_IN	28	DTB6	
29	BIDIR_OUT	28	DTB6	
28	BIDIR_IN	26	DTB5	
27	BIDIR_OUT	26	DTB5	
26	BDIR_IN	24	DTB4	
25	BIDIR_OUT	24	DTB4	
24	BIDIR_IN	22	DTB3	

Scan Cell No.	I/O	Pin No.	Symbol	Comments
23	BIDIR_OUT	22	DTB3	
22	BDIR_IN	21	DTB2	
21	BIDIR_OUT	21	DTB2	
20	BIDIR_IN	20	DTB1	
19	BIDIR_OUT	20	DTB1	
18	BDIR_IN	19	DTB0	
17	BIDIR_OUT	19	DTB0	
16	INPUT	18	ADDR8	
15	INPUT	16	ADDR7	
14	INPUT	15	ADDR6	
13	INPUT	14	ADDR5	
12	INPUT	12	ADDR4	
11	INPUT	10	ADDR3	
10	INPUT	9	ADDR2	
9	INPUT	8	ADDR1	
8	INPUT	7	ADDR0	
7	INPUT	6	$\overline{\text{CSO}}$	
6	INPUT	4	$\overline{\text{RSTI}}$	
5	INPUT	3	$\overline{\text{HIGHZ}}$	
4	INPUT	2	TSTB	
3	INPUT	1	TSTA	
2	OUTPUT	208	$\overline{\text{IAO}}$	
1	INPUT	207	T1SI	
0	INPUT	206	SRCLK	

MEMORY MAP

Hex Address Range	Channel	Functions
000 - 03F	Common	Component ID. Serial Port Control, Global Control, Device Controls and Interrupt Control
040 - 07F	#1	Status, Control, PM/FM and Error Counters
080 - 0BF	#2	Status, Control, PM/FM and Error Counters
0C0 - 0FF	#3	Status, Control, PM/FM and Error Counters
100 - 13F	#4	Status, Control, PM/FM and Error Counters
140 - 17F	#5	Status, Control, PM/FM and Error Counters
180 - 1BF	#6	Status, Control, PM/FM and Error Counters
1C0 - 1FF	#7	Status, Control, PM/FM and Error Counters

COMMON MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	MI7=1	MI6=1	MI5=0	MI4=1	MI3=0	MI2=1	MI1=1	MI0=1
001	R	PN3=1	PN2=0	PN1=0	PN0=1	MI11=0	MI10=0	MI9=0	MI8=0
002	R	PN11=0	PN10=0	PN9=0	PN8=0	PN7=0	PN6=1	PN5=1	PN4=0
003	R	V3=0	V2=0	V1=1	V0=0	PN15=0	PN14=0	PN13=0	PN12=1
004	R/W	Notebook							
005	R/W	Reset							
006	R/W	GIM	RISE	FALL	IPOL	ENPMFM	ENHWM	R	R
007	R/W	TCAE	RCAE	SDH	RXNRZP	TBPIS	TBPE	VC3VC4	TXNRZP
008	R/W	MTBRCF	MTBRSF	MTBRPF	R	MMCKF	MTBTCF	MTBTSF	MTBTPF
009	R/W	R	R	R	R	MTBRPY	MPRBSE	MTBIE	MTBXE
00A	R	TBRCKS	TBRSNS	TBRPAS	R	MCKS	TBTCKS	TBTSNS	TBTPAS
00B	R	R	R	R	R	TBRPYS	PRBSS	TBIES	TBXES
00C	R/W=clr	TBRCKE	TBRSNE	TBRPAE	R	MCKE	TBTCKE	TBTSNE	TBTPAE
00D	R/W=clr	R	R	R	R	TBRPYE	PRBSE	TBIEE	TBXEE
00E	R/W=clr	TBRCKPM	TBRSNPM	TBRPAPM	R	MCKPM	TBTCKPM	TBTSNPM	TBTPAPM
00F	R/W=clr	R	R	R	R	TBRPYPM	PRBSPM	TBIEPM	TBXEPM
010	-	SPARE							
011	R	R	CH7	CH6	CH5	CH4	CH3	CH2	CH1
012	-	SPARE							

Notes:
*R/W: Read/write; R: Read-only; W: Write-only; R/W=clr: Read/write zero bits only (one bits ignored during write).
Bits shown as 'R' and bytes shown as 'Reserved' must be set to 0/00H for proper device operation, where write capability is provided.
SPARE registers must not be accessed by the microprocessor.

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
013	R	GXPE	GDMPE	GLOSE	GMPE	GDAISE	GRPOE	GPGOE	GCVOE
014	R	GFEOE	GBIPOE	GVAISE	GLOPE	GRFIE	GUNEE	GSLME	GRDIE
015	R/W	GXPM	GDMPM	GLOSM	GMPM	GDAISM	GRPOM	GPGOM	GCVOM
016	R/W	GFEOM	GBIPOM	GVAISM	GLOPM	GRFIM	GUNEM	GSLMM	GRDIM
017	R/W	D7	D6	D5	D4	D3	D2	D1	D0
018	R/W	D7	D6	D5	D4	D3	D2	D1	D0
019	R	D7	D6	D5	D4	D3	D2	D1	D0
01A	R/W	BDCST	R	EPRBSA	ENSRP	R	DS1 Channel number (0-6)		
01B	R/W	ETBRCF	ETBRSF	ETBRPF	R	EMCKF	ETBTCF	ETBTSF	ETBTPF
01C	R/W	R	R	R	R	ETBRPY	EPRBSE	ETBIE	ETBXE
01D	R/W	ECTL7	ECTL6	ECTL5	ECTL4	ECTL3	ECTL2	ECTL1	ECTL0
01E	R/W	TBLPBK	FTBTPE	TBTCI	TBRCI	TBDD	R	R	RDID10
01F - 03B	-	SPARE							
03C	R/W	DPLLLK	DPLL6	DPLL5	DPLL4	DPLL3	DPLL2	DPLL1	DPLL0
03D	R/W	R	R	R	BYPLB	PRBSCK	TMDIS	C2PH1	C2PH0
03E	R/W=clr	TBRCKFM	TBRSNFM	TBRPAFM	R	MCKFM	TBTCKFM	TBTSNFM	TBTPAFM
03F	R/W=clr	R	R	R	R	TBRPYFM	PRBSFM	TBIEFM	TBXEFM

PER CHANNEL MEMORY MAP

NOTE: In the address, X= 040H for DS1 channel 1; 080H for DS1 channel 2; 0C0H for DS1 channel 3; 100H for DS1 channel 4; 140H for DS1 channel 5; 180H for DS1 channel 6; 1C0H for DS1 channel 7.

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+00	R/W	IDLE	EXPLOS	DATACOM	ENZC	LCODE	ENCOD	MODE1	MODE0
X+01	R/W	SH2VAIS	LOS2AIS	LOF2VAIS	CRC6	VAIS2AIS	RFI2YEL	YEL2RFI	AIS2VAIS
X+02	R/W	SRDI-VPD	SRDI-VSD	SRDI-VCD	R	RDIIS	SLM2AIS	FEBEIS	UNE2AIS
X+03	R/W	SFEBE	SDAISS	SBIPE	R	SDAISL	SYELL	SRFI	SVTAIS
X+04	R/W	TBRVAL	Tel Bus RX STS-1 number (1-3)		Tel Bus RX VT Group or TUG number (1-7)			Tel Bus RX VT or TU number (1-4)	
X+05	R/W	TBTVAL	Tel Bus TX STS-1 number (1-3)		Tel Bus TX VT Group or TUG number (1-7)			Tel Bus TX VT or TU number (1-4)	
X+06	R/W	PL8	PL7	PL6	PL5	PL4	PL3	PL2	PL1
X+07	R/W	R	Expected Signal Label (2-0)			R	Transmit Signal Label (2-0)		
X+08	R/W	XPM	DMPM	LOSM	MPM	DAISM	RPOM	PGOM	CVOM
X+09	R/W	FEOM	BIPOM	VAISM	LOPM	RFIM	UNEM	SLMM	RDIM
X+0A	R/W	R	R	R	R	R	RDI-VPDM	RDI-VSDM	RDI-VCDM

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+0B	R/W	R	R	R	RINGEN	OBAPEN	J2APEN	Z6APEN	Z7APEN
X+0C	R/W	DTLPBK	DFLPBK	RSTCH	SPRBS	R	R	R	R
X+0D - X+0F	-	Reserved							
X+10	R	XPS	DMPS	LOSS	MPS	DAISS	RPOS	PGOS	CVOS
X+11	R	FEOS	BIPOS	VAISS	LOPS	RFIS	UNES	SLMS	RDI-VS
X+12	R	R	R	R	R	R	RDI-VPDS	RDI-VSDS	RDI-VCDS
X+13	-	SPARE							
X+14	R/W=clr	XPE	DMPE	LOSE	MPE	DAISE	RPOE	PGOE	CVOE
X+15	R/W=clr	FEOE	BIPOE	VAISE	LOPE	RFIE	UNEE	SLME	RDI-VE
X+16	R/W=clr	R	R	R	R	R	RDI-VPDE	RDI-VSDE	RDI-VCDE
X+17	-	SPARE							
X+18	R	XPPM	DMPPM	LOSPM	MPPM	DAISPM	RPOPM	PGOPM	CVOPM
X+19	R	FEOPM	BIPOPM	VAISPM	LOPPM	RFIPM	UNEPM	SLMPM	RDI-VPM
X+1A	R	R	R	R	R	R	RDI-VPDPM	RDI-VSDPM	RDI-VCDPM
X+1B	-	SPARE							
X+1C	R	XPFM	DMPFM	LOSFM	MPFM	DAISFM	RPOFM	PGOFM	CVOFM
X+1D	R	FEOFM	BIPOFM	VAISFM	LOPFM	RFIFM	UNEFM	SLMFM	RDI-VFM
X+1E	R	R	R	R	R	R	RDI-VPDFM	RDI-VSDFM	RDI-VCDFM
X+1F	-	SPARE							
X+20	R	SHDAIS	SHYEL	R	RXSS1	RXSS0	Received Signal Label (2-0)		
X+21	-	SPARE							
X+22	R/W=clr	CVC7	CVC6	CVC5	CVC4	CVC3	CVC2	CVC1	CVC0
X+23	R/W=clr	R	R	R	R	CVC11	CVC10	CVC9	CVC8
X+24	R/W=clr	Count of pointer increments received				Count of pointer decrements received			
X+25	R/W=clr	Count of pointer increments generated				Count of pointer decrements generated			
X+26	R/W=clr	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
X+27	R/W=clr	R	R	R	R	BEC11	BEC10	BEC9	BEC8
X+28	R/W=clr	FEC7	FEC6	FEC5	FEC4	FEC3	FEC2	FEC1	FEC0
X+29	R/W=clr	R	R	R	R	FEC11	FEC10	FEC9	FEC8
X+2A	R/W	LCVC7	LCVC6	LCVC5	LCVC4	LCVC3	LCVC2	LCVC1	LCVC0
X+2B	R/W	R	R	R	R	LCVC11	LCVC10	LCVC9	LCVC8
X+2C	R/W	Latched count of pointer increments received				Latched count of pointer decrements received			
X+2D	R/W	Latched count of pointer increments generated				Latched count of pointer decrements generated			
X+2E	R/W	LBEC7	LBEC6	LBEC5	LBEC4	LBEC3	LBEC2	LBEC1	LBEC0

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+2F	R/W	R	R	R	R	LBEC11	LBEC10	LBEC9	LBEC8
X+30	R/W	LFEC7	LFEC6	LFEC5	LFEC4	LFEC3	LFEC2	LFCE1	LFEC0
X+31	R/W	R	R	R	R	LFEC11	LFEC10	LFEC9	LFEC8
X+32	R	Rx O-bits							
X+33	R	Rx J2							
X+34	R	Rx Z6/N2							
X+35	R	Rx Z7/K4							
X+36	R/W	Tx O-bits							
X+37	R/W	Tx J2							
X+38	R/W	Tx Z6/N2							
X+39	R/W	Tx Z7/K4							
X+3A	R	R	R	R	R	RGFEBE-V	RGRDI-VPD	RGRDI-VSD	RGRDI-VCD
X+3B - X+3F		Reserved							

MEMORY MAP DESCRIPTIONS

COMMON MEMORY MAP

Component ID

Address	Bit	Symbol	Description
000	7-0	MI7-MI0	**Manufacturer Identity:** Read-only register containing the seven least significant bits of the component manufacturer's identity (107 decimal) followed by a 1 in bit 0 (D7 Hex).
001	7-4	PN3-PN0	**Part Number:** Read-only register containing the four least significant bits of the component part number (9 Hex).
	3-0	MI11-MI8	**Manufacturer Identity:** Read-only register containing the four most significant bits of the component manufacturer's identity (0 Hex).
002	7-0	PN11-PN4	**Part Number:** Read-only register containing the middle eight bits of the component part number (06 Hex).
003	7-4	V3-V0	**Version:** Read-only register containing the component version number (2 Hex).
	3-0	PN15-PN12	**Part Number:** Read-only register containing the four most significant bits of the component part number (1 Hex).
004	7-0	Notebook	**User Register:** Read/write register for end-user application. The content of this register will have no effect on the operation of the device.
005	7-0	Reset	**Software Reset:** Writing a 91 Hex into this location will generate a software reset to the component (all but configuration registers are reset). Writing other than 91 Hex will remove the DS1MX7 from the reset state. Reading this location will return a 00 Hex if the DS1MX7 is not in reset and 01 Hex if the DS1MX7 is in reset. The DS1MX7 will default to reset on application of external hardware reset ($\overline{\text{RSTI}}$).

Global Registers

Address	Bit	Symbol	Description
006	7	GIM	**Global Interrupt Mask:** When cleared (this bit set to zero), the external interrupt output (INTO/$\overline{\text{IRQO}}$, pin 32) will be asserted when an internal interrupt event occurs. The internal interrupt status may still be polled by software to detect interrupt events when this bit is set to one.
	6	RISE	**Rising Edge Interrupt:** When set to one, a status change will be registered as a one in the latched value bits on the start of an event.
	5	FALL	**Falling Edge Interrupt:** When set to one, a status change will be registered as a one in the latched value bits on the end of an event.
	4	IPOL	**Interrupt Polarity:** When set to one, the polarity of the interrupt pin will be inverted at the pin.

Address	Bit	Symbol	Description
006 (cont.)	3	ENPMFM	**Enable PM/FM function:** When set to one, the Performance and Fault Monitoring function is in the PM/FM registers (00E/F, 03E/F, X+18H to X+1EH) and the latched counters (X+2AH to X+31H); latching takes place after T1SI rising edge. Both RISE and FALL must be set to one.
	2	ENHWM	**Enable Hardware Mask:** When set to one, global errors (e.g., DCLK fails; TBRCKS = 1) may be used to generate an active low internal alarm output on pin $\overline{IAO}$, if enabled (e.g., control bit ETBRCF = 1). When set to zero, pin $\overline{IAO}$ will remain high.
	1-0	R	**Reserved:** These bits must be set to zero.
007	7	TCAE	**Tributary Transmit Clock Active Edge:** If this bit is set to one, the TPOSn, TNEGn/TSIGLn and TSYNCn signals are clocked out of the DS1MX7 on the rising edge of LTCLKn. When set to zero, they are clocked out on the falling edge of LTCLKn.
	6	RCAE	**Tributary Receive Clock Active Edge:** If this bit is set to one, the RPOSn, RNEGn/RSIGLn/RCVn and RSYNCn signals are clocked into or out of the DS1MX7 on the rising edge of LRCLKn. When set to zero, they are clocked in or out on the falling edge of LRCLKn.
	5	SDH	**SDH functions:** When this bit is set to one, the pointer tracking state machine will transition from the AIS state to the LOP state on receipt of eight Invalid pointers and a block count of BIP-2 errors will be recorded by the BIP-2 error counter. This is used in SDH applications. When set to zero, the pointer tracking state machine will not include the AIS state to the LOP state transition and the actual number of BIP-2 errors will be recorded by the BIP-2 error counter. This setting is used in SONET applications.
	4	RXNRZP	**Receive NRZ Polarity:** When set to one, the polarity of the data received at RPOSn and LAISn will be inverted at these pins; a low will be interpreted as a logic one.
	3	TBPIS	**Telecom Bus Parity Includes Sync.:** When set to one, the signals AC1J1V1 and ASPE are included with AD(0-7) in the parity calculation for APAR. When set to zero, APAR includes parity calculated for AD(0-7) only.
	2	TBPE	**Telecom Bus Parity Even/Odd:** When set to one, even parity is calculated for APAR and checked for DPAR. When set to zero, odd parity is calculated for APAR and checked for DPAR.
	1	VC3VC4	**VC3 / VC4 Telecom Bus Operation:** When set to one, the Telecom Bus operates with stuffing per SONET requirements and SDH requirements for a TU-11 in a TUG-2, VC-3, AU-3 at either 6.48 or 19.44 MHz. When set to zero, the Telecom Bus operates with stuffing per SDH requirements for a TU-11 in a TUG-2 via a TUG-3, VC-3, AU-4 at 19.44 MHz only. Pin CONFIGI must be set to low if SDH stuffing is required.
	0	TXNRZP	**Transmit NRZ Polarity:** When set to one, the polarity of the data transmitted at TPOSn will be inverted at the pin; a logic one will generate a low output signal.

Address	Bit	Symbol	Description
008	7	MTBRCF	**Mask Telecom Bus Receive Clock Fail:** When set to one, the fault detector for DCLK is masked from generating an interrupt (status and event not affected).
	6	MTBRSF	**Mask Telecom Bus Receive Sync. Fail:** When set to one, the fault detector for DC1J1V1 is masked from generating an interrupt (status and event not affected).
	5	MTBRPF	**Mask Telecom Bus Receive Payload Indicator Fail:** When set to one, the fault detector for DSPE is masked from generating an interrupt (status and event not affected).
	4	R	**Reserved:** This bit must be set to zero.
	3	MMCKF	**Mask Master Clock Fail:** When set to one, the fault detector for SRCLK is masked from generating an interrupt (status and event not affected).
	2	MTBTCF	**Mask Telecom Bus Transmit Clock Fail:** When set to one, the fault detector for ACLK is masked from generating an interrupt (status and event not affected).
	1	MTBTSF	**Mask Telecom Bus Transmit Sync. Fail:** When set to one, the fault detector for AC1J1V1 is masked from generating an interrupt (status and event not affected).
	0	MTBTPF	**Mask Telecom Bus Transmit Payload Indicator Fail:** When set to one, the fault detector for ASPE is masked from generating an interrupt (status and event not affected).
009	7-4	R	**Reserved:** These bits must be set to zeros.
	3	MTBRPY	**Mask Telecom Bus Receive Parity Error:** When set to one, the parity error detector for the received Telecom Bus is masked from generating an interrupt (status and event not affected).
	2	MPRBSE	**Mask PRBS Out of Lock Events:** When set to one, the PRBS analyzer out of lock output is masked from generating an interrupt (status and event not affected).
	1	MTBIE	**Mask Telecom Bus Internal Error:** When set to one, the fault detector for Telecom Bus transmit internal collisions is masked from generating an interrupt (status and event not affected).
	0	MTBXE	**Mask Telecom Bus External Error:** When set to one, the fault detector for Telecom Bus transmit external collisions is masked from generating an interrupt (status and event not affected).

Address	Bit	Symbol	Description
00A	7	TBRCKS	**Telecom Bus Receive Clock Fail Status:** When set to one, the fault detector for DCLK is currently detecting loss of transitions. This bit is set to a 1 when no DCLK transitions are detected for a time between 32 and 64 cycles of PCKI. This bit is cleared to 0 when DCLK transitions are present for between 32 and 64 cycles of PCKI.
	6	TBRSNS	**Telecom Bus Receive Sync. Fail Status:** When set to one, the fault detector for DC1J1V1 is currently detecting loss of transitions. Detection time is 2000 ± 500 microseconds; clear time is a single transition of DC1J1V1.
	5	TBRPAS	**Telecom Bus Receive Payload Indicator Fail Status:** When set to one, the fault detector for DSPE is currently detecting loss of transitions. Detection time is 40 ± 10 microseconds; clear time is a single transition of DSPE.
	4	R	**Reserved:** This bit reads out as zero.
	3	MCKS	**Master Clock Fail Status:** When set to one, the fault detector for SRCLK is currently detecting loss of transitions. Detection time is 2.0 ± 0.5 microseconds (32 cycles of PCKI @ 16 MHz); This bit is cleared to zero when SRCLK is present for 32 cycles of PCKI.
	2	TBTCKS	**Telecom Bus Transmit Clock Fail Status:** When set to one, the fault detector for ACLK is currently detecting loss of transitions. This bit is set to a 1 when no ACLK transitions are detected for a time between 32 and 64 cycles of PCKI. This bit is cleared to 0 when ACLK transitions are present for between 32 and 64 cycles of PCKI.
	1	TBTSNS	**Telecom Bus Transmit Sync. Fail Status:** When set to one, the fault detector for AC1J1V1 is currently detecting loss of transitions. Detection time is 2000 ± 500 microseconds; clear time is a single transition of AC1J1V1.
	0	TBTPAS	**Telecom Bus Transmit Payload Indicator Fail Status:** When set to one, the fault detector for ASPE is currently detecting loss of transitions. Detection time is 40 ± 10 microseconds; clear time is a single transition of ASPE.
00B	7-4	R	**Reserved:** These bits read out as zeros.
	3	TBRPYS	**Telecom Bus Receive Parity Error Status:** When set to one, the parity error detector for the received Telecom Bus is detecting a parity error.
	2	PRBSS	**PRBS Out of Lock Status:** When set to one, the PRBS analyzer is out of lock.
	1	TBIES	**Telecom Bus Internal Error Status:** When set to one, the fault detector for Telecom Bus transmit internal collisions is detecting simultaneous bus slot access (i.e., two or more channel registers at X+05H set to same slot).
	0	TBXES	**Telecom Bus External Error Status:** When set to one, the fault detector for Telecom Bus transmit external collisions is detecting simultaneous bus slot access as determined by the $\overline{\text{AADD}}$ and $\overline{\text{BUSCHK}}$ pin levels.

Address	Bit	Symbol	Description
00C	7	TBRCKE	**Telecom Bus Receive Clock Fail Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for DCLK loss of clock. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	6	TBRSNE	**Telecom Bus Receive Sync. Fail Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for DC1J1V1 loss of signal. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	5	TBRPAE	**Telecom Bus Receive Payload Indicator Fail Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for DSPE loss of signal. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	4	R	**Reserved:** This bit must be set to zero.
	3	MCKE	**Master Clock Fail Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for SRCLK loss of clock. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	2	TBTCKE	**Telecom Bus Transmit Clock Fail Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for ACLK loss of clock. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	1	TBTSNE	**Telecom Bus Transmit Sync. Fail Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for AC1J1V1 loss of signal. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	0	TBTPAE	**Telecom Bus Transmit Payload Indicator Fail Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for ASPE loss of signal. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.

Address	Bit	Symbol	Description
00D	7-4	R	**Reserved:** These bits must be set to zeros.
	3	TBRPYE	**Telecom Bus Receive Parity Error Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for a parity error. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	2	PRBSE	**PRBS Out of Lock Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for a PRBS out of lock condition. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	1	TBIEE	**Telecom Bus Internal Error Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for an internal bus error. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
	0	TBXEE	**Telecom Bus External Error Latched Event:** This bit will be set to one when the active edge, as selected by RISE and FALL, has occurred for an external bus error. If not masked, an interrupt and/or internal alarm is generated when this bit is set. This bit is cleared only by writing it to zero.
00E	7	TBRCKPM	**Telecom Bus Receive Clock Performance Monitor:** This bit will be set to one if DCLK loss of clock has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRCKE has been cleared.
	6	TBRSNPM	**Telecom Bus Receive Sync. Performance Monitor:** This bit will be set to one if DC1J1V1 loss of signal has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRSNE has been cleared.
	5	TBRPAPM	**Telecom Bus Receive Payload Indicator Performance Monitor:** This bit will be set to one if DSPE loss of signal has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRPAE has been cleared.
	4	R	**Reserved:** This bit must be set to zero.
	3	MCKPM	**Master Clock Performance Monitor:** This bit will be set to one if SRCLK loss of clock has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit MCKE has been cleared.
	2	TBTCKPM	**Telecom Bus Transmit Clock Performance Monitor:** This bit will be set to one if ACLK loss of clock has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBTCKE has been cleared.

Address	Bit	Symbol	Description
00E (cont.)	1	TBTSNPM	**Telecom Bus Transmit Sync. Performance Monitor:** This bit will be set to one if AC1J1V1 loss of signal has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBTSNE has been cleared.
	0	TBTPAPM	**Telecom Bus Transmit Payload Indicator Performance Monitor:** This bit will be set to one if ASPE loss of clock has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBTPAE has been cleared.
00F	7-4	R	**Reserved:** These bits must be set to zeros.
	3	TBRPYPM	**Telecom Bus Receive Parity Error Performance Monitor:** This bit will be set to one if a parity error has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRPYE has been cleared.
	2	PRBSPM	**PRBS Out of Lock Performance Monitor:** This bit will be set to one if a PRBS out of lock has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit PRBSE has been cleared.
	1	TBIEPM	**Telecom Bus Internal Error Performance Monitor:** This bit will be set to one if an internal bus collision has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBXIE has been cleared.
	0	TBXEPM	**Telecom Bus External Error Performance Monitor:** This bit will be set to one if an external bus collision has occurred at any time in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBXEE has been cleared.
010	7-0	SPARE	**Spare:** This register should not be accessed.
011	7	R	**Reserved:** This bit reads out as zero.
	6-0	CH7 - CH1	**Channel Activity:** A bit is set to one for any channel that has one or more pending events. It is used as a polling register to identify channels in need of service or to locate channels that have generated an interrupt.
012	7-0	SPARE	**Spare:** This register should not be accessed.

Address	Bit	Symbol	Description
013	7	GXPE	**Global External LAIS Pin Event:** This bit will be set to one if an active signal is present (XPE is one) in any of the channels for LAIS. This bit will be cleared when all LAIS events have been cleared in the individual channel event registers.
	6	GDMPE	**Global Demap Error Event:** This bit will be set to one if a demap error event (DMPE) is present in any of the channels. This bit will be cleared when all demap error events have been cleared in the individual channel event registers.
	5	GLOSE	**Global LOS Event:** This bit will be set to one if a DS1 loss of signal event (LOSE) is present in any of the channels. This bit will be cleared when all DS1 loss of signal events have been cleared in the individual channel event registers.
	4	GMPE	**Global Map Error Event:** This bit will be set to one if a map error event (MPE) is present in any of the channels. This bit will be cleared when all map error events have been cleared in the individual channel event registers.
	3	GDAISE	**Global DS1 AIS Event:** This bit will be set to one if a DS1 AIS event (DAISE) is present in any of the channels. This bit will be cleared when all DS1 AIS events have been cleared in the individual channel event registers.
	2	GRPOE	**Global Received Pointer Justification Counter Overflow Event:** This bit will be set to one if a received pointer justification counter overflow event (RPOE) is present in any of the channels. This bit will be cleared when all receive pointer counter overflow events have been cleared in the individual channel event registers.
	1	GPGOE	**Global Generated Pointer Justification Counter Overflow Event:** This bit will be set to one if a generated pointer justification counter overflow event (PGOE) is present in any of the channels. This bit will be cleared when all pointer generation counter overflow events have been cleared in the individual channel event registers.
	0	GCVOE	**Global Code Violation Counter/CRC-6 Error Counter Overflow Event:** This bit will be set to one if a code violation counter/CRC-6 error counter overflow event (CVOE) is present in any of the channels. This bit will be cleared when all code violation counter/CRC-6 error counter overflow events have been cleared in the individual channel event registers.

Address	Bit	Symbol	Description
014	7	GFEOE	**Global REI (FEBE) Counter Overflow Event:** This bit will be set to one if a REI (FEBE) counter overflow event (FEOE) is present in any of the channels. This bit will be cleared when all REI (FEBE) counter overflow events have been cleared in the individual channel event registers.
	6	GBIPOE	**Global BIP-2 Error Counter Overflow Event:** This bit will be set to one if a BIP-2 error counter overflow event (BIPOE) is present in any of the channels. This bit will be cleared when all BIP-2 error counter overflow events have been cleared in the individual channel event registers.
	5	GVAISE	**Global VT AIS Event:** This bit will be set to one if a VT AIS event (VAISE) is present in any of the channels. This bit will be cleared when all VT AIS events have been cleared in the individual channel event registers.
	4	GLOPE	**Global Loss of Pointer Event:** This bit will be set to one if a loss of pointer event (LOPE) is present in any of the channels. This bit will be cleared when all loss of pointer events have been cleared in the individual channel event registers.
	3	GRFIE	**Global RFI Event:** This bit will be set to one if a remote failure indication event (RFIE) is present in any of the channels. This bit will be cleared when all RFI events have been cleared in the individual channel event registers.
	2	GUNEE	**Global Unequipped Event:** This bit will be set to one if an unequipped event (UNEE) is present in any of the channels. This bit will be cleared when all unequipped events have been cleared in the individual channel event registers.
	1	GSLME	**Global Signal Label Mismatch Event:** This bit will be set to one if a signal label mismatch event (SLME) is present in any of the channels. This bit will be cleared when all signal label mismatch events have been cleared in the individual channel event registers.
	0	GRDIE	**Global RDI Event:** This bit will be set to one if a remote defect indication event (RDI-VE, RDI-VPDE, RDI-VSDE or RDI-VCDE) is present in any of the channels. This bit will be cleared when all RDI events have been cleared in the individual channel event registers.

Address	Bit	Symbol	Description
015	7	GXPM	**Global External LAIS Pin Event Mask:** When set to one, all per channel LAIS events (XPE) are masked from generating interrupts (overrides per channel mask when set).
	6	GDMPM	**Global Demap Error Event Mask:** When set to one, all per channel demap error events (DMPE) are masked from generating interrupts (overrides per channel mask when set).
	5	GLOSM	**Global LOS Event Mask:** When set to one, all per channel LOS events (LOSE) are masked from generating interrupts (overrides per channel mask when set).
	4	GMPM	**Global Map Error Event Mask:** When set to one, all per channel map error events (MPE) are masked from generating interrupts (overrides per channel mask when set).
	3	GDAISM	**Global DS1 AIS Event Mask:** When set to one, all per channel DS1 AIS events (DAISE) are masked from generating interrupts (overrides per channel mask when set).
	2	GRPOM	**Global Received Pointer Justification Counter Overflow Event Mask:** When set to one, all received pointer justification counter overflow events (RPOE) are masked from generating interrupts (overrides per channel mask when set).
	1	GPGOM	**Global Generated Pointer Justification Counter Overflow Event Mask:** When set to one, all per channel generated pointer justification counter overflow events (PGOE) are masked from generating interrupts (overrides per channel mask when set).
	0	GCVOM	**Global Code Violation Counter/CRC-6 Error Counter Overflow Event Mask:** When set to one, all per channel code violation counter/CRC-6 error counter overflow events (CVOE) are masked from generating interrupts (overrides per channel mask when set).

Address	Bit	Symbol	Description
016	7	GFEOM	**Global REI (FEBE) Counter Overflow Event Mask:** When set to one, all per channel REI (FEBE) counter overflow events (FEOE) are masked from generating interrupts (overrides per channel mask when set).
	6	GBIPOM	**Global BIP-2 Error Counter Overflow Event Mask:** When set to one, all per channel BIP-2 error counter overflow events (BIPOE) are masked from generating interrupts (overrides per channel mask when set).
	5	GVAISM	**Global VT AIS Event Mask:** When set to one, all per channel VT AIS events (VAISE) are masked from generating interrupts (overrides per channel mask when set).
	4	GLOPM	**Global Loss of Pointer Event Mask:** When set to one, all per channel LOP events (LOPE) are masked from generating interrupts (overrides per channel mask when set).
	3	GRFIM	**Global RFI Event Mask:** When set to one, all per channel RFI events (RFIE) are masked from generating interrupts (overrides per channel mask when set).
	2	GUNEM	**Global Unequipped Event Mask:** When set to one, all per channel unequipped events (UNEE) are masked from generating interrupts (overrides per channel mask when set).
	1	GSLMM	**Global Signal Label Mismatch Event Mask:** When set to one, all per channel signal label mismatch events (SLME) are masked from generating interrupts (overrides per channel mask when set).
	0	GRDIM	**Global RDI Event Mask:** When set to one, all per channel RDI events (RDI-VE, RDI-VPDE, RDI-VSDE or RDI-VCDE) are masked from generating interrupts (overrides per channel mask when set).
017	7-0	D7-D0	**Command Byte:** This register contains the command byte for the serial port. The definitions of the bits will depend on the external device that is selected. The serial port control logic does not depend on the values in this register for operation. This byte is shifted out LSB (D0) first and represents the first byte sent out at pin LSDO.
018	7-0	D7-D0	**Line Interface Serial Data Output:** This register contains the serial data to be written to the selected line interface transceiver. The data is shifted out LSB (D0) first and represents the second byte sent out at pin LSDO.
019	7-0	D7-D0	**Line Interface Serial Data Input:** This register contains the read back data from the line interface transceiver when a read operation is performed. The data is shifted in LSB (D0) first (see pin LSDI).

Address	Bit	Symbol	Description
01A	7	BDCST	**Broadcast:** When this bit is set to one, serial port command and data output registers are broadcast to all seven line interface transceivers.
	6	R	**Reserved:** This bit must be set to zero.
	5	EPRBSA	**PRBS Enable:** When set to one, both the internal PRBS analyzer and PRBS generator are enabled. Bits 2, 1 and 0 of this register select which channel's line decoder output is connected to the analyzer. The analyzer's output is a one for bits PRBSS, PRBSE, PRBSPM and PRBSFM as controlled by bits MPRBSE and EPRBSE. When this bit is set to zero or when the PRBS analyzer is in lock, a zero is present in PRBSS, PRBSE, PRBSPM and PRBSFM. To operate with an ITU-T O.151 compliant 2^{15} - 1 signal, the output of the PRBS generator and/or the input to the PRBS analyzer must be inverted. This is controlled by setting either or both TXNRZP and RXNRZP in the global registers to a 1.
	4	ENSRP	**Enable Serial Port:** When set to one, a single transfer takes place to the selected device (single or broadcast) in serial port mode. This bit must be toggled to zero before setting it to one for another transfer.
	3	R	**Reserved:** This bit must be set to zero.
	2-0		**DS1 Channel Number (0-6):** When decoded with bit 0 as least significant bit the value (N=0-6) selected drives the active low chip select pin, $\overline{LCS(N+1)}$. BDCST causes all seven $\overline{LCSn}$ pins to be selected in serial port mode. In PRBS operation these bits select the channel to be monitored by the PRBS analyzer.
01B	7	ETBRCF	**EnableTelecom Bus Receive Clock Fail:** When set to one, the fault detector for DCLK is enabled to drive pin $\overline{IAO}$ if DCLK fails.
	6	ETBRSF	**Enable Telecom Bus Receive Sync. Fail:** When set to one, the fault detector for DC1J1V1 is enabled to drive pin $\overline{IAO}$ if DC1J1V1 fails.
	5	ETBRPF	**Enable Telecom Bus Receive Payload Indicator Fail:** When set to one, the fault detector for DSPE is enabled to drive pin $\overline{IAO}$ if DSPE fails.
	4	R	**Reserved:** This bit must be set to zero.
	3	EMCKF	**Enable Master Clock Fail:** When set to one, the fault detector for SRCLK is enabled to drive pin $\overline{IAO}$ if SRCLK fails.
	2	ETBTCF	**Enable Telecom Bus Transmit Clock Fail:** When set to one, the fault detector for ACLK is enabled to drive pin $\overline{IAO}$ if ACLK fails.
	1	ETBTSF	**Enable Telecom Bus Transmit Sync. Fail:** When set to one, the fault detector for AC1J1V1 is enabled to drive pin $\overline{IAO}$ if AC1J1V1 fails.
	0	ETBTPF	**Enable Telecom Bus Transmit Payload Indicator Fail:** When set to one, the fault detector for ASPE is enabled to drive pin $\overline{IAO}$ if ASPE fails.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>01C</td><td>7-4</td><td>R</td><td>Reserved: These bits must be set to zeros.</td></tr>
<tr><td></td><td>3</td><td>ETBRPY</td><td>Enable Telecom Bus Receive Parity Error: When set to one, the parity error detector for the receive Telecom Bus is enabled to drive pin $\overline{IAO}$ if a parity error is detected.</td></tr>
<tr><td></td><td>2</td><td>EPRBSE</td><td>Enable PRBS Out of Lock Events: When set to one, the PRBS analyzer out of lock output is enabled to drive pin $\overline{IAO}$ if the PRBS analyzer goes out of lock.</td></tr>
<tr><td></td><td>1</td><td>ETBIE</td><td>Enable Telecom Bus Internal Error: When set to one, the fault detector for Telecom Bus transmit internal collisions is enabled to drive pin $\overline{IAO}$ if an internal collision occurs.</td></tr>
<tr><td></td><td>0</td><td>ETBXE</td><td>Enable Telecom Bus External Error: When set to one, the fault detector for Telecom Bus transmit external collisions is enabled to drive pin $\overline{IAO}$ if an external collision occurs.</td></tr>
<tr><td>01D</td><td>7-0</td><td>ECTL7 - ECTL0</td><td>Error Control Length: These bits meter the number of BIP-2 or REI (FEBE) errors introduced when a channel’s SFEBE or SBIPE bit is set to one. Note that when a channel is set to idle (control bit IDLE is zero), this register has no effect on SFEBE or SBIPE and SFEBE set to one or SBIPE set to one will cause continuous REI-V (FEBE) or BIP-2 errors to be sent.
<table>
<tr><th>ECTL(7-0)</th><th>Resulting Errors Sent</th></tr>
<tr><td>00</td><td>1 Frame</td></tr>
<tr><td>01</td><td>2 Frames</td></tr>
<tr><td>02
↓</td><td>3 Frames
↓</td></tr>
<tr><td>FD</td><td>254 Frames</td></tr>
<tr><td>FE</td><td>255 Frames</td></tr>
<tr><td>FF</td><td>Continuous</td></tr>
</table></td></tr>
</table>

Address	Bit	Symbol	Description
01E	7	TBLPBK	**Telecom Bus Loopback:** When set to one, internally the Telecom Bus is placed in loopback with all 28 or 84 timeslots out of the mappers connected to the 28 or 84 timeslots of the demappers. ACLK is the only Telecom Bus signal used in Telecom Bus Loopback; payload and reference signals are internally generated. This is an off-line test for the entire DS1MX7 with invalid data sent to the Telecom Bus; individual channels may be tested with the PRBS generator / analyzer in this mode.
	6	FTBTPE	**Force Telecom Bus Transmit Parity Error:** When set to one, the parity to the Telecom Bus (APAR) is inverted, forcing continuous parity errors.
	5	TBTCI	**Telecom Bus Transmit Clock Inversion:** When set to zero, the active edge of ACLK is the falling edge for AD(0-7) and APAR and the rising edge for ASPE and AC1J1V1. When set to one, the active edge of ACLK is the rising edge for AD(0-7) and APAR and the falling edge for ASPE and AC1J1V1.
	4	TBRCI	**Telecom Bus Receive Clock Inversion:** When set to zero, the active edge of DCLK is the rising edge. When set to one, the active edge of DCLK is the falling edge.
	3	TBDD	**Telecom Bus Data Delay:** When set to zero, AD(0-7) and APAR are prefetched and made available on the active edge of ACLK as defined by ASPE and AC1J1V1 (as shown in Figure 9) with drive control as determined by drive pins DATEN and $\overline{\text{MASTER}}$ (as described in the Block Diagram Description and Operation-Telecom Bus Interface section). When set to one, AD(0-7) and APAR are delayed by one full clock period of ACLK; DATEN and $\overline{\text{MASTER}}$ function as described in the same location except that they are delayed by one column.
	2-1	R	**Reserved:** These bits must be set to zeros.
	0	RDID10	**RDI De-bouncing equals 10:** When set to zero, RDI is de-bounced for 5 VT superframes. This means it must be set for 5 VT superframes in a row to be declared as RDI for a channel and it must be cleared for 5 VT superframes in a row to be cleared. When set to one, RDI is de-bounced for 10 VT superframes.
01F - 03B	7-0	SPARE	**Spare:** These registers should not be accessed.
03C	7	DPLLLK	**Digital Phase Lock Loop Lock:** When set to one, the DPLL FIFO depth is determined by the value of DPLL(6-0) in this register. This forces a constant frequency from all DPLLs (LTCLKn). When set to zero, the DPLL bias offset is determined by DPLL(6-0). For normal DS1MX7 operation set DPLLLK to zero. This control bit is for test purposes.
	6-0	DPLL6 - DPLL0	**Digital Phase Lock Loop Control:** When DPLLLK is set to zero, the value of DPLL(6-0) is the ones complement of the DPLL bias offset; for DPLL(6-0) = 00 Hex, the nominal design value is chosen. When DPLLLK is set to one, DPLL(6-0) determines the FIFO depth. For normal operation, set to zero. These control bits are for test purposes.

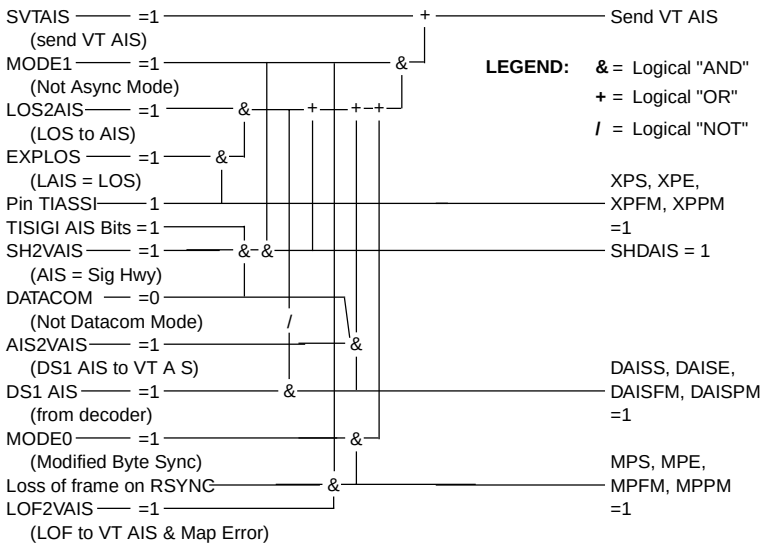
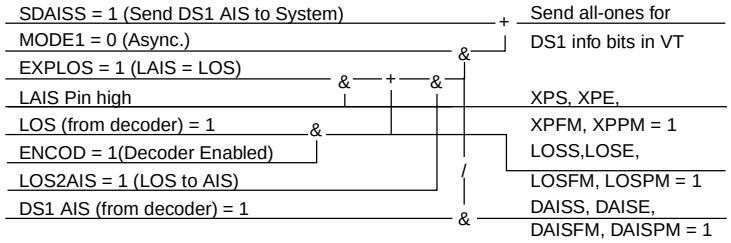
Address	Bit	Symbol	Description
03D	7-5	R	**Reserved:** These bits must be set to zeros.
	4	BYPLB	**Bypass Pointer Leak Buffer:** When set to zero, the pointer leak buffer is enabled in all channels. When set to one, the pointer leak buffer is bypassed. For normal operation, set this bit to zero. This control bit is for test purposes.
	3	PRBSCK	**PRBS Clock:** When set to zero, SRCLK is selected as the source of PRBS clock. This bit is used for manufacturing tests; do not set it to a 1.
	2	TMDIS	**Threshold Modulator Disable:** When set to zero, the threshold modulator is enabled. When set to one, the threshold modulator is disabled. For normal operation this bit should be set to zero. This control bit is for test purposes and may not be available in future versions.
	1, 0	C2PH(1-0)	**C2 Stuff Bit Phase:** When both bits are set to zero, normal threshold modulator phase is chosen for the C2 stuff bits. Setting either or both of these bits to one chooses an alternate phase for the threshold modulator. For normal operation, both of these bits should be set to zero. These control bits are for test purposes and may not be available in future versions.
03E	7	TBRCKFM	**Telecom Bus Receive Clock Fault Monitor:** This bit will be set to one if DCLK loss of clock is present but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRCKE has been cleared.
	6	TBRSNFM	**Telecom Bus Receive Sync. Fault Monitor:** This bit will be set to one if DC1J1V1 loss of signal is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRSNE has been cleared.
	5	TBRPAFM	**Telecom Bus Receive Payload Indicator Fault Monitor:** This bit will be set to one if DSPE loss of signal is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRPAE has been cleared.
	4	R	**Reserved:** This bit must be set to zero.
	3	MCKFM	**Master Clock Fault Monitor:** This bit will be set to one if SRCLK loss of clock is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit MCKE has been cleared.
	2	TBTCKFM	**Telecom Bus Transmit Clock Fault Monitor:** This bit will be set to one if ACLK loss of clock is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBTCKE has been cleared.

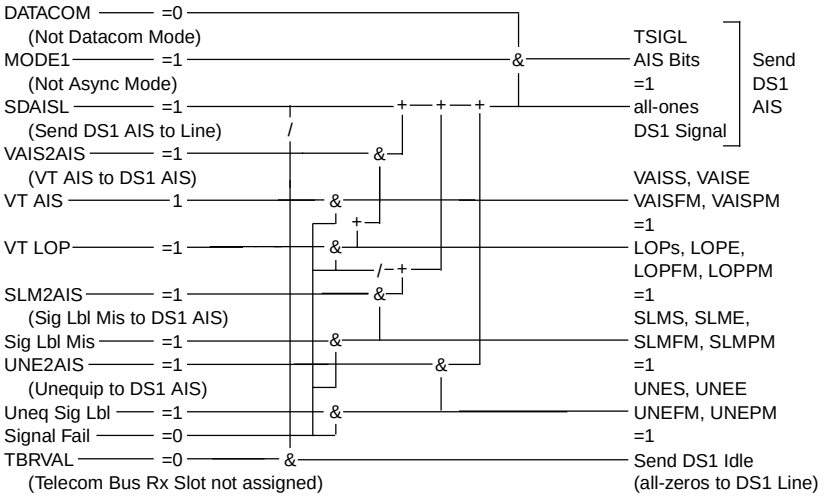
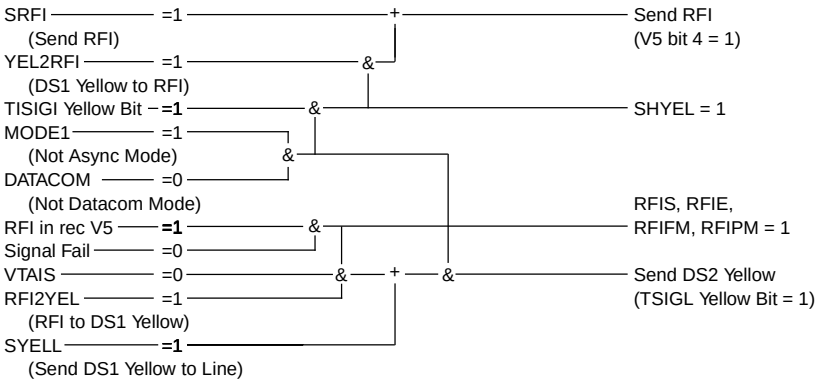
Address	Bit	Symbol	Description
03E (cont.)	1	TBTSNFM	**Telecom Bus Transmit Sync. Fault Monitor:** This bit will be set to one if AC1J1V1 loss of signal is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI.This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBTSNE has been cleared.
	0	TBTPAFM	**Telecom Bus Transmit Payload Indicator Fault Monitor:** This bit will be set to one if ASPE loss of clock is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBTPAE has been cleared.
03F	7-4	R	**Reserved:** These bits must be set to zeros.
	3	TBRPYFM	**Telecom Bus Receive Parity Error Fault Monitor:** This bit will be set to one if a parity error is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI.This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBRPYE has been cleared.
	2	PRBSFM	**PRBS Out of Lock Fault Monitor:** This bit will be set to one if a PRBS out of lock is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit PRBSE has been cleared.
	1	TBIEFM	**Telecom Bus Internal Error Fault Monitor:** This bit will be set to one if an internal bus collision is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBIEE has been cleared.
	0	TBXEFM	**Telecom Bus External Error Fault Monitor:** This bit will be set to one if an external bus collision is present, but the transition to this state did not occur in the last one-second interval as defined by T1SI. This bit is cleared by writing it to zero or by T1SI rising edge if the condition no longer exists and event bit TBXEE has been cleared.

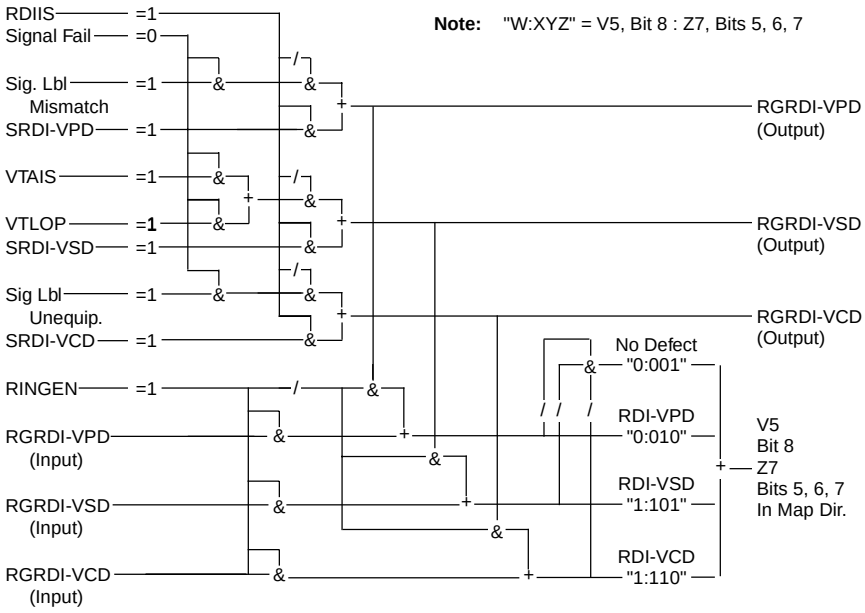
PER CHANNEL CONTROL REGISTERS

*Note: In the address, X= 040H for DS1 channel 1; 080H for DS1 channel 2; 0C0H for DS1 channel 3; 100H for DS1 channel 4; 140H for DS1 channel 5; 180H for DS1 channel 6; 1C0H for DS1 channel 7.

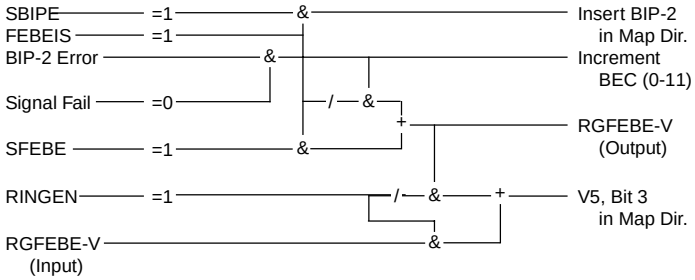
<table>
<tr><th>Address*</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="6">X+00</td><td>7</td><td>IDLE</td><td>Set the Channel to Idle: When set to zero, the channel is powered down; all-zeros are substituted for the payload and overhead bytes except V5. Either an all-zeros V5 may be sent, indicating an unequipped condition, or a valid V5 may be sent (unassigned); V5 is determined by per channel control bits RDIIS, FEBEIS, SFEBE, SRDI and Transmit Signal Label. For normal operation, including sending VT AIS, this bit should be set to one. Note that for proper idle operation register TXZ7 (reg. X+39H) should also be set to 00H.</td></tr>
<tr><td>6</td><td>EXPLOS</td><td>External Pin enables LOS: When set to one, LAIS active (as determined by RXNRZP) is treated as LOS from the decoder. Set this bit to one if using an external decoder or external Loss of Clock detector. Set this bit to zero if LAIS pin is unused or used for another purpose (e.g., interrupt from an external line transceiver). See SH2AIS and LOS2AIS below for logic (register X+01H).</td></tr>
<tr><td>5</td><td>DATACOM</td><td>Datacom Mode: This bit, in conjunction with MODE0 and MODE1, enables Datacom Mode. If MODE1 is set to zero, this bit is disregarded. See MODE0, MODE1 in this register.</td></tr>
<tr><td>4</td><td>ENZC</td><td>Enable Excess Zeros Count: When set to one, this bit will enable the BPV counter to also count excess zeros. When B8ZS transcoding is enabled, 8 or more consecutive zeros is an error. When B8ZS transcoding is disabled, 16 or more consecutive zeros is an error.</td></tr>
<tr><td>3</td><td>LCODE</td><td>Line Code Select: When set to one and ENCOD is set to one, B8ZS is selected for coding and decoding. When set to zero and ENCOD is set to one, AMI is selected for coding and decoding. When ENCOD is set to zero, this bit selects the signal level on TNEGn.
<table>
<tr><th>ENCOD</th><th>LCODE</th><th>MODE1</th><th>Line Code</th><th>TNEGn</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>AMI</td><td>per codec</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>B8ZS</td><td>per codec</td></tr>
<tr><td>0</td><td>0</td><td>0,1</td><td>NRZ</td><td>logic low</td></tr>
<tr><td>0</td><td>1</td><td>0,1</td><td>NRZ</td><td>logic high</td></tr>
</table></td></tr>
<tr><td>2</td><td>ENCOD</td><td>Enable Codec: When set to one, the line coder and decoder are enabled if MODE1 is set to zero with the code selected by LCODE. When set to zero, or if MODE1 is set to one, NRZ is selected.</td></tr>
</table>

<table>
<tr><th>Address*</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X+00
(cont.)</td><td>1
0</td><td>MODE1,
MODE0</td><td>Mode of Operation: These bits select among two Byte Synchronous or Datacom modes and the Asynchronous mode. Modified Byte Synchronous/Datacom mode accepts clock and frame from the framer; in Byte Synchronous/Datacom mode, DS1MX7 supplies clock and frame for both directions of transmission.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>DATACOM</th><th>Line Code</th><th>Mapping Mode</th></tr>
<tr><td>0</td><td>0</td><td>-</td><td>AMI, B8ZS, NRZ</td><td>Asynchronous</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>AMI, B8ZS, NRZ</td><td>Asynchronous</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>NRZ</td><td>Byte Synchronous</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>NRZ</td><td>Byte Synchronous Datacom</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>NRZ</td><td>Modified Byte Synchronous</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>NRZ</td><td>Modified Byte Synchronous Datacom</td></tr>
</table></td></tr>
<tr><td rowspan="2">X+01</td><td>7</td><td>SH2VAIS</td><td>Enable Signaling Highway to VT AIS: When set to one and Datacom set to zero, the AIS bit on the signaling highway (RSIGLn) in Byte Synchronous mode maps to VT AIS.

</td></tr>
<tr><td>6</td><td>LOS2AIS</td><td>Enable LOS to VT or DS1 AIS: When set to one, LOS from the DS1 side maps to VT AIS (Byte Synchronous; see SH2VAIS for logic) or DS1 AIS.

</td></tr>
</table>

Address*	Bit	Symbol	Description
X+01 (cont.)	5	LOF2VAIS	**Enable Loss of Frame to VT AIS and Map Error:** When set to one, the loss of multiframe synchronization signal (RSYNCn) maps to VT AIS and is indicated as a map error (see SH2VAIS for logic)
	4	CRC6	**Enable CRC-6 generation:** When set to one in the True Byte Sync mode only, CRC-6 is generated into the transmit VT payload. CRC-6 is calculated on the Received VT payload and compared with the received CRC-6 code.
	3	VAIS2AIS	**Enable VT AIS to DS1 AIS:** When set to one, VT AIS received in V1 and V2 is mapped to DS1 AIS. 
	2	RFI2YEL	**Enable RFI to DS1 Yellow:** When set to one, RFI received in V5 is mapped to DS1 Yellow on the signaling highway. If DATACOM is set to one, this bit is disregarded. 
	1	YEL2RFI	**Enable DS1 Yellow to RFI:** When set to one, DS1 Yellow on the signaling highway maps to RFI in V5 (see RFI2YEL for logic). If DATACOM is set to one, this bit is disregarded.
	0	AIS2VAIS	**Enable DS1 AIS to VT AIS:** When set to one, DS1 AIS detected in the decoder (99.9% or more ones) maps to VT AIS in the byte sync. mode (see SH2VAIS for logic). If DATACOM is set to one, this bit is disregarded.

Address*	Bit	Symbol	Description
X+02	7	SRDI-VPD*	**Send RDI-VPD:** When set to one, RDI-VPD is sent continuously if RDIIS is also set to one. See RDIIS below for logic. Set to zero if this channel is programmed unequipped.
	6	SRDI-VSD*	**Send RDI-VSD:** When set to one, RDI-VSD is sent continuously if RDIIS is also set to one. See RDIIS below for logic. Set to zero if this channel is programmed unequipped.
	5	SRDI-VCD*	**Send RDI-VCD:** When set to one, RDI-VCD is sent continuously if RDIIS is also set to one. See RDIIS below for logic. Set to zero if this channel is programmed unequipped.
	4	R	**Reserved:** This bit must be set to zero.
	3	RDIIS	**RDI Insert Select:** When set to zero, RDI-Vxx is generated autonomously from either internally detected faults or from values input at the Ring Port. When set to one RDI-Vxx is sent continuously if SRDI-Vxx is set to one.  Set to one if this channel is programmed unequipped.
	2	SLM2AIS	**Enable Signal Label Mismatch to AIS:** When set to one, a Signal Label Mismatch detected maps to DS1 AIS (see VAIS2AIS above for logic). This bit should be set to one if this channel is programmed unequipped.

* Note: When forcing by microprocessor selection, set only one of the bits SRDI-VPD, SRDI-VSD and SRDI-VCD to one at any given time, to retain proper alarm priority.

Address*	Bit	Symbol	Description
X+02 (cont)	1	FEBEIS	**REI (FEBE) Insert Select:** When set to zero, REI (FEBE) is generated from received BIP-2 errors or from the Ring Port Input. When set to one, REI (FEBE) or BIP-2 errors can be created with SFEBE or SPIBE. The required REI (FEBE) value is always output at the Ring Port (RGFEBE-V). The REI (FEBE) value appearing in the outgoing V5, Bit 3 results from received BIP-2 errors if RINGEN is set to zero or from the Input Ring Port value, RGFEBE-V, if RINGEN is set to one. 
	0	UNE2AIS	**Enable Unequipped to DS1 AIS:** When set to one, an Unequipped Signal Label received is mapped to DS1 AIS (see VAIS2AIS for logic). This bit should be set to a zero if this channel is unequipped. Use SDAIS to force AIS to DS1 line if required when UNE2AIS is set to zero.
X+03	7	SFEBE	**Send REI (FEBE):** When set to one, REI (FEBE) is sent the number of times specified by ECTL(0-7) if control bit FEBEIS is set to one, control bit IDLE is set to one and if control bit RINGEN is set to zero. When set to one, REI (FEBE) is sent continuously if control bit FEBEIS is set to one, control bit IDLE is set to zero and if control bit RINGEN is set to zero. If RINGEN is set to one, the FEBEs from the ring port are placed in the outgoing V5, Bit 3.
	6	SDAISS	**Send DS1 AIS to System:** When set to one, DS1 AIS (all-ones) is used for the VT1.5 or TU-11 payload in the map direction.
	5	SBIPE	**Send BIP-2 Errors:** When set to one, inverted BIP-2 is sent the number of times specified by ECTL(0-7) if FEBEIS is set to one. This bit must be cleared to zero and set again to send a second set of inverted BIP-2.
	4	R	**Reserved:** This bit must be set to zero.
	3	SDAISL	**Send DS1 AIS to the DS1 Line:** When set to one, DS1 AIS is sent out of the coder using nominal timing (derived from SRCLK by dividing by 31.5)
	2	SYELL	**Send DS1 Yellow:** When set to one, DS1 Yellow is sent on the signaling highway (TSIGLn) in Byte Synchronous mode. If DATACOM is set to one, this bit is disregarded.
	1	SRFI	**Send RFI:** When set to one, the RFI bit is set in V5.
	0	SVTAIS	**Send VT AIS:** When set to one, VT AIS is generated in the mapping direction by generating an all-ones VT1.5 or TU-11.

<table>
<tr><th>Address*</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="4">X+04</td><td>7</td><td>TBRVAL</td><td>Telecom Bus Receive Valid: When set to one, the Telecom Bus receive slot (information to DD(0-7)), as defined by the rest of the bits in this register, is considered valid and this channel’s VT1.5 or TU-11 reads the bus. When set to zero, this channel does not read the DD(0-7) bus, nor does it send data to the auxiliary port.</td></tr>
<tr><td>6-5</td><td>Tel Bus RX STS-1 # (1-3)</td><td>Telecom Bus Receive STS-1 Number:
These bits select the STS-1 if the CONFIGI pin is grounded.
<table>
<tr><th>bit 6</th><th>bit 5</th><th>STS-1 Number</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>Not valid - do not use</td></tr>
</table></td></tr>
<tr><td>4-2</td><td>Tel Bus RX VT Group or TUG # (1-7)</td><td>Telecom Bus Receive VT Group or TUG Number:
These bits select the VT Group or TUG.
<table>
<tr><th>bit 4</th><th>bit 3</th><th>bit 2</th><th>VT Group or TUG number</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Not valid - do not use</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>Tel Bus RX VT or TU # (1-4)</td><td>Telecom Bus REceive VT or TU Number:
These bits select the individual VT or TU in the group or TUG.
<table>
<tr><th>bit 1</th><th>bit 0</th><th>VT or TU number</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>4</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Address*</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="3">X+05</td><td>7</td><td>TBTVAL</td><td>Telecom Bus Transmit Valid: When set to one, the Telecom Bus transmit slot (information from AD(0-7)), as defined by the rest of the bits in this register, is considered valid and this channel's VT1.5 or TU-11 drives the bus. When set to zero, this channel does not drive the AD(0-7) bus nor does it request data from the auxiliary port.</td></tr>
<tr><td>6-5</td><td>Tel Bus TX STS-1 # (1-3)</td><td>Telecom Bus Transmit STS-1 Number:
These bits select the STS-1 if the CONFIGI pin is grounded.
<table>
<tr><th>bit 6</th><th>bit 5</th><th>STS-1 Number</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>Not valid - do not use</td></tr>
</table></td></tr>
<tr><td>4-2</td><td>Tel Bus TX VT Group or TUG # (1-7)</td><td>Telecom Bus Transmit VT Group or TUG Number:
These bits select the VT Group or TUG.
<table>
<tr><th>bit 4</th><th>bit 3</th><th>bit 2</th><th>VT Group or TUG number</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>Tel Bus TX VT or TU # (1-4)</td><td>Telecom Bus Transmit VT or TU Number:
These bits select the individual VT or TU in the group or TUG.
<table>
<tr><th>bit 1</th><th>bit 0</th><th>VT or TU number</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>4</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Address*</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X+06</td><td>7-0</td><td>PL(8-1)</td><td>Pointer Leak Rate: These bits determine the rate at which a pointer movement is leaked out of the pointer leak buffer into the DPLL. If PL(8-1) is set to 00H the maximum leak rate of one bit per 16 VT superframes (8 ms) is used, with each count decreasing the rate by 16 VT superframes (8 ms). The times shown in the table below apply when the pointer leak buffer (which is ±40 bits) is 12 bits or more above or below center. When the pointer leak buffer is less than 12 bits above or below center, the time between bits leaked is twice that shown in the table.
<table>
<tr><th>PL8 - PL1</th><th>Time between bits leaked from Pointer Leak Buffer</th></tr>
<tr><td>00H</td><td>8 ms</td></tr>
<tr><td>01H</td><td>16 ms</td></tr>
<tr><td>02H
↓</td><td>24 ms
↓</td></tr>
<tr><td>FDH</td><td>2,032 ms</td></tr>
<tr><td>FEH</td><td>2,040 ms</td></tr>
<tr><td>FFH</td><td>2,048 ms</td></tr>
</table></td></tr>
<tr><td rowspan="4">X+07</td><td>7</td><td>R</td><td>Reserved: This bit must be set to zero.</td></tr>
<tr><td>6-4</td><td>Exp. Sig. Label (2-0)</td><td>Expected Signal Label: Bits 6 through 4 correspond to bits 5 through 7 respectively of V5 (GR-253-CORE Issue 2, Fig. 3-25) received from the Telecom Bus. The signal label mismatch detector compares these bits with those received from the Telecom Bus. Set to 000 for unequipped, to 010 for Asynchronous operation, to 001 for equipped non-specific, or to 100 for Byte Synchronous operation.</td></tr>
<tr><td>3</td><td>R</td><td>Reserved: This bit must be set to zero.</td></tr>
<tr><td>2-0</td><td>TX Sig. Label (2-0)</td><td>Transmit Signal Label: Bits 2 through 0 correspond to bits 5 through 7 respectively of V5 (GR-253-CORE Issue 2, Fig. 3-25) to be sent out on the Telecom Bus.</td></tr>
</table>

Address*	Bit	Symbol	Description
X+08	7	XPM	**External LAIS Pin Event Mask:** When set to one, this channel's LAIS events (XPE) are masked from generating interrupts (status and event not affected).
	6	DMPM	**Demap Error Event Mask:** When set to one, this channel's demap error events (DMPE) are masked from generating interrupts (status and event not affected).
	5	LOSM	**LOS Event Mask:** When set to one, this channel's LOS events(LOSE) are masked from generating interrupts (status and event not affected).
	4	MPM	**Map Error Event Mask:** When set to one, this channel's map error events (MPE) are masked from generating interrupts (status and event not affected).
	3	DAISM	**DS1 AIS Event Mask:** When set to one, this channel's DS1 AIS events (DAISE) are masked from generating interrupts (status and event not affected).
	2	RPOM	**Received Pointer Justification Counter Overflow Event Mask:** When set to one, received pointer justification counter overflow events (RPOE) from this channel are masked from generating interrupts (status and event not affected).
	1	PGOM	**Generated Pointer Justification Counter Overflow Event Mask:** When set to one, this channel's generated pointer justification counter overflow events (PGOE) are masked from generating interrupts (status and event not affected).
	0	CVOM	**Code Violation Counter/CRC-6 Error Counter Overflow Event Mask:** When set to one, this channel's code violation counter/CRC-6 error counter overflow events (CVOE) are masked from generating interrupts (status and event not affected).
X+09	7	FEOM	**REI (FEBE) Counter Overflow Event Mask:** When set to one, this channel's REI (FEBE) counter overflow events (FEOE) are masked from generating interrupts (status and event not affected).
	6	BIPOM	**BIP-2 Error Counter Overflow Event Mask:** When set to one, this channel's BIP-2 error counter overflow events (BIPOE) are masked from generating interrupts (status and event not affected).
	5	VAISM	**VT AIS Event Mask:** When set to one, this channel's VT AIS events (VAISE) are masked from generating interrupts (status and event not affected).
	4	LOPM	**Loss of Pointer Event Mask:** When set to one, this channel's LOP events (LOPE) are masked from generating interrupts (status and event not affected).
	3	RFIM	**RFI Event Mask:** When set to one, this channel's RFI events (RFIE) are masked from generating interrupts (status and event not affected).
	2	UNEM	**Unequipped Event Mask:** When set to one, this channel's unequipped events (UNEE) are masked from generating interrupts (status and event not affected). Set to one when this channel is programmed unequipped.

Address*	Bit	Symbol	Description
X+09 (cont)	1	SLMM	**Signal Label Mismatch Event Mask:** When set to one, this channel's signal label mismatch events (SLME) are masked from generating interrupts (status and event not affected). Set to one when this channel is programmed unequipped.
	0	RDIM	**RDI Event Mask:** When set to one, this channel's RDI events (RDI_VE) are masked from generating interrupts (status and event not affected).
X+0A	7-3	R	**Reserved:** These bits must be set to zeros.
	2	RDI-VPDM	**RDI-VPD Event Mask:** When set to one, this channels's RDI-VPD events (RDI-VPDE) are masked from generating interrupts (status and event not affected).
	1	RDI-VSDM	**RDI-VSD Event Mask:** When set to one, this channels's RDI-VSD events (RDI-VSDE) are masked from generating interrupts (status and event not affected).
	0	RDI-VCDM	**RDI-VCD Event Mask:** When set to one, this channels's RDI-VCD events (RDI-VCDE) are masked from generating interrupts (status and event not affected).
X+0B	7-5	R	**Reserved:** These bits must be set to zeros.
	4	RINGEN	**Ring Port Enable:** When set to one, the outgoing V5 REI (FEBE) and RDI-Vxx values are accepted from the Ring Port Input. See RDIIS and FEBEIS above for logic. Information input at the Ring Port is readable by the microprocessor in register X+3AH.
	3	OBAPEN	**O-bits Auxiliary Port Enable:** When set to zero, register X+36H contains microprocessor-written data that will appear on AD(0-7). When set to one, the O-bit incoming at the Auxiliary Port will appear on AD(0-7) and will also be written in register X+36H for access by the microprocessor.
	2	J2APEN	**J2 Auxiliary Port Enable:** When set to zero, register X+37H contains microprocessor- written data that will appear on AD(0-7). When set to one, the J2 Byte incoming at the Auxiliary Port will appear on AD(0-7) and will also be written in register X+37H for access by the microprocessor.
	1	Z6APEN	**Z6/N2 Auxiliary Port Enable:** When set to zero, register X+38H contains microprocessor–written data that will appear on AD(0-7). When set to one, the Z6/N2 Byte incoming at the Auxiliary Port will appear on AD(0-7) and will also be written in register X+38H for access by the microprocessor.
	0	Z7APEN	**Z7/K4 Auxiliary Port Enable:** When set to zero, register X+39H contains microprocessor–written data that will appear on AD(0-7). When set to one, the Z7/K4 Byte incoming at the Auxiliary Port will appear on AD(0-7) and will also be written in register X+39H for access by the microprocessor. When RINGEN is set to one, RDI insert is from the ring port even if this bit is set to one.

Address*	Bit	Symbol	Description
X+0C	7	DTLPBK	**DS1 Tributary Loopback:** When set to one, the output of the coder is looped to the input of the decoder. Clock, multiframe synchronization and signaling are also looped back. This loopback is useful for DS1MX7 self test with the PRBS generator and analyzer.
	6	DFLPBK	**DS1 Remote Facility Loopback:** When set to one, the output of the decoder is looped to the input of the coder. Clock, multiframe synchronization and signaling are also looped back. This loopback is used to provide remote facility loopback testing.
	5	RSTCH	**Reset Channel:** When this bit is set to one, this channel is held in reset; it provides the same function that the Reset register (005H) provides for all channels.
	4	SPRBS	**Send PRBS:** When set to one, the output of the PRBS generator is substituted for the output of the decoder for this channel. This bit, used in conjunction with DTLPBK (DS1 facility loopback), bit 7 in this register, TBLPBK (Telecom bus loopback) at register 01EH bit 7, EPRBSA (enable PRBS Generator/Analyzer) at register 01AH bit 5, which must be set to one, and the DS1 Channel number, provides a self test of this channel.
	3-0	R	**Reserved:** These bits must be set to zeros.
X+0D - X+0F	7-0	R	**Reserved:** These registers should not be accessed.

PER CHANNEL STATUS REGISTERS

Address*	Bit	Symbol	Description
X+10	7	XPS	**External Pin Status:** When this bit is a one, the external pin (LAIS) for this channel is active per RXNRZP (LAIS is high if RXNRZP is zero or LAIS is low if RXNRZP is one).
	6	DMPS	**Demap Error Status:** When this bit is a one, a fault (e.g. internal FIFO overflow/underflow) is occurring in the desynchronizer for this channel.
	5	LOSS	**Loss of Signal Status:** When this bit is a one, LOS is currently being detected in this channel. LOS is entered on 175 ± 75 contiguous pulse positions with no pulses of either positive or negative polarity. LOS exits on 12.5% or greater ones density for 175 ± 75 contiguous pulse positions. LOS does not function in NRZ mode.
	4	MPS	**Map Error Status:** When this bit is a one, a map error is occurring in this channel. If bit LOF2VAIS is one, this bit represents a loss of multiframe input in Byte Synchronous operation.
	3	DAISS	**DS1 AIS Status:** When this bit is a one, DS1 AIS is being detected in the line decoder for this channel. DS1 AIS is declared if 99.9% ones are detected for between 3 and 75 milliseconds. AIS exits on less than 99.9% all-ones for between 3 and 75 milliseconds.
	2	RPOS	**Received Pointer Justification Counter Overflow Status:** When this bit is a one, the received pointer justification counter for this channel has overflowed.
	1	PGOS	**Generated Pointer Justification Counter Overflow Status:** When this bit is a one, the generated pointer justification counter has overflowed for this channel.
	0	CVOS	**Code Violation Counter/CRC-6 Error Counter Overflow Status:** When this bit is a one, the code violation counter/CRC-6 error counter for this channel has overflowed.

Address*	Bit	Symbol	Description
X+11	7	FEOS	**REI (FEBE) Counter Overflow Status:** When this bit is a one, the REI (FEBE) counter for this channel has overflowed.
	6	BIPOS	**BIP-2 Error Counter Overflow Status:** When this bit is a one, the BIP-2 error counter for this channel has overflowed.
	5	VAISS	**VT AIS Status:** When this bit is a one, VT AIS is currently being detected for this channel. VT AIS is declared if 3 consecutive V1 and V2 bytes are all-ones. VT AIS is removed when a valid VT pointer is received with valid SS-bits, with a NDF, or with 3 consecutive VT superframes having a valid VT pointer and valid SS-bits with no NDF.
	4	LOPS	**LOP Status:** When this bit a one, loss of pointer is currently being detected for this channel. LOP is entered with 8 consecutive NDF enables or invalid pointers. LOP is exited to normal if 3 consecutive valid VT pointers are received with valid SS-bits. LOP is exited to AIS if 3 consecutive all-ones pointers are received.
	3	RFIS	**RFI Status:** When this bit is a one, the receive failure indication has been de-bounced for 10 consecutive V5 bytes and is set for this channel. RFI is only a valid indication in Byte Synchronous modes of operation. This bit will clear if RFI is reset in 10 consecutive V5 bytes.
	2	UNES	**Unequipped Status:** This bit reflects the current status of the receive signal label for this channel (de-bounced for 5 consecutive V5 bytes) with respect to unequipped (signal label = 000). When this bit is a one, the incoming VT1.5 or TU-11 is unequipped. This bit will clear if 5 consecutive V5 bytes do not have an all-zero signal label.
	1	SLMS	**Signal Label Mismatch Status:** When this bit is set to a one, a mismatch has been de-bounced and detected for 5 consecutive V5 bytes between the expected signal label and the received signal label for this channel. A received or expected value of 'equipped non-specific' (signal label = 001) is not a mismatch for any non-zero signal label. This bit will clear if 5 consecutive V5 bytes match. An unequipped signal label (signal label = 000) received will cause this bit to be set unless the expected signal label (bits 6-4 of register X+07H) is set to unequipped.
	0	RDI-VS	**RDI-V Status:** When this bit is a one, a remote defect indication (from equipment that does not support Enhanced RDI) has been de-bounced for 5 or 10 consecutive V5 bytes and detected for this channel. This bit will clear if RDI is reset for 5 or 10 consecutive V5 bytes. RDID10 selects the de-bounce period.

Address*	Bit	Symbol	Description
X+12	7-3	R	**Reserved:** These bits have indeterminate status on read.
	2	RDI-VPDS	**RDI-VPD Status:** When this bit is set to one, a VT Remote Payload Defect Indication has been de-bounced for 5 or 10 consecutive Z7/K4 Bytes and detected for this channel. This bit will clear if RDI-VPD is not received for 5 or 10 consecutive Z7/K4 Bytes. RDID10 selects the de-bounce period.
	1	RDI-VSDS	**RDI-VSD Status:** When this bit is set to one, a VT Remote Server Defect Indication has been de-bounced for 5 or 10 consecutive Z7/K4 Bytes and detected for this channel. This bit will clear if RDI-VSD is not received for 5 or 10 consecutive Z7/K4 Bytes. RDID10 selects the de-bounce period.
	0	RDI-VCDS	**RDI-VCD Status:** When this bit is set to one, a VT Remote Connectivity Defect Indication has been de-bounced for 5 or 10 consecutive Z7/K4 Bytes and detected for this channel. This bit will clear if RDI-VCD is not received for 5 or 10 consecutive Z7/K4 Bytes. RDID10 selects the de-bounce period.
X+13	7-0	SPARE	**Spare:** This register should not be accessed.
X+14	7	XPE	**External Pin Event:** This bit will be set to one by the DS1MX7 when the active edge of the external pin (LAIS) for this channel (XPS), as determined by RISE and FALL, and the sense as determined by RXNRZP, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	6	DMPE	**Demap Error Event:** This bit will be set to one by the DS1MX7 when the active edge of a demap error for this channel (DMPS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	5	LOSE	**Loss of Signal Event:** This bit will be set to one by the DS1MX7 when the active edge of an LOS for this channel (LOSS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	4	MPE	**Map Error Event:** This bit will be set to one by the DS1MX7 when the active edge of a map error for this channel (MPS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	3	DAISE	**DS1 AIS Event:** This bit will be set to one by the DS1MX7 when the active edge of a DS1 AIS for this channel (DAISS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	2	RPOE	**Received Pointer Justification Counter Overflow Event:** This bit will be set to one by the DS1MX7 when the active edge of a received pointer justification counter overflow for this channel (RPOS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.

Address*	Bit	Symbol	Description
X+14 (cont.)	1	PGOE	**Generated Pointer Justification Counter Overflow Event:** This bit will be set to one by the DS1MX7 when the active edge of a generated pointer justification counter overflow for this channel (PGOS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	0	CVOE	**Code Violation Counter/CRC-6 Error Counter Overflow Event:** This bit will be set to one by the DS1MX7 when the active edge of a code violation counter/CRC-6 Error counter overflow for this channel (CVOS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
X+15	7	FEOE	**REI (FEBE) Counter Overflow Event:** This bit will be set to one by the DS1MX7 when the active edge of a REI (FEBE) counter overflow for this channel (FEOS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	6	BIPOE	**BIP-2 Error Counter Overflow Event:** This bit will be set to one by the DS1MX7 when the active edge of a BIP-2 error counter overflow for this channel (BIPOS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	5	VAISE	**VT AIS Event:** This bit will be set to one by the DS1MX7 when the active edge of a VT AIS for this channel (VAISS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	4	LOPE	**LOP Event:** This bit will be set to one by the DS1MX7 when the active edge of a LOP for this channel (LOPS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	3	RFIE	**RFI Event:** This bit will be set to one by the DS1MX7 when the active edge of an RFI for this channel (RFIS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	2	UNEE	**Unequipped Event:** This bit will be set to one by the DS1MX7 when the active edge of an unequipped signal label for this channel (UNES), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	1	SLME	**Signal Label Mismatch Event:** This bit will be set to one by the DS1MX7 when the active edge of a signal label mismatch for this channel (SLMS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	0	RDI-VE	**RDI-V Event:** This bit will be set to one by the DS1MX7 when the active edge of an RDI for this channel (RDI-VS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.

Address*	Bit	Symbol	Description
X+16	7-3	R	**Reserved:** These bits must be set to zeros.
	2	RDI-VPDE	**RDI-VPD Event:** This bit will be set to one when the active edge of an RDI-VPD for this channel (RDI-VPDS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	1	RDI-VSDE	**RDI-VSD Event:** This bit will be set to one when the active edge of an RDI-VSD for this channel (RDI-VSDS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
	0	RDI-VCDE	**RDI-VCD Event:** This bit will be set to one when the active edge of an RDI-VCD for this channel (RDI-VCDS), as determined by RISE and FALL, has occurred. This bit is cleared by writing a zero to this bit location or by T1SI if ENPMFM is set to one.
X+17	7-0	SPARE	**Spare:** This register should not be accessed.
X+18	7	XPPM	**External Pin Performance Monitor:** This bit will be set to one by the DS1MX7 if an external pin event (XPE) has occurred in the last one-second interval as defined by T1SI.
	6	DMPPM	**Demap Error Performance Monitor:** This bit will be set to one by the DS1MX7 if a demap error event (DMPE) has occurred in the last one-second interval as defined by T1SI.
	5	LOSPM	**Loss of Signal Performance Monitor:** This bit will be set to one by the DS1MX7 if an LOS event (LOSE) has occurred in the last one-second interval as defined by T1SI.
	4	MPPM	**Map Error Performance Monitor:** This bit will be set to one by the DS1MX7 if a map error event (MPE) has occurred in the last one-second interval as defined by T1SI.
	3	DAISPM	**DS1 AIS Performance Monitor:** This bit will be set to one by the DS1MX7 if a DS1 AIS event (DAISE) has occurred in the last one-second interval as defined by T1SI.
	2	RPOPM	**Received Pointer Justification Counter Overflow Performance Monitor:** This bit will be set to one by the DS1MX7 if a received pointer justification counter overflow event (RPOE) has occurred in the last one-second interval as defined by T1SI.
	1	PGOPM	**Generated Pointer Justification Counter Overflow Performance Monitor:** This bit will be set to one by the DS1MX7 if a generated pointer justification counter overflow event (PGOE) has occurred in the last one-second interval as defined by T1SI.
	0	CVOPM	**Code Violation Counter/CRC-6 Error Counter Overflow Performance Monitor:** This bit will be set to one by the DS1MX7 if a code violation counter/CRC-6 error counter overflow event (CVOE) has occurred in the last one-second interval as defined by T1SI.

Address*	Bit	Symbol	Description
X+19	7	FEOPM	**REI (FEBE) Counter Overflow Performance Monitor:** This bit will be set to one by the DS1MX7 if a REI (FEBE) counter overflow event (FEOE) has occurred in the last one-second interval as defined by T1SI.
	6	BIPOPM	**BIP-2 Error Counter Overflow Performance Monitor:** This bit will be set to one by the DS1MX7 if a BIP-2 counter overflow event (BIPOE) has occurred in the last one-second interval as defined by T1SI.
	5	VAISPM	**VT AIS Performance Monitor:** This bit will be set to one by the DS1MX7 if a VT AIS event (VAISE) has occurred in the last one-second interval as defined by T1SI.
	4	LOPPM	**LOP Performance Monitor:** This bit will be set to one by the DS1MX7 if an LOP event (LOPE) has occurred in the last one-second interval as defined by T1SI.
	3	RFIPM	**RFI Performance Monitor:** This bit will be set to one by the DS1MX7 if an RFI event (RFIE) has occurred in the last one-second interval as defined by T1SI.
	2	UNEPM	**Unequipped Performance Monitor:** This bit will be set to one by the DS1MX7 if an unequipped signal label event (UNEE) has occurred in the last one-second interval as defined by T1SI.
	1	SLMPM	**Signal Label Mismatch Performance Monitor:** This bit will be set to one by the DS1MX7 if a signal label mismatch event (SLME) has occurred in the last one-second interval as defined by T1SI.
	0	RDI-VPM	**RDI-V Performance Monitor:** This bit will be set to one by the DS1MX7 if an RDI event (RDI-VE) has occurred in the last one-second interval as defined by T1SI.
X+1A	7-3	R	**Reserved:** These bits have indeterminate status on read.
	2	RDI-VPDPM	**RDI-VPD Performance Monitor:** This bit will be set to one, if an RDI-VPD event (RDI-VPDE) has occurred in the last one-second interval as defined by T1SI.
	1	RDI-VSDPM	**RDI-VSD Performance Monitor:** This bit will be set to one, if an RDI-VSD event (RDI-VSDE) has occurred in the last one-second interval as defined by T1SI.
	0	RDI-VCDPM	**RDI-VCD Performance Monitor:** This bit will be set to one, if an RDI-VCD event (RDI-VCDE) has occurred in the last one-second interval as defined by T1SI.
X+1B	7-0	SPARE	**Spare:** This register should not be accessed.

Address*	Bit	Symbol	Description
X+1C	7	XPFM	**External Pin Fault Monitor:** This bit will be set to one by the DS1MX7 if an external pin event (XPE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	6	DMPFM	**Demap Error Fault Monitor:** This bit will be set to one by the DS1MX7 if a demap error event (DMPE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	5	LOSFM	**Loss of Signal Fault Monitor:** This bit will be set to one by the DS1MX7 if an LOS event (LOSE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	4	MPFM	**Map Error Fault Monitor:** This bit will be set to one by the DS1MX7 if a map error event (MPE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	3	DAISFM	**DS1 AIS Fault Monitor:** This bit will be set to one by the DS1MX7 if a DS1 AIS event (DAISE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	2	RPOFM	**Received Pointer Justification Counter Overflow Fault Monitor:** This bit will be set to one by the DS1MX7 if a received pointer justification counter overflow event (RPOE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	1	PGOFM	**Generated Pointer Justification Counter Overflow Fault Monitor:** This bit will be set to one by the DS1MX7 if a generated pointer justification counter overflow event (PGOE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	0	CVOFM	**Code Violation Counter/CRC-6 Error Counter Overflow Fault Monitor:** This bit will be set to one by the DS1MX7 if a code violation counter/CRC-6 error counter overflow event (CVOE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.

Address*	Bit	Symbol	Description
X+1D	7	FEOFM	**REI (FEBE) Counter Overflow Fault Monitor:** This bit will be set to one by the DS1MX7 if a REI (FEBE) counter overflow event (FEOE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	6	BIPOFM	**BIP-2 Error Counter Overflow Fault Monitor:** This bit will be set to one by the DS1MX7 if a BIP-2 error counter overflow event (BIPOE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	5	VAISFM	**VT AIS Fault Monitor:** This bit will be set to one by the DS1MX7 if a VT AIS event (VAISE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	4	LOPFM	**LOP Fault Monitor:** This bit will be set to one by the DS1MX7 if a LOP event (LOPE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	3	RFIFM	**RFI Fault Monitor:** This bit will be set to one by the DS1MX7 if an RFI event (RFIE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	2	UNEFM	**Unequipped Fault Monitor:** This bit will be set to one by the DS1MX7 if an unequipped signal label event (UNEE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	1	SLMFM	**Signal Label Mismatch Fault Monitor:** This bit will be set to one by the DS1MX7 if a signal label mismatch event (SLME) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	0	RDI-VFM	**RDI-V Fault Monitor:** This bit will be set to one by the DS1MX7 if an RDI event (RDI-VE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
X+1E	7-3	Reserved	**Reserved:** These bits have indeterminate status on read.
	2	RDI-VPDFM	**RDI-VPD Fault Monitor:** This bit will be set to one if an RDI-VPD event (RDI-VPDE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	1	RDI-VSDFM	**RDI-VSD Fault Monitor:** This bit will be set to one if an RDI-VSD event (RDI-VSDE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
	0	RDI-VCDFM	**RDI-VCD Fault Monitor:** This bit will be set to one if an RDI-VCD event (RDI-VCDE) is active but the transition to the active state has not occurred in the last one-second interval as defined by T1SI.
X+1F	7-0	SPARE	**Spare:** This register should not be accessed.

Address*	Bit	Symbol	Description
X+20	7	SHDAIS	**Signaling Highway DS1 AIS Status:** This bit is a one if a DS1 AIS indication is received from the signaling highway in Byte Synchronous mode only.
	6	SHYEL	**Signaling Highway Yellow:** This bit is a one if a DS1 Yellow indication is received from the signaling highway in Byte Synchronous mode only.
	5	R	**Reserved:** This bit reads out as zero.
	4, 3	RXSS1, RXSS0	**Received SS-bits:** These two bits represent the SS-bits (SS-bit 1 and SS-bit 0 respectively) received from the VT1.5 or TU-11 V1 and V2 bytes.
	2-0	RX Signal Label (2-0)	**Receive Signal Label:** These bits represent the signal label received from the V5 byte for this channel. Bits 2 through 0 correspond to bits 5 through 7 respectively of the V5 byte received from the Telecom Bus.
X+21	7-0	SPARE	**Spare:** This register should not be accessed.
X+22	7-0	CVC (7-0)/ CRC6(7-0)	**Line Code Violation Counter/CRC-6 Error Counter:** This is the lower byte of a 12-bit free running counter which will increment by one for each received line code violation. If excessive zeros counting is enabled (ENZC is set to one) they will also be counted with the line code errors. This counter can be cleared by writing its value to zero. If the counter overflows the CVOS and CVOE bits (plus CVOPM and CVOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at LCVC(7-0) and this counter is subsequently cleared for the next one-second interval. When CRC-6 (X+01H, bit 4) is set, this counter is used as the CRC-6 error counter lower byte in Byte Synchronous modes only.
X+23	7-4	R	**Reserved:** These bits must be set to zeros.
	3-0	CVC (11-8)/ CRC6(11-8)	**Line Code Violation Counter/CRC-6 Error Counter:** This is the upper nibble of a 12-bit free running counter which will increment by one for each received line code violation. If excessive zeros counting is enabled (ENZC is set to one) they will also be counted with the line code errors. This counter can be cleared by writing its value to zero. If the counter overflows the CVOS and CVOE bits (plus CVOPM and CVOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at LCVC(11-8) and this counter is subsequently cleared for the next one-second interval. When CRC-6 (X+01H, bit 4) is set, this counter is used as CRC-6 error counter upper nibble in Byte Synchronous modes only.

Address*	Bit	Symbol	Description
X+24	7-4	RX Ptr. Inc. Counter	**Pointer Increments Received Counter:** This four-bit counter represents the number of VT pointer increments received for this channel. This counter can be cleared by writing its value to zero. If the counter overflows the RPOS and RPOE bits (plus RPOPM and RPOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at address X+23H and this counter is subsequently cleared for the next one-second interval.
	3-0	RX Ptr. Dec. Counter	**Pointer Decrements Received Counter:** This four-bit counter represents the number of VT pointer decrements received for this channel. This counter can be cleared by writing its value to zero. If the counter overflows the RPOS and RPOE bits (plus RPOPM and RPOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at address X+23H and this counter is subsequently cleared for the next one-second interval.
X+25	7-4	Ptr. Inc. Gen. Counter	**Pointer Increments Generated Counter:** This four-bit counter represents the number of VT pointer increments generated by this channel for Byte Synchronous mode of operation. This counter can be cleared by writing its value to zero. If the counter overflows the PGOS and PGOE bits (plus PGOPM and PGOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at address X+24H and this counter is subsequently cleared for the next one-second interval.
	3-0	Ptr Dec. Gen. Counter	**Pointer Decrements Generated Counter:** This four-bit counter represents the number of VT pointer decrements received for this channel. This counter can be cleared by writing its value to zero. If the counter overflows the PGOS and PGOE bits (plus PGOPM and PGOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at address X+24H and this counter is subsequently cleared for the next one-second interval.
X+26	7-0	BEC (7-0)	**BIP-2 Error Counter:** This is the lower byte of a 12-bit free running counter. When control bit SDH is set to zero, it will increment by one for each BIP-2 error received. When SDH is set to one, it will increment block counts of BIP-2 errors. This counter can be cleared by writing its value to zero. If the counter overflows the BIPOS and BIPOE bits (plus BIPOPM and BIPOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at LBEC(7-0) and this counter is subsequently cleared for the next one-second interval.
X+27	7-4	R	**Reserved:** These bits must be set to zeros.
	3-0	BEC (11-8)	**BIP-2 Error Counter:** This is the upper nibble of a 12-bit free running counter. When control SDH is set to zero, it will increment by one for each BIP-2 error received. When SDH is set to one, it will increment block counts of BIP-2 errors. This counter can be cleared by writing its value to zero. If the counter overflows the BIPOS and BIPOE bits (plus BIPOPM and BIPOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at LBEC(11-8) and this counter is subsequently cleared for the next one-second interval.

Address*	Bit	Symbol	Description
X+28	7-0	FEC (7-0)	**REI (FEBE) Counter:** This is the lower byte of a 12-bit free running counter which will increment by one for each far end block error received. This counter can be cleared by writing its value to zero. If the counter overflows the FEOS and FEOE bits (plus FEOPM and FEOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at LFEC(7-0) and this counter is subsequently cleared for the next one-second interval.
X+29	7-4	R	**Reserved:** These bits must be set to zeros.
	3-0	FEC (11-8)	**REI (FEBE) Counter:** This is the upper nibble of a 12-bit free running counter which will increment by one for each far end block error received. This counter can be cleared by writing its value to zero. If the counter overflows the FEOS and FEOE bits (plus FEOPM and FEOFM bits if ENPMFM is set) will be set. If ENPMFM is set, this counter's latched value is updated every one-second at LFEC(11-8) and this counter is subsequently cleared for the next one-second interval.
X+2A	7-0	LCVC (7-0)/ LCRC6(7-0)	**Latched Line Code Violation Counter / CRC-6 Error Counter:** This is the lower byte of a 12-bit shadow register which is updated from the Line Code Violation Counter once a second. The one-second interval is derived from the external one-second input, T1SI. When CRC6 (X+01H, Bit 4) is set, this counter is used as CRC-6 error counter lower byte in Byte Synchronous modes only.
X+2B	7-4	R	**Reserved:** These bits must be set to zeros.
	3-0	LCVC (11-8)/ LCRC6(11-8)	**Latched Line Code Violation Counter / CRC-6 Error Counter:** This is the upper nibble of a 12-bit shadow register which is updated from the Line Code Violation Counter once a second. The one-second interval is derived from the external one-second input, T1SI. When CRC6 (X+01H, Bit 4) is set, this counter is used as CRC-6 error counter upper nibble in Byte Synchronous modes only.
X+2C	7-4	Latched RX Ptr. Inc. Counter	**Latched Pointer Increments Received Counter:** This is the 4-bit shadow register which is updated from the pointer increments received counter once a second. The one-second interval is derived from the external one-second input, T1SI.
	3-0	Latched RX Ptr. Dec. Counter	**Latched Pointer Decrements Received Counter:** This is the 4-bit shadow register which is updated from the pointer decrements received counter once a second. The one-second interval is derived from the external one-second input, T1SI.
X+2D	7-4	Latched Ptr. Inc. Gen. Counter	**Latched Pointer Increments Generated Counter:** This is the 4-bit shadow register which is updated from the pointer increments generated counter once a second. The one-second interval is derived from the external one-second input, T1SI.
	3-0	Latched Ptr Dec. Gen. Counter	**Latched Pointer Decrements Generated Counter:** This is the 4-bit shadow register which is updated from the pointer decrements generated counter once a second. The one-second interval is derived from the external one-second input, T1SI.

Address*	Bit	Symbol	Description
X+2E	7-0	LBEC (7-0)	**Latched BIP-2 Error Counter:** This is the lower byte of a 12-bit shadow register which is updated from the BIP-2 Error Counter once a second. The one-second interval is derived from the external one-second input, T1SI.
X+2F	7-4	R	**Reserved:** These bits must be set to zeros.
	3-0	LBEC (11-8)	**Latched BIP-2 Error Counter:** This is the upper nibble of a 12-bit shadow register which is updated from the BIP-2 Error Counter once a second. The one-second interval is derived from the external one-second input, T1SI.
X+30	7-0	LFEC (7-0)	**Latched REI (FEBE) Counter:** This is the lower byte of a 12-bit shadow register which is updated from the REI (FEBE) Counter once a second. The one-second interval is derived from the external one-second input, T1SI.
X+31	7-4	R	**Reserved:** These bits must be set to zeros.
	3-0	LFEC (11-8)	**Latched REI (FEBE) Counter:** This is the upper nibble of a 12-bit shadow register which is updated from the REI (FEBE) Counter once a second. The one-second interval is derived from the external one-second input, T1SI.
X+32	7-0	RXOB(7-0)	**Received O-bits:** Bits 3, 2, 1 and 0 are the first four O-bits (Byte following J2, Bits 3, 4, 5 and 6) incoming on DD(0-7). The second four O-bits (Byte following Z6/N2, Bits 3, 4, 5 and 6) are placed in Bits 7, 6, 5 and 4.
X+33	7-0	RXJ2(7-0)	**Received J2 Byte:** Bit 7 is Bit 1 of the J2 Byte incoming on DD(0-7). Bit 0 is Bit 8 of the J2 Byte.
X+34	7-0	RXZ6(7-0)	**Received Z6/N2 Byte:** Bit 7 is Bit 1 of the Z6/N2 Byte incoming on DD(0-7). Bit 0 is Bit 8 of the Z6/N2 Byte.
X+35	7-0	RXZ7(7-0)	**Received Z7/K4 Byte:** Bit 7 is Bit 1 of the Z7/K4 Byte incoming on DD(0-7). Bit 0 is Bit 8 of the Z7/K4 Byte.
X+36	7-0	TXOB(7-0)	**Transmit O-bits:** Bits 3, 2, 1 and 0 are the first four O-bits (Byte following J2, Bits 3, 4, 5 and 6). The second four O-bits (Byte following Z6/N2, Bits 3, 4, 5 and 6) are Bits 7, 6, 5 and 4. When OBAPEN is set to zero, the microprocessor–written data, in this location is output on AD(0-7). If OBAPEN is set to one, the O-bit information is taken from the Auxiliary Port and is output on AD(0-7). It is also written here for access by the microprocessor.
X+37	7-0	TXJ2(7-0)	**Transmit J2 Byte:** Bit 7 is Bit 1 of the J2 Byte and Bit 0 is the Bit 8 of the J2 Byte. When J2APEN is set to zero, the microprocessor-written data in this location, is output on AD(0-7). If J2APEN is set to one, the J2 information is taken from the Auxiliary Port and output on AD(0-7). It is also written here for access by the microprocessor.
X+38	7-0	TXZ6(7-0)	**Transmit Z6/N2 Byte:** Bit 7 is Bit 1 of the Z6/N2 Byte and Bit 0 is Bit 8 of the Z6/N2 Byte. When Z6APEN is set to zero, the microprocessor-written data, in this location, is output on AD(0-7). If Z6APEN is set to one, the Z6/N2 information is taken from the Auxiliary Port and output on AD(0-7). It is also written here for access by the microprocessor.

Address*	Bit	Symbol	Description
X+39	7-0	TXZ7(7-0)	**Transmit Z7/K4 Byte:** Bit 7 is Bit 1 of the Z7/K4 Byte and Bit 0 is Bit 8 of the Z7/K4 Byte. When Z7APEN is set to zero, the microprocessor–written data, in this location, is output on AD(0-7). If Z7APEN is set to one, the Z7/K4 information is taken from the Auxiliary Port and output on AD(0-7). It is also written here for access by the microprocessor. In either case, only bits 7-4 and 0 will appear in the output. Bits 1, 2 and 3 are controlled by the Transmit RDI circuity. For proper idle operation this register should be set to 00H.
X+3A	7-4	R	**Reserved:** These bits have indeterminate status on read.
	3	RGFEBE-V	**Ring Port REI (FEBE) Input:** This location contains the information input at the Ring Port. Control bit RINGEN (bit 4) in register X+0BH must be set to a one.
	2	RGRDI-VPD	**Ring Port Path Defect Input:** This location contains the information input at the Ring Port. Control bit RINGEN (bit 4) in register X+0BH must be set to a one.
	1	RGRDI-VSD	**Ring Port Server Defect Input:** This location contains the information input at the Ring Port. Control bit RINGEN (bit 4) in register X+0BH must be set to a one.
	0	RGRDI-VCD	**Ring Port Connectivity Defect Input:** This location contains the information input at the Ring Port. Control bit RINGEN (bit 4) in register X+0BH must be set to a one.
X+3B - X+3F	7-0	Reserved	**Reserved:** These registers should not be accessed.

APPLICATION DIAGRAMS

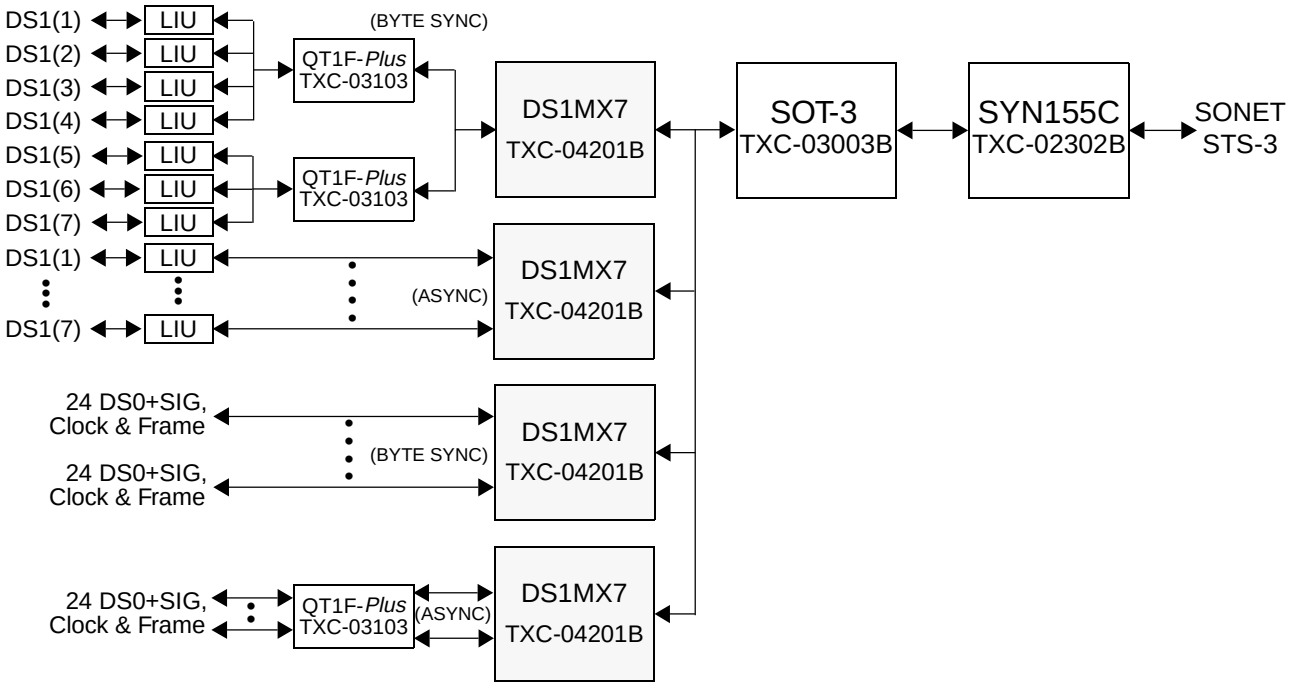


Figure 40. DS1MX7 TXC-04201B Applications

The Application diagram in Figure 40 shows four different uses for the DS1MX7. For SONET Byte Synchronous application the DS1MX7 connected to the QT1F-*Plus* provides for mapping seven DS1s Byte Synchronously. LIU control can be provided by either QT1F-*Plus* or DS1MX7. For Asynchronous mappings the DS1MX7 can connect directly to most commercial LIU devices and control them. Direct DS0 access is available for Byte Synchronous mappings (external slip buffers are required for common clocks across more than 24 DS0s). With the QT1F-*Plus*, DS0 access is also available from DS1s mapped asynchronously. Note that a single DS1MX7 can support all applications simultaneously.

The diagram in Figure 41 shows a direct Byte Synchronous to multichannel HDLC connection for Internet access. This diagram also depicts asynchronously mapped DS1 channels, which are mapped by the DS1MX7 from a framed DS1 signal, providing DS0 multiplexing into SONET for voice, data or video applications.**[**

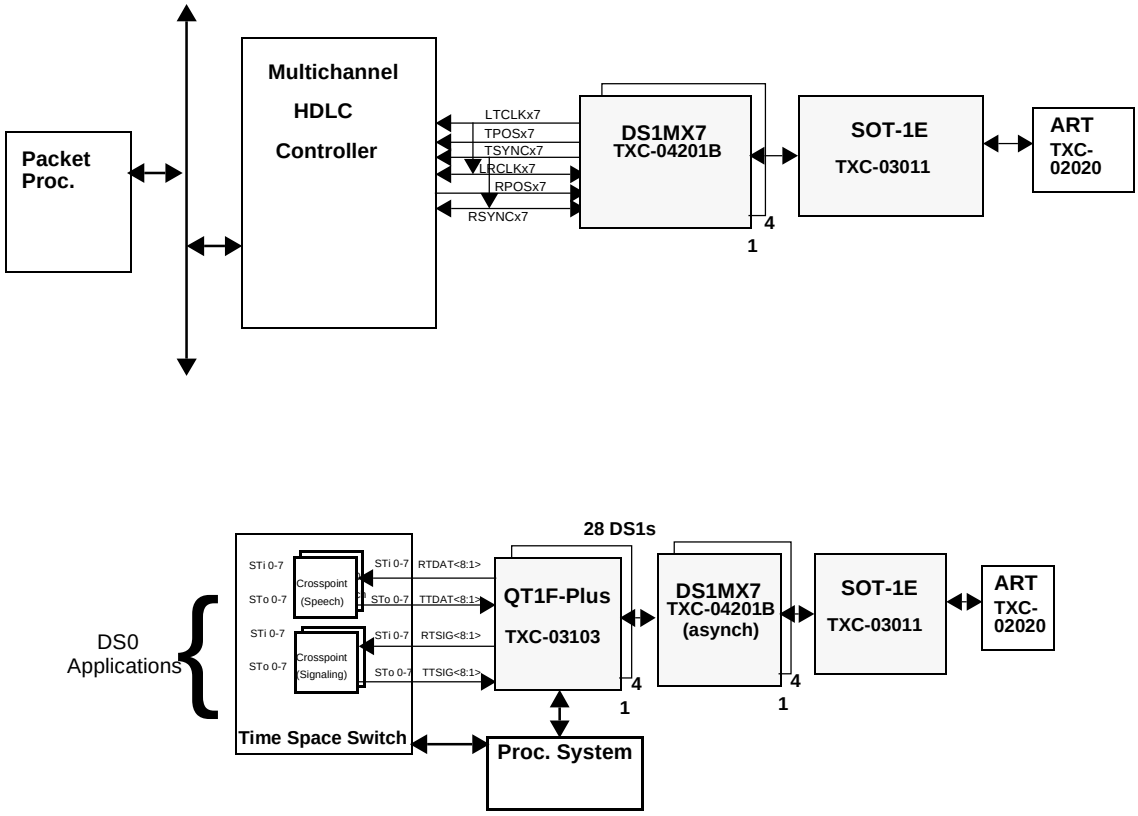


Figure 41. Multichannel HDLC and DS0 from Asynchronous DS1 Applications

The diagram in Figure 42 illustrates some uses of the DS1MX7 device to provide framing and DS0 access for a variety of DS1 sources. Direct control of most commercial line interface unit devices (LIUs) is provided.

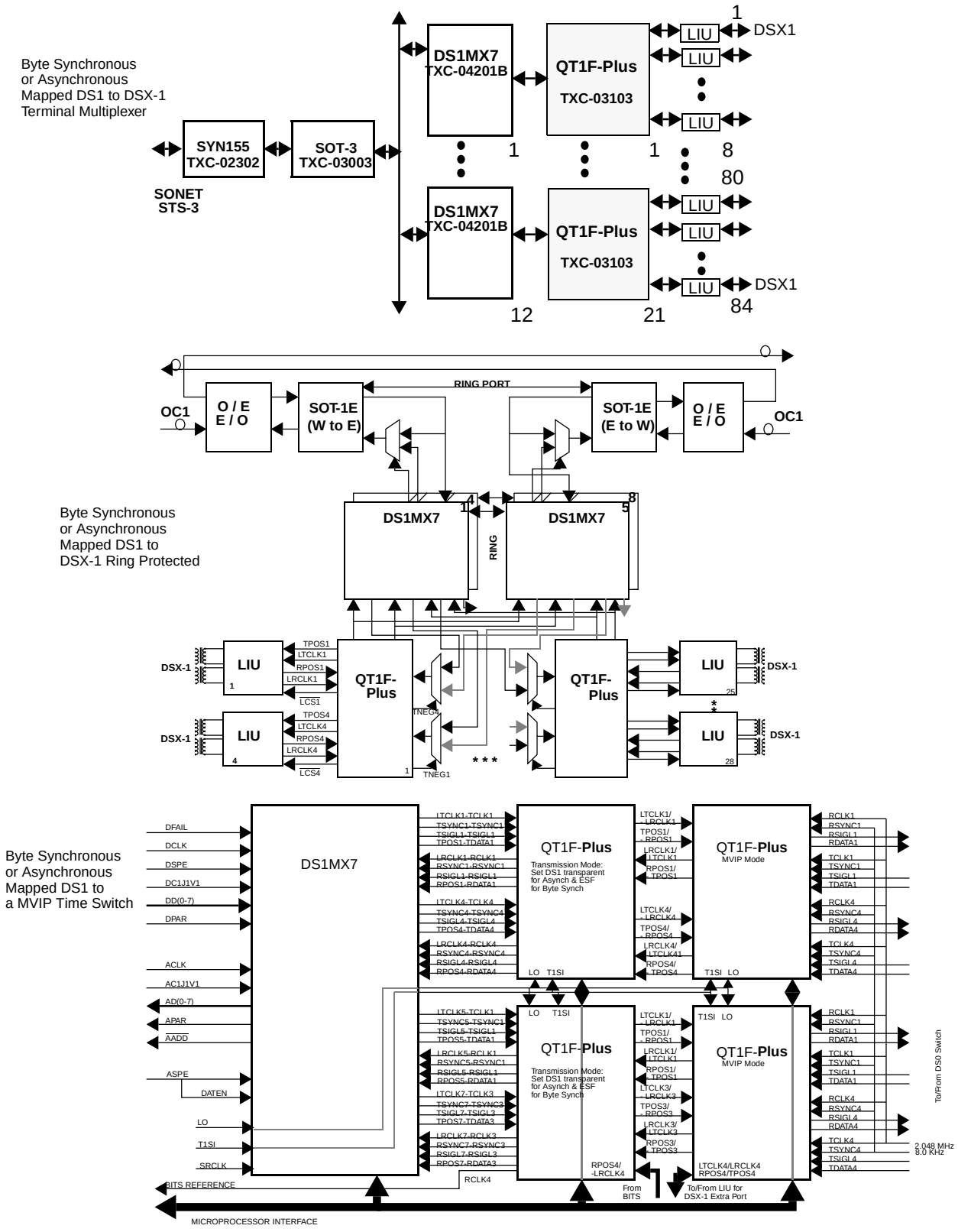


Figure 42. Some DS1MX7 TXC-04201B Byte Synchronous Applications

PACKAGE INFORMATION

The DS1MX7 device is packaged in a 208-pin plastic quad flat package (PQFP) suitable for surface mounting, as shown in Figure 43.

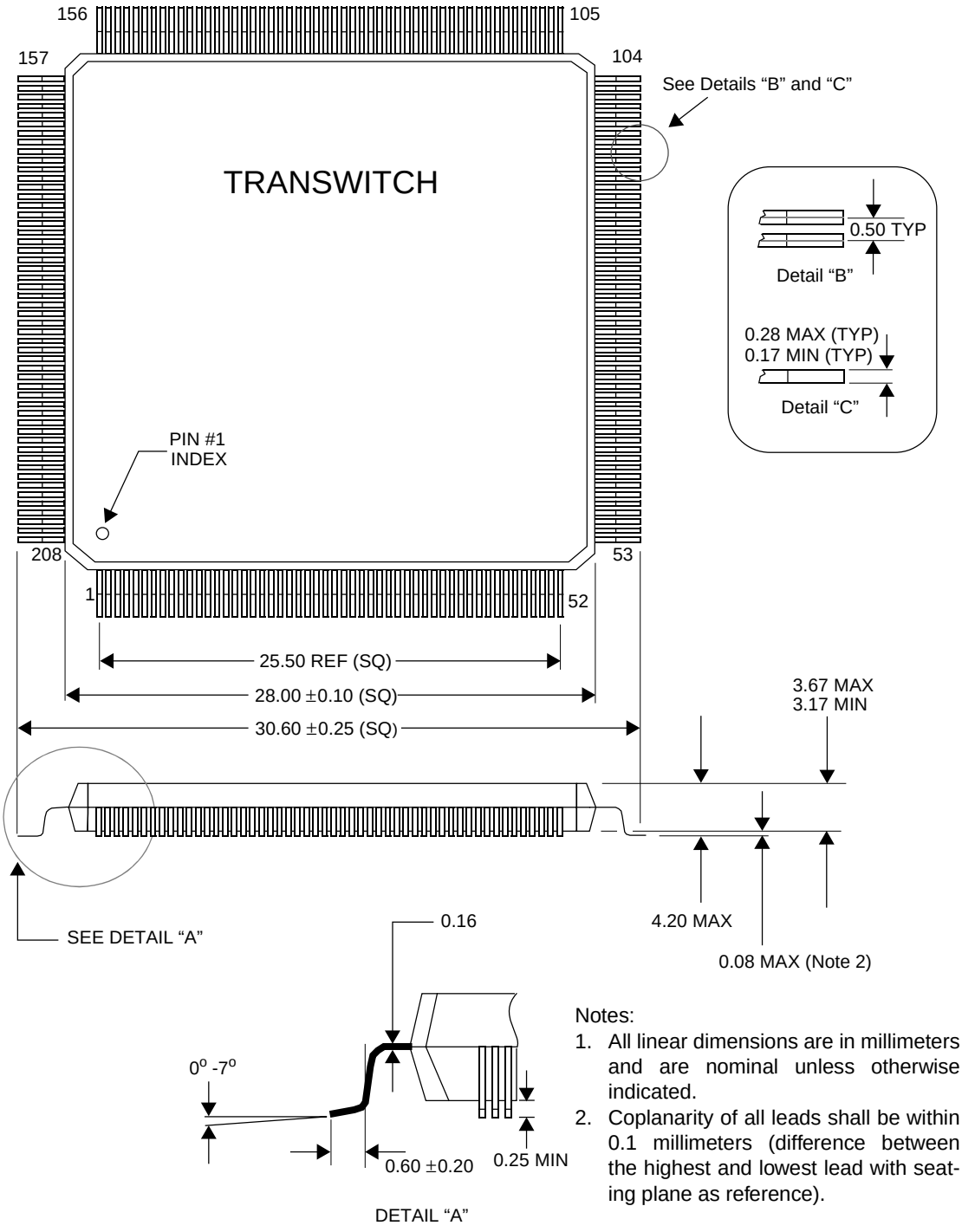


Figure 43. DS1MX7 TXC-04201B 208-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-04201-BIPQ 208-Pin Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus expanded features, in a larger package (68 pins instead of 44).

TXC-02301B, SYN155 VLSI Device (155-Mbit/s Synchronizer, Data Output only). Performs the complete SONET STS-3 or SDH STM-1 frame synchronization algorithm for 155.52 Mbit/s signals with byte/nibble-parallel to bit-serial conversion.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03001, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. Has programmable STS-1 or STS-N modes. This device is not recommended for use in new designs; TXC-03001B, TXC-03011 0r TXC-06101 should be used instead.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03001 device or to provide additional capabilities.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-T standards. This device is not recommended for use in new designs; TXC-03003B should be used instead.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03003 device or to provide additional capabilities.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). This device provides extended features relative to the 84-pin TXC-03001 and TXC-03001B SOT-1 devices, and it has a 144-pin package.

TXC-03102, QDS1F VLSI Device (Quad DS1 Framer). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. This device is not recommended for use in new designs; TXC-03103 should be used instead.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). The QT1F-*Plus* is a 4-channel DS1 framer designed for voice and data communications applications. AMI, B8ZS, and NRZ line codes are supported.

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals. This device is not recommended for use in new designs; TXC-03303 should be used instead.

TXC-03303, M13E VLSI Device, Extended features version of the TXC-03301 (M13).

TXC-04001, ADMA-T1 VLSI Device (DS1 to VT1.5 Async Mapper-Desync). Interconnects two DS1 signals with any two asynchronous mode VT1.5 virtual tributaries carried in a SONET STS-1 rate payload envelope. This device is not recommended for use in new designs; TXC-04001B should be used instead.

TXC-04001B, ADMA-T1 VLSI Device (Dual DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects two DS1 signals with any two asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-04251, QT1M VLSI Device (Quad T1 Mapper). Interconnects four T1 1.544 Mbit/s signals with any four asynchronous 1.5 virtual tributaries (VT1.5s) or Tributary Unit-11s (TU-11s) carried in a SONET/SDH STS-1, STS-3/AU-3 or STM-1 VC-4 signal.

TXC-05101C, HDLC VLSI Device (HDLC Controller, 36-Bit Terminal I/O). High Speed High Level Data Link Controller that sends and receives packets at line rates up to 51.84 Mbit/s using either a nibble, byte-parallel, or serial interface.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides features similar to the TXC-03011 SOT-1E device, and it operates at 3.3 volts.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multirate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

- NOTES -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