Audio/Video 60MHz 16 x 16 Crosspoint Switch

PRELIMINARY DATA SHEET

AD8113

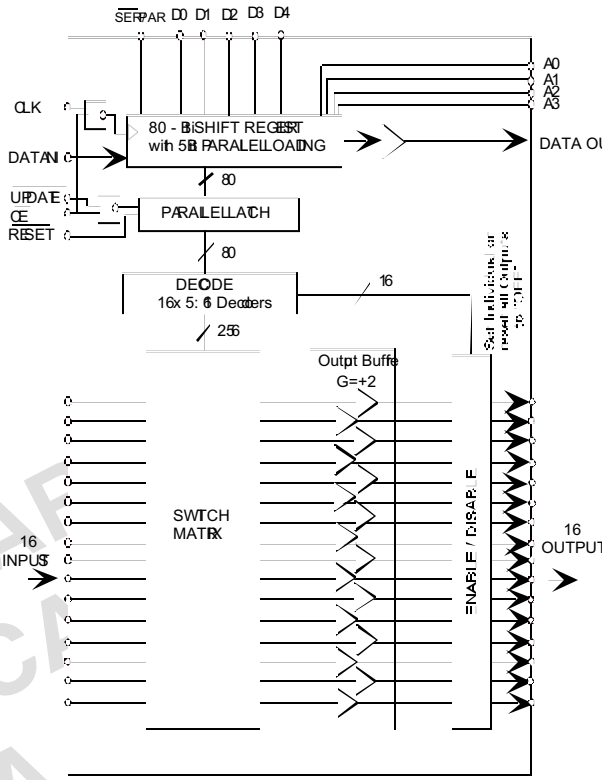
FEATURES

- 16 x 16 High Speed Non-Blocking Switch Array
- Serial or Parallel Programming of Switch Array
- Serial Data Out Allows "Daisy Chaining" Control of Multiple 16 x 16's to Create Larger Switch Arrays
- High Impedance Output Disable Allows Connection of Multiple Devices w/o Loading the Output Bus
- Complete Solution
  - Buffered Inputs
  - 16 Output Amplifiers, AD8113 (G=+2)
  - Operates on ±5V or ±12V supplies
  - Low Supply Current of 60 mA
- Excellent Audio Performance Vs = ±12V
  - ±10V Output Swing
  - 0.01% THD @ 20kHz Max., 20V p-p (R_L=600Ω)
- Excellent Video Performance Vs = ±5V
  - 10MHz 0.1dB Gain Flatness
  - 0.1%/0.1° Diff Gain/Diff Phase Error (R_L=150Ω)
- Excellent AC Performance
  - -3dB Bandwidth 60MHz
- Low All Hostile Crosstalk of
  - -100dB @ 20kHz, -55dB @ 5MHz
- Reset Pin Allows Disabling of All Outputs (Connected Through a Capacitor to Ground Provides "Power-On" Reset Capability)
- 100 Lead LQFP package (14mm x 14mm)

APPLICATIONS

- Analog/Digital Audio Routers
- Video Routers (NTSC, PAL, S, SECAM)
- Multimedia Systems
- Video Conferencing
- Ultrasound

FUNCTIONAL BLOCK DIAGRAM



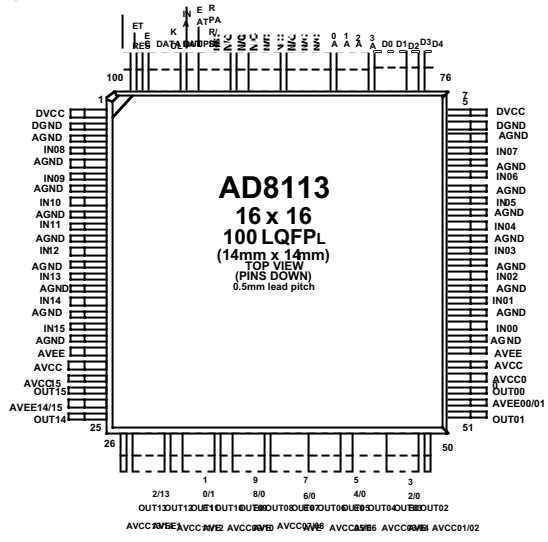


Figure 1. AD8113 Pin Assignment

PRODUCT DESCRIPTION

The AD8113 is a fully buffered crosspoint switch matrix that operates on ±12V for Audio applications and ±5V for Video applications. It offers a -3dB signal bandwidth greater than 60MHz and channel switch times of less than 60ns with 0.1% settling for use in both analog and digital audio. The AD8113 operated at 20kHz has crosstalk performance of -100dB and isolation of 100dB. In addition, ground/power pins surround all inputs and outputs to provide extra shielding for operatation in the most demanding audio routing applications. The differential gain and differential phase of better than 0.1% and 0.1° respectively along with 0.1dB flatness out to 10MHz make the AD8113 suitable for many video applications.

The AD8113 includes 16 independent output buffers which can be placed into a high impedance state for paralleling crosspoint outputs so that off channels do not load the output bus. The AD8113 has is a gain of +2. It operates on voltage supplies of ±5V or ±12V while consuming only 60mA of idle current at ±5V . The channel switching is performed via a serial digital control (which can accommodate "daisy chaining" of several devices) or via a parallel control allowing updating of an individual output without re-programing the entire array.

The AD8113 is packaged in an 100 lead LQFP package and is available over the extended commercial temperature range of 0°C to +70°C.

AD8113 SPECIFICATIONS (V_S=±12V, T_A=+25°C, R_L= 600Ω unless otherwise specified)

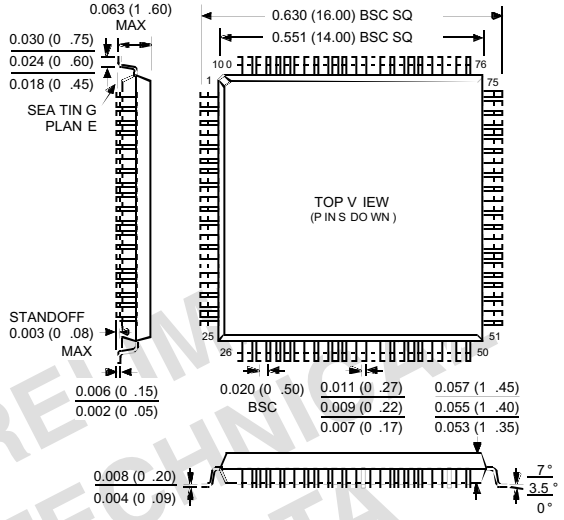
Parameter	Conditions	AD8113 Min	AD8113 Typ	AD8113 Max	Units
DYNAMIC PERFORMANCE					
-3dB Bandwidth	200mVp-p, R_L=600Ω,V_s= ±12V		60		MHz
	200mVp-p, R_L=150Ω, V_s= ±5V		40		MHz
	20Vp-p, R_L=600Ω,V_s= ±12V		20		MHz
Gain Flatness	0.1dB, 200mVp-p, R_L=150Ω, V_s= ±5V		10		MHz
Propagation Delay	2Vp-p, R_L=150Ω		TBD		ns
Settling Time	1% , 2V step, R_L=150Ω, V_s= ±5V		45		ns
Slew Rate	2V Step, R_L=150Ω, V_s= ±5V		100		V/µs
Slew Rate	20V Step, R_L=600Ω, V_s= ±12V		120		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL, R_L=1KΩ, V_s= ±5V		0.10		%
Differential Phase Error	NTSC or PAL, R_L=1KΩ, V_s= ±5V		0.10		Degrees
Total Harmonic Distortion	20KHz, R_L= 600Ω, 20Vp-p		0.002		%
Crosstalk , All Hostile	∨= 5MHz, V_s= ±5V, R_L=150Ω		-55		dB
	∨=20kHz		-100		dB
Off Isolation, Input-Output	∨=5MHz, R_L=150Ω, One Channel		-96		dB
	∨=20kHz, One Channel		-100		dB
Input Voltage Noise	20kHz		14		nV/ Hz
	0.1MHz - 10MHz		12		nV/ Hz
DC PERFORMANCE					
Gain Error	No Load, V_s= ±12V		TBD		%
	R_L=1KΩ, V_s= ±12V		TBD		%
	R_L=150Ω, V_s= ±5V		TBD		%
Gain Matching	No Load, Channel-Channel		TBD		%
	R_L=1KΩ, Channel-Channel		TBD		%
Gain Temperature Coefficient			TBD		ppm/°C
OUTPUT CHARACTERISTICS					
Output Impedance	DC, Enabled		0.1		Ω
	Disabled		4		KΩ
Output Disable Capacitance	Disabled		5		pF
Output Leakage Current	Disabled		1		µA
Output Voltage Range	V_s= ±5V, R_L=150Ω		±3		V
	V_s= ±12V, R_L=600Ω		±10		V
Voltage Range	Iout = 20mA, V_s= ±5V		±3		V
	Iout = 20mA, V_s= ±12V		TBD		V
	Short Circuit Current		55		mA
INPUT CHARACTERISTICS					
Input Offset Voltage	All Configurations		2		mV
	Temperature Coefficient		TBD		µV/°C
Input Voltage Range	No load, V_s= ±5V		±1.5		V
	V_s= ±12V		±5.0		V
Input Capacitance	Any Switch Configuration		4		pF
Input Resistance		1	10		MΩ
Input Bias Current	Any number of enabled Inputs		1		µA
SWITCHING CHARACTERISTICS					
Enable On Time			80		ns
Switching Time, 2V Step	50% UPDATE to 1% Settling		TBD		ns
Switching Transient(Glitch)			TBD		mVp-p
POWER SUPPLIES					
Supply Current	AVCC, Outputs Enabled, No Load		54		mA
	Outputs Disabled, V_s= ±12V		34		mA
	AVCC, Outputs Enabled, No Load		45		mA
	Outputs Disabled, V_s= ±5V		31		mA
	AVEE, Outputs Enabled, No Load		54		mA
	Outputs Disabled, V_s= ±12V		34		mA
	AVEE, Outputs Enabled, No Load		45		mA
	Outputs Disabled, V_s= ±5V		31		mA
	DVCC, Outputs Enabled, No Load		8		mA

AD8113 SPECIFICATIONS (V_s=±12V, T_A=+25°C, R_L= 600Ω unless otherwise specified)

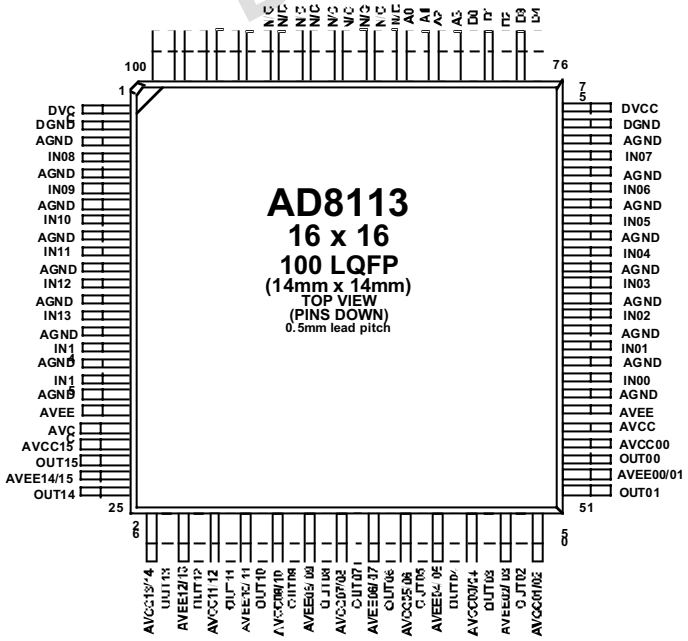
Parameter	Conditions	AD8113 Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
Supply Voltage Range	AVCC - AVEE		±4.5 to ±12.6		V
	DVCC		4.5 to 5.5		V
PSRR	DC	60	95		dB
	f=100kHz		70		dB
	f=1MHz		45		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (Still Air)		0 to +70		°C
θ_{JA}	Operating (Still Air)		40		°C/W
θ_{JC}	Operating (Still Air)		TBD		°C/W

OUTLINE DIMENSIONS

100-Lead Plastic Thin Quad Flatpack (LQFP)
(ST-100)



AD8113 PIN CONFIGURATION



THEORY OF OPERATION

The AD8113 is a gain of two crosspoint array with 16 outputs, each of which can be connected to any one of 16 inputs. Organized by output row, 16 switchable transconductance stages are connected to each output buffer, in the form of a 16-to-1 multiplexer. Each of the 16 rows of transconductance stages are wired in parallel to the 16 input pins, for a total array of 256 transconductance stages. Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The transconductance stages are NPN-input differential pairs, sourcing current into the folded cascode output stage. The compensation networks and emitter follower output buffers are in the output stage. Voltage feedback sets the gain at +2.

When operated with ±12 V supplies, this architecture provides ±10 V drive for 600 Ω audio loads with extremely low distortion (<0.01%) at audio frequencies. Provided the supplies are lowered to ±5 V (to limit power consumption), the AD8113 can drive reverse-terminated video loads, swinging ±2.5 V into 150 Ω. On-chip power consumption is minimized by disabling unused outputs and transconductance stages.

Features of the AD8113 facilitate the construction of larger switch matrices. The unused outputs can be disabled, leaving only a feedback network resistance of 4 kΩ on the output. This allows multiple ICs to be bussed together, provided the output load impedance is greater than minimum allowed values. Because no additional input buffering is necessary, high input resistance and low input capacitance are easily achieved without additional signal degradation.

The AD8113 inputs have a unique bias current compensation scheme that overcomes a problem common to transconductance input array architectures. Typically, input bias current increases as more and more transconductance stages connected to the same input are turned on. Anywhere from zero to sixteen inputs can be sharing one input pin, so there is a varying amount of bias current supplied through the source impedance driving the input. For audio systems with larger source impedances, this has the potential of creating large offset voltages, audible as “pops” when switching between channels. The AD8113 samples and cancels the input bias current contributions from each transconductance stage so that the residual bias current is nominally zero regardless of the number of enabled inputs.

Due to the flexibility in allowed supply voltages, internal crosstalk isolation clamps have variable bias levels. These levels were chosen to allow for the necessary input range to accommodate the full output swing with a gain of two. Overdriving the inputs beyond the device’s linear range will eventually forward-bias these clamps, increasing power dissipation. The valid input range for ±12 V supplies is ±5 V. The valid input range for ±5 V supplies is ±1.5 V. When outputs are disabled and being driven externally, the voltage applied to them should not exceed the valid output swing range for the AD8113. Exceeding ±10 V on the outputs of the AD8113 may apply a large differential voltage on the unused transconductance stages and should be avoided.

A flexible TTL-compatible logic interface simplifies the programming of the matrix. Both parallel and serial loading into a first rank of latches programs each output. A global latch simulateously updates all outputs. In serial mode, a serial-out pin allows devices to be daisy-chained together for single pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs. Regardless of the supply voltage applied to the AVCC and AVEE pins, the digital logic requires +5 V on the DVCC pin with respect to DGND. In order for the digital to analog interface to work properly, DVCC must be at least +7 V above AVEE. Finally, internal ESD protection diodes require that the DGND and AGND pins be at the same potential.

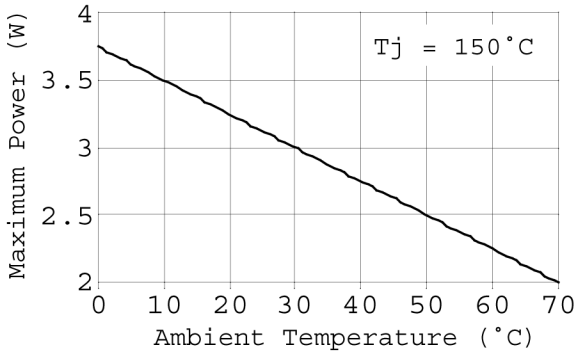
AD8113 POWER DISSIPATION

The AD8113 is operated with ±12V to ±5V supplies and can drive loads down to 600 Ω (±12V) or 150 Ω (±5V) , resulting in a large range of possible power dissipations. For this reason, extra care must be taken derating the operating conditions based on ambient temperature.

Packaged in a 100-lead LQFP, the junction-to-ambient thermal impedance (θ_{JA}) of the AD8113 is 40°*C/W*.

For long-term reliability, the maximum allowed junction temperature of the plastic-encapsulated die should

not exceed 150°*C*. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°*C* for an extended period can result in device failure. The following curve shows the range of allowed power dissipations that meet these conditions over the commercial range of ambient temperatures.



The above curve was calculated from

$$P_{d,max} = \frac{T_{junction,max} - T_{ambient}}{\theta_{ja}}$$

As an example, if the AD8113 is enclosed in a environment at 50°C (T_a), the total on-chip dissipation under all load and supply conditions must not be allowed to exceed 2.5 *W*.

When calculating on-chip power dissipation, it is necessary to include the rms current being delivered to the load, multiplied by the rms voltage drop on the AD8113 output devices. The dissipation of the on-chip 4 *k*Ω feedback resistor network must also be included. For the class-AB output, the on-chip power dissipation due to the load and feedback network is

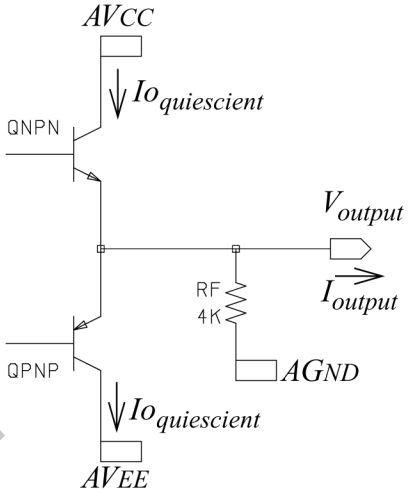
$$P_{d,output} = (AVcc - V_{output,rms}) \times I_{output,rms} + V_{output,rms}{}^2 / 4k\Omega$$

The user may subtract the quiescent current for the class AB output stage when calculating the loaded power dissipation. For each output stage driving a load, subtract a quiescent power according to

$$P_{dq,output} = (AVcc - AVee) \times I_{o,quiescient}$$

For the AD8113, $I_{o,quiescient}$ = 0.67 *mA*.

For each *disabled* output, the quiescent power supply current in *AVcc* and *AVee* drops by approximately 1.25 *mA*, although there is a power dissipation of $V_{out}{}^2/(4k\Omega)$ in the on-chip feedback resistors if the disabled output is being driven from an external source.



AD8113 simplified output stage

An example: AD8113, in an ambient temperature of 70°C, with all 16 outputs driving 6V$_{rms}$ into 600 Ω loads. Power supplies are ±12V.

Step 1: Calculate power dissipation of AD8113 using datasheet quiescient currents.

$$P_{d,quiescient} = (AVcc \times I_{AVcc}) + (AVee \times I_{AVee}) + (DVcc \times I_{DVdd})$$

$$P_{d,\,quiescient} = (12V \times 54mA) + (-12V \times -54mA) + (5V \times 9mA)$$

$$P_{d,\,quiescient} = 1.3W$$

Step 2: Calculate power dissipation from loads.

$$P_{d,output} = (AVcc - V_{output,rms}) \times I_{output,rms} + V_{output,rms}{}^2 / 4k\Omega$$

$$P_{d,\,output} = (12V - 6V) \times (6V/600\Omega) + 6V^2/4k\Omega = 69mW$$

There are 16 outputs, so

$$nP_{d,\,output} = 16 \times 69mW = 1.1W$$

Step 3: Subtract quiescient output current for number of loads (assumes output voltage >> 0.5V).

$$P_{dq,output} = (AVcc - AVee) \times I_{o,quiescient}$$

$$P_{dq,output} = [12v - (-12v)] \times 0.67mA = 16mW$$

There are 16 outputs, so

$$nP_{d,\,output} = 16 \times 16mW = 0.3W$$

Step 4: Verify that power dissipation does not exceed maximum allowed value.

$$P_{d,\,on-chip} = P_{d,\,quiescient} + nP_{d,\,output} - nP_{dq,output}$$

$$P_{d,\,on-chip} = 1.3W + 1.1W - 0.3W = 2.1W$$

From the figure or the equation, this power dissipation is below the maximum allowed dissipation for all ambient temperatures approaching 70˚*C*.

Note: It can be shown that for a dual supply of ±*a*, a class-AB output stage dissipates maximum power into a grounded load when the output voltage is *a/2*. So for a ±12V supply, the above example demonstrates the worse-case power dissipation into 600 Ω. It can be seen from this example that the minimum load resistance for ±12V operation is 600 Ω (for full rated operating temperature range). When operating with ±5V supplies, this load resistance may be lowered to 150 Ω. For larger safety margins, loads of 1 kΩ and greater are recommended.

Short Circuit Output Conditions

Although there is short circuit current protection on the AD8113 outputs, the output current can reach values of 70 *mA* into a grounded output. Any *sustained* operation with even one shorted output will exceed the maximum die temperature and can result in device failure.

Absolute Maximum Ratings[1]

Analog Supply Voltage (AVCC–AVEE) ..... 26.0 V

Digital Supply Voltage (DVCC–DGND) ..... 6 V

Ground Potential Difference (AGND–DGND) .... ±0.5 V

Internal Power Dissipation[2] ..... 3.1 W

Input Voltage[3] ..... maintain linear output

Output Voltage (disabled output) .....

.....(AVCC – 1.5 V) to (AVEE + 1.5 V)

Output Short Circuit Duration ..... momentary

Storage Temperature Range ..... –65˚C to +125˚C

Lead Temperature Range (soldering 10 sec) ... +300˚C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Specification is for device in free air (T_A = +25˚C): 100-lead plastic LQFP (ST): θ_{JA} = 40˚C/W

[3] To avoid differential input breakdown, in no case should any output voltage×0.5 and any input voltage be greater than 10V potential difference. See Output Voltage Swing specifications for linear output range.