18-Bit, 2.5 LSB INL, 800 kSPS SAR ADC

Preliminary Technical Data — AD7674

FEATURES

18 Bits Resolution with No Missing Codes
No Pipeline Delay (SAR architecture)
Differential Input Range: $\pm V_{REF}$ (V_{REF} up to 5V)
Throughput:
800 kSPS (Warp Mode)
666 kSPS (Normal Mode)
570 kSPS (Impulse Mode)
INL: ±2.5 LSB Max (±9.5 ppm of Full-Scale)
Dynamic Range : 103 dB Typ (V_{REF} = 5V)
S/(N+D): 100 dB Typ @ 2 kHz (V_{REF} = 5V)
THD: –115 dB Typ @ 2 kHz
Parallel (18,16 or 8bits bus) and Serial 5V/3V Interface
SPI/QSPI/MICROWIRE/DSP Compatible
On-board Reference Buffer
Single 5 V Supply Operation
Power Dissipation: 98 mW Typ @ 800 kSPS
68 mW @ 500 kSPS (Impulse)
136 µW @ 1 kSPS (Impulse)
Power-Down Mode: 7 µW Max
Package: 48-Lead Quad Flat Pack (LQFP)
48-Lead Frame Chip Scale Package (LFCSP)
Pin-to-Pin Compatible Upgrade of the AD7676/AD7678/ AD7679

APPLICATIONS

CT Scanners
High Dynamic Data Acquisition
Geophone and hydrophone sensor
Sigma-Delta replacement (low power, multichannel)
Instrumentation
Spectrum Analysis
Medical Instruments

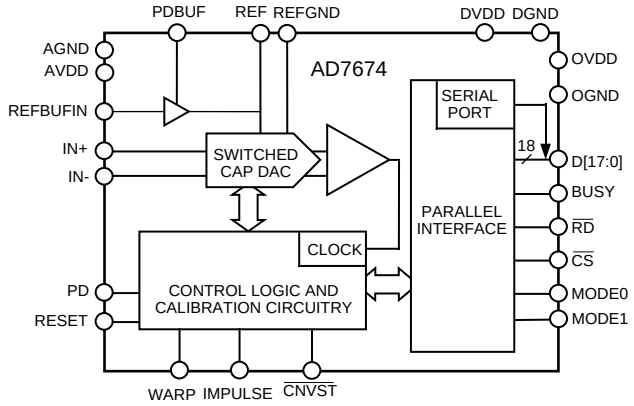
GENERAL DESCRIPTION

The AD7674 is a 18-bit, 800 kSPS, charge redistribution SAR, fully differential analog-to-digital converter that operates from a single 5 V power supply. The part contains a high-speed 18-bit sampling ADC, an internal conversion clock, an internal reference buffer, error correction circuits, and both serial and parallel system interface ports.

It features a very high sampling rate mode (Warp) and, for asynchronous conversion rate applications, a fast mode (Normal) and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput.

It is available in a 48-lead LQFP or a 48-lead LFCSP with operation specified from –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PulSAR Selection

Type / kSPS	100 - 250	500 - 570	800 - 1000
Pseudo Differential	AD7651 AD7660/61	AD7650/52 AD7664/66	AD7653 AD7667
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677
18 Bit	AD7678	AD7679	AD7674
Multichannel/ Simultaneous		AD7654 AD7655	

PRODUCT HIGHLIGHTS

1. High resolution and Fast Throughput
   The AD7674 is a 800 kSPS, charge redistribution, 18-bit SAR ADC (no latency).
2. Excellent accuracy
   The AD7674 has a maximum integral nonlinearity of 2.5 LSB with no missing 18-bit code.
3. Single-Supply Operation
   The AD7674 operates from a single 5 V supply and typically dissipates only 98 mW. In impulse mode, its power dissipation decreases with the throughput as 68mW at 500kSPS. It consumes 7 µW maximum when in power-down.
5. Serial or Parallel Interface
   Versatile parallel (18, 16 or 8 bits bus) or 2-wire serial interface arrangement compatible with both 3 V or 5 V logic.

REV. PrC

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AD7674–SPECIFICATIONS

(–40°C to +85°C, V_{REF} = 4.096V, AVDD = DVDD= 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	–0.1		AVDD	V
Analog Input CMRR	f_{IN} = TBD kHz		TBD		dB
Input Current	TBD kSPS Throughput		TBD		µA
Input Impedance			See Analog Input Section		
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1.25	µs
Throughput Rate	In Warp Mode	1		800	kSPS
Time Between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			1.5	µs
Throughput Rate	In Normal Mode	0		666	kSPS
Complete Cycle	In Impulse Mode			1.75	µs
Throughput Rate	In Impulse Mode	0		570	kSPS
DC ACCURACY					
Integral Linearity Error		–2.5		+2.5	LSB[1]
Differential Linearity Error		–1		+1.5	LSB
No Missing Codes		18			Bits
Transition Noise	V_{REF}=5V		0.7		LSB
Gain Error, T_{MIN} to T_{MAX}[2]				±TBD	% of FSR
Gain Error Temperature Drift			±TBD		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[2]			±TBD	±TBD	LSB
Zero Error Temperature Drift			±TBD		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±TBD		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 2 kHz, V_{REF}=5V		101		dB[3]
	V_{REF}=4.096V	98	99		dB
	f_{IN} = 10 kHz		TBD		dB
	f_{IN} = 100 kHz		TBD		dB
Dynamic range	$V_{IN+}=V_{IN-}=V_{REF}/2$=2.5V	101	103		dB
Spurious Free Dynamic Range	f_{IN} = 2 kHz		115		dB
	f_{IN} = 10 kHz		TBD		dB
	f_{IN} = 100 kHz		TBD		dB
Total Harmonic Distortion	f_{IN} = 2 kHz		–115		dB
	f_{IN} = 10 kHz		TBD		dB
	f_{IN} = 100 kHz		TBD		dB
Signal-to-(Noise+Distortion)	f_{IN} = 2 kHz,		100		dB
	f_{IN} = 2 kHz,–60 dB Input		40		dB
–3 dB Input Bandwidth			TBD		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			TBD		ps rms
Transient Response	Full-Scale Step			250	ns
Overvoltage recovery				250	ns
REFERENCE					
External Reference Voltage Range	REF	2.5	4.096	AVDD	V
REF Voltage with reference buffer	REFBUFIN = 2.5V	4.05	4.096	4.15	V
Reference Buffer Input Voltage Range	REFBUFIN	1.5	2.5	TBD	V
REFBUFIN Input Current		–1		+1	µA
REF Current Drain	800 kSPS Throughput		TBD		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.0		DVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format			Parallel or Serial 18-Bits		
Pipeline Delay			Conversion Results Available Immediately After Completed Conversion		
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = –500 µA	OVDD – 0.6			V

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		DVDD+0.3[4]	V
Operating Current[5]	800 kSPS Throughput				
AVDD			15		mA
DVDD[6]			4.5		mA
OVDD[6]			130		µA
Power Dissipation[6]	PDBUF low @500 kSPS[7]		73	TBD	mW
	PDBUF high @500 kSPS[7]		68		mW
	PDBUF high @1 kSPS[7]		136		µW
	PDBUF high @800 kSPS[5]		98		mW
	PDBUF low @800 kSPS[5]		103	TBD	mW
	In Power-Down Mode[8]			7	µW
TEMPERATURE RANGE[9]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[1]LSB means Least Significant Bit. With the ±4.096 V input range, one LSB is 31.25 µV.
[2]See Definition of Specifications section. These specifications do not include the error contribution from the external reference.
[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.
[4]The max should be the minimum of 5.25V and DVDD+0.3V.
[5]In warp mode.
[6]Tested in parallel reading mode.
[7]In impulse mode.
[8]With all digital inputs forced to DVDD or DGND respectively.
[9]Contact factory for extended temperature range.

Specifications subject to change without notice.

TIMING SPECIFICATIONS

(–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

	Symbol	Min	Typ	Max	Unit
REFER TO FIGURES 12 AND 13					
Convert Pulsewidth	t_1	5			ns
Time Between Conversions (Warp Mode/Normal Mode/Impulse Mode)	t_2	1.25/1.5/1.75		Note 1	µs
$\overline{CNVST}$ LOW to BUSY HIGH Delay	t_3			30	ns
BUSY HIGH All Modes Except in Master Serial Read After Convert (Warp Mode/Normal Mode/Impulse Mode)	t_4			1/1.25/1.5	µs
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t_7			1/1.25/1.5	µs
Acquisition Time	t_8	250			ns
RESET Pulsewidth	t_9	10			ns
REFER TO FIGURES 14, 15, AND 16 (Parallel Interface Modes)					
$\overline{CNVST}$ LOW to Data Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{10}			1/1.25/1.5	µs
Data Valid to BUSY LOW Delay	t_{11}	45			ns
Bus Access Request to Data Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	5		15	ns

TIMING SPECIFICATIONS (continued)

	Symbol	Min	Typ	Max	Unit
REFER TO FIGURES 18 AND 19 (Master Serial Interface Modes)[2]					
$\overline{CS}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ LOW to Internal SCLK Valid Delay	t_{15}			10	ns
$\overline{CS}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ LOW to SYNC Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{17}		25/275/525		ns
SYNC Asserted to SCLK First Edge Delay[3]	t_{18}	3			ns
Internal SCLK Period[3]	t_{19}	25		40	ns
Internal SCLK HIGH[3]	t_{20}	12			ns
Internal SCLK LOW[3]	t_{21}	7			ns
SDOUT Valid Setup Time[3]	t_{22}	4			ns
SDOUT Valid Hold Time[3]	t_{23}	2			ns
SCLK Last Edge to SYNC Delay[3]	t_{24}	3			
$\overline{CS}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{CS}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{CS}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert[3]	t_{28}		See Table I		µs
$\overline{CNVST}$ LOW to SYNC Asserted Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{29}		1/1.25/1.5		µs
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
REFER TO FIGURES 20 AND 22 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		18	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

NOTES

[1]In warp mode only, the maximum time between conversions is 1ms; otherwise, there is no required maximum time.

[2]In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.

[3]In serial master read during convert mode. See Table I for serial master read after convert mode.

Specifications subject to change without notice.

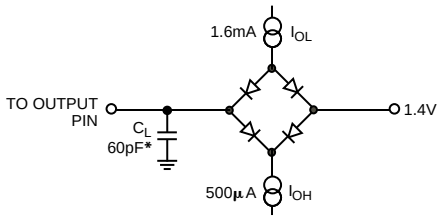
Table I. Serial clock timings in Master Read after Convert

DIVSCLK[1] / **DIVSCLK[0]**		**0** / **0**	**0** / **1**	**1** / **0**	**1** / **1**	**unit**
SYNC to SCLK First Edge Delay Minimum	t_{18}	3	17	17	17	ns
Internal SCLK Period minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period Maximum	t_{19}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{21}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	89	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	60	140	300	ns
Busy High Width Maximum (Warp)	t_{28}	1.75	2.25	3.25	5.5	µs
Busy High Width Maximum (Normal)	t_{28}	2	2.5	3.5	5.8	µs
Busy High Width Maximum (Impulse)	t_{28}	2.25	2.75	3.75	6	µs

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
IN+[2], IN-[2], REF, REFBUFIN, REFGND to AGND
. . . . . AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences
AGND, DGND, OGND . . . . . ±0.3 V
Supply Voltages
AVDD, DVDD, OVDD . . . . . -0.3V to +7 V
AVDD to DVDD, AVDD to OVDD . . . . . ±7 V
DVDD to OVDD . . . . . -0.3V to +7 V
Digital Inputs . . . . . –0.3 V to DVDD + 0.3V
Internal Power Dissipation[3] . . . . . 700 mW
Internal Power Dissipation[4] 2.5W
Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]See Analog Input section.
[3]Specification is for device in free air: 48-Lead LQFP: θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[4]Specification is for device in free air: 48-Lead LFCSP: θ_{JA} = 26°C/W.



*IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDOUT TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 60pF MAXIMUM.

Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

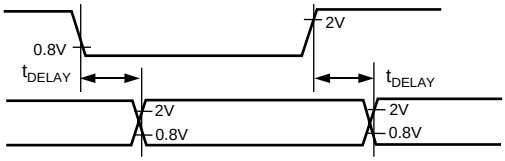


Figure 2. Voltage Reference Levels for Timing

ORDERING GUIDE

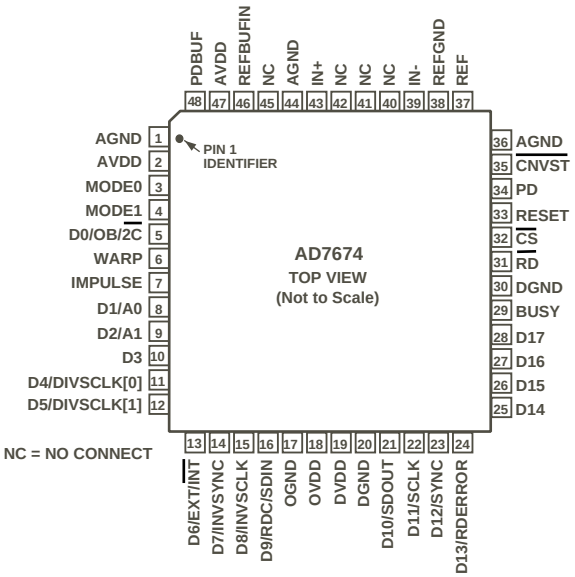
Model	Temperature Range	Package Description	Package Option
AD7674AST	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7674ASTRL	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7674ACP	–40°C to +85°C	Chip Scale (LFCSP)	CP-48
AD7674ACPRL	–40°C to +85°C	Chip Scale (LFCSP)	CP-48
EVAL-AD7674CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	

NOTES
[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.
[2]This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7674 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
48-Lead LQFP and 48-Lead LFCSP
(ST-48 and CP-48)



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1, 44	AGND	P	Analog Power Ground Pin.
2, 47	AVDD	P	Input Analog Power Pins. Nominally 5 V.
40–42,45	NC		No Connect.
3	MODE0	DI	Data Output Interface mode Selection.
4	MODE1	DI	Data Output Interface mode Selection:
5	D0/OB/$\overline{2C}$	DI/O	When MODE=0 (18 bit interface mode), this pin is Bit 0 of the parallel port data output bus and the data coding is straight binary. In all other modes, this pin allows choice of Straight Binary/Binary Two's Complement.When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a two's complement output from its internal shift register.
6	WARP	DI	Conversion mode selection. When HIGH and IMPULSE LOW, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
7	IMPULSE	DI	Conversion mode selection. When HIGH and WARP LOW, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	D1/A0	DI/O	When MODE=0 (18-bit interface mode), this pin is Bit 1 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table II.
9	D2/A1	DI/O	When MODE=0 or MODE=1 (18-bit or 16-bit interface mode), this pin is Bit 2 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table II.
10	D3	DO	In all modes except MODE=3, this output is used as Bit 3 of the Parallel Port Data Output Bus. This pin is always an output regard less of the interface mode.
11,12	D[4:5]or	DI/O	In all modes except MODE=3, these pins are Bit 4 and Bit 5 of the Parallel Port Data Output Bus.
	DIVSCLK[0:1]		In MODE=3 (serial mode), when EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW, which is serial master read after convert, these inputs, part of the serial port, are used to slow down if desired the internal serial clock which clocks the data output. In other serial modes, these pins are not used.
13	D6	DI/O	In all modes except MODE=3, this output is used as Bit 6 of the Parallel Port Data Output Bus.
	or EXT/$\overline{INT}$		When MODE=3 (serial mode), this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D7	DI/O	In all modes except MODE=3, this output is used as Bit 7 of the Parallel Port Data Output Bus.
	or INVSYNC		When MODE=3 (serial mode), this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D8	DI/O	In all modes except MODE=3, this output is used as Bit 8 of the Parallel Port Data Output Bus.
	or INVSCLK		When MODE=3 (serial mode), this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	D9	DI/O	In all modes except MODE=3, this output is used as Bit 9 of the Parallel Port Data Output Bus.
	or RDC/SDIN		When MODE=3 (serial mode), this input, part of the serial port, is used as either an

Interface MODE #	MODE0	MODE1	Description
0	0	0	18-bit Interface
1	0	1	16-bit Interface
2	1	0	Byte Interface
3	1	1	Serial Interface

Pin No.	Mnemonic	Type	Description
			external data input or a read mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 18 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply than the supply of the host interface (5 V or 3 V). Should not exceed DVDD by more than 0.3V.
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground.
21	D10	DO	In all modes except MODE=3, this output is used as Bit 10 of the Parallel Port Data Output Bus.
	or SDOUT		When MODE=3 (serial mode), this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7674 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/$\overline{2C}$. In serial mode, when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when EXT/$\overline{INT}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D11	DI/O	In all modes except MODE=3, this output is used as the Bit 11 of the Parallel Port Data Output Bus.
	or SCLK		When MODE=3 (serial mode), this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D12	DO	In all modes except MODE=3, this output is used as the Bit 12 of the Parallel Port Data Output Bus.
	or SYNC		When MODE=3 (serial mode), this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	D13	DO	In all modes except MODE=3, this output is used as the Bit 11 of the Parallel Port Data Output Bus.
	or RDERROR		In MODE=3 (serial mode) and when EXT/$\overline{INT}$ is HIGH, this output, part of the serial port, is used as a incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25–28	D[14:17]	DO	Bit 14 to Bit 17 of the Parallel Port Data output bus. These pins are always outputs regard less of the interface mode.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must be tied to digital ground.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7674. Current conversion if any is aborted. If not used, this pin could be tied to DGND.

Pin No.	Mnemonic	Type	Description
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{CNVST}$	DI	Start Conversion. A falling edge on $\overline{CNVST}$ puts the internal sample/hold into the hold state and initiates a conversion. In impulse mode (IMPULSE HIGH and WARP LOW), if $\overline{CNVST}$ is held LOW when the acquisition phase (t_8) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
36	AGND	P	Must be tied to analog ground.
37	REF	AI	Reference Input Voltage and Internal Reference Buffer Output. Apply an external reference on this pin if the internal reference buffer is not used. Should be decoupled effectively with or without the internal buffer.
38	REFGND	AI	Reference Input Analog Ground.
39	IN-	AI	Differential Negative Analog Input.
43	IN+	AI	Differential Negative Analog Input.
46	REFBUFIN	AI	Reference Buffer Input Voltage. The internal reference buffer has a fixed gain. It outputs 4.096V typically when 2.5V is applied on this pin.
48	PDBUF	DI	Allows choice of buffering reference. When LOW, the buffer is selected. When HIGH, the buffer is switched off.

NOTES
AI = Analog Input
AI/O = Bidirectional Analog
AO = Analog Output
DI = Digital Input
DI/O = Bidirectional Digital
DO = Digital Output
P = Power

Table II. Data Bus Interface Definition

MODE	MODE0	MODE1	D0/OB/$\overline{2C}$	D1/A0	D2/A1	D[3]	D[4:9]	D[10:11]	D[12:15]	D[16:17]	DESCRIPTION
0	0	0	R[0]	R[1]	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	18-Bit Parallel
1	0	1	OB/$\overline{2C}$	A0:0	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	16-Bit High Word
1	0	1	OB/$\overline{2C}$	A0:1	R[0]	R[1]	All Zeros				16-Bit Low Word
2	1	0	OB/$\overline{2C}$	A0:0	A1:0	All Hi-Z		R[10:11]	R[12:15]	R[16:17]	8-Bit HIGH Byte
2	1	0	OB/$\overline{2C}$	A0:0	A1:1	All Hi-Z		R[2:3]	R[4:7]	R[8:9]	8-Bit MID Byte
2	1	0	OB/$\overline{2C}$	A0:1	A1:0	All Hi-Z		R[0:1]	All Zeros		8-Bit LOW Byte
2	1	0	OB/$\overline{2C}$	A0:1	A1:1	All Hi-Z		All Zeros		R[0:1]	8-Bit LOW Byte
3	1	1	OB/$\overline{2C}$	All Hi-Z		Serial Interface					Serial Interface

R[0:17] is the 18-bit ADC value stored in its output register.

DEFINITION OF SPECIFICATIONS

Integral nonlinearity error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale". The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential nonlinearity error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain error
The first transition (from 000 . . . 00 to 000 . . . 01) should occur for an analog voltage 1/2 LSB above the nominal –full scale (-4.095991 V for the ±4.096V range). The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (4.095977 V for the ±4.096V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero error
The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Spurious free dynamic range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective number of bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = (S/[N+D]_{dB} - 1.76)/6.02)$$

and is expressed in bits.

Total harmonic distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

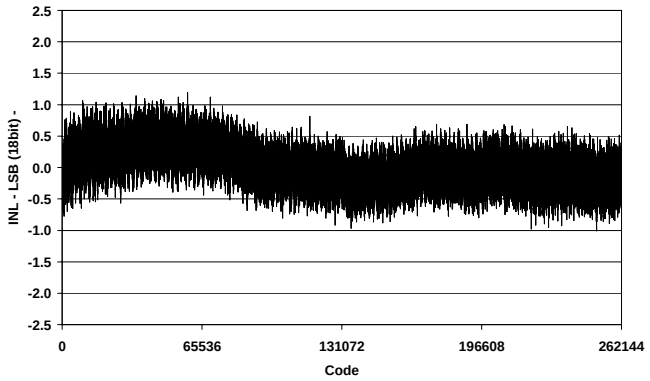
Signal-to-noise ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal to (noise + distortion) ratio (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

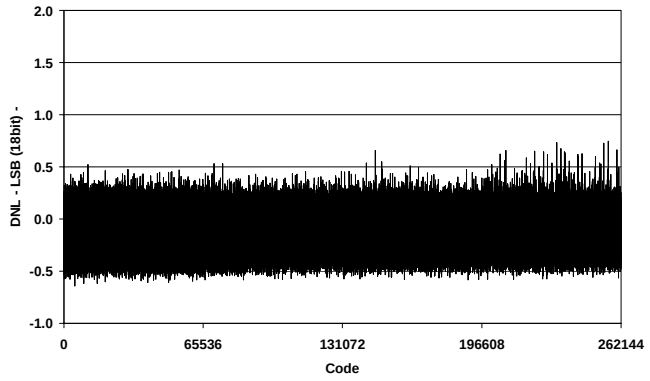
Aperture delay
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{CNVST}$ input to when the input signal is held for a conversion.

Transient response
The time required for the AD7674 to achieve its rated accuracy after a full-scale step function is applied to its input.

Typical Performance Characteristics- AD7674



TPC 1. Integral Nonlinearity vs. Code



TPC 4. Differential Nonlinearity vs. Code

To Be Supplied

TPC 2. Histogram of 131,072 Conversions of a DC Input at the Code Transition

To Be Supplied

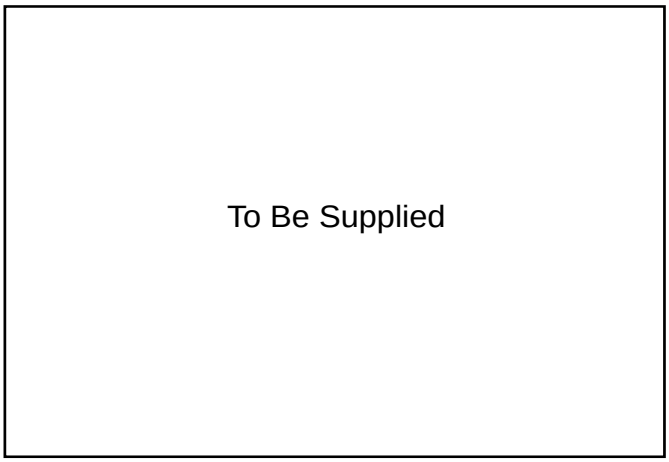
TPC 5. Histogram of 131,072 Conversions of a DC Input at the Code Center

To Be Supplied

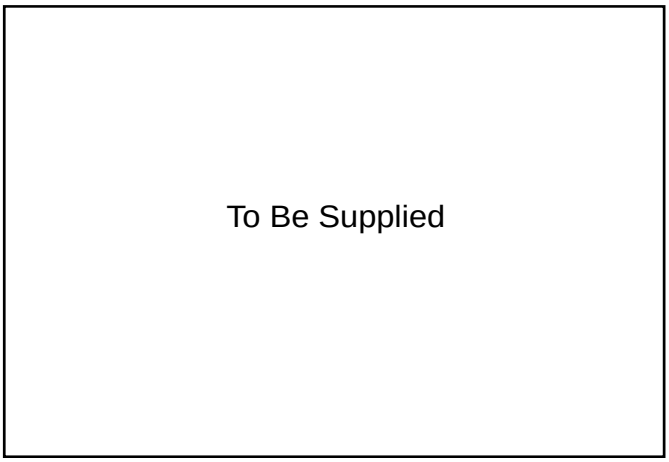
TPC 3. Typical Positive INL Distribution (TBD Units)

To Be Supplied

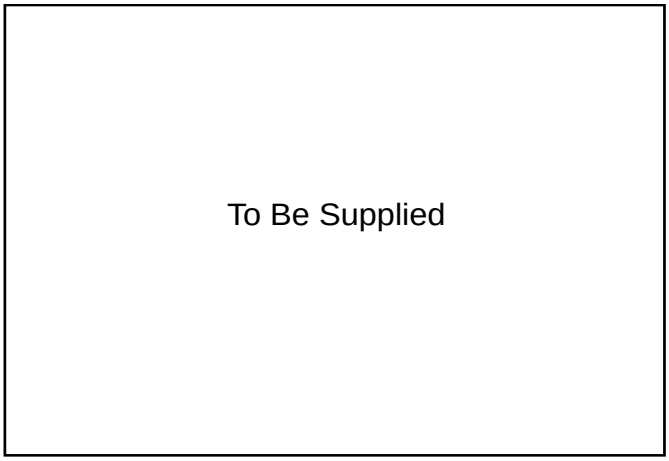
TPC 6. Typical Negative INL Distribution (TBD Units)



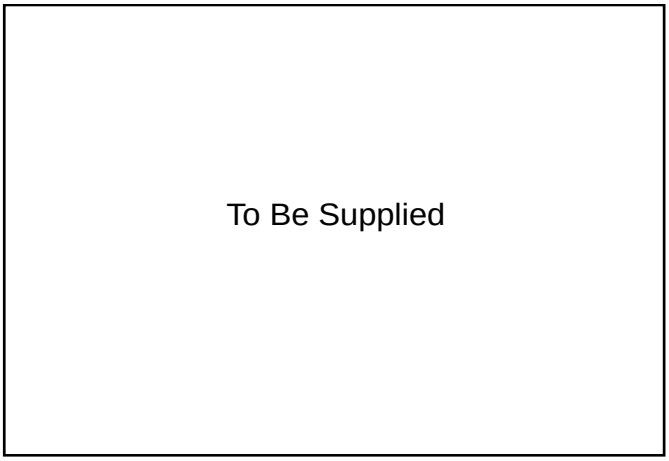
TPC 7. Typical INL and DNL vs Temperature



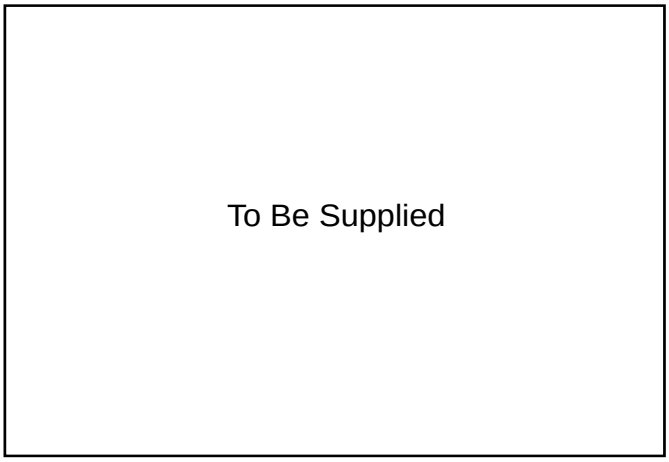
TPC 10. Typical INL and DNL vs Sampling rate



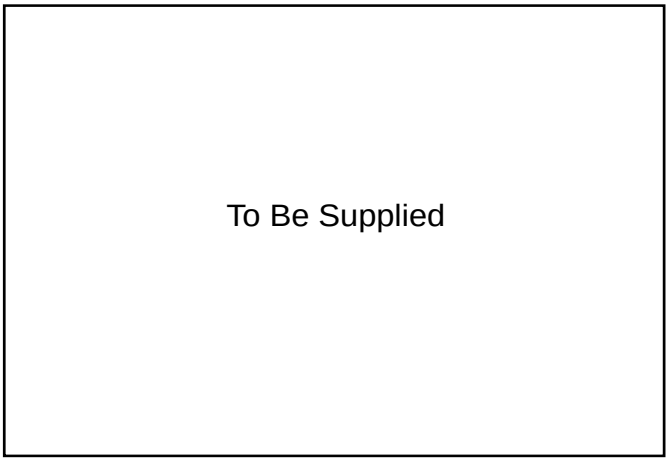
TPC 8. FFT



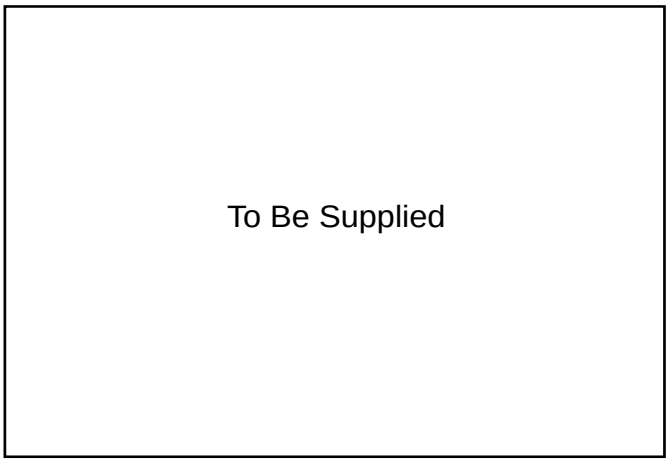
TPC 11. SNR, S/(N+D) and ENOB vs. Frequency



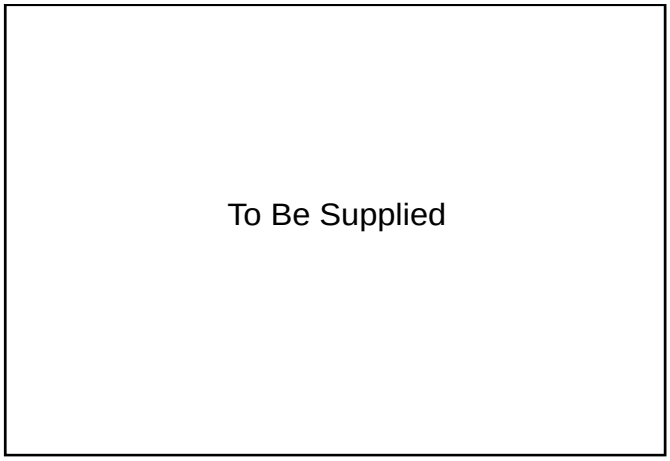
TPC 9. FFT after digital filtering



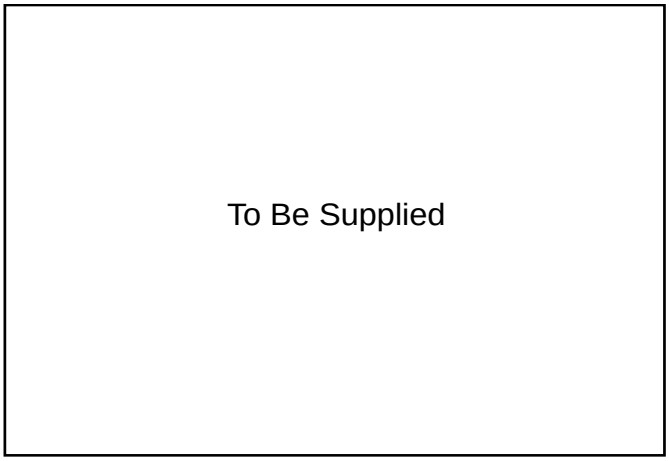
TPC 12. THD, SFDR and Harmonics vs. Frequency



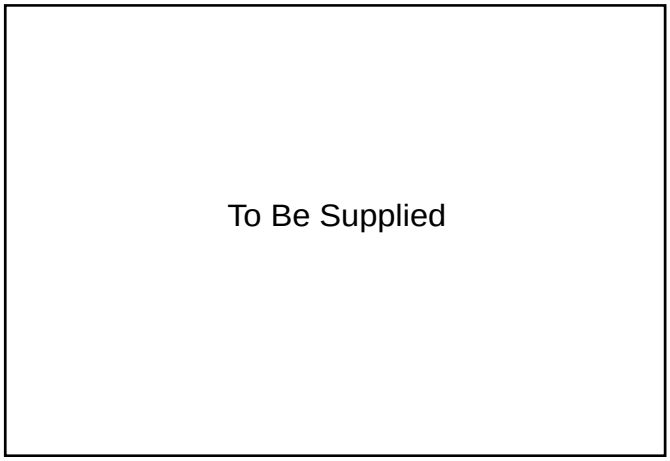
TPC 13. SNR, S/(N+D) and THD vs. Input Level



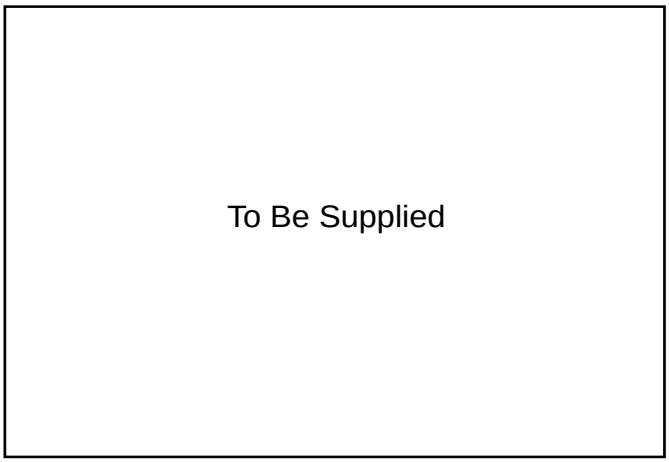
TPC 16.Operating Current vs. Sampling Rate



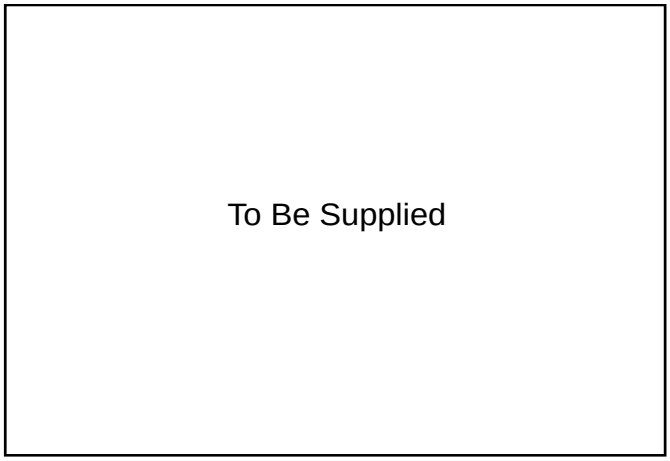
TPC 14. SNR, S/(N+D) and ENOB vs Temperature



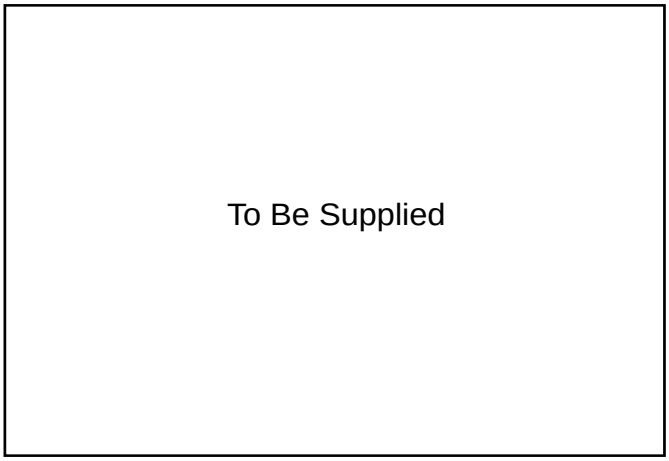
TPC 17. Power-Down Operating Currents vs. Temperature



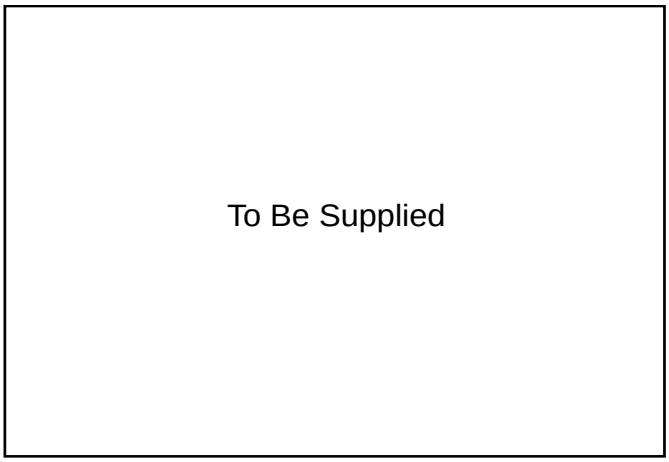
TPC 15. THD, SFDR and Harmonics vs Temperature



TPC 18. Positive and Negative Full Scale, Offset and Reference Buffer Gain vs. Temperature



TPC 19.Positive and Negative Full Scale, Offset and Reference Buffer Gain vs. Supply .



TPC 20.Typical Delay vs. Load Capacitance CL

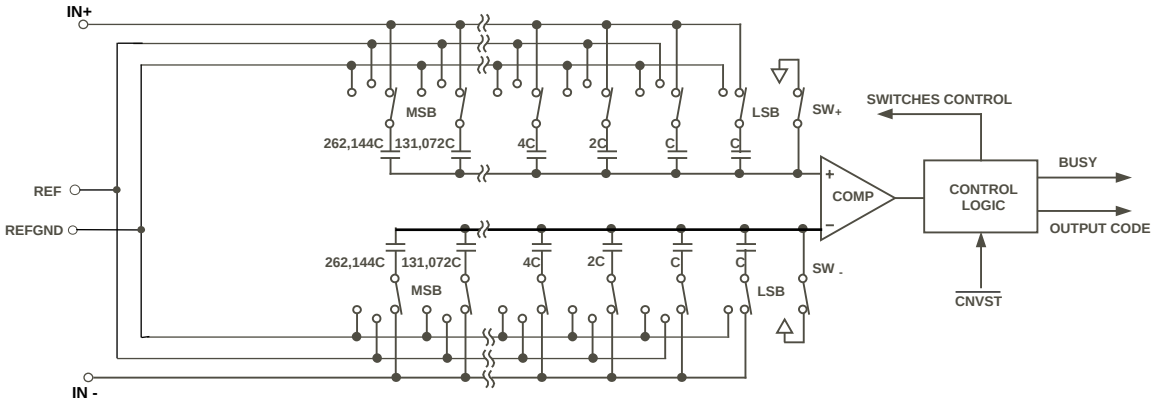


Figure 3. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7674 is a very fast, low-power, single-supply, precise 18-bit analog-to-digital converter (ADC) using successive approximation architecture.

The AD7674 linearity and dynamic range are similar or better than many sigma-delta ADCs. With the advantages of its succesive architecture which ease multiplexing and reduce power with throughput, it can be used advantageously in applications usually using sigma-delta ADCs.

The AD7674 features different modes to optimize performances according to the applications.

In Warp mode, the AD7674 is capable of converting 800,000 samples per second (800 kSPS).

The AD7674 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7674 can be operated from a single 5 V supply and be interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP or a tiny LFCSP packages that combines space savings and allows flexible configurations as either serial or parallel interface. The AD7674 is a pin-to-pin-compatible upgrade of the AD7676, AD7678, AD7679.

CONVERTER OPERATION

The AD7674 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary weighted capacitors which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW_+ and SW_-. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN- inputs. When the acquisition phase is complete and the $\overline{CNVST}$ input goes low, a conversion phase is initiated. When the conversion phase begins, SW_+ and SW_- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs IN+ and IN- captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ . . . $V_{REF}/262144$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

Modes of Operation

The AD7674 features three modes of operations, Warp, Normal, and Impulse. Each of these modes is more suitable for specific applications.

The Warp mode allows the fastest conversion rate up to 800 kSPS. However, in this mode, and this mode only, the full specified accuracy is guaranteed only when the time between conversion does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the AD7674 ideal for applications where fast sample rate are required.

The normal mode is the fastest mode (666 kSPS) without any limitation about the time between conversions. This mode makes the AD7674 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

The impulse mode, the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 570 kSPS. When operating at 100 SPS, for example, it typically consumes only 15 µW. This feature makes the AD7674 ideal for battery-powered applications.

Transfer Functions

Except in 18 Bit interface mode, using the OB/$\overline{2C}$ digital input, the AD7674 offers two output codings: straight binary and two's complement. The ideal transfer characteristic for the AD7674 is shown in Figure 4 and Table III.

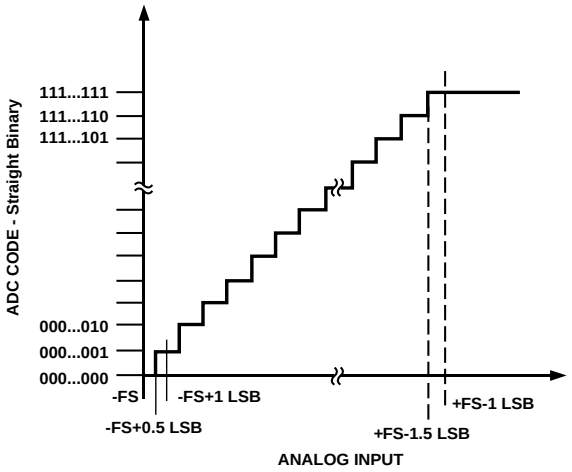
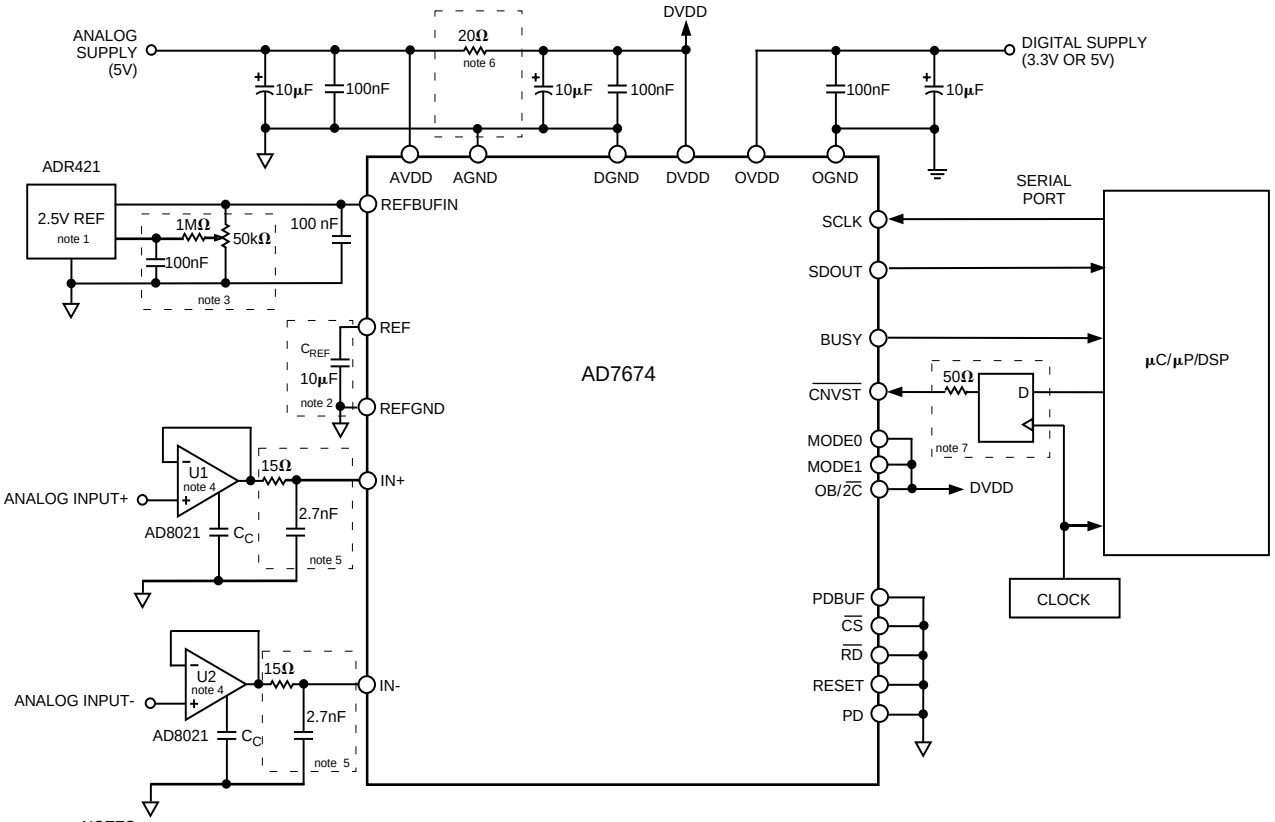


Figure 4. ADC Ideal Transfer Function

Table I. Output Codes and Ideal Input Voltages

		Digital Output Code Hexa	
Description	**Analog Input V_{REF} = 4.096V**	**Straight Binary**	**Two's Comple-ment**
FSR –1 LSB	4.095962 V	3FFFF[1]	1FFFF[1]
FSR – 2 LSB	4.095924 V	3FFFE	1FFE
Midscale + 1 LSB	31.25µV	20001	00001
Midscale	0 V	20000	00000
Midscale – 1 LSB	-31.25µV	1FFFF	3FFFF
–FSR + 1 LSB	-4.095962 V	00001	20001
–FSR	-4.096 V	00000[2]	20000[2]

NOTES
[1]This is also the code for overrange analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{REFGND}).
[2]This is also the code for underrange analog input (V_{IN+} – V_{IN-} below $-V_{REF}$ + V_{REFGND}).



NOTES :
Note 1 : See Voltage Reference Input Section.
Note 2 : C_{REF} is 10µF ceramic capacitor or low esr tantalum. Ceramic size 1206 Panasonic ECJ-3xB0J106 is recommended. See Voltage Reference Input Section.
Note 3 : Optional circuitry for hardware gain calibration.
Note 4 : The AD8021 is recommended. See Driver Amplifier Choice Section.
Note 5 : See Analog Inputs Section.
Note 6 : Option. See Power Supply Section.
Note 7 : Optional Low jitter CNVST. See Conversion Control Section.

Figure 5. Typical Connection Diagram (internal reference buffer, serial interface).

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7674. Different circuitry shown on this diagram are optional and are discussed below.

Analog Inputs

Figure 6 shows a simplified analog input section of the AD7674.

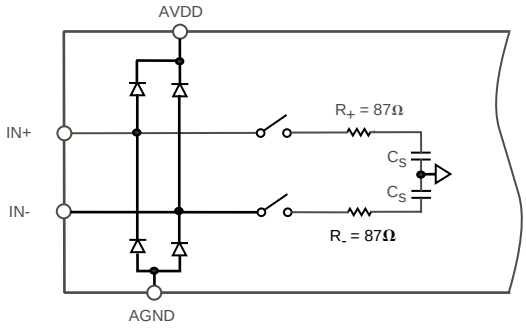


Figure 6. AD7674 simplified Analog Input.

The diodes shown in Figure 6 provide ESD protection for the inputs. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. This condition could eventually occur when the input buffer's (U1) or (U2) supplies are different from AVDD. In such case, an input buffer with a short-circuit current limitation can be used to protect the part.

This analog input structure is a true differential structure. By using these differential inputs, signals common to both inputs are rejected as shown in Figure 7 which represents the typical CMRR over frequency.

To Be Supplied

Figure 7. Analog Input CMRR vs. Frequency

During the acquisition phase, for AC signals, the AD7674 behaves like a one pole RC filter consisted of the equivalent resistance R+ , R- and C_S. The resistors R+ and R- are typically 87 Ω and are lumped component made up of some serial resistor and the on resistance of the switches. The capacitor C_S is typically 60 pF and is mainly the ADC sampling capacitor. This one pole filter with a typical -3dB cutoff frequency of 30 MHz reduces undesirable aliasing effect and limits the noise coming from the inputs.

Because the input impedance of the AD7674 is very high, the AD7674 can be driven directly by a low impedance source without gain error. That allows to put, as shown in Figure 5, an external one-pole RC filter between the output of the amplifier output and the ADC analog inputs to even further improve the noise filtering done by the AD7674 analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency as shown in Figure 8.

To Be Supplied

Figure 8. THD Vs. Analog Input Frequency and Source Resistance.

Driver Amplifier Choice

Although the AD7674 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7674 analog input circuit have to be able together to settle for a full-scale step the capacitor array at a 18-bit level (0.0004%). In the amplifier's datasheet, the settling at 0.1% or 0.01% is more commonly specified. It could significantly differ from the settling time at 18 bit level and, therefore, it should be verified prior to the driver selection. The tiny op-amp AD8021 which combines ultra low noise and a high gain bandwidth meets this settling time requirement.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR

and transition noise performance of the AD7674. The noise coming from the driver is filtered by the AD7674 analog input circuit one-pole low-pass filter made by R_+, R_- and C_S. The SNR degradation due to the amplifier is :

$$SNR_{LOSS} = 20LOG\left(\frac{25}{\sqrt{625+\pi f_{-3dB}\left(Ne_N\right)^2}}\right),$$

where :

f_{-3dB} is the -3dB input bandwidth in MHz of the AD7674 (30 MHz) or the cutoff frequency of the input filter if any used

N is the noise factor of the amplifiers (1 if in buffer configuration)

e_N is the equivalent input noise voltage of each op-amp in $nV/(Hz)^{1/2}$

For instance, a driver with an equivalent input noise of $2nV/\sqrt{Hz}$ like the AD8021 and configured as a buffer, thus with a noise gain of +1, the SNR degrades by only 0.34 dB with the filter in figure 5, and 2 dB without.

- The driver needs to have a THD performance suitable to that of the AD7674.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where dual version is needed and gain of 1 is used.

The AD829 is another alternative where high frequency (above 100 kHz) performances is not required. In gain of 1, it requires a 82pF compensation capacitor.

The AD8610 is also another option where low bias current is needed in low frequency applications.

Single to Differential Driver

For applications using unipolar analog signals, a single-ended to differential driver will allow for a differential input into the part. The schematic is shown in Figure 9. This configuration, when provided an input signal of 0 to V_{REF} , will produce a differential ± V_{REF} with midscale at $V_{REF}/2$.

If the application can tolerate more noise, the AD8138, differential driver, can be used.

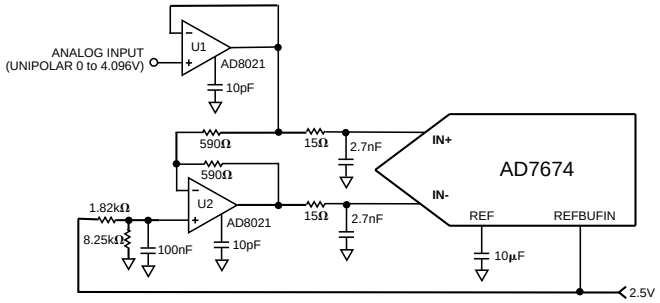


Figure 9. Single Ended to Differential Driver Circuit (internal reference buffer used)

Voltage Reference

The AD7674 allows the use of an external voltage reference either with or without the internal reference buffer.

It is recommended to use the internal reference buffer when it is desired to share a common reference voltage between multiple ADCs.

However, the advantages to use the external reference voltage directly are :

- The power saving of about 5mW typical when the internal reference buffer is powered down (PDBUF High)

- The SNR and dynamic range improvement of about 1.7 dB resulting of the use of a reference voltage very close to the supply (5V) instead of a typical 4.096V reference when the internal buffer is used.

To use the internal reference buffer, PDBUF should be LOW. A 2.5V reference voltage applied on REFBUFIN input will result in a 4.096V reference on REF pin.

In both cases, the voltage reference input REF has a dynamic input impedance and requires, therefore, an efficient decoupling between REF and REFGND inputs. When the internal reference buffer is used, this decoupling consists of a 10 µF ceramic capacitor (e.g. : Panasonic ECJ-3xB0J106 1206 size).
When external reference is used, the decoupling consists of a low ESR 47 µF tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance.

Care should also be taken with the reference temperature coefficient of the voltage reference which directly affects the full-scale accuracy if this parameter matters. For instance, a ±4 ppm/°C tempco of the reference changes the full scale by ±1 LSB/°C.

Power Supply

The AD7674 uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The

OVDD supply allows direct interface with any logic working between 2.7 V and DVDD + 0.3 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 5. The AD7674 is independent of power supply sequencing, once OVDD does not exceed DVDD by more than 0.3V, and thus free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 10.

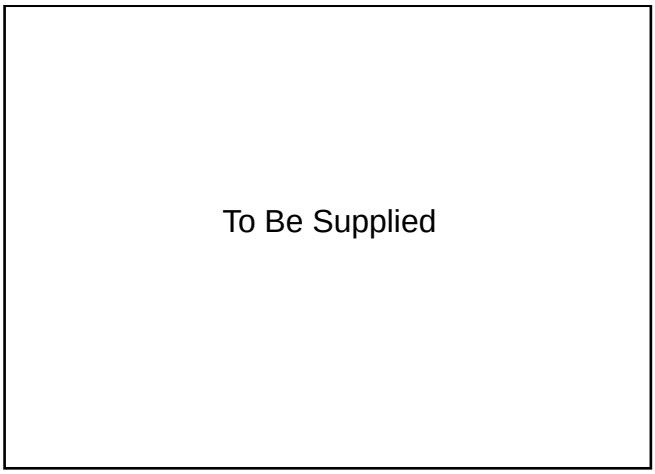


Figure 10. PSRR vs. Frequency

POWER DISSIPATION Vs. THROUGHPUT

In Impulse mode, the AD7674 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low which allows a significant power saving when the conversion rate is reduced as shown in Figure 11. This feature makes the AD7674 ideal for very low-power battery applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (i.e., DVDD and DGND) and OVDD should not exceed DVDD by more than 0.3V.

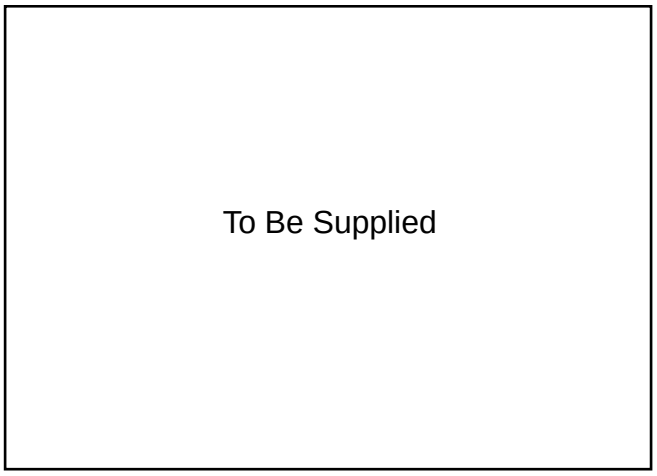


Figure 11. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 12 shows the detailed timing diagrams of the conversion process. The AD7674 is controlled by the signal $\overline{CNVST}$ which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{CNVST}$ signal operates independently of $\overline{CS}$ and $\overline{RD}$ signals.

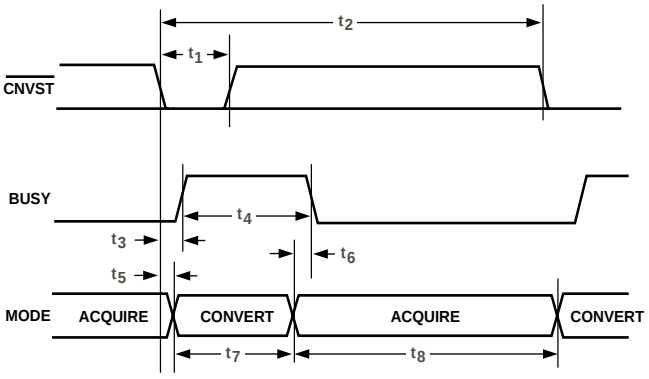


Figure 12. Basic Conversion Timing

Although $\overline{CNVST}$ is a digital signal, it should be designed with this special care with fast, clean edges and levels, with minimum overshoot and undershoot or ringing.

For applications where the SNR is critical, the $\overline{CNVST}$ signal should have a very low jitter. Some solutions to achieve that are to use a dedicated oscillator for $\overline{CNVST}$ generation or, at least, to clock it with a high frequency low jitter clock as shown in Figure 5.

In impulse mode, conversions can be automatically initiated. If $\overline{CNVST}$ is held low when BUSY is low, the AD7674 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{CNVST}$ low, the AD7674 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{CNVST}$ should be brought low once to initiate the conversion process. In this mode, the AD7674 could sometimes run slightly faster then the guaranteed limits in the impulse mode of 570 kSPS. This feature does not exist in warp or normal modes.

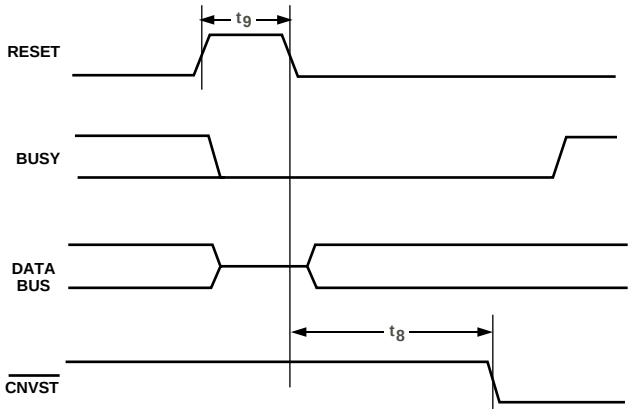


Figure 13. RESET Timing

DIGITAL INTERFACE

The AD7674 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7674 digital interface also accommodates both 3 V or 5 V logic by simply connecting the OVDD supply pin of the AD7674 to the host system interface digital supply. Finally, except in 18 bit interface mode, by using the OB/$\overline{2C}$ input pin, both two's complement or straight binary coding can be used.

The two signals $\overline{CS}$ and $\overline{RD}$ control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7674 in multi-circuits applications and is held low in a single AD7674 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

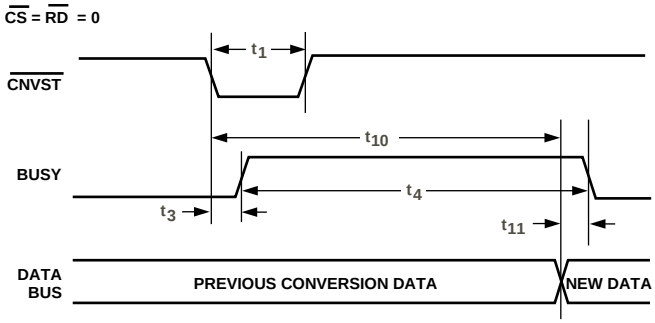


Figure 14. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7674 is configured to use the parallel interface with either a 18-bit, 16-bit or 8-bit bus width according to the Table II. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figure 15 and Figure 16. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. That avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry. Please refer to table II for a detailed description of the different options available.

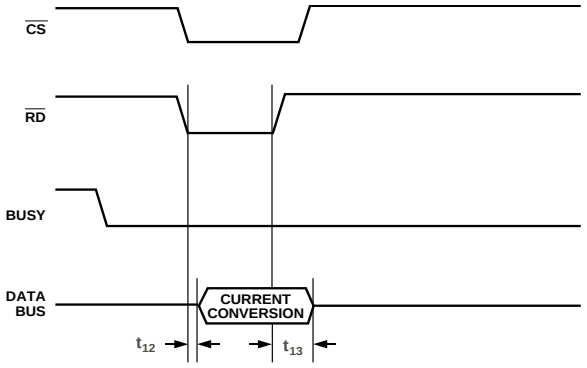


Figure 15. Slave Parallel Data Timing for Reading (Read After Convert)

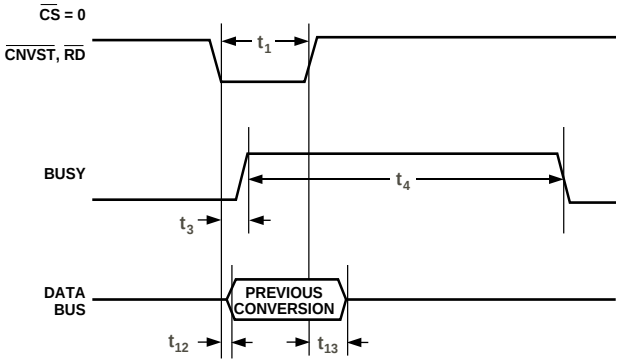


Figure 16. Slave Parallel Data Timing for Reading (Read During Convert)

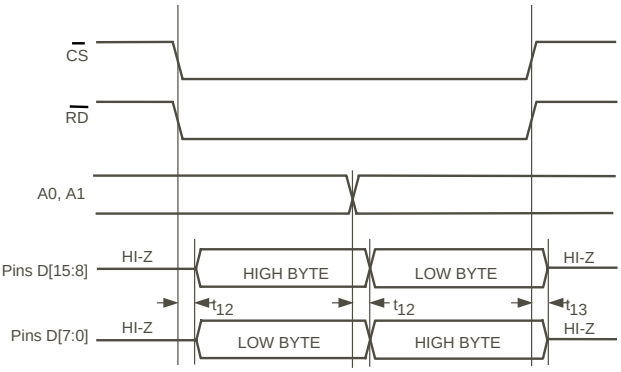


Figure 17. 8-Bit and 16-Bit Parallel Interface

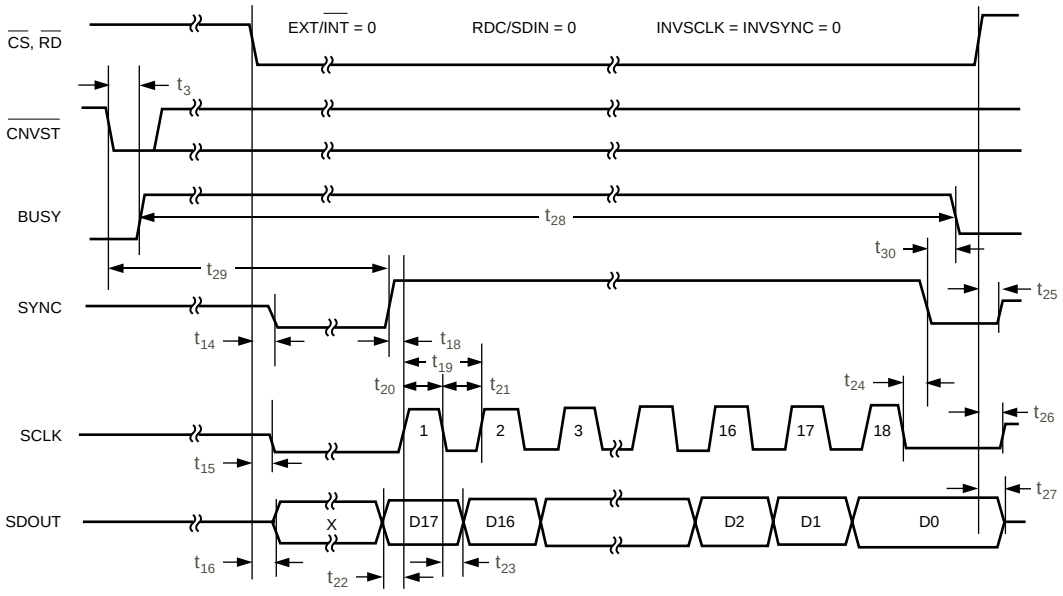


Figure 18. Master Serial Data Timing for Reading (Read After Convert)

SERIAL INTERFACE

The AD7674 is configured to use the serial interface when MODE0 and MODE1 are held high. The AD7674 outputs 18 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 18 clock pulses provided on SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7674 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{INT}$ pin is held low. The AD7674 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figure 18 and Figure 19 show the detailed timing diagrams of these two modes.

Usually, because the AD7674 is used with a fast throughput, the mode master, read during conversion is the most recommended serial mode when it can be used.

In read-during-conversion mode, the serial clock and data toggle at appropriate instants which minimize potential feedthrough between digital activity and the critical conversion decisions.

In read-after-conversion mode, it should be noted that, unlike in other modes, the signal BUSY returns low after the 18 data bits are pulsed out and not at the end of the conversion phase which results in a longer BUSY width.

To accomodate slow digital hosts, the serial clock can be slowed down by using DIVSCLK.

SLAVE SERIAL INTERFACE

External Clock

The AD7674 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{INT}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS}$. When $\overline{CS}$ and $\overline{RD}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 20 and Figure 22 show the detailed timing diagrams of these methods.

While the AD7674 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7674 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

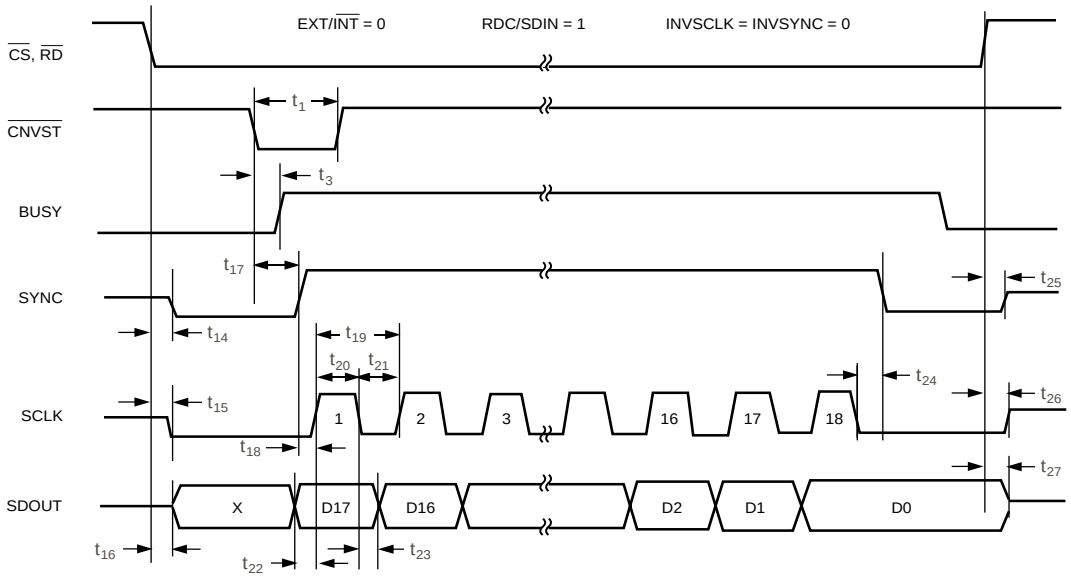


Figure 19. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 20 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the result of this conversion can be read while both $\overline{CS}$ and $\overline{RD}$ are low. The data is shifted out, MSB first, with 18 clock pulses and is valid on both rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

Another advantage is to be able to read the data at any speed up to 40 MHz which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7674 provides a "daisy-chain" feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 21. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT. Hence, the MSB of the "upstream" converter just follows the LSB of the "downstream" converter on the next SCLK cycle.

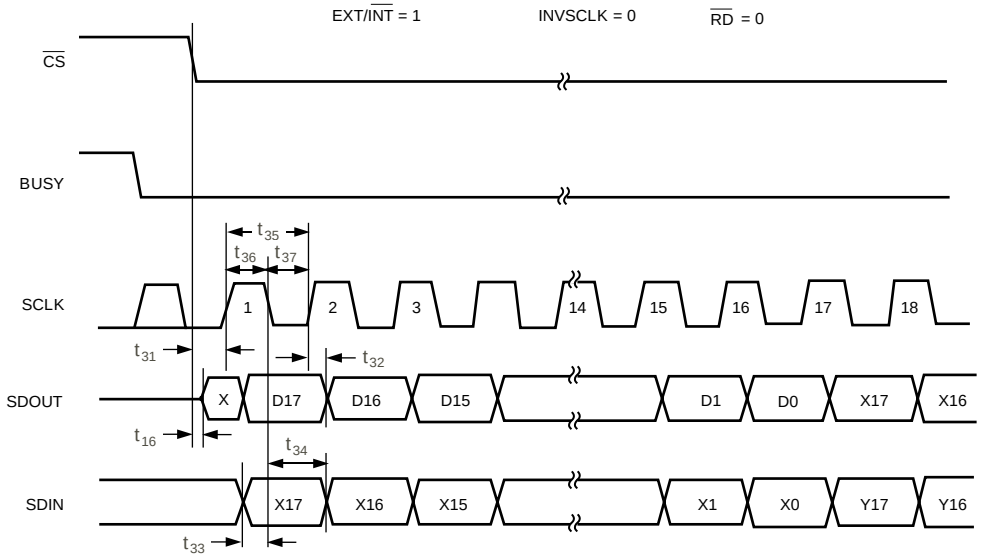


Figure 20. Slave Serial Data Timing for Reading (Read After Convert)

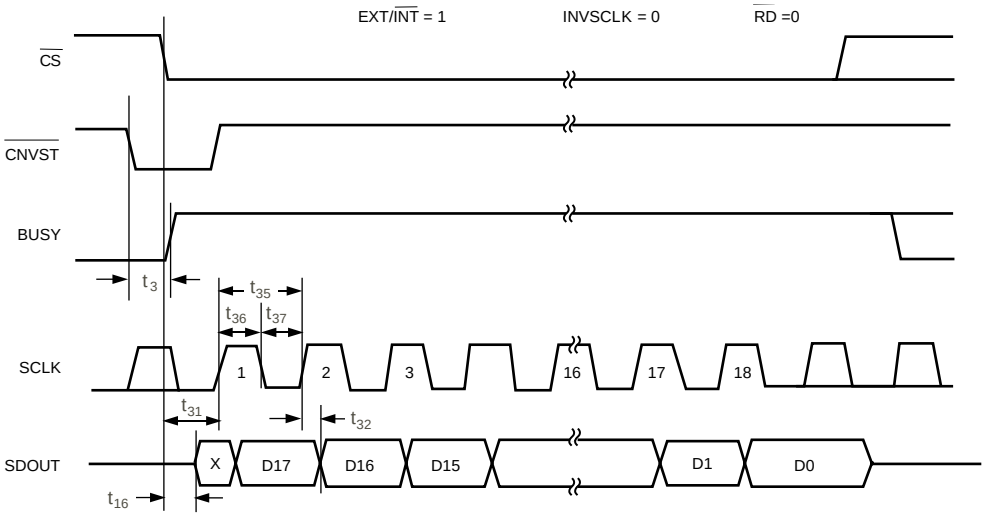


Figure 22. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

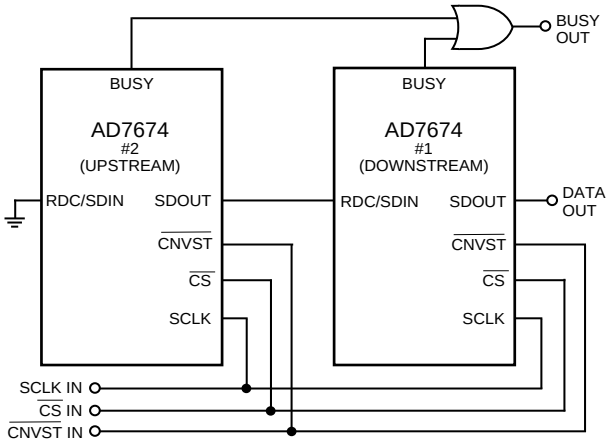


Figure 21. Two AD7674s in a "Daisy-Chain" Configuration

External Clock Data Read During Conversion

Figure 22 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are both low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 18 clock pulses and is valid on both rising and falling edge of the clock. The 18 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no "daisy chain" feature in this mode and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock of is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated.

MICROPROCESSOR INTERFACING

The AD7674 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7674 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7674 to prevent digital noise from coupling into the ADC. The following section illustrates the use of the AD7674 with an SPI equipped DSP, the ADSP-219x.

SPI Interface (ADSP-219x)

Figure 22 shows an interface diagram between the AD7674 and an SPI-equipped DSP, ADSP219x. To accommodate the slower speed of the DSP, the AD7674 acts as a slave device and data must be read after conversion. This mode also allows the "daisy chain" feature. The convert command could be initiated in response to an internal timer interrupt. The 18-bit output data are read with 3 SPI byte access. The reading process could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The Serial Peripheral Interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1 and SPI interrupt enable (TIMOD) =00 by writing to the SPI Control Register (SPICLTx). It should be noted that to meet all timing requirements, the SPI clock should be limited to 17Mbits/s which allow to read an ADC result in about 1.1 μs. When higher sampling rate is desired, it is recomended to use one of the parallel interface mode with the ADSP-219x.

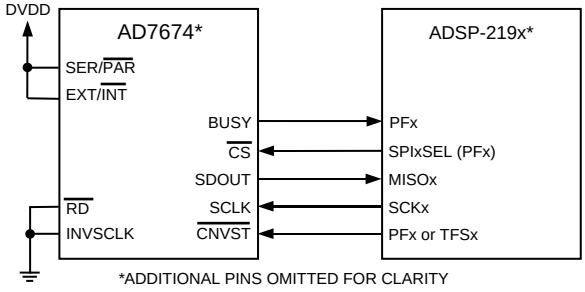


Figure 23. Interfacing the AD7674 to SPI Interface

APPLICATION HINTS

Layout

The AD7674 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7674 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7674, or, at least, as close as possible to the AD7674. If the AD7674 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7674.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7674 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board. The power supply lines to the AD7674 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supplies impedance presented to the AD7674 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supplies pins AVDD, DVDD and OVDD close to, and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7674 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if no separate supply available, to connect the DVDD digital supply to the analog supply AVDD through an RC filter as shown in Figure 5, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high-frequency spikes.

The AD7674 has four different ground pins; REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

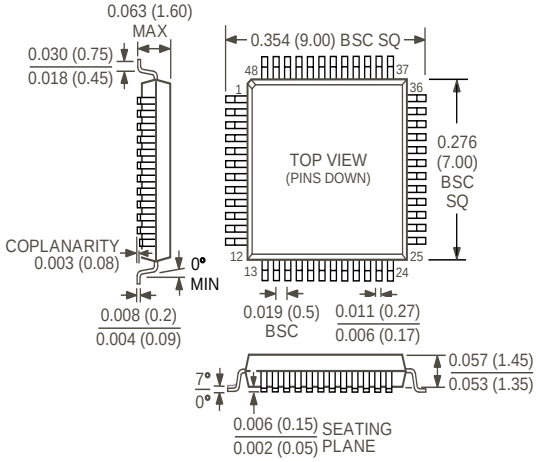
Evaluating the AD7674 Performance

A recommended layout for the AD7674 is outlined in the documentation of the EVAL-AD7674-CB, evaluation board for the AD7674. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control BRD2.

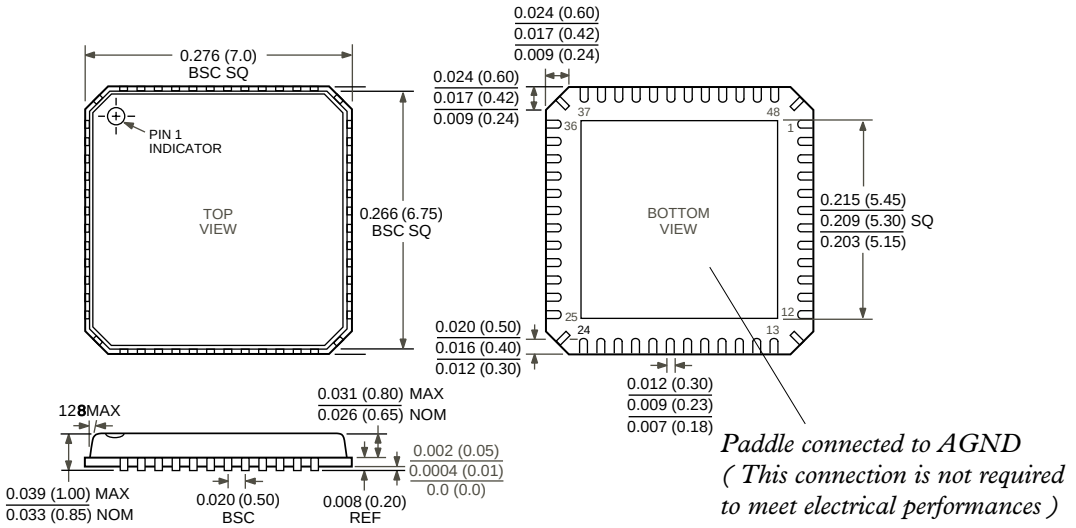
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Quad Flatpack (LQFP)
(ST-48)



48-Lead Frame Chip Scale Package (LFCSP)
(CP-48)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS