


High Speed, Constant Bandwidth Differential APC Amplifier

FEATURES

- Dual wavelength 650 and 780nm
- 150 MHz Bandwidth over all gains
- 400 V/ μ s Slew Rate
- 5 ns Setting Time
- 10 mV Differential Output Offset Voltage
- Potentiometer, Voltage or DAC programmable gain
- ± 6 dB External Gain Adjust
- Small 8-pin OPLGA package

VCC	1	 SP8027 8-Pin OPLGA	8	VOUT+
GAIN	2		7	VOUT-
VBG	3		6	VG2
GND	4		5	VG1

APPLICATION

- CD-R, and CD-RW
- DVD+/-R, DVD+/-RW, and DVD-RAM

GENERAL DESCRIPTION

The SP8027 represents the next generation in Automatic Power Control (APC) amplifiers designed specifically for demanding pick-up head applications. With its integrated photo detector, the SP8027 monitors light intensity of the laser diode in CD-R, CD-RW, DVD+/-R, DVD+/-RW, and DVD-RAM assemblies and converts this light to an output voltage. The magnitude of this voltage signal corresponds to the laser power intensity and is subsequently fed back to the laser diode driver to control the laser output power.

The SP8027 on-chip photo detector transforms incident laser light into a proportional current, which is then converted to a voltage through a trans-impedance amplifier. Adjustable gain is provided prior to the trans-impedance amplifier by means of an analog multiplier controlled by an external potentiometer. This external potentiometer is not a part of the signal path. This greatly reduces the effect of all parasitic capacitances and inductances on the flex cable at these pins. The signal is then buffered to provide reactive load drive capability.

The SP8027 achieves an unparalleled level of performance by combining excellent DC stability and low noise with outstanding AC performance. This level of performance is achieved using a proprietary fully complimentary BICMOS process with fully integrated, on-board photo detector.

The SP8027 is offered with a nominal sensitivity 3000 V/W and is packaged in a 3.0 x 3.5 mm, 8-lead OPLGA package.

PIN ASSIGNMENTS

Pin #	Pin Name	Pin Function
1	Vcc	Supply Voltage. Bypass to GND with ceramic capacitor 0.1µF
2	Gain	Gain Switch Input. Low level or Open selects pin VG1, high level selects pin VG2
3	VBG	Common connection bias voltage output for Potentiometer1 and Potentiometer2
4	GND	Power Ground
5	VG1	Gain Adjust Potentiometer1 wiper connection or control voltage input
6	VG2	Gain Adjust Potentiometer2 wiper connection or control voltage input
7	Vout(-)	Output Voltage Negative Swing
8	Vout(+)	Output Voltage Positive Swing

THEORY OF OPERATION

The SP8027 consist of a photo detector that converts light (780 or 650nm wavelength) into current and active circuitry to convert the current into voltage. The active circuitry consists of a multiplier, a trans-impedance amplifier and a buffer. The overall transfer characteristics are therefore represented by a Voltage per Watt curve. The transfer function is $V_{out}/Pin = 11.6 * (1.294 - V_g)$
 The output voltage can be calculated by: $V_{out} = 11.6 * Pin * (1.294 - V_g)$, Pin in units of mW.

There are three pins for gain adjust, using two separate external potentiometers for two separate gain modes. This allows different adjust for DVD and CD mode. The two potentiometers are each tied from the corresponding VG pin (pin #5 or #6, depending on the mode) to the common VBG pin (#3) (see Fig 1). The Vg pins can be driven by an external voltage source or DAC instead of potentiometers to set the gain. Dependence between sensitivity, gain, Rg or Vg value is shown in the table below.

Sensitivity (V/W)	Input Power * (mW)	Gain (dB)	Gain (x)	Rg-high (Ω)	Rg-low (Ω)	VG1,2 (V)	System V/I (Ohms)
6000	0.333	6.02	2.000	2000	3000	0.776	23077
4242	0.471	3.01	1.414	1413	3588	0.928	15385
3000	0.667	0.00	1.000	1000	4000	1.035	7692
2121	0.943	-3.01	0.707	708	4292	1.111	3846
1500	1.333	-6.02	0.500	500	4500	1.165	2564

Note: * Input Power to set 2Vpp Differential Output Swing; $R_g = R_{g-high} + R_{g-low} = 5k\Omega$

Fig 1 - Potentiometer (Rg) Connection

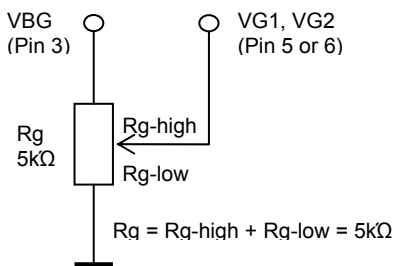
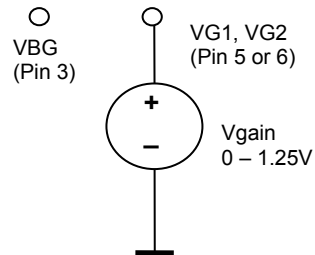


Fig 2 - Vgain (Vg) Connection



THEORY OF OPERATION (continued)

The gain adjust is proportional to the applied external voltage and is achieved by means of an analog fractional multiplier circuit that translates the gain voltage into a proportional attenuation of the photo detector output current. Since the external resistor or external voltage source is not in the signal path, better signal quality and immunity to the parasitic capacitance/inductance on pins #3, 5, and 6 is assured.

A trans-impedance amplifier (TIA) converts current from the multiplier circuit into voltage and refers the signal to the internal reference voltage. The TIA stage is fully differential. The buffers amplify the differential signals from the TIA and buffer them to the Vout pins. A balanced current feedback amplifier is used for this purpose to achieve high slew rate and fast settling.

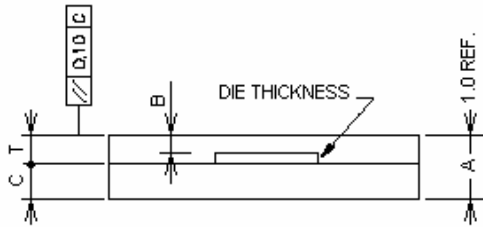
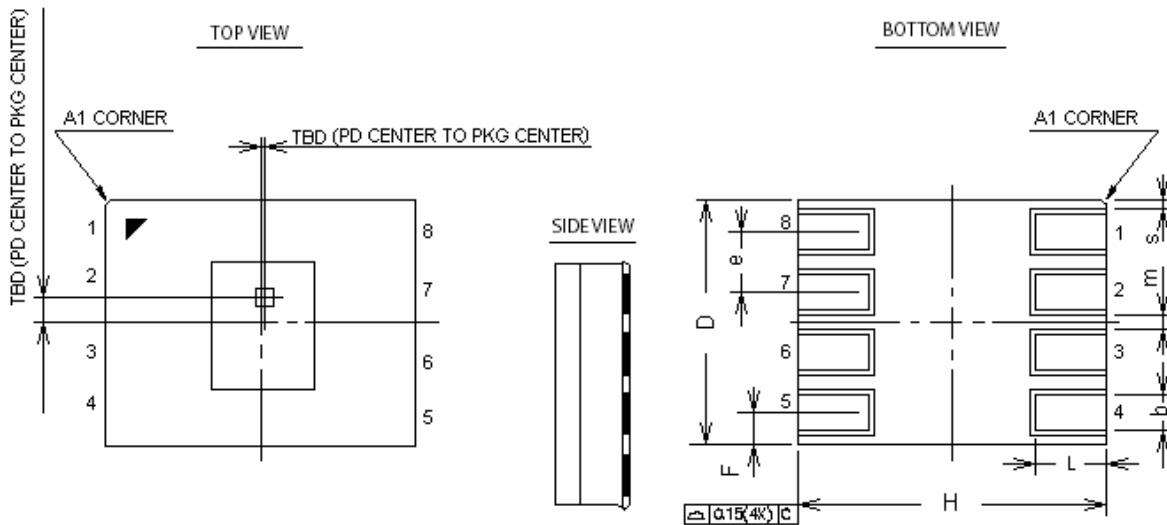
The buffers are designed to drive high capacitive load. The maximum load is 20pF bulk. The actual load is typically a flex printed circuit cable (FPC) that acts like a transmission line. This presents a distributed capacitive, inductive and resistive load to the output. In this case care should be taken to match the characteristic impedance of the line at the far end to avoid reflections and ringing. The buffers are designed to drive 1k Ω to the ground. However, this resistor can be adjusted in value to accommodate the characteristic impedance of the signal line. The output buffer amplifier is designed to be stable without load and with the load up to 20pF capacitance.

In the dark condition, the differential output voltage of the circuit will remain zero with the common mode voltage close to 2.25V. However, when light is received on the photo diode, the output Vout (+) (pin #8) will swing positive and Vout (-) (pin #7) will swing negative with respect to the common mode voltage. The linear differential output swing is guaranteed to be at least 2V at appropriate gain and input power.

BOARD LAYOUT AND GROUNDING

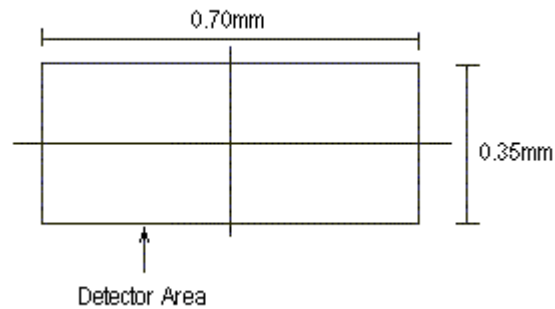
To obtain the best performance from the SP8027, a printed circuit board with ground plane is required. High quality, low series resistance ceramic 0.1 μ F bypass capacitor should be used at the Vcc pin (pin #1). This capacitor must be located as close to the pin #1 and pin #4 as possible. The traces connecting the pins and the bypassing capacitor must be kept short and should be made as wide as possible.

OPLGA 8-pin PACKAGE DIMENSIONS



NOTE: DIE THICKNESS 0.2mm (8MIL)

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.30	0.40	0.50
C	—	0.56	—
D	2.90	3.00	3.10
B	0.19	—	0.32
H	3.40	3.50	3.60
e	—	0.75	—
F	0.28	0.38	0.48
L	0.50	0.60	0.70
T	—	0.45	—
s	0.075	—	—
m	0.10	—	—

PHOTO DETECTOR PATTERN**ORDERING INFORMATION**

Part number	Temperature range	Package Type
SP8027CG	0 + 70°C	8-pin OPLGA