DATA SHEET

CX74017: RF Transceiver for Multi-Band GSM, GPRS, and EDGE Applications

APPLICATIONS

- GSM850, EGSM900, DCS1800, and PCS1900 handsets
- GPRS handsets and modules
- EDGE downlink support

FEATURES

- Direct down-conversion receiver eliminates the external image reject/IF filters
- Three separate LNAs with single-ended inputs
- Radio frequency (RF) gain range: GSM = 20 dB, DCS = 22 dB, PCS = 20 dB. Baseband gain range = 100 dB
- Gain selectable in 2 dB steps
- Integrated receive baseband filters with tunable bandwidth
- Integrated DC offset correction sequencer
- Reduced filtering requirements with translational loop transmit architecture
- Integrated transmit VCOs
- Wide RF range for quad band operation
- Single integrated, fully programmable fractional-N synthesizer suitable for multi-slot GPRS operation
- Fully integrated wideband Ultra High Frequency (UHF) VCO
- Separate enable lines for power management transmit, receive, and synthesizer modes
- Supply voltage down to 2.6 V
- Band select and front-end enable states may be exercised on output pins to control external circuitry.
- Low external component count
- Optional bypass of baseband filtering for use with high dynamic range Analog/Digital Converters (ADCs) for current savings
- Interfaces to low dynamic range ADC
- Meets Amplitude Modulation (AM) suppression requirements without baseband interaction
- 64-pin LGA 9 x 9 mm package
- Low power standby mode

DESCRIPTION

The CX74017 transceiver is a highly integrated device for multi-band Global System for Mobile Communications™ (GSM™) or General Packet Radio Service (GPRS) applications. The device requires a minimal number of external components to complete a GSM radio subsystem. The CX74017 supports GSM850, EGSM900, DCS1800, and PCS1900 applications. The receiver also supports downlink Enhanced Data-Rate GSM Evolution (EDGE).

The receive path implements a direct down-conversion architecture that eliminates the need for Intermediate Frequency (IF) components. The CX74017 receiver consists of three integrated Low Noise Amplifiers (LNAs), a quadrature demodulator, tunable receiver baseband filters, and a DC offset correction sequencer.

In the transmit path, the device consists of an In-phase and Quadrature (I/Q) modulator within a frequency translation loop designed to perform frequency up-conversion with high output spectral purity. This loop also contains a phase-frequency detector, charge pump, mixer, programmable dividers, and high power transmit Voltage Controlled Oscillators (VCOs) with no external tank required.

The CX74017 also features an integrated, fully programmable, sigma-delta fractional-N synthesizer suitable for GPRS multi-slot operation. Except for the loop filter, the frequency synthesizer function, including a wideband VCO, is completely on-chip.

The CX74017 64-pin Land Grid Array (LGA) 9 x 9 mm device package and pin configuration are seen in Figure 1. A functional block diagram is shown in Figure 2. Signal pin assignments, functional pin descriptions, and equivalent circuitry are provided in Table 1.

The CX74017 is available with two different reflow temperature ratings. A description is provided in the Package and Handling Information section of this document.

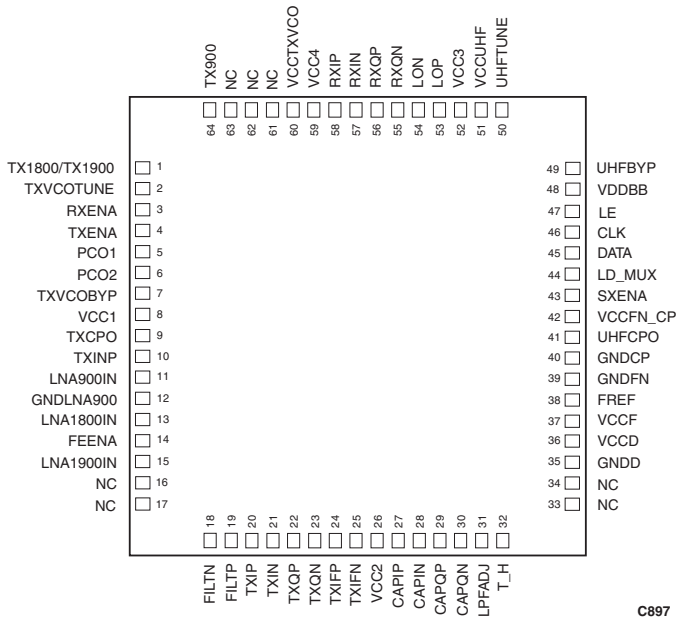


Figure 1. CX74017 Pinout – 64-Pin LGA (Top View)

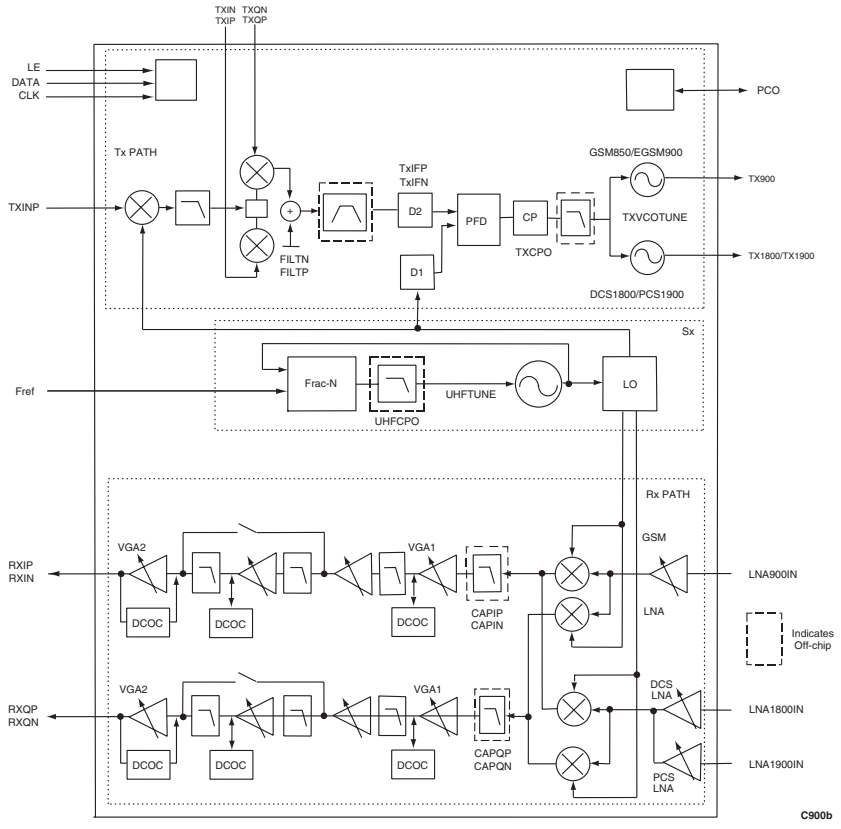


Figure 2. CX74017 Transceiver Block Diagram

Table 1. CX74017 Signal Descriptions (1 of 5)

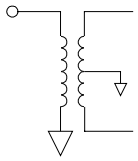
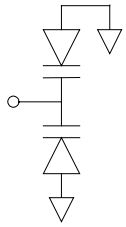
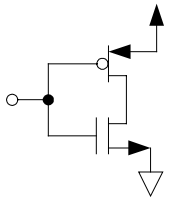
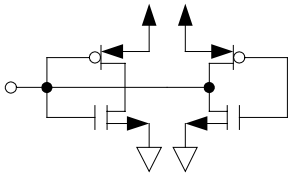
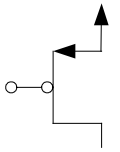
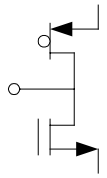
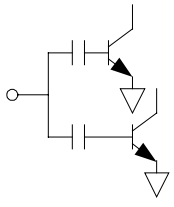
Pin #	Name	Description	Equivalent Circuit
1	TX1800/TX1900	DCS and PCS transmit VCO output	
2	TXVCOTUNE	Transmit VCO control input	
3	RXENA	Receiver enable input	
4	TXENA	Transmitter enable input	
5	PCO1	Bi-directional band select	
6	PCO2	Bi-directional band select	
7	TXVCOBYP	Bypass capacitor for TX VCO	
8	VCC1	LNA and TX charge pump supply	VCC1
9	TXCPO	Translational loop charge pump output	
10	TXINP	Translational loop feedback input	

Table 1. CX74017 Signal Descriptions (2 of 5)

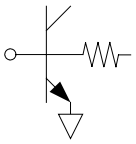
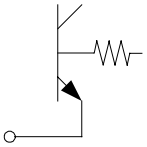
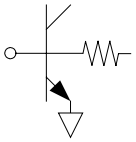
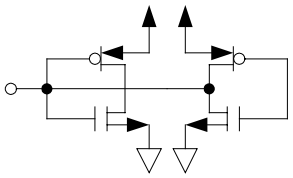
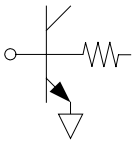
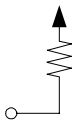
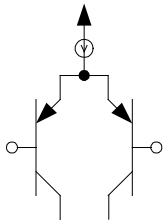
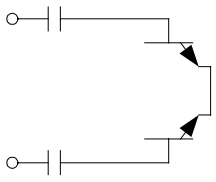
Pin #	Name	Description	Equivalent Circuit
11	LNA900IN	Low band LNA input for GSM850, EGSM900	
12	GNDLNA900	Low band LNA emitter ground	
13	LNA1800IN	DCS LNA input	
14	FEENA	Bi-directional front end control	
15	LNA1900IN	PCS LNA input	
16	NC	No connect	No connect
17	NC	No connect	No connect
18	FILTN	TX IF output negative	
19	FILTP	TX IF output positive	
20	TXIP	TX I baseband input positive	
21	TXIN	TX I baseband input negative	
22	TXQP	TX Q baseband input positive	
23	TXQN	TX Q baseband input negative	
24	TXIFP	TX IF filter output positive	
25	TXIFN	TX IF filter output negative	

Table 1. CX74017 Signal Descriptions (3 of 5)

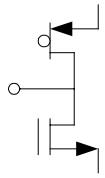
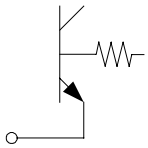
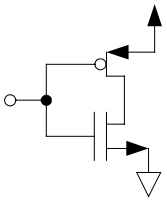
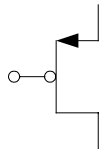
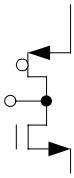
Pin #	Name	Description	Equivalent Circuit
26	VCC2	RX mixer and TX loop supply	VCC2
27	CAPIP	Capacitor filter I positive	
28	CAPIN	Capacitor filter I negative	
29	CAPQP	Capacitor filter Q positive	
30	CAPQN	Capacitor filter Q negative	
31	LPFADJ	LPF frequency setting resistor	
32	T_H	Track and hold control	
33	NC	No connect	No connect
34	NC	No connect	No connect
35	GNDD	Synthesizer digital ground	
36	VCCD	Synthesizer digital supply	VCCD
37	VCCF	Synthesizer analog supply	VCCF
38	FREF	Crystal reference input	
39	GNDFN	Synthesizer analog ground	
40	GNDCP	Synthesizer charge pump ground	
41	UHFCPO	Synthesizer charge pump output	
42	VCCFN_CP	Synthesizer charge pump supply	VCCFN_CP

Table 1. CX74017 Signal Descriptions (4 of 5)

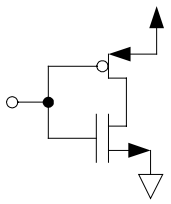
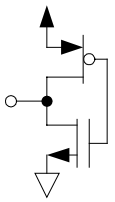
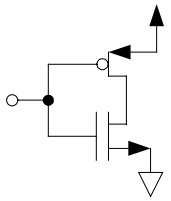
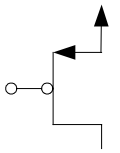
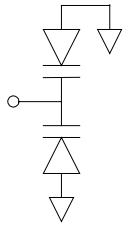
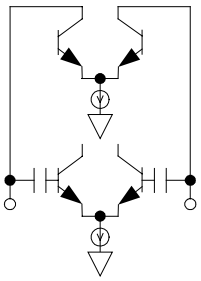
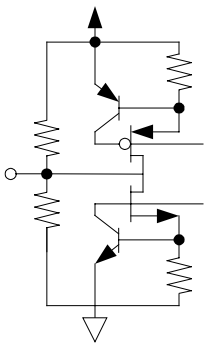
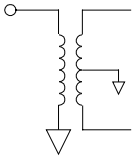
Pin #	Name	Description	Equivalent Circuit
43	SXENA	Synthesizer enable input	
44	LD_MUX	Lock_detect/Synthesizer test output	
45	DATA	Serial bus data input	
46	CLK	Serial bus clock input	
47	LE	Serial bus latch enable input	
48	VDDBB	Digital CMOS supply	VDDBB
49	UHFBYP	Bypass capacitor for UHF VCO	
50	UHFTUNE	UHF VCO control input	
51	VCCUHF	UHF VCO supply	VCCUHF
52	VCC3	LO chain supply	VCC3
53	LOP	External LO input/internal LO monitor positive	
54	LON	External LO input/internal LO monitor negative	

Table 1. CX74017 Signal Descriptions (5 of 5)

Pin #	Name	Description	Equivalent Circuit
55	RXQN	Receiver output Q negative	
56	RXQP	Receiver output Q positive	
57	RXIN	Receiver output I negative	
58	RXIP	Receiver output I positive	
59	VCC4	Baseband supply	VCC4
60	VCCTXVCO	Transmit VCO supply	VCCTXVCO
61	NC	No connect	No connect
62	NC	No connect	No connect
63	NC	No connect	No connect
64	TX900	Low band transmit VCO	

Technical Description

The CX74017 transceiver contains the following sections, as shown in Figure 2.

- Receive section. Includes three integrated LNAs, a quadrature demodulator section that performs direct down conversion, baseband amplifier circuitry with I/Q outputs, and three stages of DC offset correction. The receiver can be calibrated to optimize IP2 performance.
- Synthesizer section. Includes an integrated on-chip VCO locked by a fractional-N synthesizer loop.
- Transmit section. The TX path is a translational loop architecture consisting of I/Q modulator, integrated high power VCOs, offset mixer, programmable divider, PFD and charge pump.

A three-wire serial interface controls the transceiver and synthesizer. The receiver gain control, as well as the division ratios and charge pump currents in the synthesizer and transmitter, can be programmed using 24-bit words. These 24 bit words are programmed using the 3-wire input signals CLK, DATA, and LE. To ensure that the data stays latched in power down mode, pin 48 (VDDBB) must be continuously supplied with voltage. This pin is provided for the digital sections to allow power supply operation compatible with modern digital baseband devices.

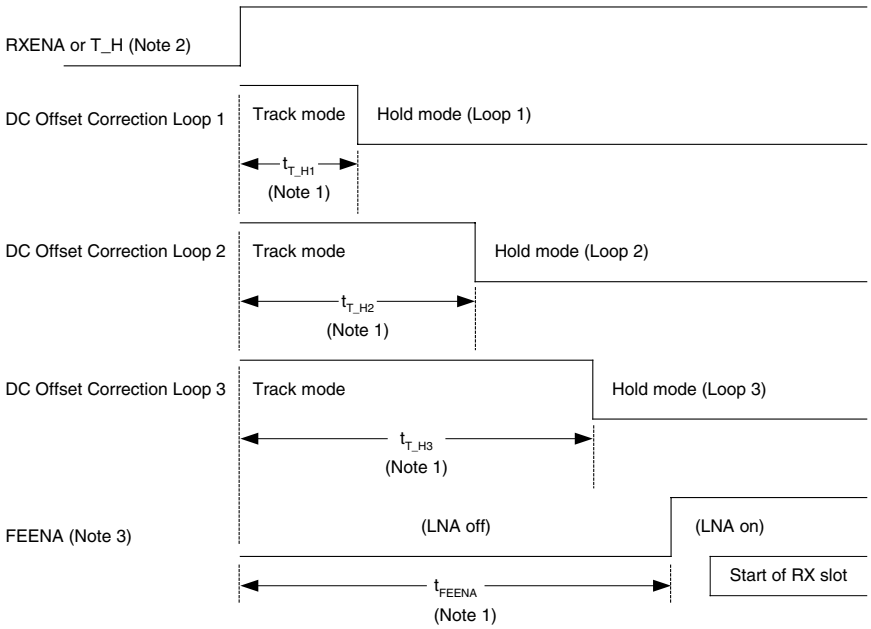
The TXENA, RXENA, and SXENA signals separately enable the CX74017 transmitter, receiver, and synthesizer sections.

TXENA, RXENA should be held low during programming. Detailed timing is shown in Figure 3 and Figure 4. SXENA should be held high during programming of register 3 (IP2 calibration).

Receive Section

LNA & Quadrature Demodulator

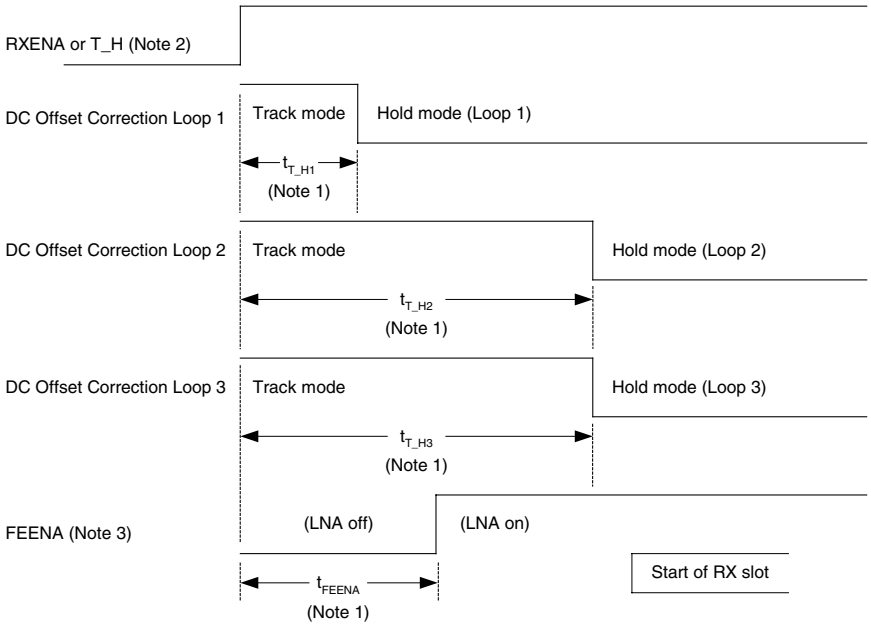
Three separate LNAs are integrated to address different bands of operation. These LNAs have separate single-ended inputs, which are externally matched to 50W. The gain is switchable between high (i.e., 15 dB typical) and low (i.e., –5 dB GSM, –7 dB DCS, and –5 dB PCS typical) settings. The LNA outputs feed into a quadrature demodulator that downconverts the RF signals directly to baseband. Two external 470 pF capacitors are required at the demodulator output to suppress the out-of-band blockers.



Note 1. t_{T_H1}, t_{T_H2}, t_{T_H3}, and t_{FEENA} are programmed in Register 2.
Note 2. DCOC sequence start trigger is programmed in Register 2 (either RXENA rising edge or T_H rising edge.)
Note 3. Front End control mode is programmed in Register 2 (either controlled from pin 14, FEENA, or from the internal sequencer.)

S057

Figure 3. DC Offset Correction Timing (LNA Off During All of the DC Offset Correction Sequence)



Note 1. t_{T_H1}, t_{T_H2}, t_{T_H3}, and t_{FEENA} are programmed in Register 2.
Note 2. DCOC sequence start trigger is programmed in Register 2 (either RXENA rising edge or T_H rising edge.)
Note 3. Front End control mode is programmed in Register 2 (either controlled from pin 14, FEENA, or from the internal sequencer.)

S058

Figure 4. DC Offset Correction Timing (LNA On During Part of the DC Offset Correction Sequence)

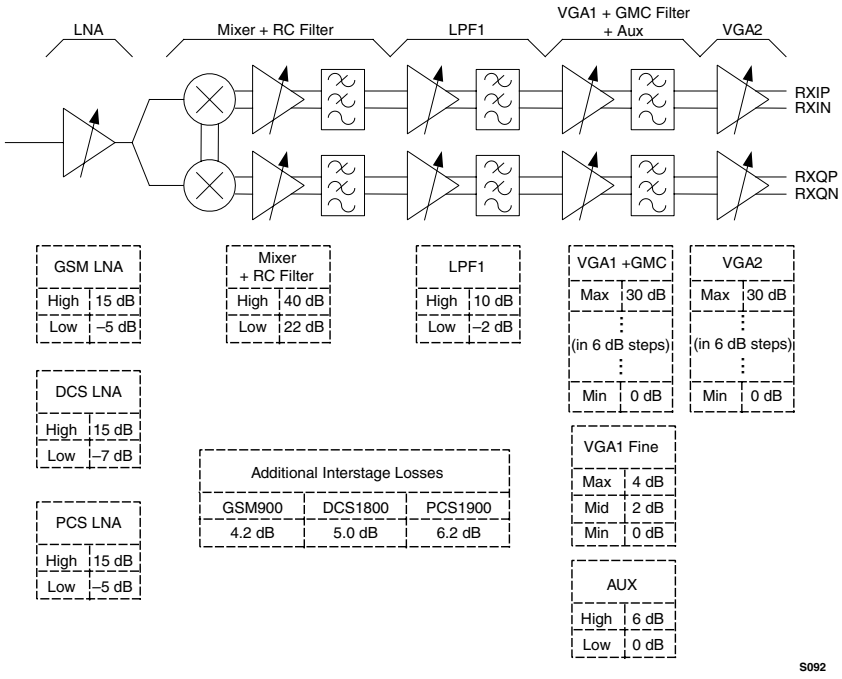


Figure 5. Gain Control Settings

Baseband Section

An off-chip capacitor and three fixed poles of on-chip, low pass filtering provide rejection of strong in- and out-of-band interferers. In addition, a tunable, four-pole gmC filter provides rejection of the adjacent channel blockers. Incorporated within the fixed pole filters are two switchable gain stages of 18 dB and 12 dB gain steps, respectively. There is an additional programmable gain amplifier with a gain range from 0 to +34 dB, selectable in 2 dB steps in the four-pole tunable filter. The final filter output feeds an amplifier with a gain range from 0 to +30 dB, selectable in 6 dB steps.

There is an additional gain stage on the four-pole tunable filter output, the auxiliary gain stage, selectable at 0 dB or + 6 dB.

The gain control ranges are shown in Figure 5.

Recommended combinations of individual block gain settings are shown in Table 23 for GSM900, Table 24 for DCS1800, and Table 25 for PCS1900.

For added baseband interface flexibility, the four-pole filter, its associated Variable Gain Amplifier (VGA), and DC offset correction loop can be bypassed and turned off for current savings.

In Table 2 the typical locations of all eight receiver baseband poles are given. The final four poles are produced by the tunable gmC filter, as set by the external resistor (recommended value is 39.2 kΩ, 1%) placed from pin 31 to ground. For these tunable poles, Table 2 gives the pole location as a function of this resistor.

DC Offset Correction

Three DC offset correction (DCOC) loops ensure that DC offsets, generated in the CX74017, do not overload the baseband chain at any point. After compensation, the correction voltages are held on capacitors for the duration of the receive slot(s). Internally, on chip timing is provided to generate the track and hold (T_H) signals for the three correction loops.

The timing diagram for the DC offset correction sequence with reference to the receive slot is shown in Figure 3. A rising edge on either the RXENA signal or the T_H signal, selected via the serial interface, places the DC compensation circuitry in the track mode.

The timing parameters for each of the three compensation loops, t_{T_H1}, t_{T_H2}, and t_{T_H3}, and the time between compensation start and the LNA being turned on, t_{FEENA}, are defined via an internal state machine. The state machine is preprogrammed with fixed default values, but may be readjusted via the serial interface.

The timing parameters for the three compensation loops and the LNA power-up are each independently defined, relative to the compensation start. Therefore, they may be programmed to occur in any order, but the sequences shown in Figure 3 and Figure 4 are recommended.

Table 2. Receive Pole Locations

State	Typical Pole Location (rad/sec)	Pole Type
Mixer + RC Filter	-1.0×10^6	Real. (capacitors at pins 27-28 and 29-30 fixed at 470 pF)
	-1.65×10^6	Real
LPF1	$(-0.91 \times 10^6) \pm j(1.35 \times 10^6)$	Conjugate
VGA1 + gmC Filter	$(-0.91 \times 10^6) \times (39.2\ k\Omega/R)$	Real. (adjust with resistor at pin 31; 39.2 kΩ nominal, 36 kΩ minimum)
	$(-0.91 \times 10^6) \times (39.2\ k\Omega/R)$	Real. (adjust with resistor at pin 31; 39.2 kΩ nominal, 36 kΩ minimum)
	$[(-0.46 \times 10^6) \pm j(1.0 \times 10^6)] \times (39.2\ k\Omega/R)$	Conjugate. (adjust with resistor at pin 31)

The device default timing is shown in Figure 4, with a total time of 60 µs. Individual default timings are given in Table 17. For user-programmed timing, the total time may be set as short as approximately 10 µs when FREF has a 13 MHz clock applied. However, the shortest recommended total time is approximately 30 µs, since at the highest gain settings, the resulting DC may degrade as correction time is reduced below that value.

AM Suppression and IP2 Calibration

For direct conversion GSM applications, it is imperative to have extremely low 2nd order distortion. Mathematically, 2nd order distortion of a constant tone generates a DC-term proportional to the square of the amplitude. A strong interfering AM signal is therefore demodulated by 2nd order distortion in the receiver front end, and generates an interfering baseband signal.

A commonly used measure for receiver 2nd order distortion is the 2nd order intercept point (IP2). For example, to ensure that the unwanted baseband signals are 9 dB below the wanted signal required under the AM suppression test for type approval (see 3GPP TS 51.010-1, section 14.8), an input IP2 of 43 dBm is generally required.

The CX74017 receiver includes a circuit for minimizing 2nd order distortion. This IP2 calibration circuit effectively compensates any 2nd order distortion in the receive chain that would otherwise generate unwanted baseband signals in the presence of strong interfering signals. When calibrated correctly, the CX74017 IP2 meets the GSM AM suppression test requirements in all bands with good margin.

The IP2 calibration is simply done by applying a strong Continuous Wave (CW) RF signal at the receiver input, and observing the resulting DC 2nd order Inter-Modulation (IM2) voltage level change at the receiver I/Q outputs (or, the applied RF may be a two-tone or an AM signal with an observed AC IM2). The exact frequency and level of the signal applied for the purpose of the calibration are not critical. The signal should, however, be within the receive band, but at least 6 MHz offset from the frequency to which the receiver is tuned. The level should be high enough to cause a notable IM2 product at the I/Q outputs. A recommended value is –30 dBm at the LNA input, which applies to all three LNAs.

A set of I/Q compensation coefficients can then be programmed to the device to minimize the IM2 product resulting from the 2nd order distortion. When the IM2 due to the interfering signal is minimized, the IP2 performance is optimized.

***Note**: SXENA, pin 43, must be held high, and a clock signal must be present on FREF, pin 38, during the programming of the IP2 calibration coefficients in Register 3 (see Table 18).*

The IP2 calibration is a one-time factory calibration that should be done for each band and each individual device for optimum performance. The determined coefficients must be stored in nonvolatile memory and programmed to the CX74017 upon each power-up as part of device initialization. There are on-chip registers that must be programmed through Register 3 with the appropriate IP2 coefficients for the band in use.

As long as a supply voltage is maintained on pin 48, VDDBB, the IP2 coefficients for $I_{LOWBAND}$, $I_{HIGHBAND}$, $Q_{LOWBAND}$, $Q_{HIGHBAND}$, programmed to the device remain in the registers. After the supply voltage has been removed from VDDBB, the coefficients must be re-programmed to the device again.

Synthesizer Section

The CX74017 includes a fully integrated UHF VCO with an on chip LC tank.

A single sigma-delta fractional-N synthesizer can phase-lock the local oscillator used in both transmit and receive paths to a precision frequency reference input. Fractional-N operation offers low phase noise and fast settling times, allowing for multiple slot applications such as GPRS. The CX74017 frequency stepping function with a 3 Hz resolution allows triple band operation in both transmit and receive bands using a single, fully integrated UHF VCO. The fine synthesizer

resolution allows direct compensation or adjustment for reference frequency errors.

The fractional-N synthesizer consists of the following:

- VCO
- High frequency prescaler
- N-divider with a sigma-delta modulator
- Reference buffer and divider
- Fast phase frequency detector and charge pump

The user must provide the following three parameters:

- The reference divider value, from 1 to 15
- The N-divider value, in a manner similar to an integer-N synthesizer
- A fractional ratio

The generated frequency is given by the following equation:

$$f_{VCO} = \frac{\left(N + 3.5 + \frac{FN}{2^{22}}\right) f_{ref}}{R}$$

where: f_{VCO} = Generated VCO frequency
N = N-divider ratio integer part
FN = Fractional setting
R = R-divider ratio
f_{REF} = Reference frequency

UHF VCO Frequency Setting

For the receiver, to tune the receive frequency, f_{RX}, set the VCO frequency, f_{VCO}, as follows:

- $f_{VCO} = \frac{3}{2} f_{RX}$ for GSM850/900
- $f_{VCO} = \frac{3}{4} f_{RX}$ for DCS1800 and PCS1900

For the transmitter VCO frequency, refer to the equations shown in Figure 6.

Digital Frequency Centering

The CX74017 uses a novel technique whereby the UHF VCO frequency range is re-centered each time the synthesizer is programmed. This technique is called Digital Frequency Centering (DFC). The DFC technique:

- Extends the VCO frequency coverage
- Speeds up settling time
- Ensures robust performance since the VCO is always operated at the center of its tuning range.

Each time the synthesizer is programmed, the DFC circuit is activated, and the VCO is centered to the programmed frequency in less than 20ms. After this, normal Phase Locked Loop (PLL) operation is resumed and the fine settling of the frequency is finalized. The DFC typically adjusts the VCO center frequency to within a few MHz and no more than 5 MHz offset, and presets the tuning voltage to the center of the range before the PLL takes over. This speeds up frequency settling and ensures that the PLL control voltage never operates close to the rails.

The DFC is an adaptive circuit that corrects for any VCO center frequency errors caused by variations of the integrated VCO circuit, temperature, supply voltage, aging etc. The VCO can be centered at any frequency in the range from 1.2 GHz to 1.55 GHz. Once centered, the VCO has a minimum analog tuning range of 30 MHz.

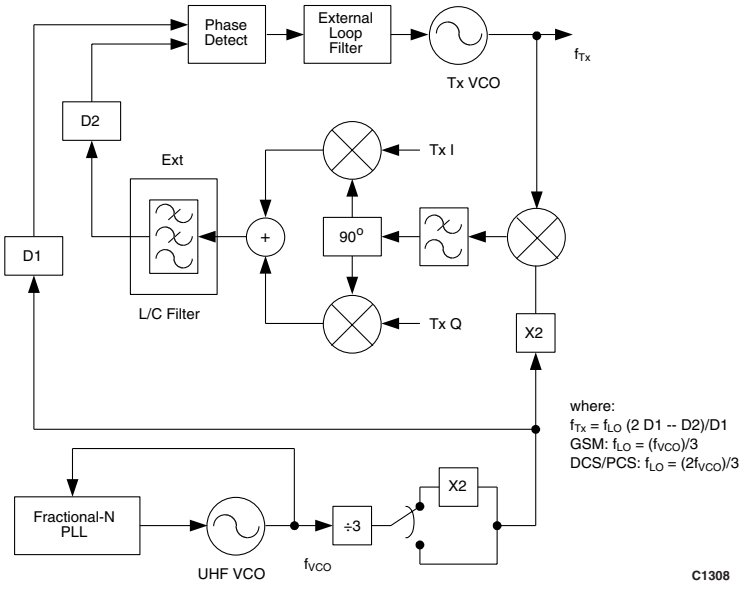


Figure 6. Transmitter Frequency Generation

No calibration or data storage is needed for DFC operation. It is activated by one of two events:

- When the synthesizer is programmed, the rising edge of the LE signal starts the DFC cycle and,
- When changing the level of the SXENA signal from low to high, thereby turning on the synthesizer, the rising edge of the SXENA signal starts the DFC cycle.

Transmit Section

To minimize the post-PA filtering requirements and any additional post-PA losses, the transmit path consists of a vector modulator within a frequency translation loop. The translation loop consists of the following:

- Phase Frequency Detector (PFD) and charge pump
- Mixer with an operating range of 800 MHz to 2 GHz
- An in-loop modulator
- Two programmable dividers
- Two transmit VCOs

Translational Loop

The translational loop takes baseband analog I/Q signals and modulates them with the mixed product of transmitter output and LO signal, as shown in Figure 6. The unmodulated result is compared with a divided down LO at the PFD and the difference is used to control the transmit VCO. The on-chip Lowpass Filter (LPF) following the mixer attenuates the unwanted sidebands as well as harmonics.

Transmit VCOs

Two on-chip transmit VCOs are designed to meet GSM850, EGSM900, DCS1800, and PCS1900 requirements. The transmit VCOs use the same digital frequency centering technique as described in the Synthesizer section to lock the translational loop. The rising edge on TXENA initializes the transmit DFC.

Electrical and Mechanical Specifications

The absolute maximum ratings of the CX74017 are provided in Table 3. The recommended operating conditions are specified in Table 4 and power consumption specifications are provided in Table 5. Electrical specifications are provided in Tables 6 through 11.

Serial interface programming details are shown in Tables 12 through 22, and serial interface timing curves are shown in Figures 7, 8, and 9.

Receiver data is provided in Tables 23 through 31. Figures 10 through 27 show frequency and impedance characterization curves.

Figure 28 shows a typical application circuit diagram. Package dimensions for the 64-pin LGA are shown in Figure 29, Figure 30 provides the tape and reel dimensions, and Figure 31 provides shipping tray dimensions.

Package and Handling Information

Because this device package is sensitive to moisture absorption, it is baked and vacuum packed before shipment according to IPC J-STD 033 guidelines. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. These instructions adhere to IPC J-STD 020A guidelines for handling moisture sensitive devices. If these instructions are not followed, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

If the CX74017-16 part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second. Maximum temperature should not exceed 225 °C and the time spent at a temperature that exceeds 210 °C should be limited to less than 10 seconds.

If the CX74017-16 part is manually attached, precaution should be taken to ensure that the part is not subjected to a temperature exceeding 300 °C for more than 10 seconds. Care must be taken when this product is attached, whether it is done manually or in a production solder reflow environment.

If the CX74017-17 part is attached in a reflow oven, the temperature ramp rate should not exceed 3 °C per second. Maximum temperature should not exceed 250 °C and the time spent at a temperature that exceeds 245 °C should be limited to less than 15 seconds.

If the CX74017-17 part is manually attached, precaution should be taken to ensure that the part is not subjected beyond a maximum temperature of 250 °C or exceeds 245 °C for more than 15 seconds. Care must be taken when this product is attached, whether it is done manually or in a production solder reflow environment, to NOT heat the part beyond the recommended temperature. Measure the temperature on the package itself by attaching thermocouples to the package body.

For additional details on both attachment techniques, precautions, and recommended handling procedures, refer to the Skyworks' Application Note, *PCB Design & SMT Assembly Guidelines for RFLGA Packages*, document number 103147.

Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks' Application Note, *Tape and Reel*, document number 101568. Typical case markings for the CX74017 are shown in Figure 32.

Electrostatic Discharge (ESD) Sensitivity

The CX74017 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

Table 3. CX74017 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply voltage (VCC)	–0.3	+3.6	V
Ambient operating temperature range	–40	+95	°C
Storage temperature range	–50	+125	°C
Input voltage range	GND	VCC	V
Maximum power dissipation		600	mW

Note: Stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.

Table 4. CX74017 Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
LNA input level (pins 11, 13, 15), RXEN = Off			10	dBm
Power supply	2.6	2.8	3.3	V
Digital power supply, VDDBB	1.8		3.3	V
Operating junction temperature	–40		+110	°C
Operating ambient temperature	–20		+85	°C

Table 5. Power Consumption Specifications
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Total supply current:	I_{CC}					
Rx section, EGSM/GSM850		RXENA = H; SXENA = L		41	48	mA
Tx section, EGSM/GSM850 (includes TX VCO)		TXENA = H; SXENA = L		118	135	mA
Synthesizer section, EGSM/GSM850 (includes UHF VCO)		SXENA = H		38	45	mA
Rx section, DCS/PCS		RXENA = H; SXENA = L		49	58	mA
Tx section, DCS/PCS (includes TX VCO)		TXENA = H; SXENA = L		124	141	mA
Synthesizer section, DCS/PCS (includes UHF VCO)		SXENA = H		38	45	mA
Sleep mode		@ VCC = 3.3 V RXENA = L; TXENA = L; SXENA = L		20	100	µA

Table 6. CX74017 Electrical Specifications – EGSM/GSM850 Receiver (1 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition (Note 1)	Min	Typical	Max	Units
Input impedance. See Figure 12 for unmatched input impedance.	Z_{IN}	With external match		50		Ω
Input operating frequency	Band 1		869		960	MHz
Receiver maximum voltage gain	G_{RXMAX}	Highest gain mode	120	126		dB
Receiver minimum voltage gain	G_{RXMIN}	Lowest gain mode		11	17	dB
Receiver gain temperature variation	$G_{TEMPVAR}$	T_A = –20 °C to +85 °C			4	dB
Gain step	ΔA_V			2		dB
Gain step accuracy	G_{STEP}	Over range recommended in Table 23	–0.75		+0.75	dB
Gain variation versus frequency	G_{FREQ}	Over 869-894 MHz Over 925-960 MHz			2 2	dB dB
Noise Figure	NF_{GAIN1}	G = 15/40/10/12/0/18		3.2	3.9	dB
Noise Figure (temperature)	NF_{TEMP}	T_A = +75 °C T_A = +85 °C G = 15/40/10/12/0/18			5.0 5.2	dB dB
Noise Figure degradation in presence of blocker	NF_{BLOC}	With –26 dBm input blocker @ 3 MHz offset (ideal LO) Internal LO G = 15/40/10/12/0/18		2 4		dB dB
Input 2nd order intercept point	IIP2	Referred to LNA input calibrated and measured at middle of EGSM or GSM850 band	50	65		dBm
DC shift in presence of blocker	AM Supp	With –34 dBm @ 6 MHz offset G = 15/40/10/12/0/18			17	mV
LO re-radiation @ LNA input	LOREV	@ wanted frequency		–110	–100	dBm
Selectivity		@ 3 MHz offset @ 1.6 MHz offset @ 600 kHz offset @ 400 kHz offset @ 200 kHz offset T_A = –20 °C to + 85 °C	143 128 61 37 9	 137 68 44 13		dB dB dB dB dB
I/Q amplitude imbalance		T_A = –20 °C to +85 °C			1	dB
I/Q phase imbalance		T_A = –20 °C to +85 °C	–3		3	degrees

Table 6. CX74017 Electrical Specifications – EGSM/GSM850 Receiver (2 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition (Note 1)	Min	Typical	Max	Units
Input 1 dB compression point	IP1dB	F = 200 kHz, G = 15/40/–2/8/0/18	–65	–60		dBm
		F = 400 kHz, G = 15/40/–2/8/0/18	–45	–40		dBm
		F = 600 kHz, G = 15/40/10/12/0/18	–35	–30		dBm
		F = 1.6 MHz, G = 15/40/10/12/0/18	–32	–28		dBm
		F = 3.0 MHz, G = 15/40/10/12/0/18	–25	–22		dBm
3rd order input intercept point @ +25 °C	IIP3	F = 3.0 MHz G = 15/40/10/12/0/18	–15	–12		dBm
3rd order input intercept point @ –20 °C	IIP3	F = 3.0 MHz G = 15/40/10/12/0/18	–15	–12		dBm
Output offset voltage		With DC offset corrected while LNA is off			200	mV
		T_A = +85°C			220	mV
		With DC offset corrected while LNA is on G = 15/40/10/12/0/18			20	mV
		T_A = +85 °C			25	mV
		(Note: 60 µs total DC correction time)				
Offset drift (long term)	DCDRFT1	G = 15/40/10/12/0/18 50 ms after correction			100	mV
Offset drift (short term)	DCDRFT2	G = 15/40/10/12/0/18 577 µs after correction			10	mV
Baseband Tunable Active Filter						
3 dB corner frequency (tunable)	F_C	Variable resistance at pin 31 (36 kΩ minimum)	80		100	kHz
Corner frequency variation	dF_C	39.2 kΩ at pin 31, 470 pF at pins 27-28 and 29-30	–11		+11	%
Receiver Output Stage						
Differential output amplitude (pk/pk differential)		VGA2 = 30 dB	3.7			V
		VGA2 = 0 dB	0.3			V
Output common mode voltage		T_A = –20 °C to +85 °C	VCC/2 – 0.1	VCC/2	VCC/2 + 0.1	V
Maximum current drive	I_{OUT}				0.5	mA
Output resistance	R_{OUT}		160	200	240	Ω
Output capacitance	C_{OUT}				1	pF

Note 1: Gain codes refer to LNA/mixer/LPF1/VGA1/AUX/VGA2 gains in dB.

Table 7. CX74017 Electrical Specifications – DCS1800 Receiver (1 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition (Note 1)	Min	Typical	Max	Units
Input impedance See Figure 13 for unmatched input impedance.	Z_{IN}	With external match		50		Ω
Input operating frequency	Band 2	DCS Rx band	1805		1880	MHz
Receiver maximum voltage gain	G_{RXMAX}	Highest gain mode	117	123		dB
Receiver minimum voltage gain	G_{RXMIN}	Lowest gain mode		9	15	dB
Gain step	ΔA_V			2		dB
Receiver gain temperature variation	$G_{TEMPVAR}$	T_A = – 20 °C to +85 °C			4	dB
Gain step accuracy	G_{STEP}	Over range recommended in Table 24	–0.75		+0.75	dB
Gain variation versus frequency	G_{FREQ}	Over band 2			2	dB
Noise Figure	NF_{GAIN1}	G = 15/40/10/12/0/18		3.6	4.3	dB
Noise Figure (temperature)	NF_{TEMP}	T_A = +75 °C T_A = +85 °C			5.4 5.6	dB dB
Noise Figure degradation in presence of blocker	NF_{BLOC}	With –30 dBm input blocker @ 3.0 MHz offset (ideal LO) Internal LO G = 15/40/10/12/0//18		2 4		dB dB
Input 2nd order intercept point	IIP2	Referred to LNA input calibrated and measured at middle of DCS1800 band	50	65		dBm
DC shift in presence of blocker	AM Supp	With –33 dBm @ 6 MHz offset G = 15/40/10/12/0/18			17	mV
LO re-radiation @ LNA input	LOREV	@ wanted frequency		–110	–100	dBm
Selectivity		@ 3 MHz offset @ 1.6 MHz offset @ 600 kHz offset @ 400 kHz offset @ 200 kHz offset T_A = –20 °C to +85 °C	143 128 61 37 9	 137 68 41 13		dB dB dB dB dB
I/Q amplitude imbalance		T_A = –20 °C to +85 °C			1	dB
I/Q phase imbalance		T_A = –20 °C to +85 °C	–3		+3	degrees

Table 7. CX74017 Electrical Specifications – DCS1800 Receiver (2 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition (Note 1)	Min	Typical	Max	Units
Input 1 dB compression point	IP1dB	F = 200 kHz, G = 15/40/–2/8/0/18	–65	–60		dBm
		F = 400 kHz, G = 15/40/–2/8/0/18	–45	–40		dBm
		F = 600 kHz, G = 15/40/10/12/0/18	–35	–30		dBm
		F = 1.6 MHz, G = 15/40/10/12/0/18	–32	–28		dBm
		F = 3.0 MHz, G = 15/40/10/12/0/18	–25	–22		dBm
3rd order input intercept point @ + 25 °C	IIP3	F = 3.0 MHz G = 15/40/10/12/0/18	–15	–12		dBm
3rd order input intercept point @ –20 °C	IIP3	F = 3.0 MHz G = 15/40/10/12/0/18	–15	–12		dBm
Output offset voltage		With DC offset corrected while LNA is off			200	mV
		T_A = +85°C			220	mV
		With DC offset corrected while LNA is on G = 15/40/10/12/0/18			20	mV
		T_A = +85 °C			25	mV
		(Note: 60 µs total DC correction time)				
Offset drift (long term)	DCDRFT1	G = 15/40/10/12/0/18 50 ms after correction			100	mV
Offset drift (short term)	DCDRFT2	G = 15/40/10/12/0/18 577 µs after correction			10	mV
Baseband Tunable Active Filter						
3 dB corner frequency (tunable)	F_C	Variable resistance at pin 31 (36 kΩ minimum)	80		100	kHz
Corner frequency variation	dF_C	39.2 kΩ at pin 31, 470 pF at pins 27-28 and 29-30	–11		+11	%
Receiver Output Stage						
Differential output amplitude (pk/pk differential)		VGA2 = 30 dB	3.7			V
		VGA2 = 0 dB	0.3			V
Output common mode voltage			VCC/2 – 0.1	VCC/2	VCC/2 + 0.1	V
Maximum current drive	I_{OUT}				0.5	mA
Output resistance	R_{OUT}		160	200	240	Ω
Output capacitance	C_{OUT}				1	pF

Note 1: Gain codes refer to LNA/mixer/LPF1/VGA1/AUX/VGA2 gains in dB.

Table 8. CX74017 Electrical Specifications – PCS1900 Receiver (1 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition (Note 1)	Min	Typical	Max	Units
Input impedance. See Figure 14 for unmatched input impedance.	Z_{IN}	With external match		50		Ω
Input operating frequency	Band 3	PCS Rx band	1930		1990	MHz
Receiver maximum voltage gain	G_{RXMAX}	Highest gain mode	117	123		dB
Receiver minimum voltage gain	G_{RXMIN}	Lowest gain mode		7	13	dB
Receiver gain temperature variation	$G_{TEMPVAR}$	T_A = –20 °C to +85 °C			4	dB
Gain step	ΔA_V			2		dB
Gain step accuracy	G_{STEP}	Over range recommended in Table 25	–0.75		+0.75	dB
Gain variation versus frequency	G_{FREQ}	Over band 3			2	dB
Noise Figure	NF_{GAIN1}	G = 15/40/10/14/0/18		4.2	4.9	dB
Noise Figure (Temperature)	NF_{TEMP}	T_A = +75 °C T_A = +85 °C			6.0 6.2	dB dB
Noise Figure degradation in presence of blocker	NF_{BLOC}	With –30 dBm input blocker @ 3.0 MHz offset (ideal LO) Internal LO G = 15/40/10/14/0//18		2 4		dB dB
Input 2nd order intercept point	IIP2	Referred to LNA input calibrated and measured at middle of PCS1900 band	50	65		dBm
DC shift in presence of blocker	AM Supp	With –33 dBm @ 6 MHz offset G = 15/40/10/14/0/18			17	mV
LO re-radiation @ LNA input	LOREV	@ wanted frequency		–110	–100	dBm
Selectivity		@ 3 MHz offset @ 1.6 MHz offset @ 600 kHz offset @ 400 kHz offset @ 200 kHz offset T_A = –20 °C to +85 °C	143 128 61 37 9	 137 68 41 13		dB dB dB dB dB
I/Q amplitude imbalance		T_A = –20 °C to +85 °C			1	dB
I/Q phase imbalance		T_A = –20 °C to +85 °C	–3		+3	degrees

Table 8. CX74017 Electrical Specifications – PCS1900 Receiver (2 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition (Note 1)	Min	Typical	Max	Units
Input 1 dB compression point	IP1dB	F = 200 kHz, G = 15/40/–2/8/0/18	–65	–60		dBm
		F = 400 kHz, G = 15/40/–2/8/0/18	–45	–40		dBm
		F = 600 kHz, G = 15/40/10/14/0/18	–35	–30		dBm
		F = 1.6 MHz, G = 15/40/10/14/0/18	–32	–28		dBm
		F = 3.0 MHz, G = 15/40/10/14/0/18	–25	–22		dBm
3rd order input intercept point @ +25 °C	IIP3	F = 3.0 MHz G = 15/40/10/14/0/18	–15	–12		dBm
3rd order input intercept point @ –20 °C	IIP3	F = 3.0 MHz G = 15/40/10/14/0/18	–15	–12		dBm
Output offset voltage		With DC offset corrected while LNA is off			200	mV
		T_A = +85 °C			220	mV
		With DC offset corrected while LNA is on G = 15/40/10/12/0/18			20	mV
		T_A = +85 °C			25	mV
		(Note: 60 µs total DC correction time)				
Offset drift (long term)	DCDRFT1	G = 15/40/10/14/0/18 50 ms after correction			100	mV
Offset drift (short term)	DCDRFT2	G = 15/40/10/14/0/18 577 µs after correction			10	mV
Baseband Tunable Active Filter						
3 dB corner frequency (tunable)	F_C	Variable resistance at pin 31 (36 kΩ minimum)	80		100	kHz
Corner frequency variation	dF_C	39.2 kΩ at pin 31, 470 pF at pins 27-28 and 29-30	–11		+11	%
Receiver Output Stage						
Differential output amplitude (pk/pk differential)		VGA2 = 30 dB	3.7			V
		VGA2 = 0 dB	0.3			V
Output common mode voltage			VCC/2 – 0.1	VCC/2	VCC/2 + 0.1	V
Maximum current drive	I_{OUT}				0.5	mA
Output resistance	R_{OUT}		160	200	240	Ω
Output capacitance	C_{OUT}				1	pF

Note 1: Gain codes refer to LNA/mixer/LPF1/VGA1/AUX/VGA2 gains in dB.

Table 9. CX74017 Electrical Specifications – Transmitter (1 of 3)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
I/Q Modulator						
Differential input impedance	Z_{IN}		16	20	24	kΩ
Input signal level		Differential	0.8	1	1.2	Vp-p
Input common mode voltage range	V_{CM}		0.85	1.35	VCC – 1.3	V
Input frequency 3 dB bandwidth				3		MHz
Input common mode rejection ratio		f_{IN} = 100 kHz f_{IN} = 1 MHz	65 45	75 55		dB dB
Output operating frequency	f_{OUT}		70		130	MHz
Output impedance	Z_{OUT}	Per side	170	200	230	Ω
Output voltage	V_{OUT}			–33		dBV
Output noise power	N_0	@ 10 MHz offset @ 1.8 MHz offset		–132 –130	–128 –126	dBc/Hz dBc/Hz
LO suppression			30	35		dBc
Sideband suppression			30	35		dBc
Translational Loop						
Spurious		Modulation 2nd order Modulation 3rd order		–70 –60	–40 –55	dBc dBc
Transmit frequency (input from VCO)	f_{TX}		800		2000	MHz
IF frequency	f_{IF}		70		130	MHz
Transmit input power	P_{IN}	With external 50 Ω termination	–20	–15	–10	dBm
Transmit input impedance	Z_{IN}			300// 0.3		Ω// pF
Transmitter output phase noise (Includes TX VCO and LO PLL)	N_0	@ 400 kHz offset @ 1.8 MHz offset @ 10 MHz offset EGSM/GSM850 @20 MHz offset EGSM/GSM850 @20 MHz offset DCS/PCS		–120 –130 –152 –164 –156	–118 –124 –150 –162 –154	dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Tx phase error	Tx_{PHERR}	rms Employs reference frequency source, and loop filters as shown in the reference design.		2.0		degrees

Table 9. CX74017 Electrical Specifications – Transmitter (2 of 3)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Translational Loop (continued)						
Charge pump output current: high impedance source/sink	I_{OUT}	RX/TX control register bits S15 S14 CP = 0 0 CP = 0 1 CP = 1 0 CP = 1 1		 ±0.5 ±1.0 ±2.0 ±2.0		 mA mA mA mA
Charge pump current variation		$0.3 \le V_{CPO} \le VCC - 0.5$			20	%
Charge pump current variation over temperature		$0.3 \le V_{CPO} \le VCC - 0.5$ T_A = –20 °C to +85 °C		10		%
D1 divide ratio range			9		12	
D2 divide ratio			1		2	
Tx mixer LO leakage	TXMIX LEAKAGE	Tx mixer 50 Ω terminated			–60	dBm
Low Band Translation Loop VCO						
Center frequency	f_C	T_A = –20 °C to +85 °C	800		930	MHz
Digital frequency centering resolution	e_{DFC}			2.5		MHz
Digital frequency centering time	t_{DFC}	From rising edge of TXENA (13 MHz clock frequency)		12	20	µs
Digital frequency centering voltage	V_{DFC}	(Control voltage at end of DFC/start of analog lock)	VCC/2 – 0.2	VCC/2	VCC/2 + 0.2	V
Analog frequency control range	$f_{MAX} - f_{MIN}$	$0.5 < V_{CTL} < 2.2$	20			MHz
Absolute control sensitivity	K_{VCO}	(0.9 V < V_{CTL} and 1.9 V > V_{CTL}): 820 MHz < f_C < 850 MHz 870 MHz < f_C < 915 MHz	 16 18	 21 25	 26 32	 MHz/V MHz/V
Output harmonics		2nd harmonic 3rd harmonic		–50 –55	–30 –30	dBc dBc
Phase noise		@ 400 kHz offset @ 20 MHz offset		–125 –164	–120 –162	dBc/Hz dBc/Hz
Output VSWR		with external 50 Ω match			2:1	
Pushing				2	4	MHz/V
Pulling		VSWR 2:1			± 4	MHz

Table 9. CX74017 Electrical Specifications – Transmitter (3 of 3)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Low Band Translation Loop VCO (continued)						
Output power	P_{OUT}	F_{OUT} = 897.5 MHz with external 50 Ω match	10.5	11.5	12.5	dBm
Output power temperature variation		T_A = –20°C to +85°C		±0.7		dB
High Band Translation Loop VCO						
Center frequency	f_C	T_A = –20 °C to +85 °C	1700		1930	MHz
Digital frequency centering resolution	e_{DFC}			6		MHz
Digital frequency centering time	t_{DFC}	From rising edge of TXENA (13 MHz clock frequency)		12	20	µs
Digital frequency centering voltage	V_{DFC}	(Control voltage at end of DFC/start of analog lock)	VCC/2 – 0.2	VCC/2	VCC/2 + 0.2	V
Analog frequency control range	$f_{MAX} - f_{MIN}$	0.5 < V_{CTL} < 2.2	20			MHz
Absolute control sensitivity	K_{VCO}	(0.9 V < V_{CTL} and 1.9 V > V_{CTL})				
		1710 MHz < f_C < 1785 MHz	14	18	22	MHz/V
		1850 MHz < f_C < 1910 MHz	19	23	27	MHz/V
Output harmonics		2nd harmonic		–50	–30	dBc
		3rd harmonic		–55	–30	dBc
Phase noise		@ 400 kHz offset		–125	–120	dBc/Hz
		@ 20 MHz offset		–158	–155	dBc/Hz
Output VSWR		with external 50 Ω match			2:1	
Pushing				2	4	MHz/V
Pulling		VSWR 2:1			± 4	MHz
Output power	P_{OUT}	F_{OUT} = 1747.5 MHz with external 50 Ω match	5.5	7	8.5	dBm
Output power variation		T_A = –20°C to +85°C		±1		dB

Table 10. CX74017 Electrical Specifications – Synthesizer (1 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Prescaler operating input frequency			1000		1700	MHz
Reference input frequency			10	13	26	MHz
Phase detector frequency				13	15	MHz
Input sensitivity			–15		+3	dBm
Reference oscillator sensitivity			0.4		VCC	V_{PEAK}
In-band phase noise		Measured within the loop bandwidth		–85		dBc/Hz
Charge pump output current (can be programmed in four steps)		V_{CP} = VCCFN_CP/2 (SX reg.1 b6,b5 =00)		100		µA
		V_{CP} = VCCFN_CP/2 (SX reg.1 b6,b5 =01)		200		µA
		V_{CP} = VCCFN_CP/2 (SX reg.1 b6,b5 =10)		300		µA
		V_{CP} = VCCFN_CP/2 (SX reg.1 b6,b5 =11)		400		µA
Charge pump leakage current		$0.5 < V_{CP} <$ VCCFN_CP – 0.5		0.1		nA
Charge pump sink versus source mismatch		V_{CP} = VCCFN_CP/2		5		%
Charge pump current versus voltage		$0.5 < V_{CP} <$ VCCFN_CP – 0.5		10		%
Charge pump current versus temperature		V_{CP} = VCCFN_CP/2 T_A = –20 °C to +85 °C		10		%
UHF VCO						
Center frequency	f_C	T_A = –20 °C to +85 °C	1200		1550	MHz
Digital frequency centering resolution	e_{DFC}			2		MHz
Digital frequency centering time	t_{DFC}	From rising edge of SXENA or LE when programming SX word (13 MHz clock frequency)		12	20	µs
Digital frequency centering voltage	V_{DFC}	Control voltage at end of DFC/start of analog lock	VCCUHF/2 – 0.2	VCCUHF/2	VCCUHF/2 + 0.2	V
Analog frequency control range	$f_{MAX} - _{MIN}$	$0.5 < V_{CTL} < 2.2$	30			MHz

Table 10. CX74017 Electrical Specifications – Synthesizer (2 of 2)
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
UHF VCO (continued)						
Relative control sensitivity	K_{VCO}/f_C	After DFC, within the range of V_{DFC} ±0.5 V				
		1200 MHz < f_C < 1300 MHz	1.3	1.7	2.1	%/V
		1300 MHz < f_C < 1400 MHz	1.5	2.0	2.4	%/V
		1400 MHz < f_C < 1475 MHz	1.7	2.2	2.6	%/V
		1475 MHz < f_C < 1550 MHz	1.9	2.4	2.8	%/V
Absolute control sensitivity	K_{VCO}	V_{DFC} – 0.5 V < V_{CTL} and V_{DFC} + 0.5 V > V_{CTL}				
		1200 MHz < f_C < 1300 MHz	15	21	28	MHz/V
		1300 MHz < f_C < 1400 MHz	19	27	34	MHz/V
		1400 MHz < f_C < 1475 MHz	24	32	39	MHz/V
		1475 MHz < f_C < 1550 MHz	28	36	44	MHz/V
Phase noise		@ 400 kHz offset		–123	–121	dBc/Hz
		@ 3.0 MHz offset		–140	–137	dBc/Hz
Slow center frequency drift	$\Delta f_C/\Delta t$	T_A = –20°C to +85°C	–5		5	MHz/sec

Table 11. CX74017 Electrical Specifications – Digital Interface
(T_A = 25 °C, VCC = 2.8 V unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Data to clock setup time, see Figure 7	T_{CS}		50			ns
Data to clock hold time, see Figure 7	T_{CH}		10			ns
Clock pulse width high, see Figure 7	T_{CWH}		50			ns
Clock pulse width low , see Figure 7	T_{CWL}		50			ns
Clock to load enable setup time, see Figure 7	T_{ES}		50			ns
Load enable pulse width, see Figure 7	T_{EW}		50			ns
LE falling edge to clock rising edge, see Figure 7	T_{EFC}		50			ns
RXENA setup time TXENA setup time SXENA setup time FEENA setup time			50 50 50 50			ns ns ns ns
High level input voltage for RXENA, TXENA, DATA, CLK, LE, PCO1, PCO2, T_H, FEENA, and SXENA	V_{IH}		0.8 x VDDBB			V
Low level input voltage for RXENA, TXENA, DATA, CLK, LE, PCO1, PCO2, T_H, FEENA, and SXENA	V_{IL}				0.2 x VDDBB	V
High level input current for RXENA, TXENA, DATA, CLK, LE, PCO1, PCO2, T_H, FEENA, and SXENA	I_{IH}		–1		+1	µA
Low level input current for RXENA, TXENA, DATA, CLK, LE, PCO1, PCO2, T_H, FEENA, and SXENA	I_{IIL}		–1		+1	µA
Digital input pin capacitance for RXENA, TXENA, DATA, CLK, LE, PCO1, PCO2, T_H, FEENA, and SXENA	C_{ID}				10	pF
High level output voltage for PCO1, PCO2, and LD_MUX	V_{OH}	I_{OH} = –1.0 mA	VDDBB – 0.4			V
Low level output voltage for PCO1, PCO2, and LD_MUX	V_{OL}	I_{OL} = +1.0 mA			0.4	V
Digital output pin load capacitance for PCO1, PCO2, and LD_MUX	C_{LD}				15	pF

Serial Interface Programming

Table 12. Control and Output States

Register	Address Bits					
	B5	B4	B3	B2	B1	B0
SX register 1: Synthesizer Control	X	X	X	X	0	0
SX register 2: Fractional-N Modulo	X	X	X	X	1	0
R0: Auxiliary Control	X	X	0	0	0	1
R1: Test Register	X	X	0	1	0	1
R2: DC Offset Timing	X	X	1	0	0	1
R3: IP2 Calibration	0	0	1	1	0	1
R4: Test Register	0	1	1	1	0	1
Not used	1	0	1	1	0	1
R5: Test Register	1	1	1	1	0	1
RX/TX Control Register	X	X	X	X	1	1

Table 13. SX Register 1: Synthesizer Control Functions

Symbol	Function	State Description
ADDR	Address bits [1:0]. Must be set to 00b (see Table 12)	
EN	Enable mode [2]	0 enables synthesizer 1 disables synthesizer
EF	Integer mode [3]	0 sets integer-N mode 1 sets fractional-N mode
SP	Phase detector output polarity [4]	0 sets phase detector output for negative VCO gain 1 sets phase detector output for positive VCO gain
SC	Charge pump output current [6:5]	Bit [6:5]: 0 0 sets charge pump current to 100 µA 0 1 sets charge pump current to 200 µA 1 0 sets charge pump current to 300 µA 1 1 sets charge pump current to 400 µA
LD	Test mode [8:7]	Bit [8:7]: 0 0 multiplexes N divider output to LD_MUX (pin 44) 0 1 multiplexes R divider output to LD_MUX (pin 44) 1 0 multiplexes lock detect output to LD_MUX (pin 44) 1 1 sets charge pump output to high impedance
N	Main divider [19:9]	Sets 11-bit main divider ratio range (64 to 2047)
R	Reference divider [23:20]	Sets 4-bit reference divider ratio range (1 to 15)

Table 14. SX Register 2: Fractional-N Modulo

Symbol	Function	State Description
ADDR	Address bits [1:0]. Must be set to 10b (see Table 12)	
FN	Fractional-N modulo [23:2]	Sets fractional-N modulo up to 2^{22} range (0 to 4, 194, 303)

Table 15. Register 0: Auxiliary Control

Symbol	Function	State Description	Default (Binary)
ADDR	Address bits [3:0]. Must be set to 0001b (see Table 12)		
GMC_BYP	Bypass GMC stage [4]	0 enables gmC filter stage 1 disables and bypasses gmC filter stage	0
SK_BYP	Bypass S-K stage [5]	0 enables Sallen-Key filter stage 1 disables and bypasses Sallen-Key filter stage	0
DC_BYP1	Bypass first DC OC loop [6]	0 enables first DC offset correction loop 1 disables and bypasses first DC offset correction loop	0
DC_BYP2	Bypass second DC OC loop [7]	0 enables second DC offset correction loop 1 disables and bypasses second DC offset correction	0
DC_BYP3	Bypass second DC OC loop [8]	0 enables third DC offset correction loop 1 disables and bypasses third DC offset correction	0
NU	Not used [9]	Not used	0
TVCOEN	TXVCO select [10]	0 disables TXVCO 1 enables TXVCO via TXENA (Pin 4)	1
RSVD	Reserved [12:11]	reserved, must be programmed to default value	10
NU	Not used [13]	Not used	0
LOPORT_EN	Enable LO port [14]	0 disables bi-directional LO port 1 enables bi-directional LO port	0
EXT_INTB	INTVCO or EXTVCO [15]	0 enables internal VCO 1 enables external VCO (requires bit 14 = 1)	0
DFCPLLENA	DFC enable [16]	0 disables DFC 1 enables DFC	1
UHFVCOENA	UHFVCO enable [17]	0 disables internal UHF VCO 1 enables internal UHF VCO	1
RSVD	Reserved [20:18]	reserved, must be programmed to default value	011
CALENA	Enable IP2 calibration [21]	0 disables IP2 calibration 1 enables IP2 calibration	1
NU	Not used [22]	Not used	0
NU	Not used [23]	Not used	0

Table 16. Register 1: Test Register

Symbol	Function	State Description	Default (Binary)
ADDR	Address bits [3:0]. Must be set to 0101b (see Table 12)		
RSVD	Reserved [23:4]	Reserved	11000100101000101100

Table 17. Register 2: DC Offset Timing

Symbol	Function	State Description	Default (Binary)
ADDR	Address bits [3:0]. Must be set to 1001b (see Table 12)		
DCOCL1	DCOC control [7:4]	Tracking timing for DCOC1 (tT_H1 = (DCOCL1 x 64 x R)/Fref) (see Figure 3 and Figure 4)	0100 (20 µs with 13 MHz f_{REF})
DCOCL2	DCOC control [12:8]	Tracking timing for DCOC2 (tT_H2 = (DCOCL2 x 64 x R)/Fref) (see Figure 3 and Figure 4)	01100 (60 µs with 13 MHz f_{REF})
DCOCL3	DCOC control [16:13]	Tracking timing for DCOC3 (tT_H3 = (DCOCL3 x 128 x R)/Fref) (see Figure 3 and Figure 4)	0110 (60 µs with 13 MHz f_{REF})
FEENA_TIM	FEENA relative to initial track [20:17]	Front End Enable timing (tFEENA = (FEENA_TIM x 128 x R)/Fref) (see Figure 3 and Figure 4)	0100 (40 µs with 13 MHz f_{REF})
T_H_SEL	T_H source select [21]	0 = internal control relative to RXENA (pin 3) 1 = DCOC loop activated by T_H signal on pin 32	0
FEENA_SEL	Front end enable source select [22]	0 = internal control relative to RXENA (pin 3). FEENA (pin 14) becomes an output 1 = external control by FEENA (pin 14)	0
NU	Not used [23]	Not used	0

Table 18. Register 3: IP2 Calibration

Symbol	Function	State Description
ADDR	Address bits [5:0]. Must be set to 001101b (see Table 12)	
ADDR_SEL	Channel selection [6]	0 selects Q channel 1 selects I channel
RSVD	Reserved [7]	Must be set to 1 for correct operation
CORR_DATA	IP2 correction coefficient [15:8]	Coefficient for adjustment of receiver IP2 Bit [15] sets polarity: 0 = Positive 1 = Negative Bit [14:8] 1111111 Minimum correction • • • 0000000 Maximum correction Bit [14]: MSB Bit [8] = LSB
NU	Not used [23:16]	Not used

Table 19. Register 4: Test Register

Symbol	Function	State Description	Default (Binary)
ADDR	Address bits [5:0]. Must be set to 011101b (see Table 12)		
RSVD	Reserved [23:6]	reserved	010000000000000010

Table 20. Register 5: Test Register

Symbol	Function	State Description	Default (Binary)
ADDR	Address bits [5:0]. Must be set to 111101b (see Table 12)		
RSVD	Reserved [23:6]	reserved	000011111000000001

Table 21. RX/TX Control Register (1 of 2)

Symbol	Function	State Description
ADDR	Address bits [1:0]. Must be set to 11b (see Table 12)	
LNA	LNA gain step control [2]	0 selects low gain mode of LNA 1 selects high gain mode of LNA
MIX	Mixer gain step [3]	0 selects low gain mode of RX mixer 1 selects high gain mode of RX mixer
LPF1	1st LPF gain step [4]	0 selects low gain mode of the first active LPF 1 selects high gain mode of the first active LPF
VGA2	VGA2 gain steps [7:5]	Bit 7 to bit 5 program the VGA2 gain in 6 dB increments: Bit 7 6 5 0 0 0 sets the gain to 30 dB 0 0 1 sets the gain to 24 dB 0 1 0 sets the gain to 18 dB 0 1 1 sets the gain to 12 dB 1 0 0 sets the gain to 6 dB 1 0 1 sets the gain to 0 dB 1 1 0 not used 1 1 1 not used
AUX	Auxiliary gain [8]	0 sets 0 dB auxiliary gain post gmC filter 1 sets 6 dB auxiliary gain post gmC filter
VGA1	VGA1 gain steps [11:9]	Bit 11 to bit 9 program the VGA1 gain in the following increments: Bit 11 10 9 0 0 0 sets the gain to 0 dB 0 0 1 sets the gain to 24 dB 0 1 0 sets the gain to 12 dB 0 1 1 not used 1 0 0 sets the gain to 6 dB 1 0 1 sets the gain to 30 dB 1 1 0 sets the gain to 18 dB 1 1 1 not used
VGA1FINE	VGA1 fine gain step [13:12]	Bit 13 and bit 12 program VGA1 in 2 dB increments: Bit 13 12 0 0 sets gain to 0 dB 0 1 sets gain to 4 dB 1 0 sets gain to 2 dB 1 1 not used
TXCP	TX charge pump bits [15:14]	Translational loop charge pump current setting: Bit 15 14 0 0 sets TXCP to 0.5 mA 0 1 sets TXCP to 1.0 mA 1 0 sets TXCP to 2.0 mA 1 1 not used

Table 21. RX/TX Control Register (2 of 2)

Symbol	Function	State Description
TXD1	TX divider D1 [17:16]	Translational loop D1 divider setting: Bit 17 16 0 0 sets D1 to 9 0 1 sets D1 to 11 1 0 sets D1 to 10 1 1 sets D1 to 12
TXD2	TX divider D2 [18]	Translational loop D2 divider setting: 0 sets D2 to 1 1 sets D2 to 2
TXPOL	TX VCO Gain Slope [19]	0 sets positive gain slope 1 sets negative gain slope
SOFTSEL	Software band select [21:20]	Bit 21 20: 0 0 Band selects via external pins (5 and 6), see Table 22. 0 1 selects EGSM/GSM850, PCO1 = 0, PCO2 = 0 1 0 selects DCS, PCO1 = 1, PCO2 = 0 1 1 selects PCS, PCO1 = 1, PCO2 = 1
PREENA	Load default words [22]	0 allows changing contents of R0 to R5 1 allows loading default words into R0 to R5 Upon power up, program RX/TX control register with PREENA = 1 to load the default words into R0 to R5. If changing the default words is required, program RX/TX control register with PREENA = 0 and then program any or all of R0 to R5. PREENA should also be set to 0 when sending SX R1, SX R2, and RX/TX control register words before each time slot in normal operation. The data is stored in R0 to R5 as long as VDDBB (pin 48) is supplied with power.
NU	Not used [23]	Not used

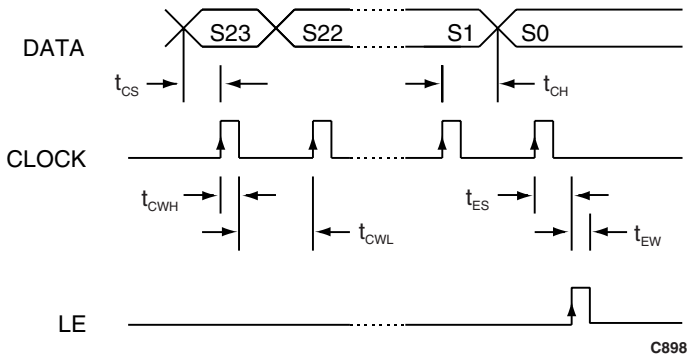


Figure 1. Serial Data Input Timing Diagram For Transceiver

Table 22. Band Select Truth Table (For SOFTSEL = [00])

PCO1 (Pin 5)	PCO2 (Pin 6)	Band
0	X	EGSM900/GSM850
1	0	DCS1800
1	1	PCS1900

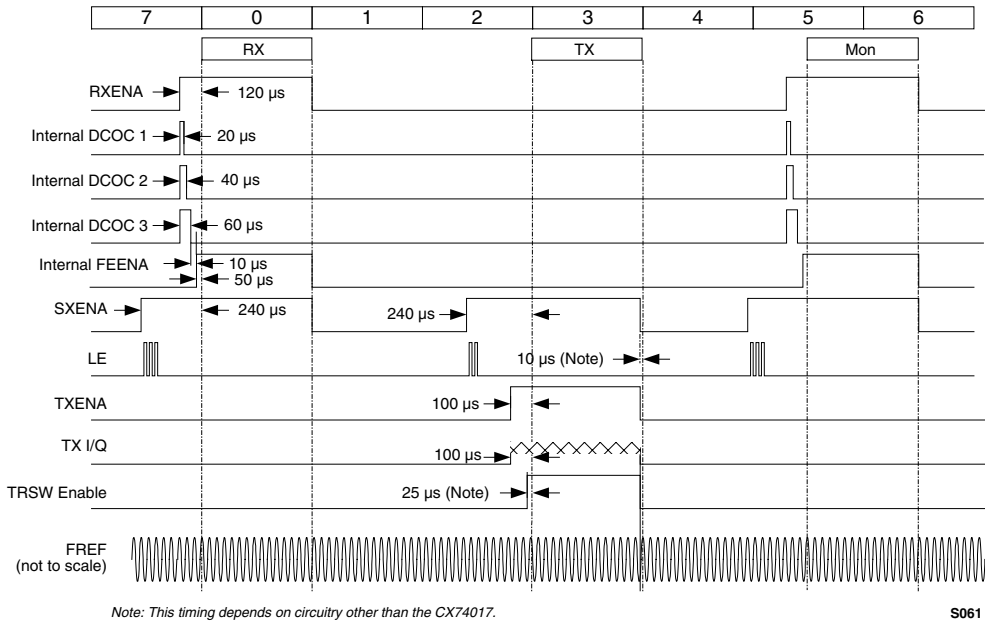
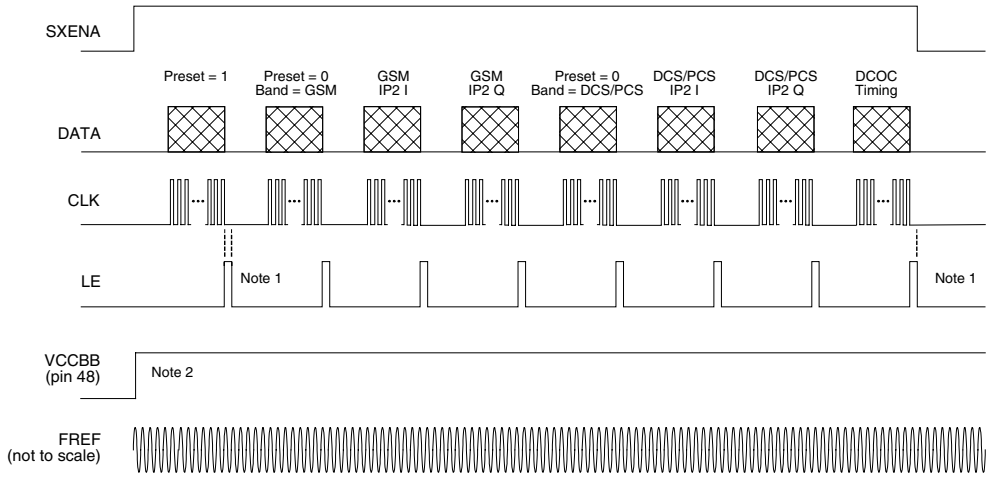


Figure 8. CX74017 Signal Timing Example (Normal Operation)



Note 1. LE should be low before the next clock goes high.
Note 2. VCCBB, pin 48, is required to hold the register settings. If VCCBB is not maintained high, the power-on programming sequence needs to be added in front of each normal slot programming sequence.

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Figure 9. CX74017 Register Programming Sequence and Timing Example (Initialization after Power Up)

Receiver Data

Table 23. Recommended EGSM900/GSM850 AGC Data (1 of 2)
(AGC Setpoint = –25.2, dBV = 55.0 mVrms)

Antenna Input (dBm)		External Front-End Losses (dB)	LNA (dB)	Mixer (dB)	LPF (dB)	VGA1 (dB)	VGA1 Fine (dB)	Aux (dB)	VGA2 (dB)	Internal Inter-Stage Losses (dB)	Total Voltage Gain (dB)	I or Q Output (dBV)	
From	To											From	To
–110	–108	–4.0	15	40	10	18	4	0	18	–4.2	96.8	–26.2	–24.2
–108	–106	–4.0	15	40	10	18	2	0	18	–4.2	94.8	–26.2	–24.2
–106	–104	–4.0	15	40	10	18	0	0	18	–4.2	92.8	–26.2	–24.2
–104	–102	–4.0	15	40	10	12	4	0	18	–4.2	90.8	–26.2	–24.2
–102	–100	–4.0	15	40	10	12	2	0	18	–4.2	88.8	–26.2	–24.2
–100	–98	–4.0	15	40	10	12	0	0	18	–4.2	86.8	–26.2	–24.2
–98	–96	–4.0	15	40	10	6	4	0	18	–4.2	84.8	–26.2	–24.2
–96	–94	–4.0	15	40	10	6	2	0	18	–4.2	82.8	–26.2	–24.2
–94	–92	–4.0	15	40	10	6	0	0	18	–4.2	80.8	–26.2	–24.2
–92	–90	–4.0	15	40	10	0	4	0	18	–4.2	78.8	–26.2	–24.2
–90	–88	–4.0	15	40	10	0	2	0	18	–4.2	76.8	–26.2	–24.2
–88	–86	–4.0	15	40	10	0	0	0	18	–4.2	74.8	–26.2	–24.2
–86	–84	–4.0	15	40	–2	6	4	0	18	–4.2	72.8	–26.2	–24.2
–84	–82	–4.0	15	40	–2	6	2	0	18	–4.2	70.8	–26.2	–24.2
–82	–80	–4.0	15	40	–2	6	0	0	18	–4.2	68.8	–26.2	–24.2
–80	–78	–4.0	15	40	–2	0	4	0	18	–4.2	66.8	–26.2	–24.2
–78	–76	–4.0	15	40	–2	0	2	0	18	–4.2	64.8	–26.2	–24.2
–76	–74	–4.0	15	40	–2	0	0	0	18	–4.2	62.8	–26.2	–24.2
–74	–72	–4.0	15	22	10	0	4	0	18	–4.2	60.8	–26.2	–24.2
–72	—70	–4.0	15	22	10	0	2	0	18	–4.2	58.8	–26.2	–24.2
–70	–68	–4.0	15	22	10	0	0	0	18	–4.2	56.8	–26.2	–24.2
–68	–66	–4.0	15	22	–2	6	4	0	18	–4.2	54.8	–26.2	–24.2
–66	–64	–4.0	15	22	–2	6	2	0	18	–4.2	52.8	–26.2	–24.2
–64	–62	–4.0	15	22	–2	6	0	0	18	–4.2	50.8	–26.2	–24.2
–62	–60	–4.0	15	22	–2	0	4	0	18	–4.2	48.8	–26.2	–24.2
–60	–58	–4.0	15	22	–2	0	2	0	18	–4.2	46.8	–26.2	–24.2
–58	–56	–4.0	15	22	–2	0	0	0	18	–4.2	44.8	–26.2	–24.2
–56	–54	–4.0	–5	22	10	6	0	0	18	–4.2	42.8	–26.2	–24.2
–54	–52	–4.0	–5	22	10	0	4	0	18	–4.2	40.8	–26.2	–24.2

Table 23. Recommended EGSM900/GSM850 AGC Data (2 of 2)
(AGC Setpoint = –25.2, dBV = 55.0 mVrms)

Antenna Input (dBm)		External Front-End Losses (dB)	LNA (dB)	Mixer (dB)	LPF (dB)	VGA1 (dB)	VGA1 Fine (dB)	Aux (dB)	VGA2 (dB)	Internal Inter-Stage Losses (dB)	Total Voltage Gain (dB)	I or Q Output (dBV)	
From	To											From	To
–52	–50	–4.0	–5	22	10	0	2	0	18	–4.2	38.8	–26.2	–24.2
–50	–48	–4.0	–5	22	10	0	0	0	18	–4.2	36.8	–26.2	–24.2
–48	–46	–4.0	–5	22	–2	6	4	0	18	–4.2	34.8	–26.2	–24.2
–46	–44	–4.0	–5	22	–2	6	2	0	18	–4.2	32.8	–26.2	–24.2
–44	–42	–4.0	–5	22	–2	6	0	0	18	–4.2	30.8	–26.2	–24.2
–42	–40	–4.0	–5	22	–2	0	4	0	18	–4.2	28.8	–26.2	–24.2
–40	–38	–4.0	–5	22	–2	0	2	0	18	–4.2	26.8	–26.2	–24.2
–38	–36	–4.0	–5	22	–2	0	0	0	18	–4.2	24.8	–26.2	–24.2
–36	–34	–4.0	–5	22	–2	0	4	0	12	–4.2	22.8	–26.2	–24.2
–34	–32	–4.0	–5	22	–2	0	2	0	12	–4.2	20.8	–26.2	–24.2
–32	–30	–4.0	–5	22	–2	0	0	0	12	–4.2	18.8	–26.2	–24.2
–30	–28	–4.0	–5	22	–2	0	4	0	6	–4.2	16.8	–26.2	–24.2
–28	–26	–4.0	–5	22	–2	0	2	0	6	–4.2	14.8	–26.2	–24.2
–26	–24	–4.0	–5	22	–2	0	0	0	6	–4.2	12.8	–26.2	–24.2
–24	–22	–4.0	–5	22	–2	0	4	0	0	–4.2	10.8	–26.2	–24.2
–22	–20	–4.0	–5	22	–2	0	2	0	0	–4.2	8.8	–26.2	–24.2
–20	–18	–4.0	–5	22	–2	0	0	0	0	–4.2	6.8	–26.2	–24.2
–18	–16	–4.0	–5	22	–2	0	0	0	0	–4.2	6.8	–24.2	–22.2
–16	–14	–4.0	–5	22	–2	0	0	0	0	–4.2	6.8	–22.2	–20.2

Note: For signal levels greater than approximately –20 dBm, the gain may be reduced due to compression. See Figure 16.

Table 24. Recommended DCS1800 AGC Data (1 of 2)
(AGC Setpoint = –24.2, dBV = 61.7 mVrms)

Antenna Input (dBm)		External Front-End Losses (dB)	LNA (dB)	Mixer (dB)	LPF (dB)	VGA1 (dB)	VGA1 Fine (dB)	Aux (dB)	VGA2 (dB)	Internal Inter-Stage Losses (dB)	Total Voltage Gain (dB)	I or Q Output (dBV)	
From	To											From	To
–110	–108	–4.2	15	40	10	24	0	0	18	–5.0	97.8	–25.2	–23.2
–108	–106	–4.2	15	40	10	18	4	0	18	–5.0	95.8	–25.2	–23.2
–106	–104	–4.2	15	40	10	18	2	0	18	–5.0	93.8	–25.2	–23.2
–104	–102	–4.2	15	40	10	18	0	0	18	–5.0	91.8	–25.2	–23.2
–102	–100	–4.2	15	40	10	12	4	0	18	–5.0	89.8	–25.2	–23.2
–100	–98	–4.2	15	40	10	12	2	0	18	–5.0	87.8	–25.2	–23.2
–98	–96	–4.2	15	40	10	12	0	0	18	–5.0	85.8	–25.2	–23.2
–96	–94	–4.2	15	40	10	6	4	0	18	–5.0	83.8	–25.2	–23.2
–94	–92	–4.2	15	40	10	6	2	0	18	–5.0	81.8	–25.2	–23.2
–92	–90	–4.2	15	40	10	6	0	0	18	–5.0	79.8	–25.2	–23.2
–90	–88	–4.2	15	40	10	0	4	0	18	–5.0	77.8	–25.2	–23.2
–88	–86	–4.2	15	40	10	0	2	0	18	–5.0	75.8	–25.2	–23.2
–86	–84	–4.2	15	40	10	0	0	0	18	–5.0	73.8	–25.2	–23.2
–84	–82	–4.2	15	40	–2	6	4	0	18	–5.0	71.8	–25.2	–23.2
–82	–80	–4.2	15	40	–2	6	2	0	18	–5.0	69.8	–25.2	–23.2
–80	–78	–4.2	15	40	–2	6	0	0	18	–5.0	67.8	–25.2	–23.2
–78	–76	–4.2	15	40	–2	0	4	0	18	–5.0	65.8	–25.2	–23.2
–76	–74	–4.2	15	40	–2	0	2	0	18	–5.0	63.8	–25.2	–23.2
–74	–72	–4.2	15	40	–2	0	0	0	18	–5.0	61.8	–25.2	–23.2
–72	–70	–4.2	15	22	10	0	4	0	18	–5.0	59.8	–25.2	–23.2
–70	–68	–4.2	15	22	10	0	2	0	18	–5.0	57.8	–25.2	–23.2
–68	–66	–4.2	15	22	10	0	0	0	18	–5.0	55.8	–25.2	–23.2
–66	–64	–4.2	15	22	–2	6	4	0	18	–5.0	53.8	–25.2	–23.2
–64	–62	–4.2	15	22	–2	6	2	0	18	–5.0	51.8	–25.2	–23.2
–62	–60	–4.2	15	22	–2	6	0	0	18	–5.0	49.8	–25.2	–23.2
–60	–58	–4.2	15	22	–2	0	4	0	18	–5.0	47.8	–25.2	–23.2

Table 24. Recommended DCS1800 AGC Data (2 of 2)
(AGC Setpoint = –24.2, dBV = 61.7 mVrms)

Antenna Input (dBm)		External Front-End Losses (dB)	LNA (dB)	Mixer (dB)	LPF (dB)	VGA1 (dB)	VGA1 Fine (dB)	Aux (dB)	VGA2 (dB)	Internal Inter-Stage Losses (dB)	Total Voltage Gain (dB)	I or Q Output (dBV)	
From	To											From	To
–58	–56	–4.2	15	22	–2	0	2	0	18	–5.0	45.8	–25.2	–23.2
–56	–54	–4.2	15	22	–2	0	0	0	18	–5.0	43.8	–25.2	–23.2
–54	–52	–4.2	–7	22	10	6	2	0	18	–5.0	41.8	–25.2	–23.2
–52	–50	–4.2	–7	22	10	6	0	0	18	–5.0	39.8	–25.2	–23.2
–50	–48	–4.2	–7	22	10	0	4	0	18	–5.0	37.8	–25.2	–23.2
–48	–46	–4.2	–7	22	10	0	2	0	18	–5.0	35.8	–25.2	–23.2
–46	–44	–4.2	–7	22	10	0	0	0	18	–5.0	33.8	–25.2	–23.2
–44	–42	–4.2	–7	22	–2	6	4	0	18	–5.0	31.8	–25.2	–23.2
–42	–40	–4.2	–7	22	–2	6	2	0	18	–5.0	29.8	–25.2	–23.2
–40	–38	–4.2	–7	22	–2	6	0	0	18	–5.0	27.8	–25.2	–23.2
–38	–36	–4.2	–7	22	–2	0	4	0	18	–5.0	25.8	–25.2	–23.2
–36	–34	–4.2	–7	22	–2	0	2	0	18	–5.0	23.8	–25.2	–23.2
–34	–32	–4.2	–7	22	–2	0	0	0	18	–5.0	21.8	–25.2	–23.2
–32	–30	–4.2	–7	22	–2	0	4	0	12	–5.0	19.8	–25.2	–23.2
–30	–28	–4.2	–7	22	–2	0	2	0	12	–5.0	17.8	–25.2	–23.2
–28	–26	–4.2	–7	22	–2	0	0	0	12	–5.0	15.8	–25.2	–23.2
–26	–24	–4.2	–7	22	–2	0	4	0	6	–5.0	13.8	–25.2	–23.2
–24	–22	–4.2	–7	22	–2	0	2	0	6	–5.0	11.8	–25.2	–23.2
–22	–20	–4.2	–7	22	–2	0	0	0	6	–5.0	9.8	–25.2	–23.2
–20	–18	–4.2	–7	22	–2	0	4	0	0	–5.0	7.8	–25.2	–23.2
–18	–16	–4.2	–7	22	–2	0	2	0	0	–5.0	5.8	–25.2	–23.2
–16	–14	–4.2	–7	22	–2	0	0	0	0	–5.0	3.8	–23.2	–21.2

Note: For signal levels greater than approximately –20 dBm, the gain may be reduced due to compression. See Figure 18.

Table 25. Recommended PCS1900 AGC Data (1 of 2)
(AGC Setpoint = –25.4, dBV = 53.7 mVrms)

Antenna Input (dBm)		External Front-End Losses (dB)	LNA (dB)	Mixer (dB)	LPF (dB)	VGA1 (dB)	VGA1 Fine (dB)	Aux (dB)	VGA2 (dB)	Internal Inter-Stage Losses (dB)	Total Voltage Gain (dB)	I or Q Output (dBV)	
From	To											From	To
–110	–108	–4.2	15	40	10	24	0	0	18	–6.2	96.6	–26.4	–24.4
–108	–106	–4.2	15	40	10	18	4	0	18	–6.2	94.6	–26.4	–24.4
–106	–104	–4.2	15	40	10	18	2	0	18	–6.2	92.6	–26.4	–24.4
–104	–102	–4.2	15	40	10	18	0	0	18	–6.2	90.6	–26.4	–24.4
–102	–100	–4.2	15	40	10	12	4	0	18	–6.2	88.6	–26.4	–24.4
–100	–98	–4.2	15	40	10	12	2	0	18	–6.2	86.6	–26.4	–24.4
–98	–96	–4.2	15	40	10	12	0	0	18	–6.2	84.6	–26.4	–24.4
–96	–94	–4.2	15	40	10	6	4	0	18	–6.2	82.6	–26.4	–24.4
–94	–92	–4.2	15	40	10	6	2	0	18	–6.2	80.6	–26.4	–24.4
–92	–90	–4.2	15	40	10	6	0	0	18	–6.2	78.6	–26.4	–24.4
–90	–88	–4.2	15	40	10	0	4	0	18	–6.2	76.6	–26.4	–24.4
–88	–86	–4.2	15	40	10	0	2	0	18	–6.2	74.6	–26.4	–24.4
–86	–84	–4.2	15	40	10	0	0	0	18	–6.2	72.6	–26.4	–24.4
–84	–82	–4.2	15	40	–2	6	4	0	18	–6.2	70.6	–26.4	–24.4
–82	–80	–4.2	15	40	–2	6	2	0	18	–6.2	68.6	–26.4	–24.4
–80	–78	–4.2	15	40	–2	6	0	0	18	–6.2	66.6	–26.4	–24.4
–78	–76	–4.2	15	40	–2	0	4	0	18	–6.2	64.6	–26.4	–24.4
–76	–74	–4.2	15	40	–2	0	2	0	18	–6.2	62.6	–26.4	–24.4
–74	–72	–4.2	15	40	–2	0	0	0	18	–6.2	60.6	–26.4	–24.4
–72	–70	–4.2	15	22	10	0	4	0	18	–6.2	58.6	–26.4	–24.4
–70	–68	–4.2	15	22	10	0	2	0	18	–6.2	56.6	–26.4	–24.4
–68	–66	–4.2	15	22	10	0	0	0	18	–6.2	54.6	–26.4	–24.4
–66	–64	–4.2	15	22	–2	6	4	0	18	–6.2	52.6	–26.4	–24.4
–64	–62	–4.2	15	22	–2	6	2	0	18	–6.2	50.6	–26.4	–24.4
–62	–60	–4.2	15	22	–2	6	0	0	18	–6.2	48.6	–26.4	–24.4
–60	–58	–4.2	15	22	–2	0	4	0	18	–6.2	46.6	–26.4	–24.4
–58	–56	–4.2	15	22	–2	0	2	0	18	–6.2	44.6	–26.4	–24.4
–56	–54	–4.2	15	22	–2	0	0	0	18	–6.2	42.6	–26.4	–24.4
–54	–52	–4.2	–5	22	10	6	0	0	18	–6.2	40.6	–26.4	–24.4
–52	–50	–4.2	–5	22	10	0	4	0	18	–6.2	38.6	–26.4	–24.4

Table 25. Recommended PCS1900 AGC Data (2 of 2)
(AGC Setpoint = –25.4, dBV = 53.7 mVrms)

Antenna Input (dBm)		External Front-End Losses (dB)	LNA (dB)	Mixer (dB)	LPF (dB)	VGA1 (dB)	VGA1 Fine (dB)	Aux (dB)	VGA2 (dB)	Internal Inter-Stage Losses (dB)	Total Voltage Gain (dB)	I or Q Output (dBV)	
From	To											From	To
–50	–48	–4.2	–5	22	10	0	2	0	18	–6.2	36.6	–26.4	–24.4
–48	–46	–4.2	–5	22	10	0	0	0	18	–6.2	34.6	–26.4	–24.4
–46	–44	–4.2	–5	22	–2	6	4	0	18	–6.2	32.6	–26.4	–24.4
–44	–42	–4.2	–5	22	–2	6	2	0	18	–6.2	30.6	–26.4	–24.4
–42	–40	–4.2	–5	22	–2	6	0	0	18	–6.2	28.6	–26.4	–24.4
–40	–38	–4.2	–5	22	–2	0	4	0	18	–6.2	26.6	–26.4	–24.4
–38	–36	–4.2	–5	22	–2	0	2	0	18	–6.2	24.6	–26.4	–24.4
–36	–34	–4.2	–5	22	–2	0	0	0	18	–6.2	22.6	–26.4	–24.4
–34	–32	–4.2	–5	22	–2	0	4	0	12	–6.2	20.6	–26.4	–24.4
–32	–30	–4.2	–5	22	–2	0	2	0	12	–6.2	18.6	–26.4	–24.4
–30	–28	–4.2	–5	22	–2	0	0	0	12	–6.2	16.6	–26.4	–24.4
–28	–26	–4.2	–5	22	–2	0	4	0	6	–6.2	14.6	–26.4	–24.4
–26	–24	–4.2	–5	22	–2	0	2	0	6	–6.2	12.6	–26.4	–24.4
–24	–22	–4.2	–5	22	–2	0	0	0	6	–6.2	10.6	–26.4	–24.4
–22	–20	–4.2	–5	22	–2	0	4	0	0	–6.2	8.6	–26.4	–24.4
–20	–18	–4.2	–5	22	–2	0	2	0	0	–6.2	6.6	–26.4	–24.4
–18	–16	–4.2	–5	22	–2	0	0	0	0	–6.2	4.6	–26.4	–24.4
–16	–14	–4.2	–5	22	–2	0	0	0	0	–6.2	4.6	–24.4	–22.4

Note: For signal levels greater than approximately –20 dBm, the gain may be reduced due to compression. See Figure 20.

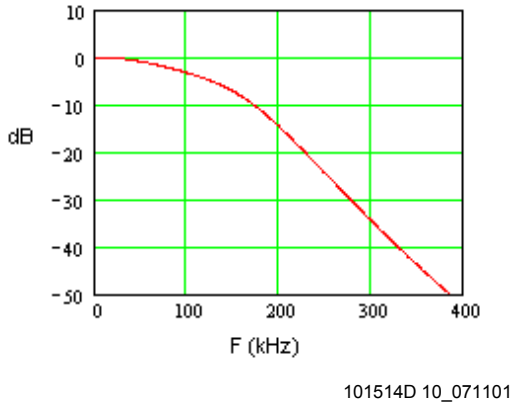


Figure 10. Typical Baseband Frequency Response

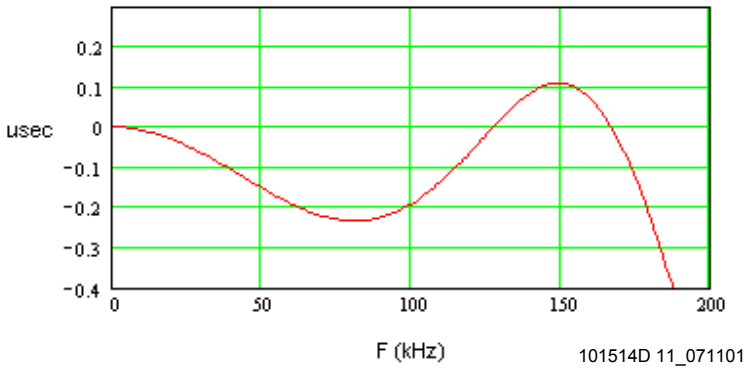


Figure 11. Typical Differential Delay Response

Receive Data

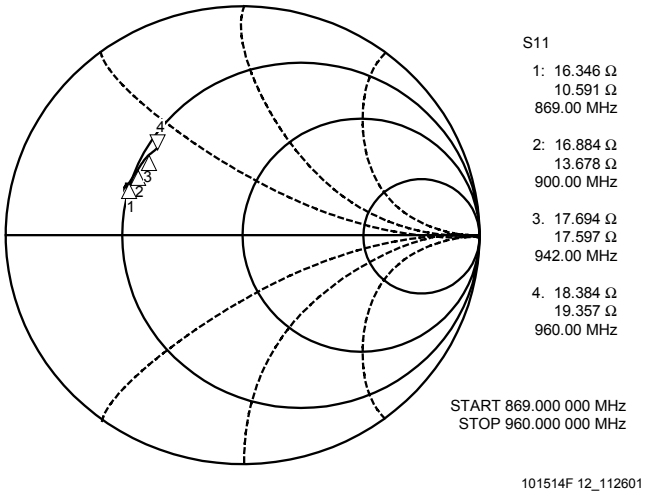


Figure 12. Typical EGSM/GSM850 LNA Input Impedance

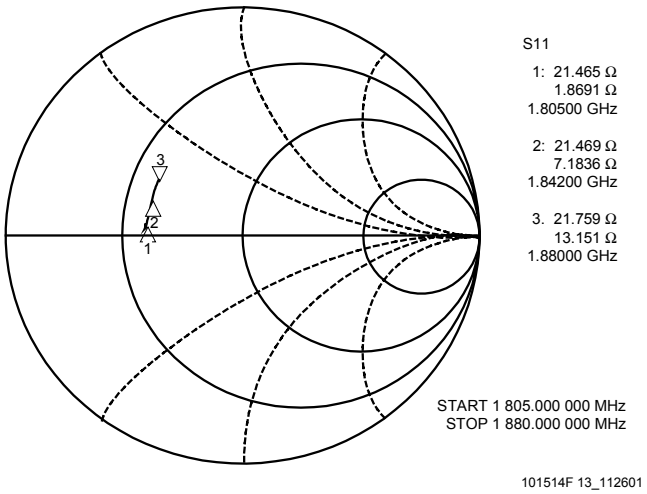


Figure 13. Typical DCS1800 LNA Input Impedance

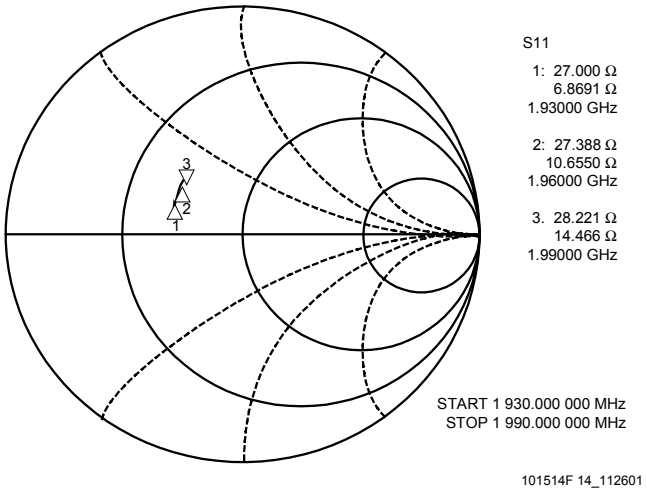


Figure 14. Typical PCS1900 LNA Input Impedance

Table 26. Typical EGSM and GSM850 Band Noise Figure vs. Gain Data

Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)
100.8	3.17	84.8	3.38	68.8	7.60	52.8	22.50	36.8	39.71	20.8	43.56
98.8	3.17	82.8	3.48	66.8	8.39	50.8	23.76	34.8	41.11	18.8	45.01
96.8	3.17	80.8	3.59	64.8	11.80	48.8	24.92	32.8	42.46	16.8	46.39
94.8	3.18	78.8	3.73	62.8	12.77	46.8	30.21	30.8	43.73	14.8	45.89
92.8	3.20	76.8	4.90	60.8	13.71	44.8	31.29	28.8	44.89	12.8	47.58
90.8	3.22	74.8	5.44	58.8	18.43	42.8	32.37	26.8	42.70	10.8	49.25
88.8	3.26	72.8	6.08	56.8	19.79	40.8	33.39	24.8	44.02		
86.8	3.31	70.8	6.82	54.8	21.16	38.8	38.32	22.8	45.24		

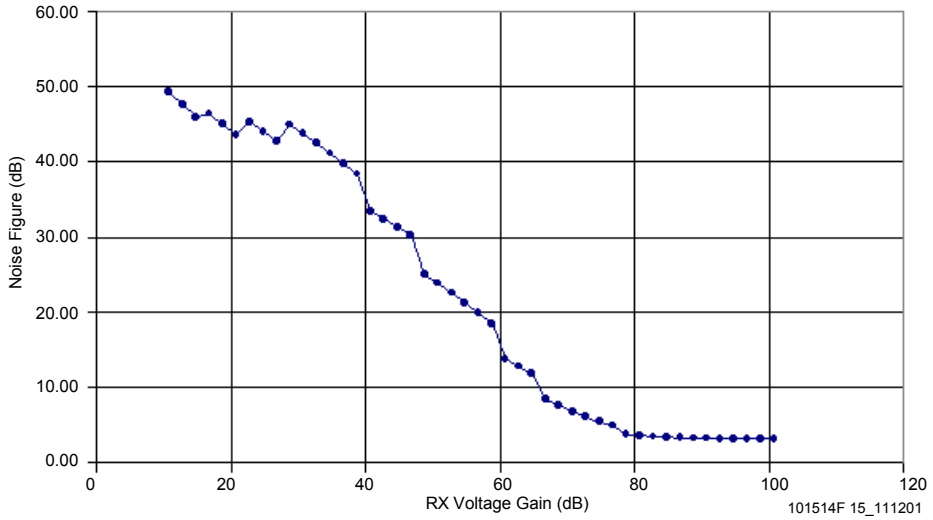


Figure 15. Typical EGSM and GSM850 Band Noise Figure vs. Voltage Gain Curve (CX74017 Only, No Front End Loss)

Table 27. Typical EGSM and GSM850 Band Dynamic Range Data (Includes 4.0 dB Front End Loss)

Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)	Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)	Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)
–109.0	–113.0	–78.6	97.8	–77.0	–108.2	–52.4	65.8	–45.0	–78.6	–21.2	33.8
–107.0	–113.0	–76.6	95.8	–75.0	–107.1	–52.0	63.8	–43.0	–74.5	–18.1	31.8
–105.0	–113.0	–74.6	93.8	–73.0	–106.0	–51.8	61.8	–41.0	–72.9	–17.7	29.8
–103.0	–113.0	–72.6	91.8	–71.0	–102.9	–43.4	59.8	–39.0	–71.4	–17.4	27.8
–101.0	–113.0	–70.6	89.8	–69.0	–101.6	–42.5	57.8	–37.0	–69.8	–17.2	25.8
–99.0	–113.0	–68.7	87.8	–67.0	–100.4	–41.9	55.8	–35.0	–68.3	–17.0	23.8
–97.0	–112.9	–66.9	85.8	–65.0	–96.4	–36.9	53.8	–33.0	–66.9	–17.0	21.8
–95.0	–112.9	–65.2	83.8	–63.0	–94.9	–35.9	51.8	–31.0	–66.9	–16.9	19.8
–93.0	–112.8	–63.7	81.8	–61.0	–93.4	–35.2	49.8	–29.0	–65.2	–16.9	17.8
–91.0	–112.7	–62.4	79.8	–59.0	–91.8	–34.6	47.8	–27.0	–63.4	–16.9	15.8
–89.0	–112.5	–61.4	77.8	–57.0	–90.3	–34.3	45.8	–25.0	–62.3	–16.8	13.8
–87.0	–112.3	–60.5	75.8	–55.0	–88.9	–34.0	43.8	–23.0	–60.3	–16.8	11.8
–85.0	–112.1	–59.9	73.8	–53.0	–83.8	–24.3	41.8	–21.0	–58.4	–16.8	9.8
–83.0	–110.8	–54.8	71.8	–51.0	–82.6	–23.2	39.8	–19.0	–56.7	–16.8	7.8
–81.0	–110.0	–53.8	69.8	–49.0	–81.3	–22.3	37.8	–17.0	–54.7	–16.8	5.8
–79.0	–109.2	–53.0	67.8	–47.0	–79.9	–21.7	35.8	–15.0	–52.7	–16.8	3.8

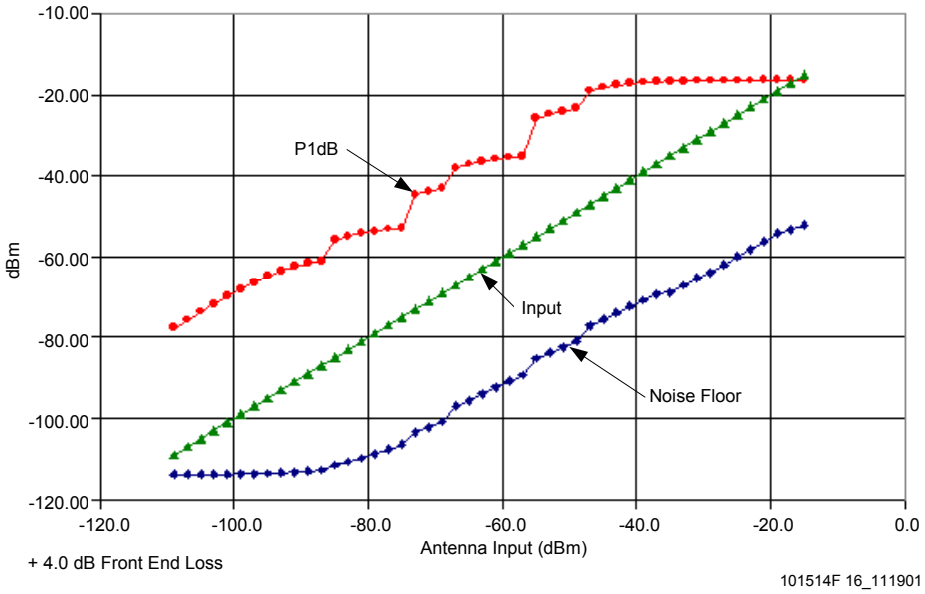


Figure 16. Typical EGSM and GSM850 Band Dynamic Range vs. Antenna Input Curve

Table 28. Typical DCS1800 Band Noise Figure vs. Gain Data

Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)
100	3.7	84	3.9	68	8.3	52	23.3	36	41.1	20	48.0
98	3.7	82	4.0	66	9.1	50	24.6	34	42.5	18	46.4
96	3.7	80	4.1	64	12.6	48	25.7	32	43.9	16	47.8
94	3.7	78	4.3	62	13.6	46	32.0	30	45.3	14	49.2
92	3.7	76	5.5	60	14.5	44	33.0	28	46.5	12	48.7
90	3.7	74	6.1	58	19.2	42	34.1	26	47.7	10	50.4
88	3.8	72	6.7	56	20.6	40	35.2	24	45.5		
86	3.8	70	7.5	54	22.0	38	36.2	22	46.8		

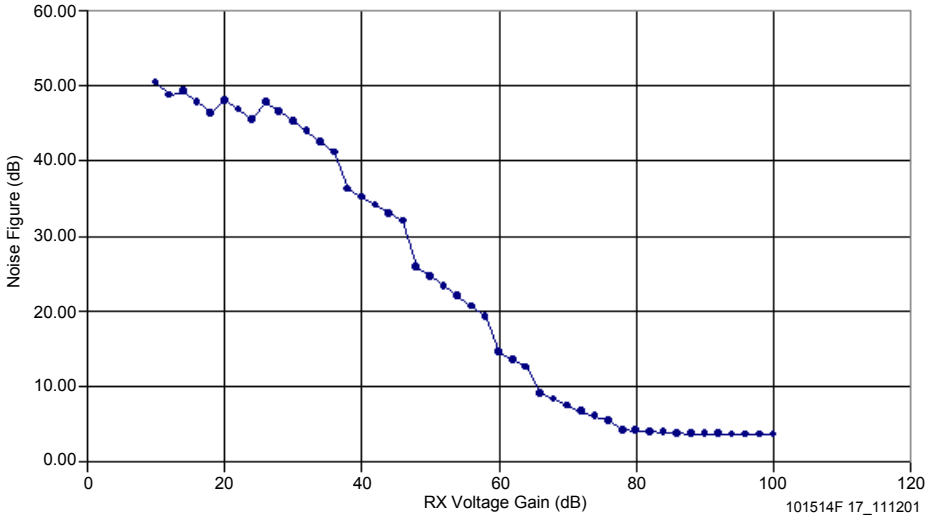


Figure 17. Typical DCS1800 Band Noise Figure vs. Voltage Gain Curve (CX74017 Only, No Front End Loss)

Table 29. Typical DCS1800 Band Dynamic Range Data (Includes 4.2 dB Front End Loss)

Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)	Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)	Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)
–109.0	–113.0	–78.6	97.8	–77.0	–108.2	–52.4	65.8	–45.0	–78.6	–21.2	33.8
–107.0	–113.0	–76.6	95.8	–75.0	–107.1	–52.0	63.8	–43.0	–74.5	–18.1	31.8
–105.0	–113.0	–74.6	93.8	–73.0	–106.0	–51.8	61.8	–41.0	–72.9	–17.7	29.8
–103.0	–113.0	–72.6	91.8	–71.0	–102.9	–43.4	59.8	–39.0	–71.4	–17.4	27.8
–101.0	–113.0	–70.6	89.8	–69.0	–101.6	–42.5	57.8	–37.0	–69.8	–17.2	25.8
–99.0	–113.0	–68.7	87.8	–67.0	–100.4	–41.9	55.8	–35.0	–68.3	–17.0	23.8
–97.0	–112.9	–66.9	85.8	–65.0	–96.4	–36.9	53.8	–33.0	–66.9	–17.0	21.8
–95.0	–112.9	–65.2	83.8	–63.0	–94.9	–35.9	51.8	–31.0	–66.9	–16.9	19.8
–93.0	–112.8	–63.7	81.8	–61.0	–93.4	–35.2	49.8	–29.0	–65.2	–16.9	17.8
–91.0	–112.7	–62.4	79.8	–59.0	–91.8	–34.6	47.8	–27.0	–63.4	–16.9	15.8
–89.0	–112.5	–61.4	77.8	–57.0	–90.3	–34.3	45.8	–25.0	–62.3	–16.8	13.8
–87.0	–112.3	–60.5	75.8	–55.0	–88.9	–34.0	43.8	–23.0	–60.3	–16.8	11.8
–85.0	–112.1	–59.9	73.8	–53.0	–83.8	–24.3	41.8	–21.0	–58.4	–16.8	9.8
–83.0	–110.8	–54.8	71.8	–51.0	–82.6	–23.2	39.8	–19.0	–56.7	–16.8	7.8
–81.0	–110.0	–53.8	69.8	–49.0	–81.3	–22.3	37.8	–17.0	–54.7	–16.8	5.8
–79.0	–109.2	–53.0	67.8	–47.0	–79.9	–21.7	35.8	–15.0	–52.7	–16.8	3.8

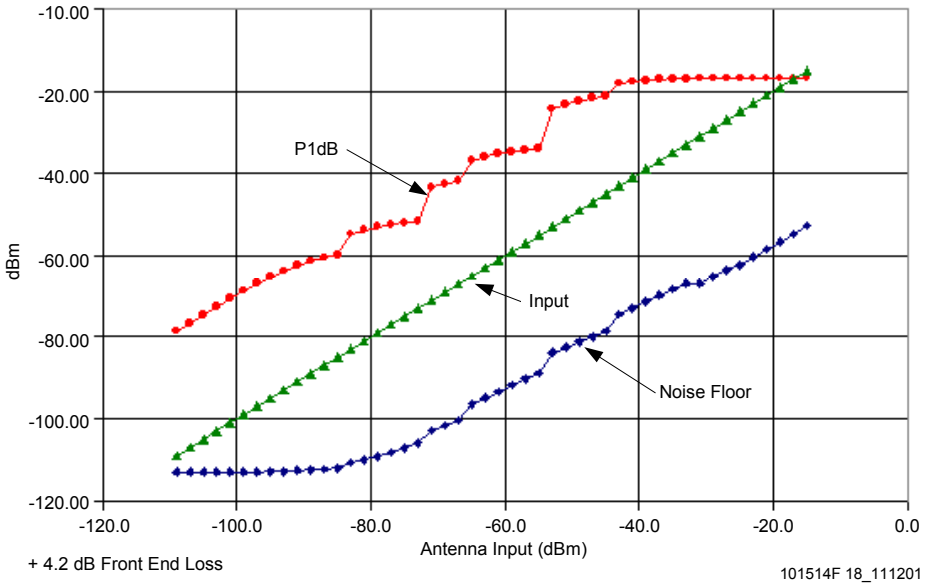


Figure 18. Typical DCS1800 Band Dynamic Range vs. Antenna Input Curve

Table 30. Typical PCS1900 Band Noise Figure vs. Gain Data

Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)
98.8	4.2	82.8	4.5	66.8	9.3	50.8	24.5	34.8	42.3	18.8	49.2
96.8	4.2	80.8	4.6	64.8	10.1	48.8	25.8	32.8	43.7	16.8	47.6
94.8	4.2	78.8	4.7	62.8	13.7	46.8	26.9	30.8	45.1	14.8	49.0
92.8	4.2	76.8	4.9	60.8	14.7	44.8	33.2	28.8	46.5	12.8	50.4
90.8	4.2	74.8	6.3	58.8	15.6	42.8	34.2	26.8	47.7	10.8	49.9
88.8	4.3	72.8	6.9	56.8	20.4	40.8	35.3	24.8	48.9	8.8	51.6
86.8	4.3	70.8	7.6	54.8	21.8	38.8	36.4	22.8	46.7	6.8	53.3
84.8	4.4	68.8	8.4	52.8	23.1	36.8	37.4	20.8	48.0		

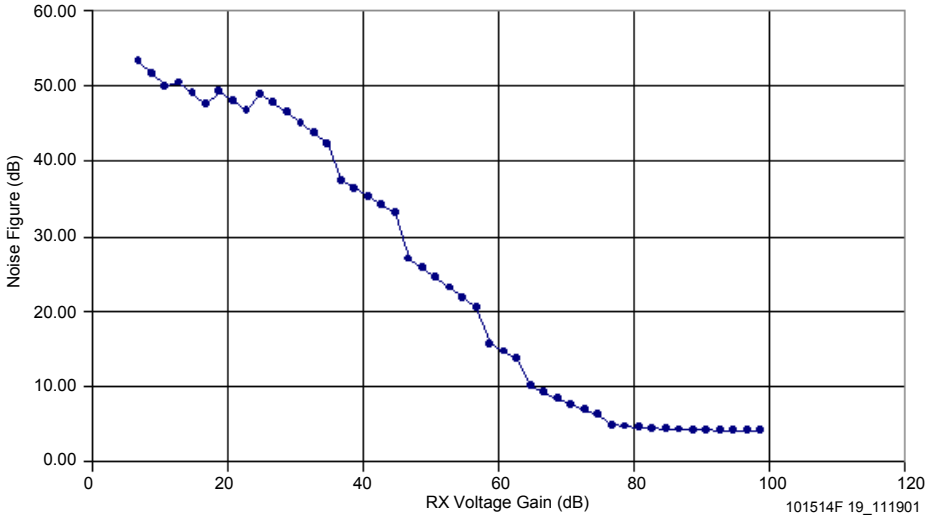


Figure 19. Typical PCS1900 Band Noise Figure vs. Voltage Gain Curve (CX74017 Only, No Front End Loss)

Table 31. Typical PCS1900 Band Dynamic Range Data (Includes 4.2 dB Front End Loss)

Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)	Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)	Input (dBm)	Noise Floor (dBm)	P1dB (dBm)	Gain (dB)
–109.0	–112.5	–77.4	96.6	–77.0	–107.4	–51.2	64.6	–45.0	–77.7	–20.3	32.6
–107.0	–112.5	–75.4	94.6	–75.0	–106.3	–50.8	62.6	–43.0	–73.5	–17.6	30.6
–105.0	–112.5	–73.4	92.6	–73.0	–105.2	–50.6	60.6	–41.0	–72.0	–17.2	28.6
–103.0	–112.5	–71.4	90.6	–71.0	–102.0	–42.2	58.6	–39.0	–70.4	–17.0	26.6
–101.0	–112.5	–69.4	88.6	–69.0	–100.7	–41.3	56.6	–37.0	–68.9	–16.8	24.6
–99.0	–112.5	–67.5	86.6	–67.0	–99.5	–40.7	54.6	–35.0	–67.4	–16.7	22.6
–97.0	–112.4	–65.7	84.6	–65.0	–95.4	–35.7	52.6	–33.0	–66.0	–16.6	20.6
–95.0	–112.4	–64.0	82.6	–63.0	–93.9	–34.7	50.6	–31.0	–66.3	–16.6	18.6
–93.0	–112.3	–62.5	80.6	–61.0	–92.4	–34.0	48.6	–29.0	–64.6	–16.5	16.6
–91.0	–112.1	–61.2	78.6	–59.0	–90.9	–33.4	46.6	–27.0	–62.9	–16.5	14.6
–89.0	–112.0	–60.2	76.6	–57.0	–89.4	–33.1	44.6	–25.0	–61.8	–16.5	12.6
–87.0	–111.8	–59.3	74.6	–55.0	–88.0	–32.8	42.6	–23.0	–59.9	–16.5	10.6
–85.0	–111.5	–58.7	72.6	–53.0	–82.8	–23.3	40.6	–21.0	–58.0	–16.5	8.6
–83.0	–110.0	–53.6	70.6	–51.0	–81.6	–22.2	38.6	–19.0	–56.3	–16.5	6.6
–81.0	–109.3	–52.6	68.6	–49.0	–80.3	–21.4	36.6	–17.0	–54.3	–16.5	4.6
–79.0	–108.4	–51.8	66.6	–47.0	–79.0	–20.8	34.6	–15.0	–52.4	–16.5	2.6

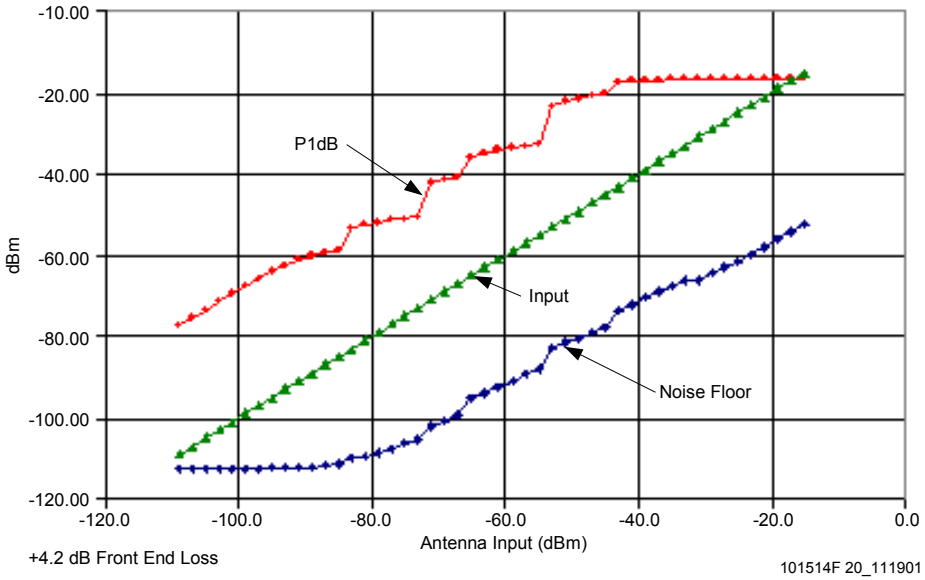


Figure 20. Typical PCS1900 Band Dynamic Range vs. Antenna Input Curve

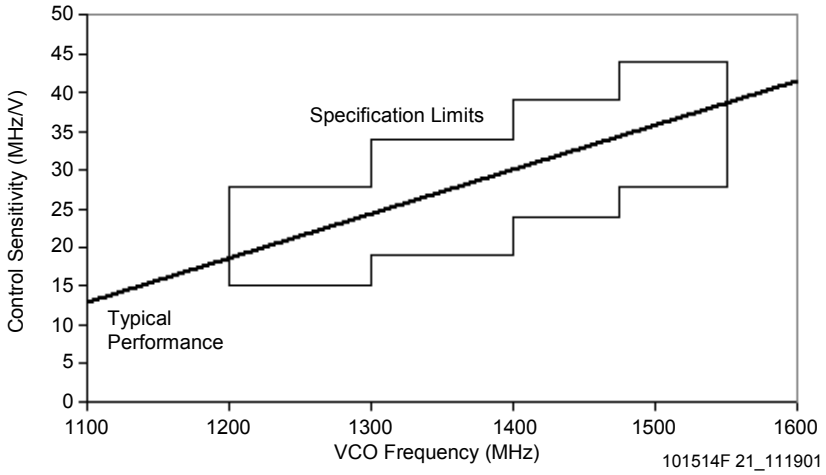


Figure 21. Typical Control Sensitivity, UHF VCO

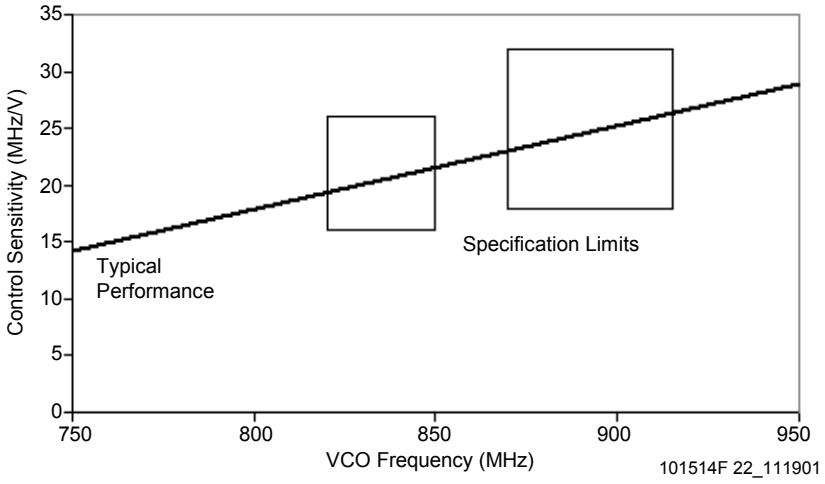


Figure 22. Typical Control Sensitivity, Low Band TX VCO

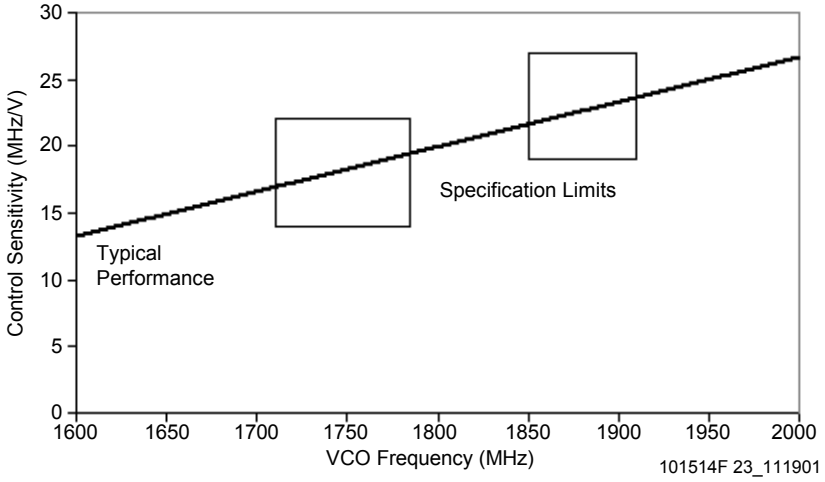


Figure 23. Typical Control Sensitivity, High Band TX VCO

Transmit Data

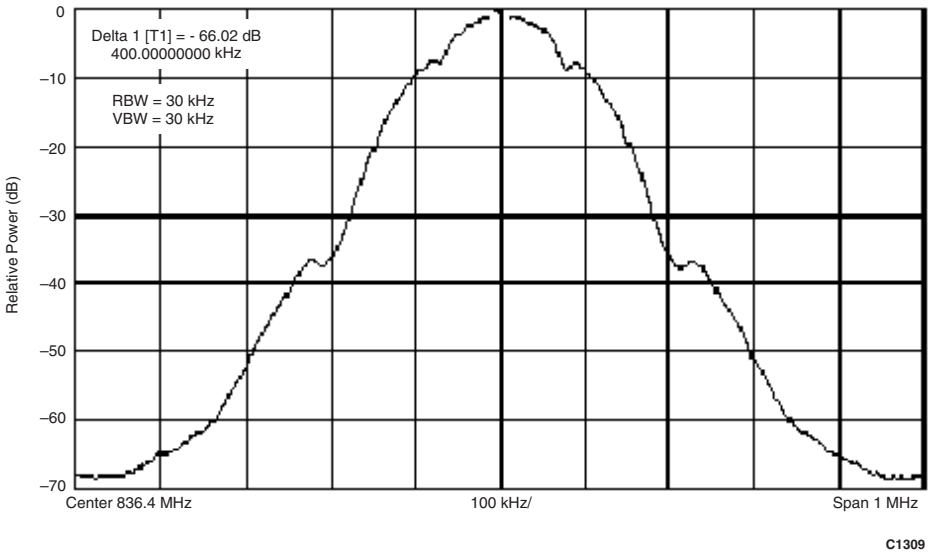


Figure 24. Typical GSM850 Band Output Spectrum

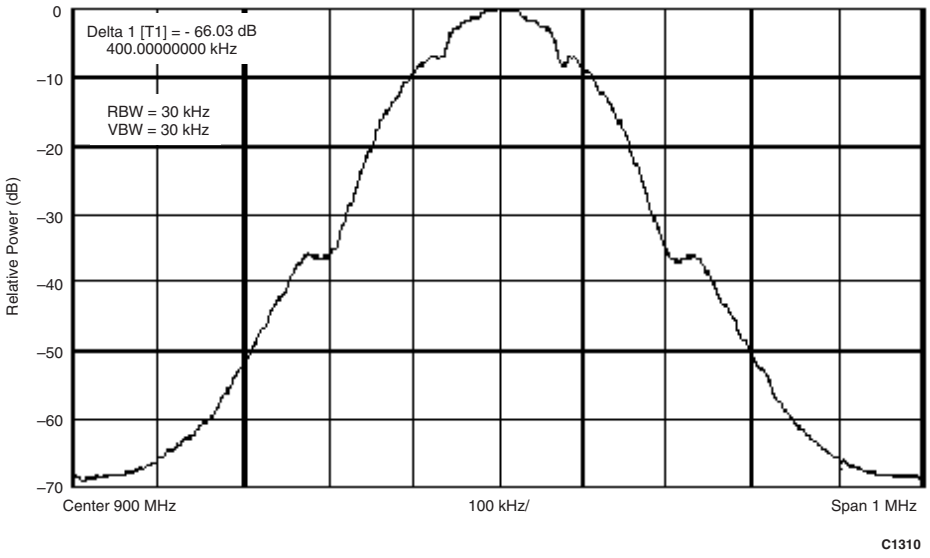


Figure 25. Typical EGSM Band Output Spectrum

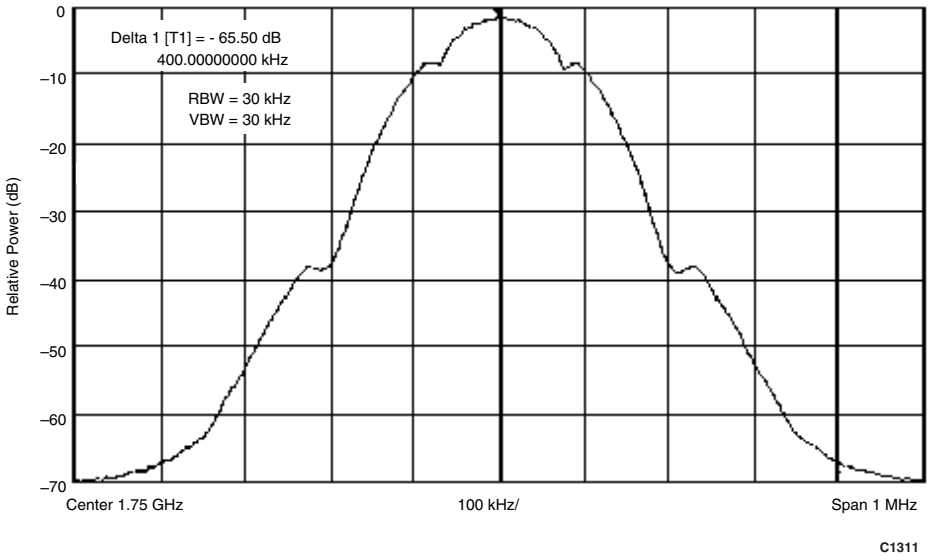


Figure 26. Typical DCS Band Output Spectrum

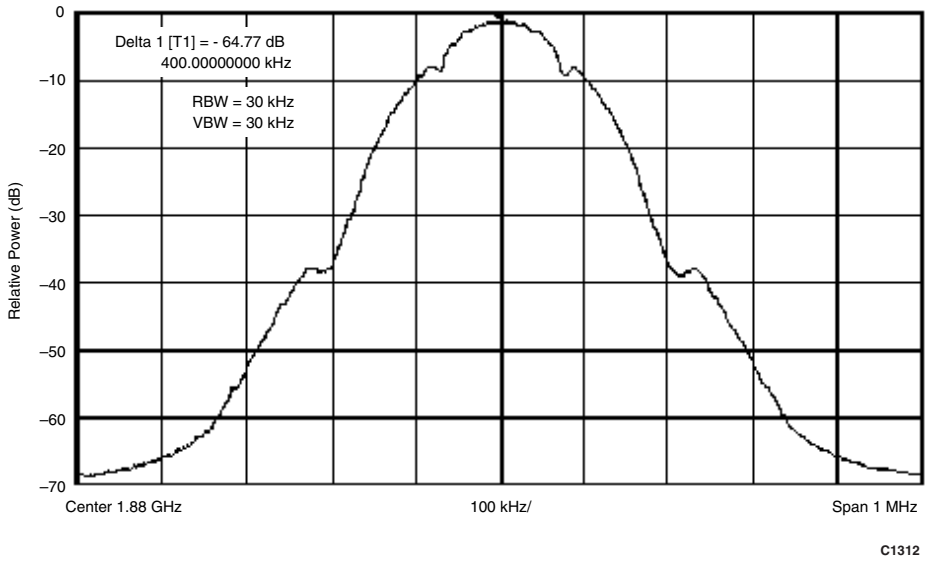


Figure 27. Typical PCS Band Output Spectrum

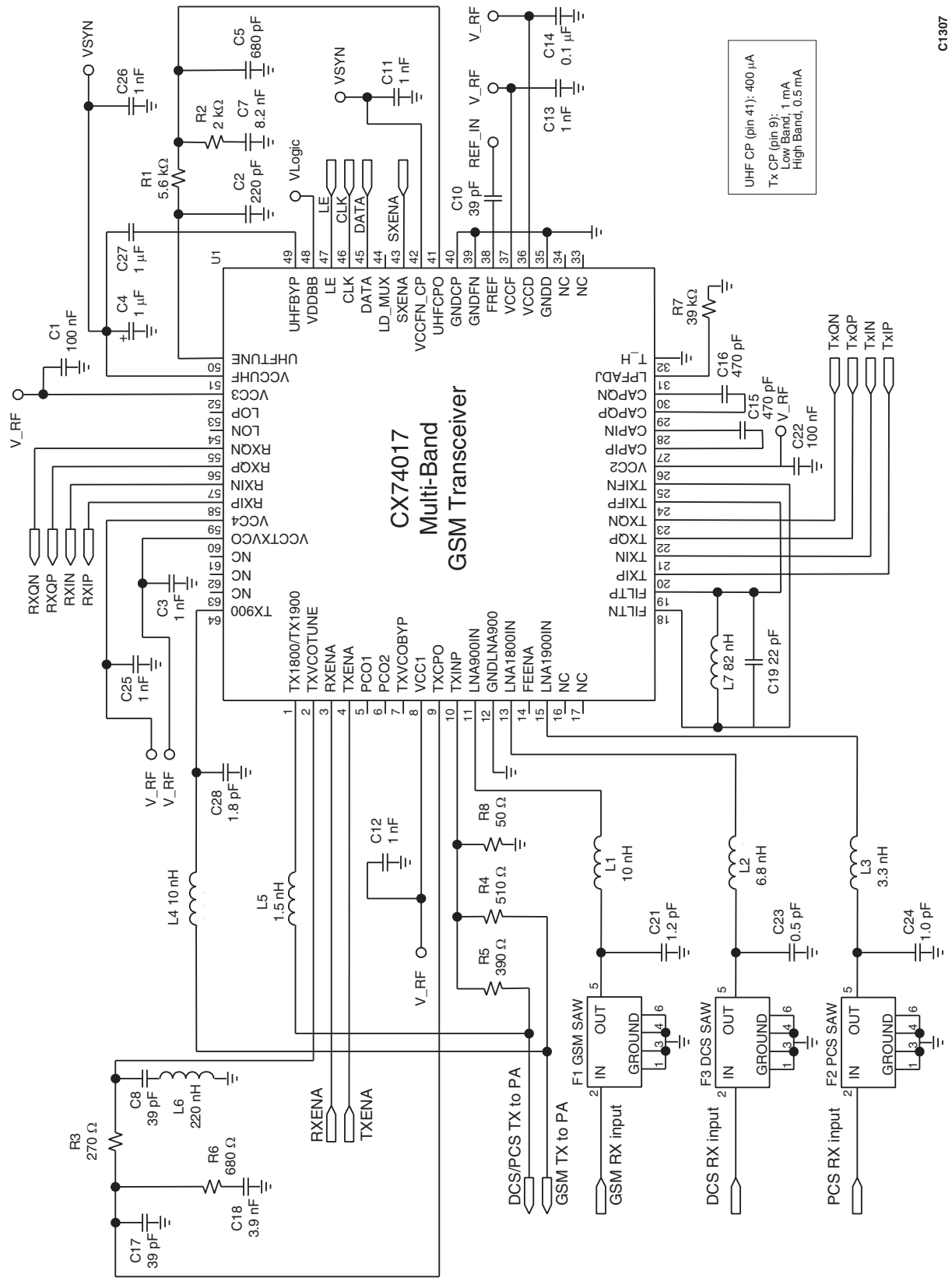


Figure 28. Typical Application Circuit

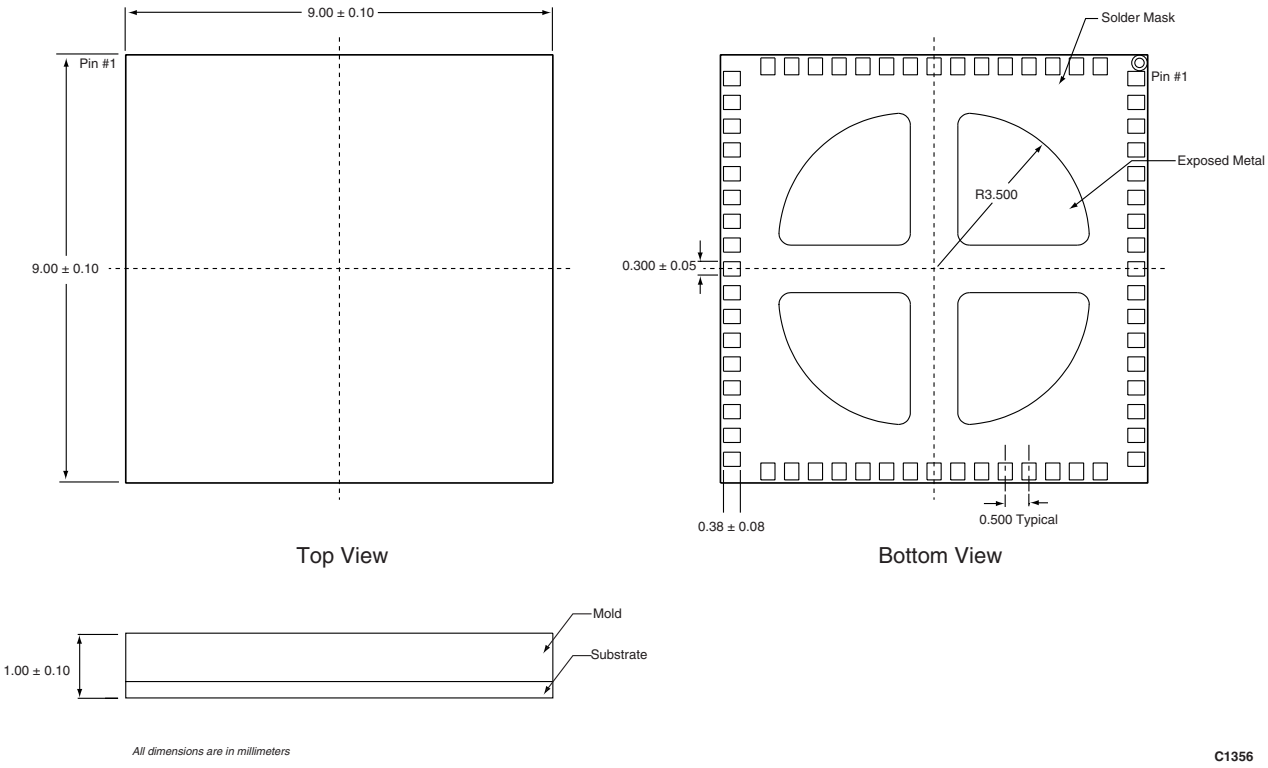
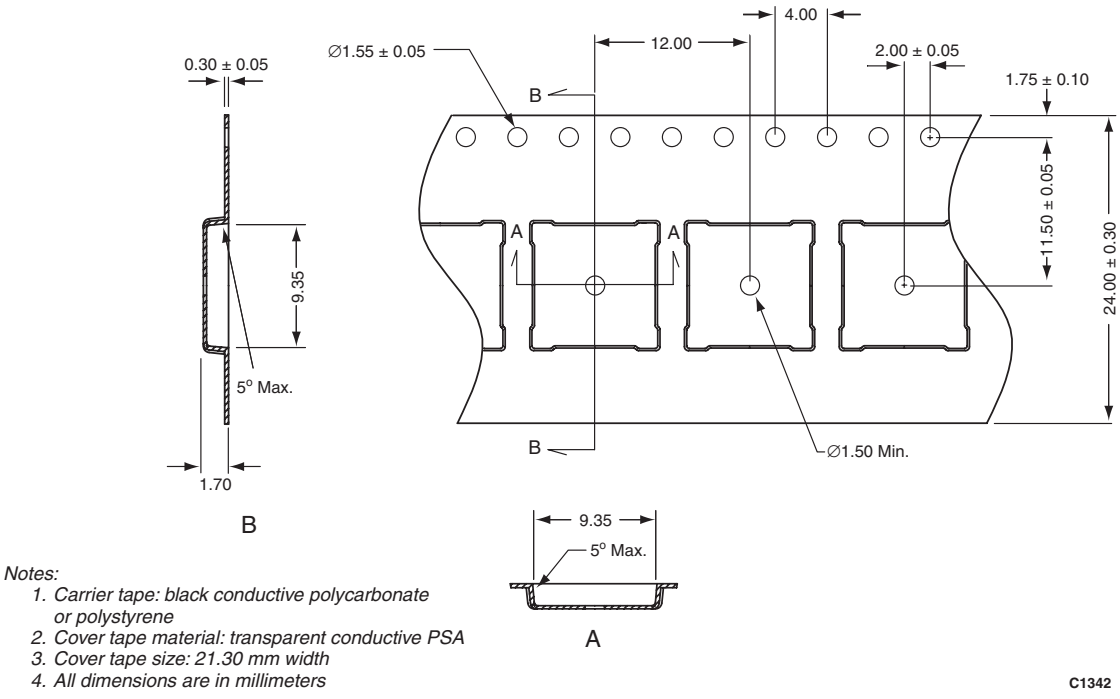


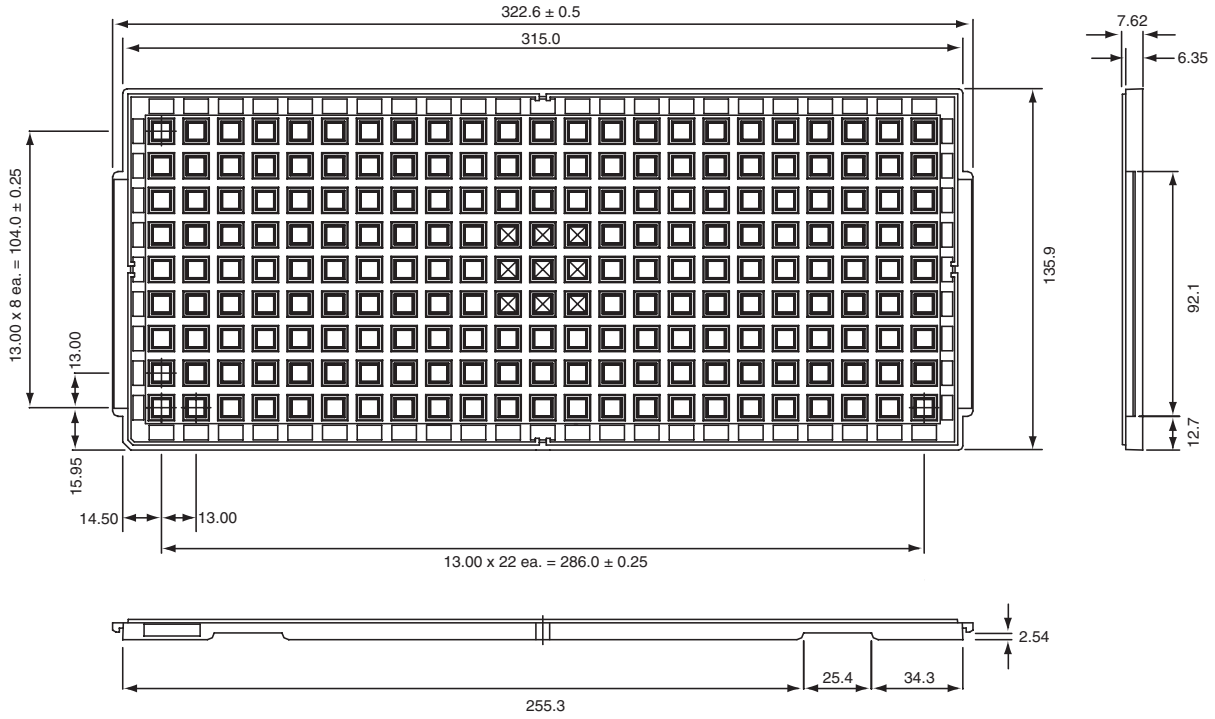
Figure 29. CX74017 64-Pin LGA Package Dimension Drawing



Notes:

1. *Carrier tape: black conductive polycarbonate or polystyrene*
2. *Cover tape material: transparent conductive PSA*
3. *Cover tape size: 21.30 mm width*
4. *All dimensions are in millimeters*

Figure 30. CX74017 Tape and Reel Dimensions

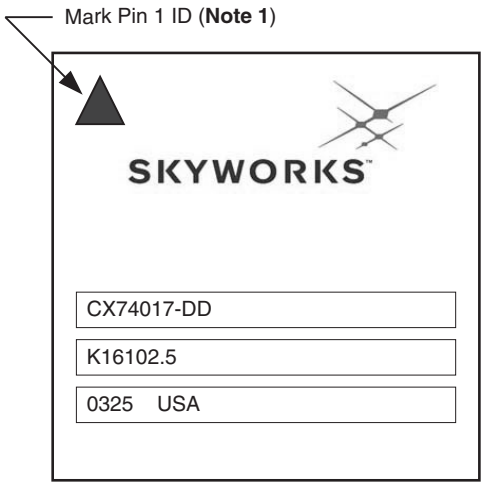


Notes:

1. *Material: bakeable carbon fiber/static dissipative with 140 ºC capability*
2. *All dimensions are in millimeters. Dimensions and tolerances in accordance with ASME Y14.5M-1994*
3. *ESD surface resistivity ≥ 1 x 10^5 ≤ 1 x 10^{12} Ω/square per EIA, JEDEC, and ACH tray specifications*

C1409

Figure 31. CX74017 Tray Drawing



Note 1: The Pin 1 ID is a triangle or circle.

Note 2: **Brand line 1**. The Part Number format is CXPPPPP-DD. The CX prefix is the company identifier. P = five-digit part number, D = dash number (for example, -16, -17). The CX prefix may not appear on small devices. The Part Number may be followed by a "P" to indicate a prototype device. (**Note 3**)

Brand line 2. Lot Number and Lot Split Identifier. The Lot Number format = 6 alphanumeric characters followed by a 1- or 2-digit Lot Split Identifier separated by a decimal point. The format is A12345.2 or A12345.21. (**Note 3**)

Brand line 3. Date Code and Country of Origin. The Date Code should be the same for the entire Lot Number and Lot Split Identifier. The first two digits of the Date Code are the current accounting calendar year. The last two digits are the current accounting calendar week. The format is YYWW (for example, 0325). The Country of Origin is the full name of the country where assembly is completed (for example, Mexico). The Country of Origin may be abbreviated (for example, USA or CN) if backside marking is not possible because of size restrictions. (**Note 3**)

A vendor-specified logo may appear below Brand line 3 (for example, ARM).

Note 3: As long as the device form, fit, and function remain the same, the data in Brand lines 1-3 may change. For example, the Lot Number and Lot Split Identifier may change; the Date Code and Country of Origin may change if Skyworks selects a second assembly source.

C1403b

Figure 32. CX74017 Typical Case Markings

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
CX74017 with Moisture Sensitivity Level 3 (MSL3) and 240 °C maximum reflow temperature	CX4017-16	
CX74017 with Moisture Sensitivity Level 3 (MSL3) and 250 °C maximum reflow temperature	CX74017-17	

General Information
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