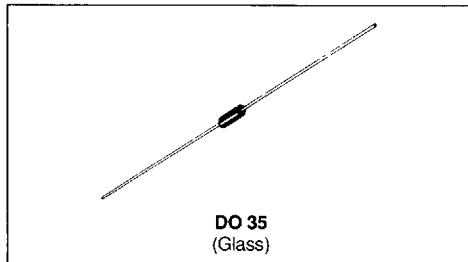


TEMPERATURE COMPENSATED ZENER DIODES

- SEMICONDUCTOR MATERIAL : SILICON
- TECHNOLOGY : LOCAL EPITAXY + GUARD RING



ABSOLUTE RATINGS (limiting values)

Symbol	Parameter	Value	Unit
P _{tot}	Power Dissipation*	0.4	W
T _{stg} T _J	Storage and Junction Temperature Range	-65 to 175 -65 to 175	°C °C
T _L	Maximum Lead Temperature for Soldering during 10s at 4mm from Case	230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R _(thJ/a)	Junction - ambient*	300	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Types	V _{ZT} typ. (V)	R _{ZT} @ I _{ZT} max. (Ω)	I _{ZT} max. (mA)	Test Temperatures			ΔV _Z ** max. (mV)	αV _Z (10 ⁻⁶ /°C)
				(°C)	(°C)	(°C)		
1N 4565	6.4	200	0.5	0	+ 25	+ 75	48	100
1N 4566	6.4	200	0.5	0	+ 25	+ 75	24	50
1N 4567	6.4	200	0.5	0	+ 25	+ 75	10	20
1N 4568	6.4	200	0.5	0	+ 25	+ 75	5	10
1N 4569	6.4	200	0.5	0	+ 25	+ 75	2	5
1N 4565 A	6.4	200	0.5	- 55	0	+ 25	99	100
1N 4566 A	6.4	200	0.5	- 55	0	+ 25	50	50
1N 4567 A	6.4	200	0.5	- 55	0	+ 25	20	20
1N 4568 A	6.4	200	0.5	- 55	0	+ 25	10	10
1N 4569 A	6.4	200	0.5	- 55	0	+ 25	5	5

* On infinite heatsink with d = 4mm

** The voltage reference diodes are characterized by the box method. The maximum allowable voltage change ΔV_Z is guaranteed any two temperature within the range. Tests are performed at the indicated temperatures and the specified current.

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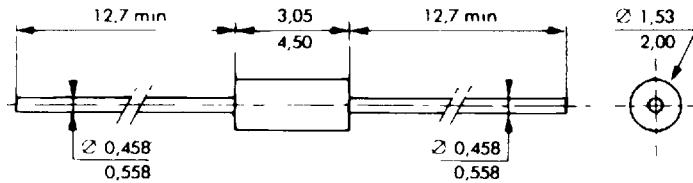
ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$ unless otherwise specified) (continued)

Types	V_{ZT} typ. (V)	R_{ZT} max. (Ω)	I_{ZT} (mA)	Test Temperatures			ΔV_z^{**} max. (mV)	αV_z ($10^{-6}/^\circ C$)
					(°C)			
1N 4570	6.4	100	1	0	+ 25	+ 75	48	100
1N 4571	6.4	100	1	0	+ 25	+ 75	24	50
1N 4572	6.4	100	1	0	+ 25	+ 75	10	20
1N 4573	6.4	100	1	0	+ 25	+ 75	5	10
1N 4574	6.4	100	1	0	+ 25	+ 75	2	5
1N 4570 A	6.4	100	1	- 55	0	+ 25	+ 75	+ 100
1N 4571 A	6.4	100	1	- 55	0	+ 25	+ 75	+ 100
1N 4572 A	6.4	100	1	- 55	0	+ 25	+ 75	+ 100
1N 4573 A	6.4	100	1	- 55	0	+ 25	+ 75	+ 100
1N 4574 A	6.4	100	1	- 55	0	+ 25	+ 75	+ 100
1N 4575	6.4	50	2		0	+ 25	+ 75	48
1N 4576	6.4	50	2		0	+ 25	+ 75	24
1N 4577	6.4	50	2		0	+ 25	+ 75	10
1N 4578	6.4	50	2		0	+ 25	+ 75	5
1N 4579	6.4	50	2		0	+ 25	+ 75	2
1N 4575 A	6.4	50	2	- 55	0	+ 25	+ 75	+ 100
1N 4576 A	6.4	50	2	- 55	0	+ 25	+ 75	+ 100
1N 4577 A	6.4	50	2	- 55	0	+ 25	+ 75	+ 100
1N 4578 A	6.4	50	2	- 55	0	+ 25	+ 75	+ 100
1N 4579 A	6.4	50	2	- 55	0	+ 25	+ 75	+ 100
1N 4580	6.4	25	4		0	+ 25	+ 75	48
1N 4581	6.4	25	4		0	+ 25	+ 75	24
1N 4582	6.4	25	4		0	+ 25	+ 75	10
1N 4583	6.4	25	4		0	+ 25	+ 75	5
1N 4584	6.4	25	4		0	+ 25	+ 75	2
1N 4580 A	6.4	25	4	- 55	0	+ 25	+ 75	+ 100
1N 4581 A	6.4	25	4	- 55	0	+ 25	+ 75	+ 100
1N 4582 A	6.4	25	4	- 55	0	+ 25	+ 75	+ 100
1N 4583 A	6.4	25	4	- 55	0	+ 25	+ 75	+ 100
1N 4584 A	6.4	25	4	- 55	0	+ 25	+ 75	+ 100

* * The voltage reference diodes are characterized by the box method. The maximum allowable voltage change ΔV_z is guaranteed any two temperature within the range. Tests are performed at the indicated temperatures and the specified current.

PACKAGE MECHANICAL DATA

DO 35 Glass



Cooling method . by convection and conduction.

Marking clear, ring at cathode end

Weight 0.15g

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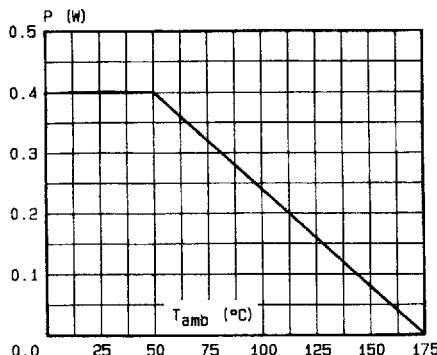


Fig.1 - Power dissipation versus ambient temperature.

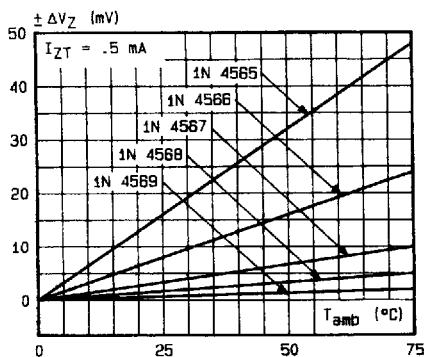


Fig.2a - Regulation voltage variation versus ambient temperature.

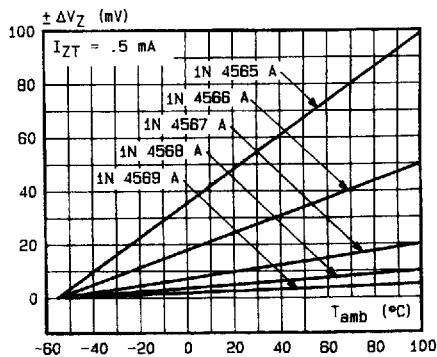


Fig.2b - Regulation voltage variation versus ambient temperature.

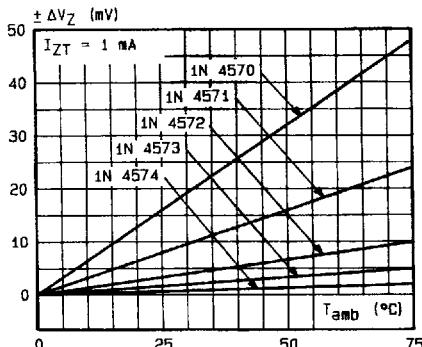


Fig.2c - Regulation voltage variation versus ambient temperature.

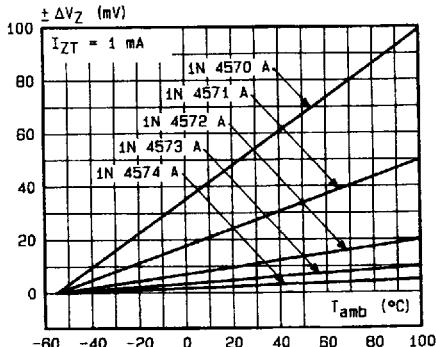


Fig.2d - Regulation voltage variation versus ambient temperature.

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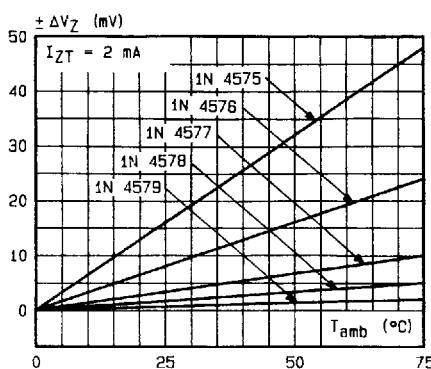


Fig.2e - Regulation voltage variation versus ambient temperature.

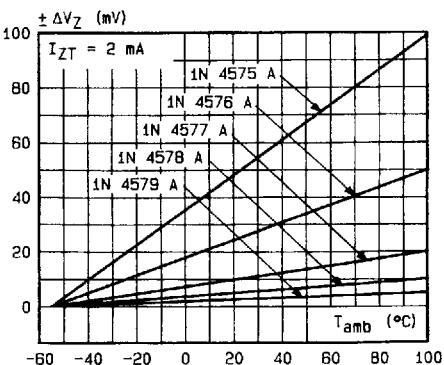


Fig.2f - Regulation voltage variation versus ambient temperature.

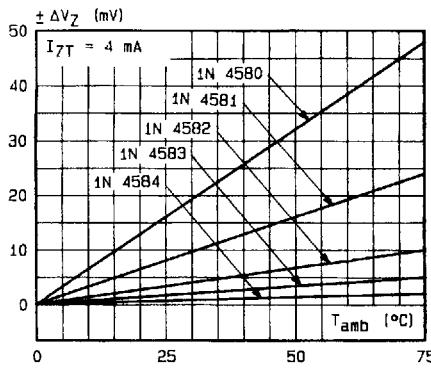


Fig.2g - Regulation voltage variation versus ambient temperature.

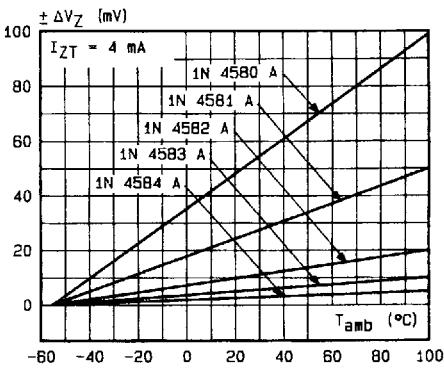


Fig.2h - Regulation voltage variation versus ambient temperature.