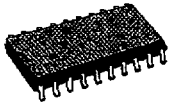
SGS-THOMSON MICROELECTRONICS

ITA6V1U3

MONOLITHIC TRANSIL® ARRAY FOR DATA LINE PROTECTION

FEATURES

- HIGH SURGE CAPABILITY TRANSIL ARRAY
  I_{PP} = 40 A 8/20µs
- UP TO 8 UNIDIRECTIONAL TRANSIL FUNCTIONS
- BREAKDOWN VOLTAGE= 6V1
- LOW LEAKAGE CURRENT
- LOW CLAMPING FACTOR (V_{CL}/ V_{BR}) AT HIGH CURRENT LEVEL.



SO 20
(Plastic)

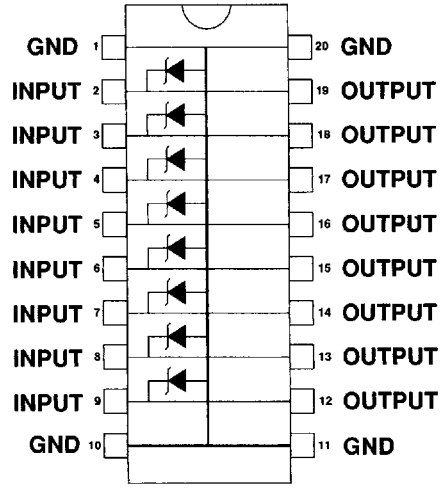
DESCRIPTION

Specially developed for RS 422 , RS 485 interface protection, this monolithic chip component offers a high surge capability and a low clamping voltage.

The internal wire bonding, "4 points connection", ensures a reliable protection against very fast transient overvoltages like ESD.

A low clamping voltage is guaranteed, eliminating all spikes due to the perturbation itself and also spikes induced by parasitic inductances created by external wiring.

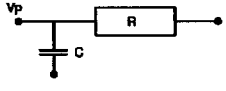
FUNCTIONAL DIAGRAM



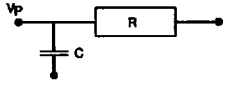
EQUIVALENT TO 8 UNIDIRECTIONAL TRANSILS

IN ACCORDANCE WITH :

- ESD standard :
  . IEC 801-2 15kV 5ns / 50ns
  . IEC 801-4 40A 5ns / 50ns
  . IEC 801-5 1kV 1.2 / 50µs
  25A 8/20µs
  . MIL STD 883C - Methode 3015-2
  V_P = 25kV
  C = 150pF
  R = 150Ω
  5 s duration



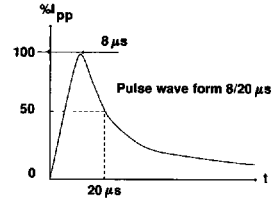
- Human body test :
  V_P = 4kV
  C = 150pF
  R = 150Ω



ABSOLUTE RATINGS (limiting values) (0°C ≤ Tamb ≤ 70°C)

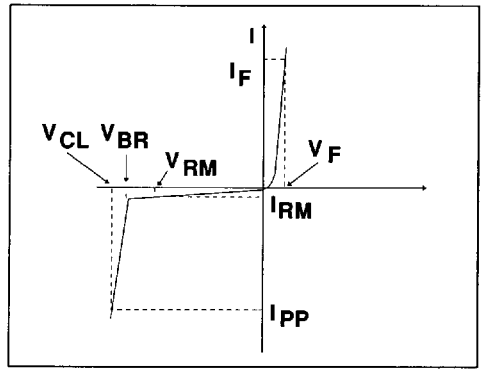
Symbol	Parameter		Value	Unit
I_{pp}	Peak pulse current - 8/20 µs	See note	40	A
I_{FSM}	Non repetitive surge peak forward current	tp= 10 ms	6	A
I^2t	Wire I^2t value	see note	0.6	A^2s
Tstg Tj	Storage and Junction Temperature Range		-55 to +150 125	°C °C

Note : For surges greater than the maximum value specified, the input/output will present first a short circuit to the common bus line and after an open circuit caused by the wire.



ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{CL}	Clamping Voltage
I_{RM}	Leakage Current @ VRM
I_{PP}	Surge Current
C	Input Capacitance
I_F	Forward Current
V_F	Forward Voltage Drop



Types	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{CL} @ I_{PP} 8/20µs		V_{CL} @ I_{PP} max 8/20µs See Note 1	
	µA	V	V	mA	V	A	V	A
ITA6V1U3	50	5	6.1	1	10	10	12	25

Types	V_F max @		C 1 max Note 2	C 2 max Note 3	α_T max
	V	A	pF	pF	10^{-4}/°C
ITA6V1U3	1.5	1	1100	700	4

All parameters tested at 25°C, except where indicated.

Note 1 : Between I/O pin and ground.
Note 2 : Between one input Pins at 0 V Bias, and ground
Note 3 : Between one input Pin at V_{RM}, and ground.

Figure 1 : Peak pulse power versus exponential pluse duration.

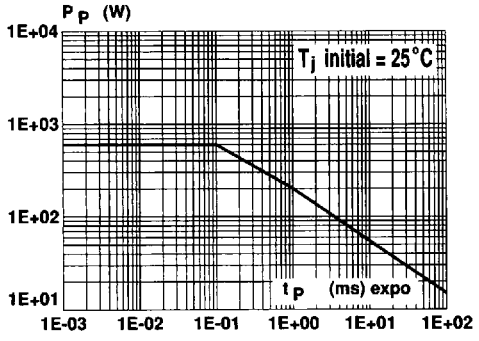


Figure 2 : Clampling voltage versus peak pulse current exponential waveform 8/20 ms.

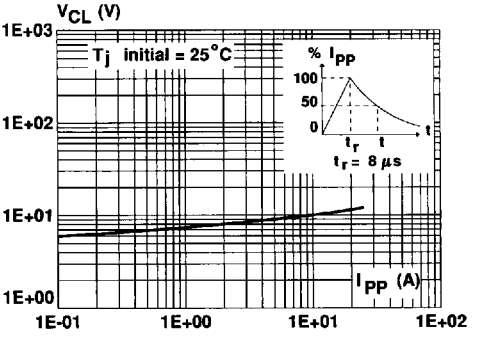


Figure 3 : Peak current IDC inducing open circuit of the wire for one input/output versus pulse duration (typical values).

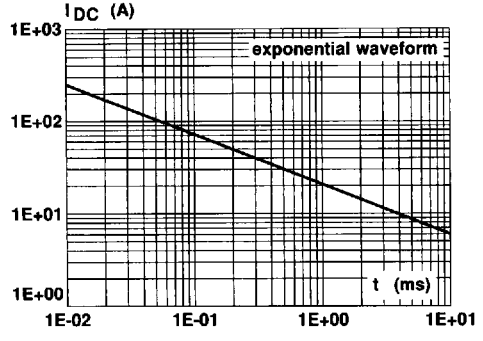
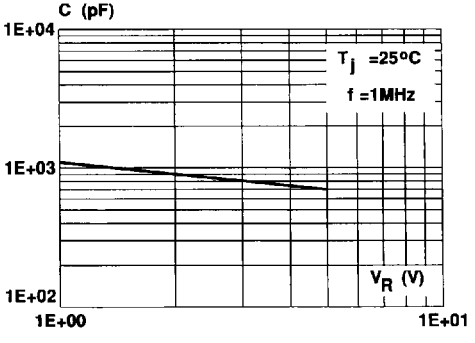


Figure 4 : Junction capacitance versus reverse applied voltage for one input/output (typical values).



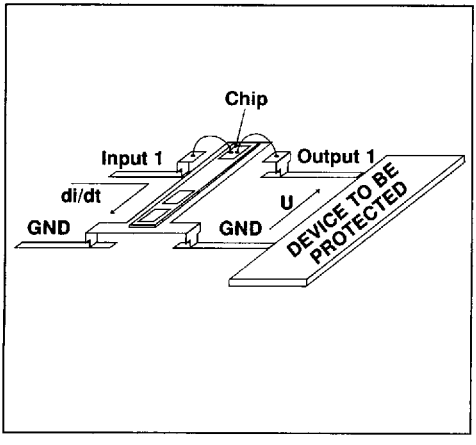
Note : The curve of the figure 2 is specified for a junction temperature of 25°C before surge

APPLICATION NOTICE

Design advantage of ITA6V1U3 used with 4 - points Structure.

The ITA6V1U3 has been designed with a 4 - points structure (Isolated Input/output) in order to efficiently protect against disturbances with very high (di/dt) rates, such as ESD.
The purpose is to eliminate the overvoltage introduced by the parasitic inductances of the wiring (L.di/dt).
But efficient protection depends not only on the component itself, but also on the schematic layout.

Figure 5 : 4 Point structure layout



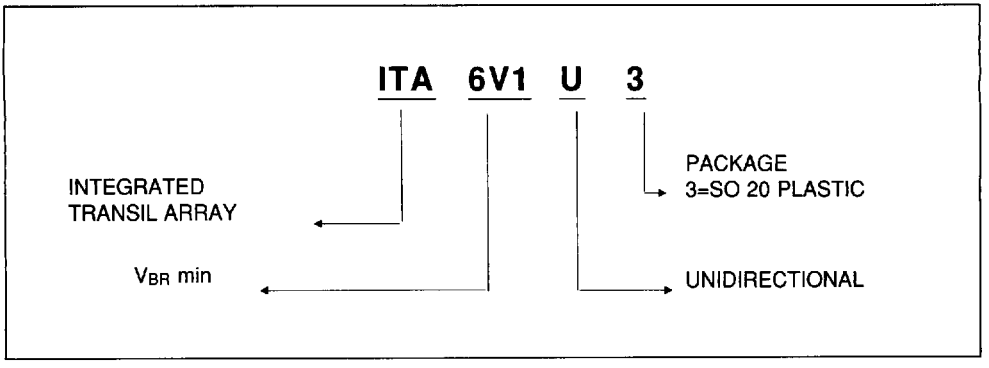
The schema given in fig. 5, shows the lay-out to be used in order to take advantage of the 4 - points structure of the ITA6V1U3.

With this lay-out, each of the lines to be protected passes through the protection device.

In this case, it works as an interface between the data line and the circuit to be protected, guaranteeing an isolation between its inputs and outputs.

The surge currrent is deviated through the input stage of the protection device.
The component to be protected is no longer exposed to any L.di/dt overvoltages.

ORDER CODE

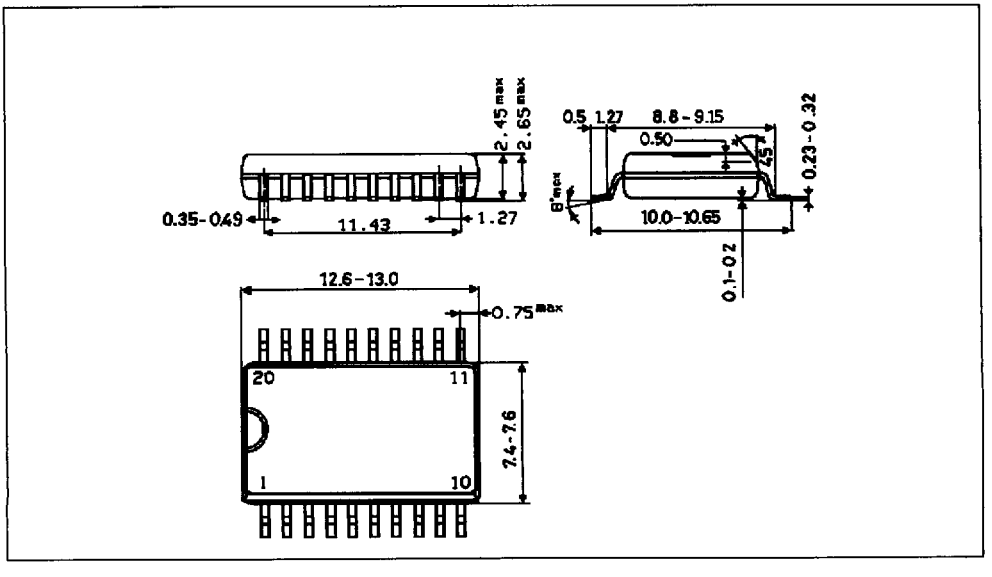


MARKING

TYPE	MARKING
ITA6V1U3	ITA6V1U3

PACKAGE MECHANICAL DATA (in millimeters)

SO 20 Plastic



Packaging : Products supplied in antistatic tubes