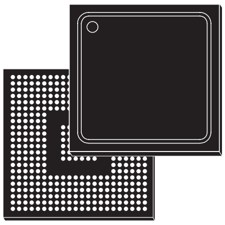
SPEAR-09-H022

SPEAr™ Head
ARM 926, 200K customizable eASIC™ gates, large IP portfolio SoC

PRELIMINARY DATA

Features

- ARM926EJ-S - f_{MAX} 266 MHz, 32 KI - 16 KD cache, 8 KI - KD tcm, ETM9 and JTAG interfaces
- 200K customizable equivalent ASIC gates (16K LUT equivalent) with 8 channels internal DMA high speed accelerator function and 112 dedicated general purpose I/Os
- Multilayer AMBA 2.0 compliant Bus with f_{MAX} 133 MHz
- Programmable internal clock generator with enhanced PLL function, specially optimized for E.M.I. reduction
- 16 KB single port SRAM embedded
- Dynamic RAM interface: 16 bit DDR, 32 / 16 bit SDRAM
- SPI interface connecting serial ROM and Flash devices
- 2 USB 2.0 Host independent ports with integrated PHYs
- USB 2.0 Device with integrated PHY
- Ethernet MAC 10/100 with MII management interface
- 3 independent UARTs up to 115 Kbps (Software Flow Control mode)
- I^2C Master mode - Fast and Slow speed
- 6 General Purpose I/Os



PBGA420

- ADC 8 bits, 230 Ksps, 16 analog input channels
- Real Time Clock
- WatchDog
- 4 General Purpose Timers
- Operating temperature: - 40 to 85 °C
- Package: PBGA 384+36 6R (23x23x2.16 mm)

Overview

SPEAr Head is a powerful digital engine belonging to SPEAr family, the innovative customizable System on Chips.

The device integrates an ARM core with a large set of proven IPs (Intellectual Properties) and a configurable logic block that allows very fast customization of unique and/or proprietary solutions, with low effort and low investment.

Optimized for embedded applications.

Order codes

Part number	Op. Temp. range, °C	Package	Packing
SPEAR-09-H022	-40 to 85	PBGA420 (23x23x2.16 mm)	Tray

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Reference Documentation

[1] ARM926EJ-S - Technical Reference Manual

[2] AMBA 2.0 Specification

[3] EIA/JESD8-9 Specification

[4] USB2.0 Specification

[5] OCHI Specification

[6] ECHI Specification

[7] UTMI Specification

[8] USB Specification

[9] IEEE 802.3 Specification

[10] I^{2}C - Bus Specification

2 Product Overview

SPEAr Head is a powerful System on Chip based on 110nm HCMOS and consists of 2 main parts: an ARM based architecture and an embedded customizable logic block.
The high performance ARM architecture frees the user from the task of developing a complete RISC system.
The customizable logic block allows user to design custom logic and special functions.

SPEAr Head is optimized for embedded applications and thanks to its high performance can be used for a wide range of different purposes.

Main blocks description:

1. CPU: ARM926EJ-S running at 266 MHz. It has:
   - MMU
   - 32 KB of instruction CACHE
   - 16 KB of data CACHE
   - 8 KB of instruction TCM (Tightly Coupled Memory)
   - 8 KB of data TCM
   - AMBA Bus interface
   - Coprocessor interface
   - JTAG
   - ETM9 (Embedded Trace Macro-cell) for debug; large size version.
2. Main Bus System: a complete AMBA Bus 2.0 subsystem connects different masters and slaves.
   The subsystem includes:
   - AHB Bus, for high performance devices
   - APB Bus, for low power / lower speed devices connectivity
   - Bus Matrix, for improving connection between the peripherals

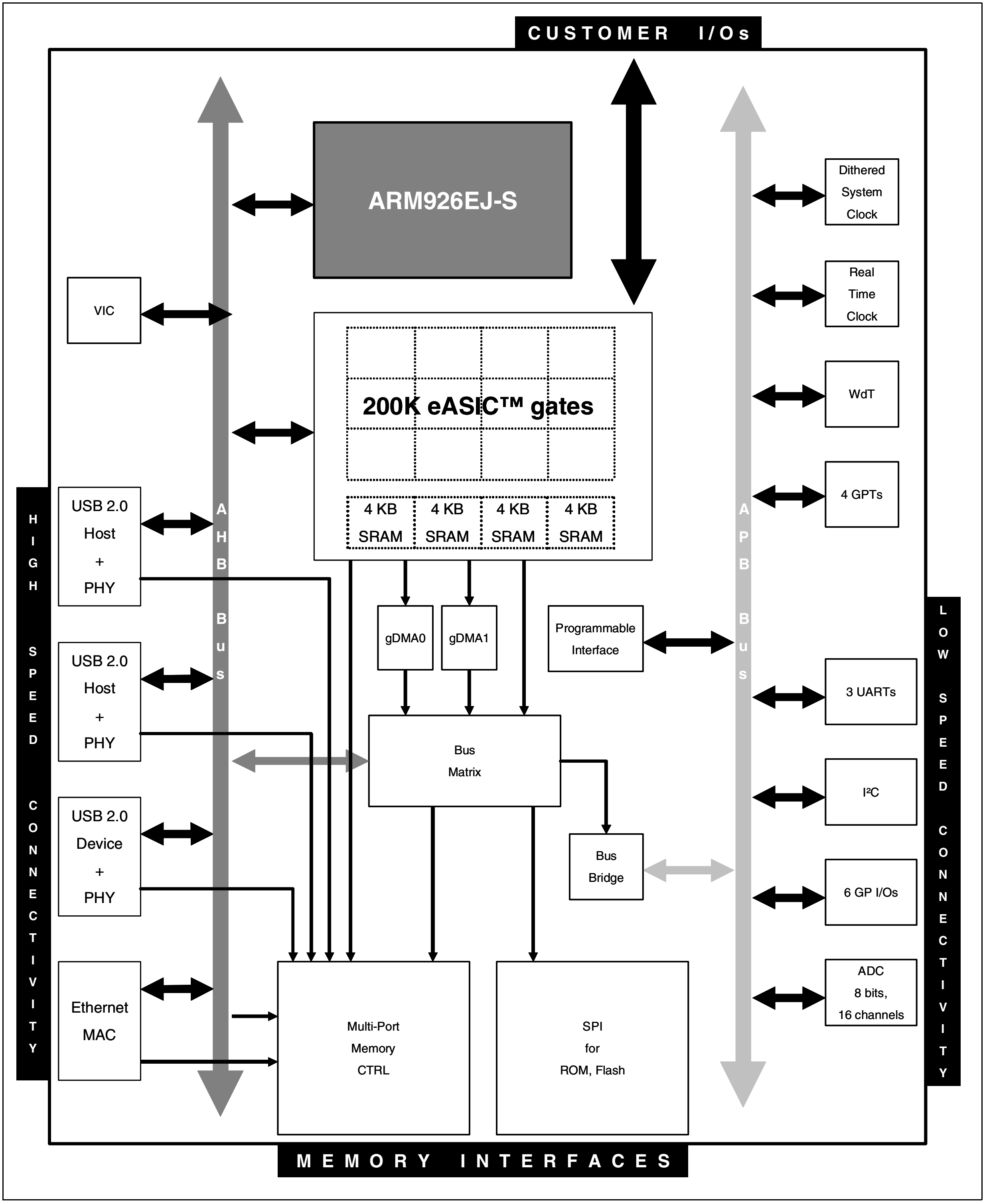
   Parts of these buses are available for the customizable logic block.
3. Clock and Reset System: fully programmable block with:
   - Separated set up between clocks of AHB Bus and APB Bus peripherals
   - E.M.I. reduction mode, replacing all traditional drop methods for Electro-Magnetic Interference
   - Debug mode, compliant with ARM debug status
4. Interrupt Controller: the Interrupt Controller has 32 interrupt sources which are prioritized and vectorized.
5. On-chip memory: 4 independent static RAM cuts, 4 KB each, are available.
   They can be used on AHB Bus or directly by the custom logic.
6. Dynamic Memory Controller: it is a Multi-Port Memory Controller which is able to connect directly to memory sizes from 16 to 512 Mbits; the data size can be 8 or 16 bits for both DDR and SDRAM, also 32 bits for SDRAM. The external data bus can be maximum 32 bit wide at maximum clock frequency of 133 MHz and have up to 4 chip selects; the accessible memory is 256 MB.
   Internally it handles 7 ports supporting the following masters: AHB Bus, Bus Matrix, 2 USB 2.0 Hosts, USB 2.0 Device, Ethernet MAC, eASIC MacroCell.

The Multi-Port Memory Controller block has a programmable arbitration scheme and the transactions happen on a different layer from the main bus.

7. Serial Peripheral Interface: it allows a serial connection to ROM and Flash.
   The block is connected as a slave on the main AHB Bus, through the Bus Matrix.
   The default bus size is 32 bit wide and the accessible memory is 64 MB at a maximum speed of 50 MHz
8. USB 2.0 Hosts: these peripherals are compatible with USB 2.0 High-Speed specification.
   They can work simultaneously either in Full-Speed or in High-Speed mode.
   The peripherals have dedicated channels to the Multi-Port Memory Controller and 4 slave ports for CPU programming.
   The PHYs are embedded.
9. USB 2.0 Device: the peripheral is compatible with USB 2.0 High-Speed specifications.
   A dedicated channel connects the peripheral with the Multi-Port Memory Controller and registers and internal FIFO are accessible from the CPU through the main AHB Bus.
   An USB-Plug Detector block is also available to verify the presence of the VBUS voltage.
   The port is provided with the following endpoints on the top of the endpoint 0:
   - 3 bulkin / bulkout endpoints
   - 2 isochronous endpoints.

   The PHY is integrated.
10. Ethernet Media Access Control (MAC) 10/100: this peripheral is compatible with IEEE 802.3 standard and supports the MII management interface for the direct configuration of the external PHY.
    It is connected to the Multi-Port Memory Controller through a dedicated channel.
    The Ethernet controller and the configuration registers are accessible from the main AHB Bus.
11. ADC: 8 bit resolution, 230 Ksps (Kilo-sample per second), with 16 analog input channels.
    Connected to APB bus.
12. UARTs: 3 independent interfaces, up to 115 Kbps each, support Software Flow Control.
    Connected to APB bus.
13. I^{2}C supporting Master mode protocol in Low and Full speed.
    Connected to APB bus.
14. 6 General Purpose I/O signals are available for user configuration.
    Connected to APB bus.
15. Embedded features: programmable Clock System and Dithered function, Real Time Clock, Watchdog, 4 General Purpose Timers.
    All blocks are interfaced with APB Bus.
16. Customizable Logic: it consists of an embedded macro where it is possible to map up to 200K equivalent ASIC gates. The same logic can be alternatively used to implement 32 KBytes of SRAM. Logic gates and RAM bits can be mixed in the same configuration so that processing elements, tightly coupled with embedded memories, can be easily implemented.
    The MacroCell has 2 dedicated buses, each of them connected with a 4 channel DMA in order to speed up the data flow with the main memories.
    8 interrupt lines and 112 dedicated general purpose I/Os are available.
    To allow a simple development of project, customizable logic can be emulated by an external FPGA, where customer can map his logic; FPGA is easy linkable and keeps the access to all on-chip and I/Os interfaces of the macro.

Figure 1. Block diagram



3 Features

3.1 CPU

- ARM926EJ-S RISC Processor
- f_{MAX} 266 MHz (downward scalable)
- Virtual address support with MMU
- 32 KB instruction CACHE (4 way set associative)
- 16 KB data CACHE (4 way set associative)
- 8 KB instruction TCM
- 8 KB data TCM
- Coprocessor interface
- JTAG
- ETM9 (rev 2.2), large size FIFO

3.2 INTERNAL BUS STRUCTURES

- Multilayer structure AMBA 2.0 compliant
- f_{MAX} 133 MHz
- High speed I/Os with embedded DMA function

3.3 CLOCK SYSTEM

- Programmable clock generator
- PLL with E.M.I. reduction
- Low Jitter PLL for USB 2.0

3.4 INTERRUPT CONTROLLER

- IRQ and FIQ interrupt generations
- Support up to 32 standard interrupts
- Support up to 16 vectored interrupts
- Software interrupt generation

3.5 MEMORY SYSTEM

MEMORY ON CHIP

16 KBytes single-port SRAM connected to eASIC MacroCell.

It can be used on AHB Bus or directly by the custom logic.

SPI

- 4 chip selects for asynchronous devices (ROM, Flash)
- Supports Normal mode 20 MHz and Fast mode 50 MHz
- AHB slave
- Accessible memory: 64 MB
- 8 / 16 / 32 bit widths
- Programmable wait states

MULTI-PORT MEMORY CONTROLLER

- Maximum clock frequency 133 MHz
- Support up to 7 AHB master requests
- AHB slave
- Support for 8, 16 and 32 bit wide SDRAM
- Support for 8 and 16 bit wide DDRAM
- 4 chip selects
- Physical addressable memory up to 256 MB
- Memory clock tuning to match the timing of different memory vendors

3.6 HIGH SPEED CONNECTIVITY

USB 2.0 HOST

- 2 USB 2.0 Host controllers with their UTMI PHY port embedded
- High-Speed / Full-Speed / Low-Speed modes USB 2.0 complaint
- DMA FIFO
- 4 AHB slaves for configuration and FIFO access
- 4 AHB masters for data transfer

USB 2.0 DEVICE

- UDC 2.0 controller with embedded PHY
- High-Speed / Full-Speed / Low-Speed modes USB 2.0 complaint
- USB Self-Power mode
- DMA FIFO
- AHB master interface for DMA transfer
- AHB slaves for: configuration, FIFO access, Plug autodetect
- Endpoints on the top of endpoint 0: 3 bulkin / bulkout, 2 isochronous

ETHERNET 10/100

- MAC110 controller compliant with IEEE 802.3 standard
- Supporting MII 10/100 Mbits/s
- MII management protocol interface
- TX FIFO (512x36 Dual Port)

- RX FIFO (512x36 Dual Port)
- AHB DMA master connected to memory system
- AHB slave for configuration

3.7 LOW SPEED CONNECTIVITY

UART

- Support for 8 bit serial data TX and RX
- Selectable 2 / 1 Stop bits
- Selectable Even, Odd and No Parity
- Parity, Overrun and Framing Error detector
- Max transfer rate: 115 Kbps

I^2C

- Standard I^2C mode (100 KHz) / Fast I^2C mode (400 KHz)
- Master interface only
- Master functions control all I^2C bus specific sequencing, protocol, arbitration and timing
- Detection of bus errors during transfers

3.8 GENERAL POURPOSE I/Os

6 programmable GP I/Os

3.9 ANALOG TO DIGITAL CONVERTER

- 8 bit resolutions
- 230 Ksps
- 16 analog input channels (0 - 3.3 V)
- INL ± 1 LSB
- DNL ± 0.5 LSB
- Programmable conversion speed - minimum conversion time 4.3 µs

3.10 REAL TIME CLOCK

- Real time clock-calendar (RTC)
- 14 digit (YYYY MM DD hh mm ss) precision
- Clocked by 32.768 KHz low power clock input
- Separated power supply (1.2 V)

3.11 WATCHDOG TIMER

- Programmable 16 bit Watchdog timer with reset output signal (more than 200 system clock period to initial peripheral devices)
- Programmable period 1 ~ 10 sec
- For recovery from unexpected system Hang-up

3.12 GENERAL PURPOSE TIMERS

- Four 16 bit timers with 8 bit prescaler
- Frequency range: 3.96 Hz - 66.5 MHz
- Operating mode: Auto Reload and Single Shot

3.13 CUSTOMIZABLE LOGIC

- 200K equivalent ASIC gate configurable either custom logic or 32 KBytes single-port SRAM or mixing logic and RAM
- 2 dedicated buses, each of them connected with a 4 channel DMA
- 8 interrupt lines (level type) available
- 112 dedicated GP I/Os
- Single VIA mask configurable interconnections
- Emulation by an external FPGA, keeping on-chip and I/O interfaces

4 Pin Description

4.1 FUNCTIONAL PIN GROUPS

With reference to *Figure 14*. Package schematic - *Section 8*, here follows the pin list, sorted by their belonging IP. All supply and ground pins are classified as power signals and gathered in the *Table 2*.

Table 1. Pin description by functional groups

Group	Signal Name	Ball	Direction	Function	Pin Type
ADC	AIN[0]	V20	Input	ADC analog input channel	Analog buffer, 3.3 V capable
	AIN[1]	V19			
	AIN[2]	V18			
	AIN[3]	V17			
	AIN[4]	V16			
	AIN[5]	V15			
	AIN[6]	V14			
	AIN[7]	V12			
	AIN[8]	V11			
	AIN[9]	V10			
	AIN[10]	V9			
	AIN[11]	V8			
	AIN[12]	U22			
	AIN[13]	U21			
	AIN[14]	U20			
	AIN[15]	U19			
	TEST_OUT	V13	Output	ADC output test pad	
DEBUG	TEST0	E22	Input	Test configuration port. For the functional mode they have to be set to 0	TTL input buffer, 3.3 V capable, with Pull Down
	TEST1	E21			
	TEST2	D22			
	TEST3	D21			
	PLL_BYPASS	Y5	Input	Enable / disable PLL bypass	TTL Schmitt trigger input buffer, 3.3 V capable
eASIC	eASICGP_IO[0]	G4	I/O	eASIC general purpose IO	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	eASICGP_IO[1]	G3			

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
eASIC	eASICGP_IO[2]	G2	I/O	eASIC general purpose IO	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	eASICGP_IO[3]	F5			
	eASICGP_IO[4]	F4			
	eASICGP_IO[5]	F3			
	eASICGP_IO[6]	F2			
	eASICGP_IO[7]	E9			
	eASICGP_IO[8]	E8			
	eASICGP_IO[9]	E7			
	eASICGP_IO[10]	E6			
	eASICGP_IO[11]	E5			
	eASICGP_IO[12]	E4			
	eASICGP_IO[13]	E3			
	eASICGP_IO[14]	E2			
	eASICGP_IO[15]	D8			
	eASICGP_IO[16]	D7			
	eASICGP_IO[17]	D6			
	eASICGP_IO[18]	D5			
	eASICGP_IO[19]	D4			
	eASICGP_IO[20]	D3			
	eASICGP_IO[21]	D2			
	eASICGP_IO[22]	C8			
	eASICGP_IO[23]	C7			
	eASICGP_IO[24]	C6			
	eASICGP_IO[25]	C5			
	eASICGP_IO[26]	C4			
	eASICGP_IO[27]	C3			
	eASICGP_IO[28]	C2			
	eASICGP_IO[29]	B8			
	eASICGP_IO[30]	B7			
	eASICGP_IO[31]	B6			
	eASICGP_IO[32]	B5			
	eASICGP_IO[33]	B4			
	eASICGP_IO[34]	B3			

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
eASIC	eASICGP_IO[35]	B2	I/O	eASIC general purpose IO	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	eASICGP_IO[36]	A8			
	eASICGP_IO[37]	A7			
	eASICGP_IO[38]	A6			
	eASICGP_IO[39]	A5			
	eASICGP_IO[40]	A4			
	eASICGP_IO[41]	A3			
	eASICGP_IO[42]	A2			
	eASICGP_IO[43]	D9			
	eASICGP_IO[44]	C9			
	eASICGP_IO[45]	B9			
	eASICGP_IO[46]	A9			
	eASICGP_IO[47]	E10			
	eASICGP_IO[48]	D10			
	eASICGP_IO[49]	C10			
	eASICGP_IO[50]	B10			
	eASICGP_IO[51]	A10			
	eASICGP_IO[52]	E11			
	eASICGP_IO[53]	D11			
	eASICGP_IO[54]	C11			
	eASICGP_IO[55]	B11			
	eASICGP_IO[56]	A11			
	eASICGP_IO[57]	E12			
	eASICGP_IO[58]	D12			
	eASICGP_IO[59]	C12			
	eASICGP_IO[60]	B12			
	eASICGP_IO[61]	A12			
	eASICGP_IO[62]	E13			
	eASICGP_IO[63]	D13			
	eASICGP_IO[64]	C13			
	eASICGP_IO[65]	B13			

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
eASIC	eASICGP_IO[66]	A13	I/O	eASIC general purpose IO	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	eASICGP_IO[67]	E14			
	eASICGP_IO[68]	D14			
	eASICGP_IO[69]	C14			
	eASICGP_IO[70]	B14			
	eASICGP_IO[71]	A14			
	eASICGP_IO[72]	E15			
	eASICGP_IO[73]	D15			
	eASICGP_IO[74]	C15			
	eASICGP_IO[75]	B15			
	eASICGP_IO[76]	A15			
	eASICGP_IO[77]	E16			
	eASICGP_IO[78]	D16			
	eASICGP_IO[79]	C16			
	eASICGP_IO[80]	B16			
	eASICGP_IO[81]	A16			
	eASICGP_IO[82]	E17			
	eASICGP_IO[83]	D17			
	eASICGP_IO[84]	C17			
	eASICGP_IO[85]	B17			
	eASICGP_IO[86]	A17			
	eASICGP_IO[87]	L18			
	eASICGP_IO[88]	K18			
	eASICGP_IO[89]	J18			
	eASICGP_IO[90]	H18			
	eASICGP_IO[91]	G18			
	eASICGP_IO[92]	F18			
	eASICGP_IO[93]	E18			
	eASICGP_IO[94]	D18			
	eASICGP_IO[95]	C18			
	eASICGP_IO[96]	B18			
	eASICGP_IO[97]	A18			
	eASICGP_IO[98]	J19			

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
eASIC	eASICGP_IO[99]	H19	I/O	eASIC general purpose IO	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	eASICGP_IO[100]	G19			
	eASICGP_IO[101]	F19			
	eASICGP_IO[102]	E19			
	eASICGP_IO[103]	D19			
	eASICGP_IO[104]	C19			
	eASICGP_IO[105]	B19			
	eASICGP_IO[106]	A19			
	eASICGP_IO[107]	G20			
	eASICGP_IO[108]	F20			
	eASICGP_IO[109]	E20			
	eASICGP_IO[110]	D20			
	eASICGP_IO[111]	C20			
	eASIC_EXT_CLOCK	B21			
	eASIC_PI_CLOCK	R18		eAISC Program Interface out clock	TTL bidirectional buffer, 3.3 V capable, 8 mA drive capability
	eASIC_CLK	G5		eASIC output clock	
	CONFIG_DEVEL	A20	Input	External FPGA emulation mode	TTL input buffer, 3.3 V capable with Pull Down
Ethernet	TX_CLK	J20	Input	Ethernet input TX clock	TTL bidirectional buffer, 5 V tolerant, 4 mA drive capability, with Pull Down
	TXD[0]	J21	Output	Ethernet TX output data	
	TXD[1]	J22			
	TXD[2]	K19			
	TXD[3]	K20			
	TX_EN	K21		Ethernet TX enable	
	CRS	K22	Input	Carrier sense input	
	COL	L19		Collision detection input	
	RX_CLK	L20		Ethernet input RX clock	
	RXD[0]	L21		Ethernet RX input data	
	RXD[1]	L22			
	RXD[2]	M19			
	RXD[3]	M20	Input		
	RX_DV	M21	Input	Data valid on RX	
	RX_ER	M22	Input	Data error detected	

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
Ethernet	MDC	N19	Output	Output timing reference for MDIO	TTL bidirectional buffer, 5 V tolerant, 4 mA drive capability, with Pull Down
	MDIO	N20	I/O	I/O data to PHY	
GPI/Os	GP_IO[0]	T22	I/O	General Purpose IO	TTL bidirectional buffer, 3.3 V capable, 8 mA drive capability
	GP_IO[1]	T21			
	GP_IO[2]	T20			
	GP_IO[3]	T19			
	GP_IO[4]	R22			
	GP_IO[5]	R21			
I^2C	SDA	N21		I^2C serial data	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability, with Pull Up
	SCL	N22			
JTAG	TDO	A21	Output	Jtag TDO	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	TDI	A22	Input	Jtag TDI	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability, with Pull Up
	TMS	B20	Input	Jtag TMS	
	RTCK	B22	Output	Jtag output clock	
	TCK	C21	Input	Jtag clock	
	nTRST	C22	Output	Jtag reset	
MASTER CLOCK	MCLK_in	T1	Input	12 MHz input cristal	Oscillator 3.3 V capable
	MCLK_out	U1	Output	12 MHz output cristal	
MASTER RESET	MRESET	H4	Input	Master reset	TTL Schmitt trigger input buffer, 3.3 V capable
MPMC	MPMCDATA[0]	AA12	I/O	DDR / SDRAM data	LVTTL / SSTL ClassII bidirectional buffer
	MPMCDATA[1]	Y12			
	MPMCDATA[2]	W12			
	MPMCDATA[3]	AB13			
	MPMCDATA[4]	AA13			
	MPMCDATA[5]	Y13			
	MPMCDATA[6]	W13			

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
MPMC	MPMCDATA[6]	W13	I/O	DDR / SDRAM data	LVTTL / SSTL ClassII bidirectional buffer
	MPMCDATA[7]	AA14			
	MPMCDATA[8]	AA16			
	MPMCDATA[9]	AB18			
	MPMCDATA[10]	AB19			
	MPMCDATA[11]	AB20			
	MPMCDATA[12]	AB21			
	MPMCDATA[13]	AA21			
	MPMCDATA[14]	AB22			
	MPMCDATA[15]	AA22			
	MPMCDATA[16]	AA18	I/O	SDRAM data	TTL bidirectional buffer, 3.3 V capable, 8 mA drive capability
	MPMCDATA[17]	AA17			
	MPMCDATA[18]	Y22			
	MPMCDATA[19]	Y21			
	MPMCDATA[20]	Y20			
	MPMCDATA[21]	Y19			
	MPMCDATA[22]	Y18			
	MPMCDATA[23]	Y17			
	MPMCDATA[24]	Y16			
	MPMCDATA[25]	W22			
	MPMCDATA[26]	W21			
	MPMCDATA[27]	W20			
	MPMCDATA[28]	W19			
	MPMCDATA[29]	W18			
	MPMCDATA[30]	W17			
	MPMCDATA[31]	W16			
	MPMCADDROUT[0]	AB8	Output	DDR / SDRAM data	LVTTL / SSTL ClassII bidirectional buffer
	MPMCADDROUT[1]	AA8			
	MPMCADDROUT[2]	Y8			
	MPMCADDROUT[3]	W8			
	MPMCADDROUT[4]	AB9			
	MPMCADDROUT[5]	AA9			
	MPMCADDROUT[6]	Y9			
	MPMCADDROUT[7]	W9			
	MPMCADDROUT[8]	AB10			

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
MPMC	MPMCADDROUT[9]	AA10	Output	DDR / SDRAM data	LVTTL / SSTL ClassII bidirectional buffer
	MPMCADDROUT[10]	Y10			
	MPMCADDROUT[11]	W10			
	MPMCADDROUT[12]	AB11			
	MPMCADDROUT[13]	AA11			
	MPMCADDROUT[14]	Y11			
	nMPMCDYCSOUT[0]	AB6		DDR / SDRAM chip select	
	nMPMCDYCSOUT[1]	AA6			
	nMPMCDYCSOUT[2]	Y6			
	nMPMCDYCSOUT[3]	W6			
	MPMCCKEOUT[0]	W11		DDR / SDRAM clock enable output	
	MPMCCKEOUT[1]	AB12			
	MPMCCLKOUT[0]	AB17		DDR / SDRAM output clock 1	LVTTL / SSTL ClassII bidirectional differential buffer
	nMPMCCLKOUT[0]	AB16		DDR / SDRAM output clock 1 neg.	
	MPMCCLKOUT[1]	AB15		DDR / SDRAM output clock 2	
	nMPMCCLKOUT[1]	AB14		DDR / SDRAM output clock 2 neg.	
	MPMCDQMOUT[0]	Y14		DDR / SDRAM data mask out	LVTTL / SSTL ClassII bidirectional buffer
	MPMCDQMOUT[1]	W15			
	MPMCDQMOUT[2]	AA19		SDRAM data mask out	TTL bidirectional buffer, 3.3 V capable, 8 mA drive capability
	MPMCDQMOUT[3]	AA20			
	MPMCDQS[0]	AA15		DDR data strobe	LVTTL / SSTL ClassII bidirectional buffer
	MPMCDQS[1]	Y15			
	nMPMCCASOUT	Y7		DDR / SDRAM CAS output strobe	
	nMPMCRASOUT	AA7			
	nMPMCWEOUT	AB7		DDR / SDRAM write enable	
	SSTL_VREF	W14	Input	Voltage reference SSTL / CMOS mode. This pin is used both as logic state and as power supply	Analog buffer, 3.3 V capable
RTC	RTCXO	AB5	Output	32 KHz output crystal	Oscillator 1.2 V capable
	RTCXI	AB4	Input	32 KHz input crystal	
SMI	SMINCS[0]	G22	Output	Serial Flash chip select	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
SMI	SMINCS[1]	G21		Serial Flash chip select	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	SMINCS[2]	F22			
	SMINCS[3]	F21			
	SMICLK	H20	Output	Serial Flash output clock	TTL bidirectional buffer, 3.3 V capable, 8 mA drive capability
	SMIDATAIN	H21	Input	Serial Flash data in	TTL bidirectional buffer, 3.3 V capable, 8 mA drive capability, with Pull Up
	SMIDATAOUT	H22	Output	Serial Flash data out	TTL bidirectional buffer, 3.3 V capable, 8 mA drive capability
UARTs	UART1_RXD	P19	Input	Uart1 RX data	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability, with Pull Down
	UART1_TXD	P20	Output	Uart1 TX data	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	UART2_RXD	P21	Input	Uart2 RX data	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability, with Pull Down
	UART2_TXD	P22	Output	Uart2 TX data	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	UART3_RXD	R19	Input	Uart3 RX data	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability, with Pull Down
	UART3_TXD	R20	Output	Uart3 TX data	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability

Table 1. Pin description by functional groups (continued)

Group	Signal Name	Ball	Direction	Function	Pin Type
USBs	DMNS	W1	I/O	D - port of USB device	Analog buffer, 5 V tolerant
	DPLS	V1	I/O	D + port of USB device	
	HOST1_DP	P1	I/O	D - port of USB host1	
	HOST1_DM	N1	I/O	D + port of USB host1	
	HOST2_DP	L1	I/O	D - port of USB host2	
	HOST2_DM	K1	I/O	D + port of USB host2	
	HOST1_VBUS	H2	Output	USB host1 VBUS signal	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	HOST2_VBUS	H1	Output	USB host2 VBUS signal	
	OVERCURH1	G1	I/O	USB host1 overcurrent	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability, with Pull Down
	OVERCURH2	F1	I/O	USB host2 overcurrent	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability
	VBUS	H3	I/O	USB device VBUS signal	TTL bidirectional buffer, 3.3 V capable, 4 mA drive capability, with Pull Down
	RREF	K5	Input	USB reference resistor	Analog buffer, 3.3 V capable

Table 2. Pins belonging to POWER group

Group	Signal Name	Ball	Function
POWER	vdde3v3	Note 1	Digital 3.3 V power
	vdd	Note 2	Digital 1.2 V power
	gnde	Note 3	Digitalground
	vdd3core	V22	Dedicated ADC 3.3 V power
	vsscore	U18	Dedicated ADC ground
	VREFP_adc	V21	ADC positive reference Voltage
	VREFN_adc	T18	ADC pegative reference Voltage
Group	**Signal Name**	**Ball**	**Function**

Table 2. Pins belonging to POWER group (continued)

POWER	vdd3core	W7	DDR / SDR dedicated digital PLL 3.3 V power
	vsscore	V7	DRR / SDR dedicated digital PLL ground
	SSTL_VREF	W14	Voltage reference SSTL / CMOS mode. This pin is used both as logic state and as power supply
	vdde3v3	Note 4	DDR / SDR digital 3.3 / 2.5V power
	vdde3v3	AB2	3.3 V dedicated power for RTC
	vdd	AA5	1.2 V dedicated power for RTC
	gnd	AA4	Dedicated digital ground for RTC
	gnde	AB3	Dedicated digital ground for RTC
	vdd3core	R2	Dedicated USB PLL analog 3.3 V power
	vsscore	P4	Dedicated USB PLL analog ground
	vddcore	R4	Dedicated USB PLL digital 1.2 V power
	vsscore	U2	Dedicated USB PLL digital ground
	vddcore	W3	Dedicated USB 1.2 V power
	vddcore	U4	Dedicated USB 1.2 V power
	vddcore	U3	Dedicated USB 1.2 V power
	vdd	P2	Dedicated USB 1.2 V power
	vddcore	N5	Dedicated USB 1.2 V power
	vddcore	N3	Dedicated USB 1.2 V power
	vddcore	L4	Dedicated USB 1.2 V power
	vddcore	K4	Dedicated USB 1.2 V power
	vddcore	K3	Dedicated USB 1.2 V power
	vddcore	J4	Dedicated USB 1.2 V power
	vdd3core	W4	Dedicated USB 3.3 V power
	vdde3v3	P5	Dedicated USB 3.3 V power
	vdd3core	L3	Dedicated USB 3.3 V power
	vdd3core	J3	Dedicated USB 3.3 V power
	vsscore	W5	Dedicated USB ground
	vsscore	W2	Dedicated USB ground
	vsscore	U5	Dedicated USB ground
	gnde	R3	Dedicated USB ground
	gnd	N4	Dedicated USB ground
	vsscore	N2	Dedicated USB ground
	vsscore	M2	Dedicated USB ground

Note: 1 Signal spread on the following balls: F7, F8, F9, F12, F13, F14, F17, G17 H6, J6, K7, L7, M5, N6, P6, P7,R7, U6, U16.

2 Signal spread on the following balls: F6, F10, F11, F15, F16, G6, H17, J17, K6, L6, M17, N17, R6, T6, T17, U17.

3 Signal spread on the following balls: J9 to J14, K9 to K14, L9 to L14, M9 to M14, N9 to N14, P9 to P14.

4 Signal spread on the following balls: U7 to U15

4.2 SPECIAL IOs

4.2.1 USB 2.0 Transceiver

SPEAr Head has three USB 2.0 UTMI + Multimode ATX transceivers. One transceiver will be used by the USB Device controller, and two will be used by the Hosts. These are all integrated into a single USB three-PHYs macro.

4.2.2 DRAM

Data and address buses of Multi-Port Memory Controller used to connect to the banks memory are constituted of programmable pins.

5 Power On Sequence

5.1 SPEAr Head SW ARCHITECTURE

5.1.1 BOOT PROCESS

Memory mapping

A major consideration in the design of an embedded ARM application is the layout of the memory map, in particular the memory that is situated at address 0x0. Following reset, the core starts to fetch instructions from 0x0, so there must be some executable code accessible from that address. In an embedded system, this requires ROM to be present, at least initially.

Serial Flash at 0x0

The SPEAr Head has been designed to use the REMAP concept into its AHB primary bus decoder. The decoder selection for the initial address range (first 64 MB) is conditioned with the content of a AHB remap register, which can be programmed by software at any time.

The Serial Flash memory space is accessible in the address range 0x9600_0000 - 0x99FF_FFFF (64 MB), with or without remap.

At reset, before remapping, the Serial Flash memory is 'aliased' at 0x0, which means that the AHB decoder selects the Serial Flash space when accessing the address range 0x0000_0000 to 0x03FF_FFFF.

Table 3. Memory mapping at reset - before remapping

ADDRESS RANGE	SIZE [MB]	DESCRIPTION
0x9600_0000 - 0x99FF_FFFF	64	Serial Flash
Unreachable in this state	n. a.	DRAM
0x0000_0000 - 0x03FF_FFFF	64	Serial Flash (remap)

DRAM at 0x0

After reset, the boot program makes the remapping, so that the system will be able to access the complete 256 MB of logic memory space associated to DRAM in the range 0x0000_0000 - 0x0FFF_FFFF.

Table 4. Memory Mapping after reset after remapping

ADDRESS RANGE	SIZE [MB]	DESCRIPTION
0x9600_0000 - 0x99FF_FFFF	64	Serial Flash
0x0000_0000 - 0x0FFF_FFFF	256	DRAM

5.1.2 BOOTING SEQUENCE

A simple initial description of the boot process is showed in the following steps:

1. Power on to fetch the RESET vector at 0x0000_0000 (from the aliased-copy of Serial Flash).
2. Perform any critical CPU initialization at this time.
3. Load into the Program Counter (PC) the address of a routine that will be executed directly from the non-aliased mapping of Serial Flash (0x9600_0000 + addr_of_routine) and which main objectives are:
   - un-map the aliased-copy of the Serial Flash (set REMAP = 1)
   - copy the program text and data into DRAM.
4. Returning from this routine will set the Program Counter back to DRAM.

6 IP Description

In this section you can find the description of the IP's embedded in SPEAr Head.

6.1 ARM926EJ-S

The processor is the powerful ARM926EJ-S, targeted for multi-tasking applications.

Belonging to ARM9 general purposes family microprocessor, it principally stands out for the Memory Management Unit, which provides virtually memory features, making it also compliant with WindowsCE, Linux and SymbianOS operating systems.

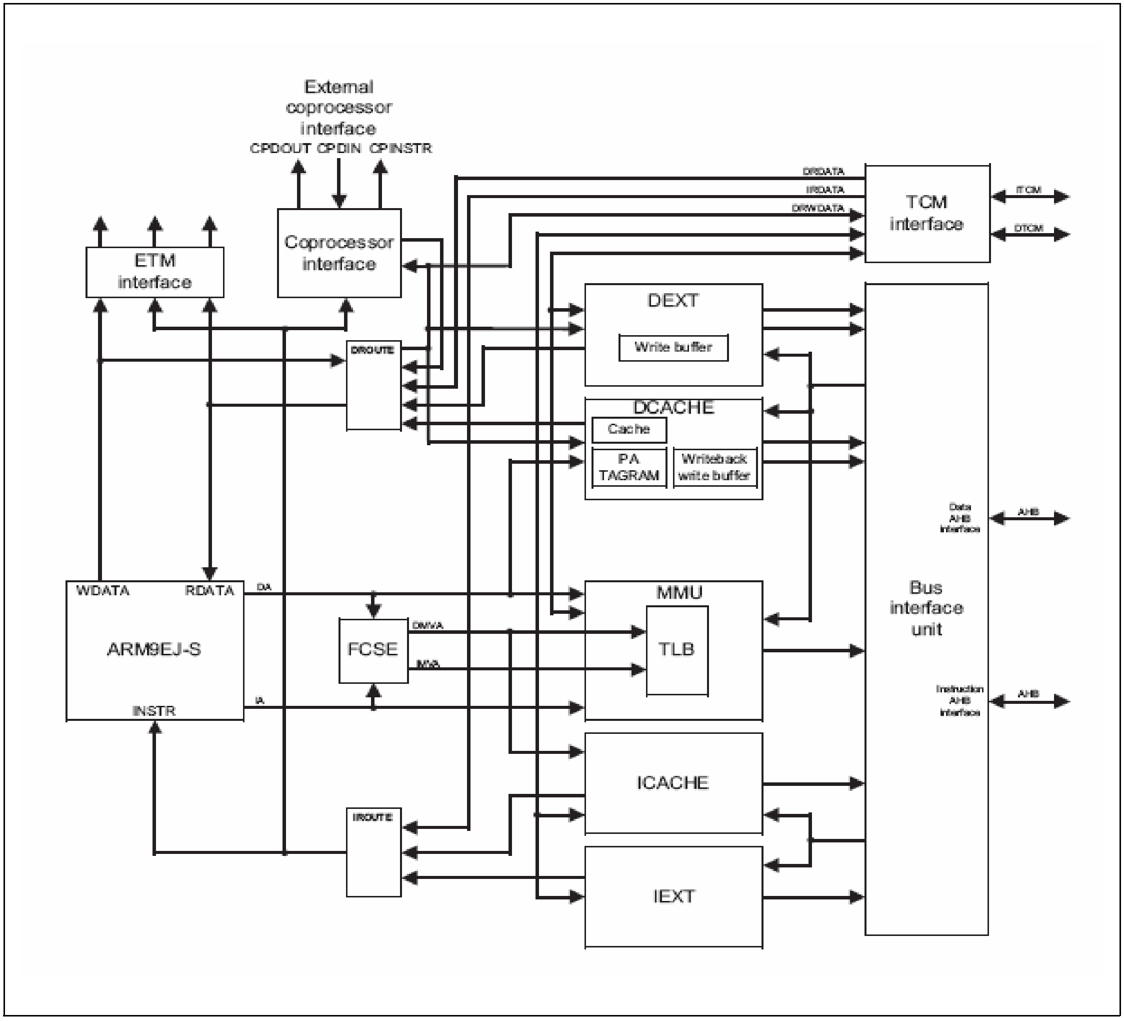
The ARM926EJ-S supports the 32 bits ARM and 16 bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

Besides, it has the ARM debug architecture and includes logic to assist in both hardware and software debug.

Its main features are:

- f_{MAX} 266 MHz (downward scalable)
- MMU
- 32 KB of instruction CACHE
- 16 KB of data CACHE
- 8 KB of instruction TCM (Tightly Coupled Memory)
- 8 KB of data TCM
- AMBA Bus interface
- Coprocessor interface
- JTAG
- ETM9 (Embedded Trace Macro-cell) for debug; large size version.

Figure 2. ARM926EJ-S block diagram



6.2 CLOCK AND RESET SYSTEM

6.2.1 OVERVIEW

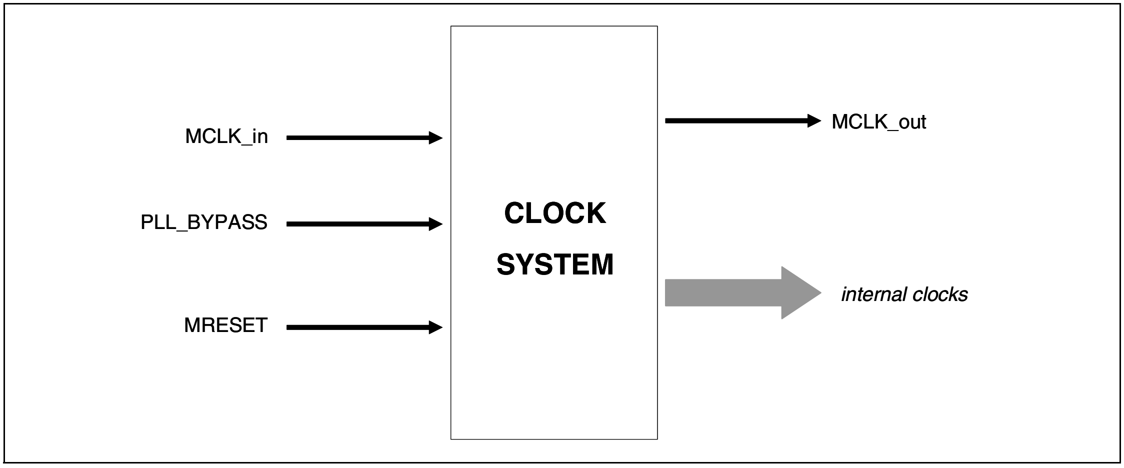
The Clock System is a fully programmable block able to generate every clock necessary at the chip (except for USB 2.0 Host and Device controllers, which have a dedicated PLL); they are:

- clock @ 266 MHz for ARM system
- clock @133MHz for all IPs on AHB Bus
- clock @ 66.5 MHz for APB Bridge and APB peripherals
- clock for eASIC MacroCell
- clock for eASIC Programmable Interface

The block has an embedded PLL, featuring Electro-Magnetic Interference reduction. User has the possibility to set up the PLL in order to add a triangular wave to the VCO clock; the resulting signal will have the spectrum (and the power) spread on a small range (programmable) of frequencies centred on F_0 (VCO Freq.), obtaining minimum electromagnetic emissions.

This method replace all the other traditional methods of E.M.I. reduction, as filtering, ferrite beads, chokes, adding power layers and ground planets to PCBs, metal shielding etc., allowing sensible cost saving for customers.

Figure 3. Clock System block interfaces



The I/O signals accessible from off-chip are listed in *Table 5*. Clock System I/O off-chip interface:

Table 5. Clock System I/O off-chip interface

SIGNALS	DIRECTION	SIZE [bit]	DESCRIPTION
MCLK_in	Input	1	Oscillator input (12 MHz)
PLL_BYPASS	Input	1	External clock in Test mode
MCLK_out	Output	1	Oscillator output. It supplies the signal MCLK_in inverted
MRESET	Input	1	Asynchronous reset

The reference clock frequency is 12 MHz and it is used to generate the 266 MHz clock by an internal PLL. Then starting by this, output signals are generated programming the Clock System registers, via APB Bus.

The purpose of PLL_BYPASS mainly is let the rest of the chip working properly even in case of PLL failure.

6.2.2 RESET AND PLL CHANGE PARAMETERS SEQUENCE

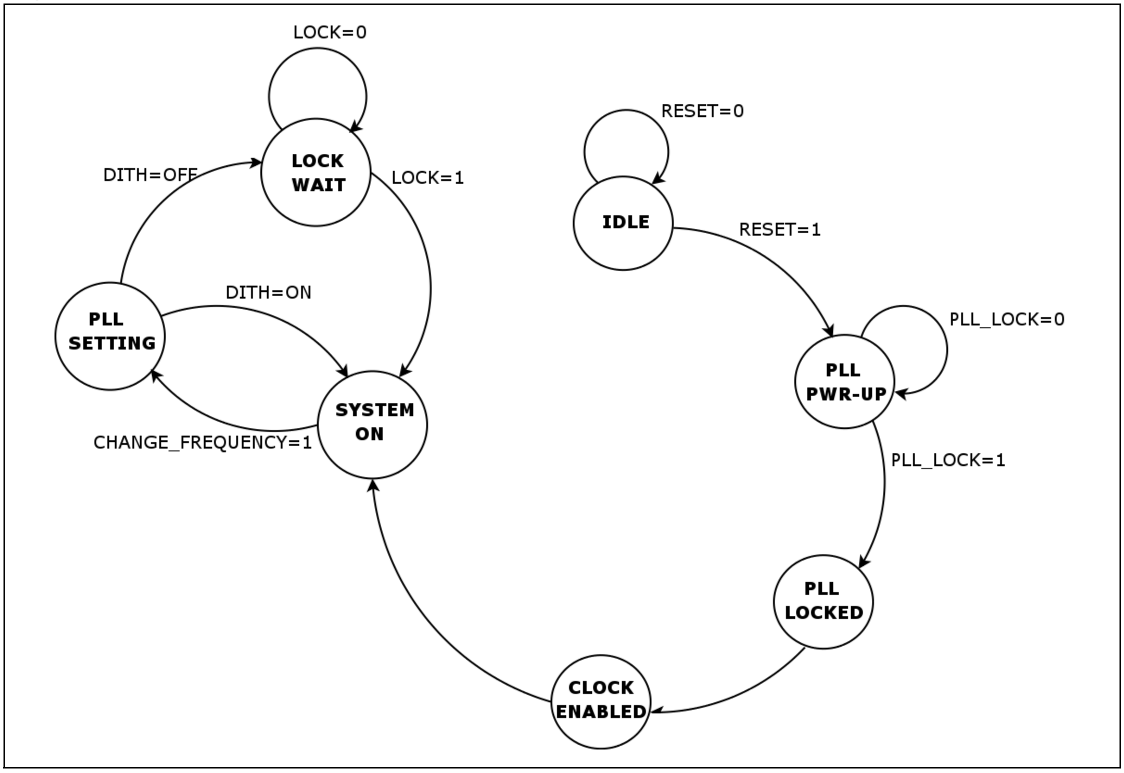
Figure 4 shows a simplified flow chart of clock system FSM.

The system remains in an IDLE state until RESET signal is asserted: RESET→ 0.

When RESET = 0 the FSM change state and reaches the PLL_PWR-UP state; when PLL locks (PLL_LOCK = 1), means that the PLL_OUT signal oscillates at 264 MHz and the PLL starts to work, so that the FSM advances in the next states.

In CLOCK_ENABLED state the clocks can propagate in the system; then the FSM goes in SYSTEM_ON state; it remains in this state in the normal chip working.

Figure 4. State Machine of Clock System



To reach at a clock frequency of 266 MHz, PLL had to be appropriately programmed because this frequency isn't an integer multiple of 12 MHz.

After this programming, the FSM stops all the clocks and exits from SYSTEM ON state proceeding in PLL SETTING state; here the new parameters are stored in the PLL.

If the PLL isn't in Dithered mode the FSM waits for PLL lock, going in LOCK WAIT state, and then will reach SYSTEM ON state when PLL locks.

If the PLL is in Dithered mode, the lock signal loses his meaning and there's no need to wait for PLL lock, so the FSM jumps directly from PLL SETTING to SYSTEM ON.

When FSM is in SYSTEM ON, all clocks are enabled.

6.3 VECTORED INTERRUPT CONTROLLER

6.3.1 OVERVIEW

The Vector Interrupt Controller provides a software interface to interrupt system, in order to determine the source that is requesting a service and where the service routing is loaded.

It supplies the starting address, or vector address, of the service routine corresponding to the highest priority requesting interrupt source.

In an ARM system 2 level of interrupt are available:

- Fast Interrupt Request (FIQ) for low latency interrupt handling
- Interrupt Request (IRQ) for standard interrupts

Generally, you only use a single FIQ source at a time to provide a true low-latency interrupt. This has the following benefits:

- You can execute the interrupt service routine directly without determining the source of the interrupt
- It reduces interrupt latency. You can use the banked registers available for FIQ interrupts more efficiently, because you do not require a context save

The interrupt inputs must be level sensitive, active HIGH, and held asserted until the interrupt service routine clears the interrupt. Edge-triggered interrupts are not compatible.

The interrupt inputs do not have to be synchronous to AHB clok.

The main features of Vectored Interrupt Controller are:

- Compliance to AMBA Specification Rev. 2.0
- IRQ and FIQ interrupt generation
- AHB mapped for faster interrupt
- Hardware priority
- Support for 32 standard interrupts
- Support for 16 vectored interrupts
- Software interrupt generation
- Interrupt masking
- Interrupt request status.

Since 32 interrupts are supported, there are 32 interrupt input lines, coming from different sources. They are selected by a bit position and the software controls every line to generate software interrupts; it can generate 16 vectored interrupts. A vectored interrupt can generate only an IRQ interrupt.

The interrupt priority is controlled by hardware and it is as follow:

1. FIQ interrupt
2. vectored IRQ interrupt. The higher priority is 0; the lower is 15
3. non vectored IRQ interrupt

6.3.2 INTERRUPTR SOURCES IN SPEAr Head

Table 6. Interrupt sources in SPEAr Head

Interrupt Line	Source
0	eASIC0
1	eASIC1
2	eASIC2
3	eASIC3
4	SPI
5	RTC
6	USB HOST 1 – OHCI
7	USB HOST 2 – OHCI
8	USB HOST 1 – EHCI
9	USB HOST 2 – EHCI
10	USB DEVICE
11	MAC
12	I²C
13	GPT4
14	GPT3
15	gDMA1
16	gDMA0
17	GPT2
18	GPT1
19	UART2
20	UART1
21	UART0
22	ADC
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	eASIC4
29	eASIC5
30	eASIC6
31	eASIC7

6.4 MULTI-PORT MEMORY CONTROLLER

6.4.1 OVERVIEW

The DRAM interface is controlled by the on-chip Multi-Port Memory Controller.

Its main features are:

- Supports for SDRAM up to 32 bit wide
- Supports for DDR up to 16 bit wide
- Maximum clock frequency 133 MHz
- 8 AHB port connections
- 4 chip selects
- Total addressable memory: 256 MB
- Maximum memory bank size: 64 MB
- READ and WRITE buffers to reduce latency
- Programmable timings

Table 7. Supported memory cuts

Size [MB]	Bank Number	Row Length	Column Length
16 (2 MB x 8 bits)	2	11	9
16 (1 MB x 16 bits)	2	11	8
64 (8 MB x 8 bits)	4	12	9
64 (4 MB x 16 bits)	4	12	8
64 (2 MB x 32 bits)	4	11	8
128 (16 MB x 8 bits)	4	12	10
128 (8 MB x 16 bits)	4	12	9
128 (4 MB x 32 bits)	4	12	8
256 (32 MB x 8 bits)	4	13	10
256 (16 MB x 16 bits)	4	13	9
256 (8 MB x 32 bits)	4	13	8
512 (64 MB x 8 bits)	4	13	11
512 (32 MB x 16 bits)	4	13	10

Table 8. Multi-Port Memory Controller AHB port assignment

Port	Size [Bit]	Priority	Master
0	32	Max	Bus Matrix
1	-		Reserved
2	32		eASIC
3	32		USB 2.0 Device
4	32		USB 2.0 Host 1

Table 8. Multi-Port Memory Controller AHB port assignment (continued)

Port	Size [Bit]	Priority	Master
5	32		USB 2.0 Host 2
6	32		Ethernet MAC
7	32	Min	Main AHB System Bus

The table is compiled in decreasing order of priority.

The I/O interfaces accessible from off-chip are listed here:

Table 9. Multi-Port Memory Controller off-chip interfaces

Signal	Direction	Size [Bit]	Description
MPMCDQS	Input	2	Data Strobe
MPMCDATA	Bidirectional	32	Read / write data
MPMCCLKOUT	Output	2	DRAM clock
nMPMCCLKOUT	Output	2	DRAM inverted clock
MPMCCKEOUT	Output	2	DRAM clock enable
MPMCDQMOUT	Output	4	Data mask
nMPMCRASOUT	Output	1	RAS (active low)
nMPMCCASOUT	Output	1	CAS (active low)
nMPMCWEOUT	Output	1	Write Enable (active low)
nMPMCDYCSOUT	Output	4	Chip Select (active low)
MPMCADDROUT	Output	15	Address
SSTL_VREF	Input	1	Voltage reference SSTL / CMOS mode: SSTL → 1.25 V CMOS → 0 V This pin is used both as logic state and as power supply.

6.4.2 MULTI-PORT MEMORY CONTROLLER DELAY LINES

As shown in *Figure 5*, there are 4 DLLs.

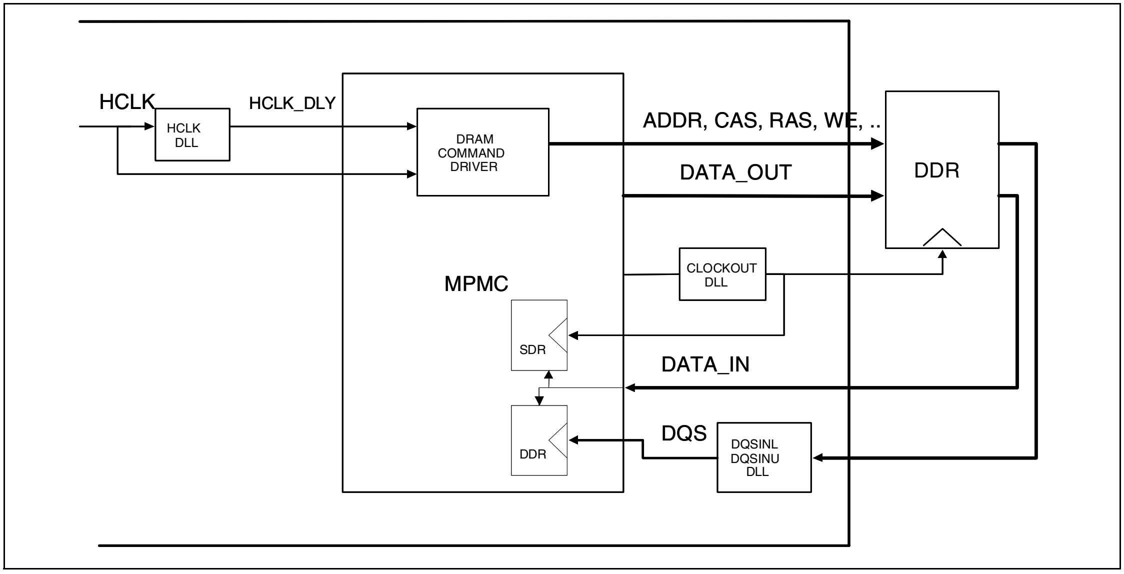
The CLOCKOUT Delay Line is used to tuner the clock driven from Multi-Port Memory Controller to external DRAM to match setup / hold constraints on external memory. This Delay Lines is used in the "clock delay methodology".

The HCLK Delay Lines delays the DRAM command signal (ADDR, CAS, RAS, ...) to capture easily read data from DRAM; this technique is called "command delay".

The DQSINL and DQSINH Delay Lines delay respectively the DQS0 (least 8 bit data strobe) and DQS1 (highest 8 bit of data strobe) signals coming from DDR.

Delay lines are setting by programming their register through APB Bus.

Figure 5. Multi-Port Memory Controller DLL



6.4.3 SSTLL PIN CONFIGRATION REGISTER

The Stub Series-Terminated Logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable.

The primary application for SSTL devices is to interface with DDRs.

In SPEAr Head THE SSTL pins are:

- MPMCDATA[15:0]
- MPMCADDROUT
- MPMCCLKOUT
- nMPMCCLKOUT.

These pins are set through configuration registers on APB Bus.

6.5 SPI MEMORIES

SPEAr Head supports the SPI memory devices Flash and EEPROM.

SPI controller provides an AHB slave interface to SPI memories and allows CPU to use them as data storage or code execution.

Main features are

- SPI master type
- Up to 20 MHz clock speed in Standard Read mode and 50 MHz in Fast Read mode
- 4 chip selects
- Up to 16 MBytes address space per bank
- Selectable 3-Bytes addressing for Flash and 2-Bytes addressing for EEPROM
- Programmable clock prescaler
- External memory boot mode capability

- 32, 16 or 8 bit AHB interface
- Interrupt request on write complete or software transfer complete

The compatible SPI memories are:

- STMicroelectronics M25Pxxx, M45Pxxx
- STMicroelectronics M95xxx except M95040, M95020 and M95010
- ATMEL AT25Fxx
- YMC Y25Fxx
- SST SST25LFxx

The I/O interfaces accessible from off-chip are listed here:

Table 10. SMC signal interfaces description

Signal	Direction	Size [Bit]	Description
SMIDATAIN	Input	1	Memory input
SMIDATAOUT	Output	1	Memory output
SMICLK	Output	1	Clock
SMINCS	Output	4	Bankchip selects (active low)

At power on the boot code is enabled from the static memory Bank0 by default; this has to be a Flash bank memory. Moreover, at power on, the memory clock signal is 19 MHz, the "RELEASE FROM DEEP POWER DOWN" is 29 µs and the base address for external memories is 0x0.

6.6 DMA

6.6.1 OVERVIEW

SPEAr Head has 2 DMA Controllers used to transfer data between aASIC™ MacroCell and memory.

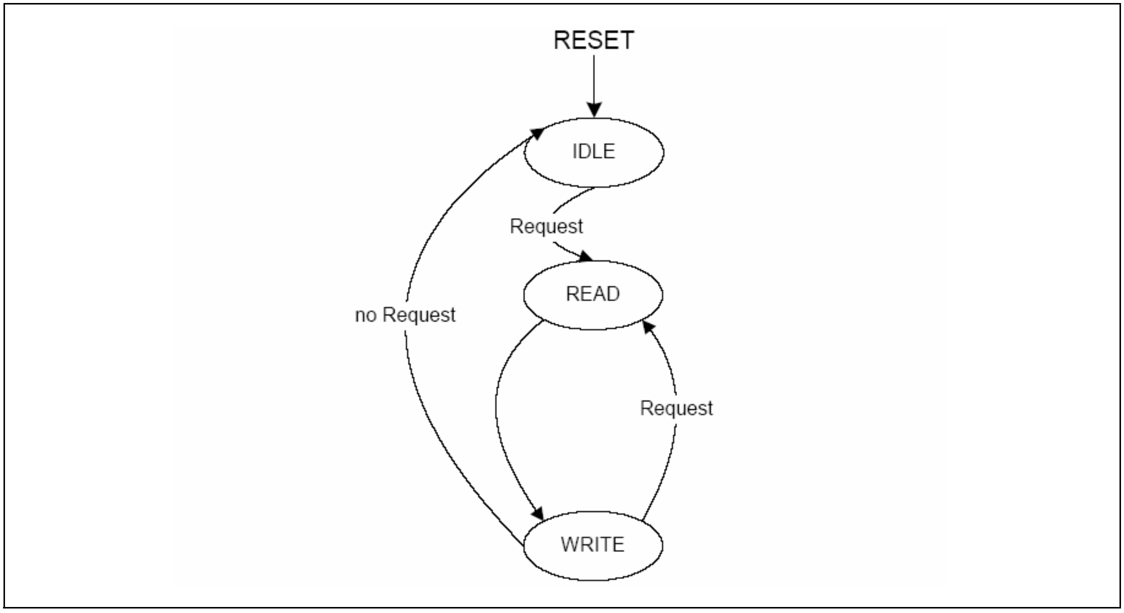
A DMA Controller can service up to 4 data streams at one time; a data transfer consists of a sequence of a DMA data packet transfers. There are two types of a data packet transfer

- one is from the source to the DMA Controller
- one other is from DMA Controller to the destination.

Each DMA Controller has an AHB Master interface to transfer data between DMA Controller and either a source or a destination, and has an APB Slave interface used to program its registers.

6.6.2 DMA CONTROL STATE MACHINE

Figure 6. DMA State Machine diagram



The DMA control SM is always reset into the IDLE state.

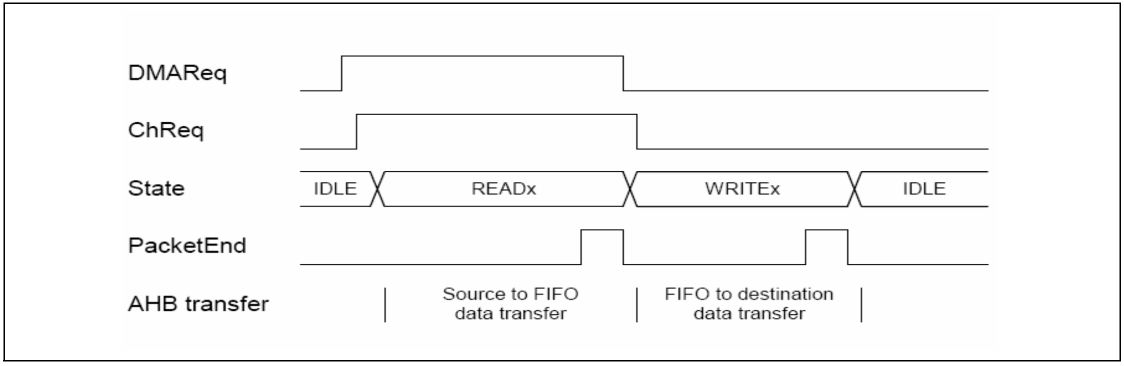
As a channel request is asserted, SM moves to READ state and the AHB Master will start a data packet transfer; SM selects appropriate source address.

When SM is in WRITE state, it selects the destination address and the data width from the Data Stream register and the AHB Master will transfer all data from the FIFO to the destination.

When the AHB Master has transferred the data packet, it asserts a PackEnd signal and the SM will move to the next state, which depends on the channel request signals.

The state transitions from the READ or WRITE states can occur only when a whole data packet has been transferred.

Figure 7. Data packet transfer


DMAReq
ChReq
State
IDLE
READx
WRITEx
IDLE
PacketEnd
AHB transfer
Source to FIFO data transfer
FIFO to destination data transfer

6.7 USB 2.0 HOST

6.7.1 OVERVIEW

Two blocks drive the USB 2.0 Host interfaces on SPEAr Head.

The first is the USB2.0PHY that executes the serialization and the de-serialization and implements the transceiver for the USB line.

The second part is the UHC (USB2.0 Host Controller). It is connected on AHB Bus and generates the commands for USB2.0PHY in UTMI+ interface.

As there are two USB Hosts, there is one PHY and one UHC for each USB Host port.

6.7.1.1 USB2.0PHY

The USB2.0PHY is a hard macro designed using standard cells and custom cells. In this way has been possible to reach the max speed of USB: 480 Mbits/sec.

The block is able to set his speed in LS / FS for USB 1.1 and in HS for USB 2.0.

6.7.1.2 UHC

The UHC is able to detect the USB speed configuration: USB 1.1 (LS / FS), USB 2.0 (HS) via UTMI+ interface.

When the speed is detected, the controller uses 2 sub-controllers: EHCI (Enhanced Host Controller Interface) for 2.0 configuration and OHCI (Open Host Controller Interface) for 1.1 configuration. There is an AHB master and a slave for everyone of these controllers.

6.8 USB 2.0 DEVICE

6.8.1 OVERVIEW

Three blocks drive the USB 2.0 Device interface on SPEAr Head.

The first one is the USB2.0PHY, which executes the serialization and the de-serialization and implements the transceiver for the USB line.

The second is the UDC (USB 2.0 Device Controller). It is connected on AHB Bus and generates the commands for USB2.0PHY in UTMI+ interface.

The last block is the USB Plug Detect, which detects the connection of the device.

6.8.1.1 USB2.0PHY

The USB2.0PHY is a hard macro designed using standard cells and custom cells. In this way is possible to reach the max speed HS of USB: 480 Mbits/Sec.

6.8.1.2 UDC

The UDC is able to detect the USB connection speed via UTMI+ interface.

There is an AHB master and three slaves.

The UDC contains 6 endpoints (0 control, 1 Bulk IN, 2 Bulk OUT, 3 ISO IN, 4 ISO OUT, 5 Interrupt IN) and 4 configurations.

6.9 ETHERNET MAC 110

The Ethernet Media Access Controller (MAC 110) incorporates the requirements for operation of an Ethernet / IEEE 802.3 compliant node and provides interface between the host system and the Media Independent Interface (which is embedded in SPEAr Head).

MAC 110 core features are:

- It can operate either in 100 Mbps mode or 10 Mbps mode, depending on the clock provided on the MII interface
- It can operate both in Half-Duplex mode and Full-Duplex mode.
  When operating in the Half-Duplex mode, the MAC110 core is fully compliant to Section 4 of ISO / IEC 8802-3 (ANSI / IEEE Standard) and ANSI / IEEE 802.3.
  When operating in the Full-Duplex mode, the MAC110 core is compliant to the IEEE 802.3x standard for Full-Duplex operations. It is also compatible with Home PNA 1.1.

The MAC110 core provides programmable enhanced features designed to minimize host supervision, bus utilization, and pre- or post-message processing. These features include:

- Ability to disable retires after a collision
- Dynamic FCS generation on a frame-by-frame basis
- Automatic Pad field insertion and deletion to enforce minimum frame size attributes
- Automatic retransmission and detection of collision frames.

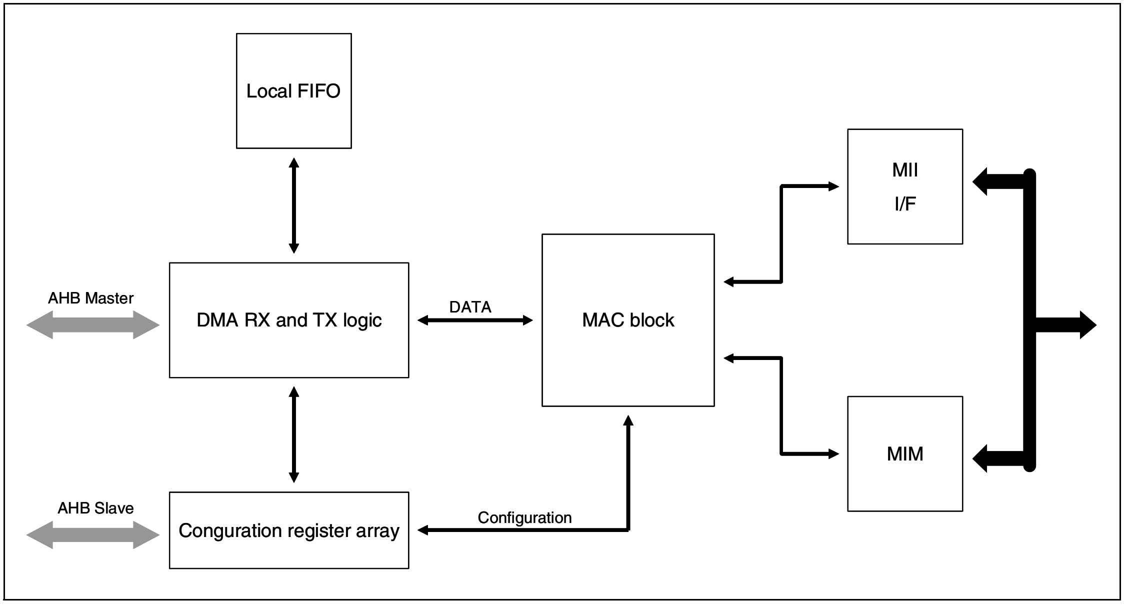
The MAC110 core can sustain transmission or reception of Minimal-Sized Back-To-Back packets at full line speed with an Inter-Packet Gap (IPG) of 90.6 µs for 10 Mb/s and 0.96 µs for 100 Mb/s.

The five primary attributes of the MAC block are:

1. Transmit and receive message data encapsulation
   - Framing (frame boundary delimitation, frame synchronization)
   - Error detection (physical medium transmission errors)
2. Media access management
   - Medium allocation (collision detection, except in Full-Duplex operation)
   - Contention resolution (collision handling, except in Full-Duplex operation)
3. Flow Control during Full Duplex mode
   - Decoding of Control frames (PAUSE command) and disabling the transmitter
   - Generation of Control frames
4. Interface to the PHY
   - Support of MII protocol to interface with a MII based PHY
5. Management Interface support on MII
   - Generation of PHY Management frames on the MDC / MDI / MDO.

To minimize the CPU load during the data transfer is available a local DMA with FIFO capable to fetch itself the descriptors for the data blocks and to manage the data according to the instruction included on the descriptor.

Figure 8. Block diagram of Ethernet Controller



6.10 UART

UART provides a standard serial data communication with transmit and receive channels that can operate concurrently to handle a full-duplex operation.

Two internal FIFO for transmitted and received data, deep 16 and wide 8 bits, are present; these FIFO can be enabled or disabled through a register.

Interrupts are provided to control reception and transmission of serial data.

The clock for both transmit and receive channels is provided by an internal Baud-Rate generator that divides the AHB Bus clock by any divisor value from 1 to 255. The output clock frequency of baud generator is sixteen times the baud rate value.

The maximum speed achieved is 115 KBauds.

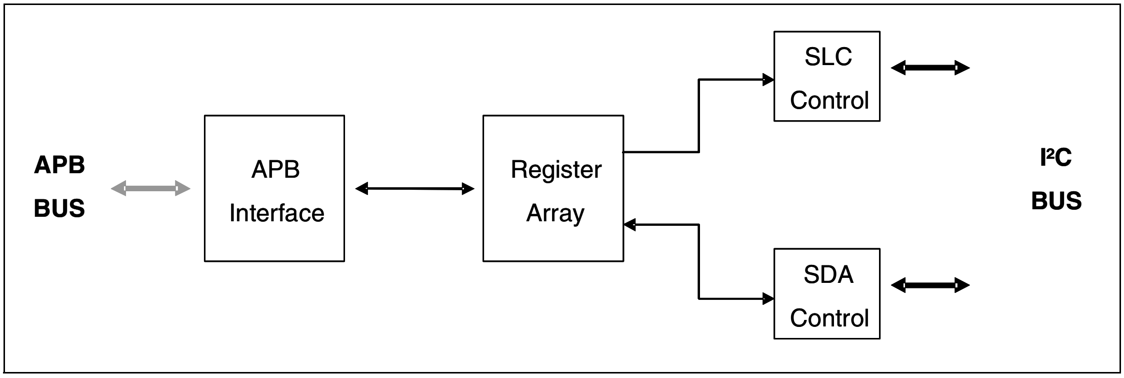
In SPEAr Head there are 3 UART's, APB Bus slaves.

6.11 I^{2}C

6.11.1 OVERVIEW

The controller serves as an interface between the APB Bus and the serial I^{2}C bus. It provides master functions, and controls all I^{2}C bus-specific sequencing, protocol, arbitration and timing. Supported Standard (100 KHz) and Fast (400 KHz) I^{2}C mode.

Figure 9. I^{2}C Controller block diagram



Main features are:

- Parallel-bus APB / I^{2}C protocol converter
- Standard I^{2}C mode (100 KHz) / Fast I^{2}C mode (400 KHz)
- Master interface (only).
- Detection of bus errors during transfers
- Control of all I^{2}C bus-specific sequencing, protocol, arbitration and timing

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and vice versa, using either an interrupt or a polled handshake. The interrupts can be enabled or disabled by software.

The interface is connected to the I^{2}C bus by a data pin (SDA) and by a clock pin (SCL). SDA signal is synchronized by SCL signal.

6.11.2 I^{2}C OPERATING MODE

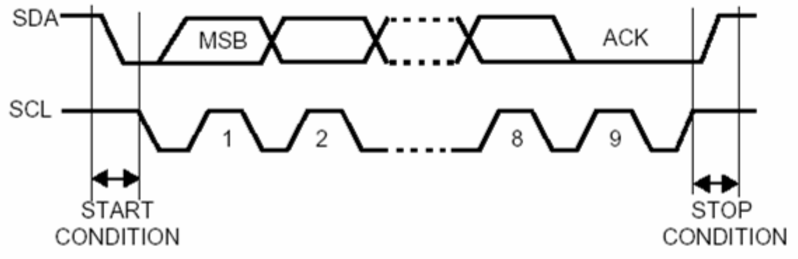
Communication flow

In Master mode, it initiates a data transfer and generates the clock signal. A serial data transfer always begins with a start condition and ends with a stop condition. Both start and stop conditions are generated by software.

The first byte following the start condition is the address byte; it is always transmitted in Master mode.

A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter.

Figure 10. I^{2}C timing



Acknowledge may be enabled and disabled by software.

The I^{2}C interface address and / or general call address can be selected by software.

The speed of the I^{2}C interface may be selected between Standard (0 - 100 KHz) and Fast (100 - 400 KHz).

SDA / SCL Line Control

Transmitter mode: the interface holds the clock line low before transmission to wait for the microcontroller to write the byte in the Data Register.

Receiver mode: the interface holds the clock line low after reception to wait for the microcontroller to read the byte in the Data Register.

The SCL frequency (FSCL) is controlled by a programmable clock divider which depends on the I^{2}C bus mode.

When the I^{2}C cell is enabled, the SDA and SCL ports must be configured as floating open-drain output or floating input. In this case, the value of the external pull-up resistance used depends on the application.

6.11.3 I^{2}C FUNCTIONAL DESCRIPTION

Master Mode

The I^{2}C clock is generated by the master peripheral.

The interface operates in Master mode through the generation of the Start condition: Start bit set to 1 in the control register and I^{2}C not busy (Busy flag set to 0).

Once the Start condition is sent, if interrupts are enabled, an Event Flag bit and a Start bit are set by hardware. Then the master waits for a read of the register used to observe bus activity (SR1 register) followed by a write in the data register DR with the Slave address byte, holding the SCL line low (see *Figure 11* Transfer sequencing EV5). Then the slave address byte is sent to the SDA line via the internal shift register.

After completion of these transfers, the Event Flag bit is set by hardware with interrupt generation. Then the master waits for a read of the SR1 register followed by a write in the control register CR (for example set the Peripheral Enable bit), holding the SCL line low (see *Figure 11* Transfer sequencing EV6).

Next the Master must enter Receiver or Transmitter mode.

Master Receiver

Following the address transmission and after SR1 and CR registers have been accessed, the Master receives bytes from the SDA line into the DR register via the internal shift register. After each byte the interface generates in sequence:

1) Acknowledge pulse if the acknowledge bit ACK in the control register is set

2) Event Flag and the Byte Transfer Finish bits are set by hardware with an interrupt.

Then the interface waits for a read of the SR1 register followed by a read of the DR register, holding the SCL line low (see *Figure 11* Transfer sequencing EV7).

To close the communication: before reading the last byte from the DR register, set the Stop bit to generate the Stop condition.

In order to generate the non-acknowledge pulse after the last received data byte, the ACK bit must be cleared just before reading the second last data byte.

Master Transmitter

Following the address transmission and after SR1 register has been read, the Master sends bytes from the DR register to the SDA line via the internal shift register.

The master waits for a read of the SR1 register followed by a write in the DR register, holding the SCL line low (see *Figure 11* Transfer sequencing EV8).

When the acknowledge bit is received, the interface sets Event Flag and the Byte Transfer Finish bits with an interrupt.

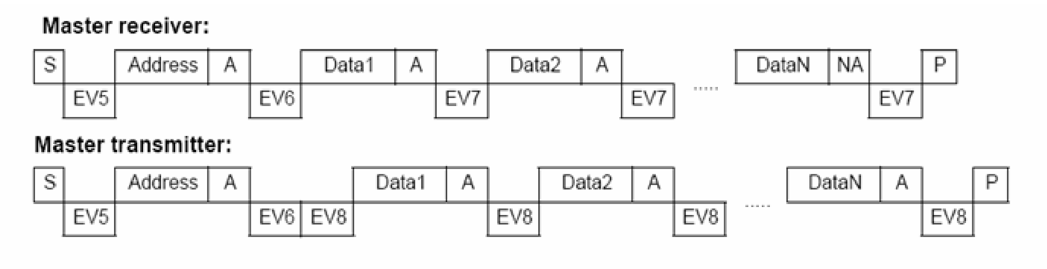
To close the communication: after writing the last byte to the DR register, set the Stop bit to generate the Stop condition.

Error Cases

- BERR: Detection of a Stop or a Start condition during a byte transfer. In this case, the Event Flag and BERR bits are set by hardware with an interrupt.
- AF: Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set by hardware with an interrupt. To resume, set the Start or Stop bit.

In all these cases, the SCL line is not held low; however, the SDA line can remain low due to possible 0 bits transmitted last. It is then necessary to release both lines by software.

Figure 11. Transfer sequencing



Legend:

S=Start, P=Stop, A=Acknowledge, NA=Non-acknowledge

EVx=Event (with interrupt if ITE=1)

EV5: EVF=1, SB=1, cleared by reading SR1 register followed by writing DR register.

EV6: EVF=1, cleared by reading SR1 register followed by writing CR register (for example PE=1).

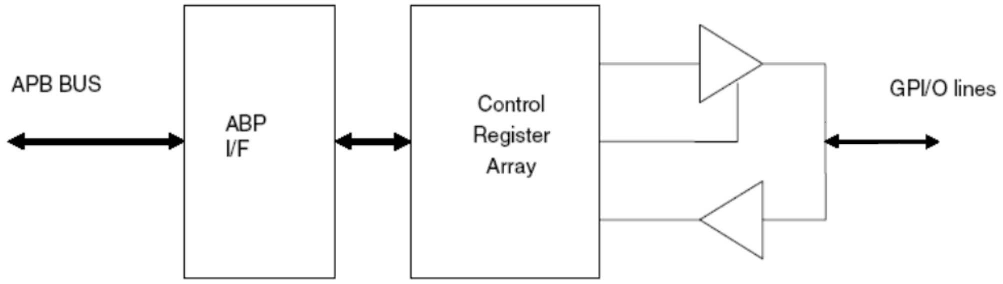
EV7: EVF=1, BTF=1, cleared by reading SR1 register followed by reading DR register.

EV8: EVF=1, BTF=1, cleared by reading SR1 register followed by writing DR register.

6.12 GENERAL POURPOSE I/Os

The GPIO block consists of 6 General Purpose IOs which act as buffers between the I/O pins and the processor core: data is stored in the GPIO block and can be written to and read from by the processor via the APB Bus.

Figure 12. GPIO block diagram



6.13 ADC

6.13.1 OVERVIEW

The ADC-APB Bus controller provides connection between APB Bus and ST-ADC8MUX16 Analog to digital Converter: it handles the acquisition request from APB Bus and generates control and configuration signals to drive ADC and also the interrupt signal when acquisition is ready. For any ADC input channel the controller can realize a single acquisition or an average up to 128 samples.

There are two operating mode:

- Normal mode: it handles all the digital ports of ST-ADC8MUX16.
- Test mode: the ST-ADC8MUX16 is directly accessible by means of external pins as a stand-alone ADC. This will allow stand-alone testing procedures (digital and analog)

ADC positive and negative reference voltages are supply by:

  - positive → VREFP_adc pin
  - negative → VREFN_adc pin

6.13.2 ADC OPERATING MODES

Normal mode

When the enable bit is set to 1, the conversion starts and as it finishes a bit of Conversion Ready (interrupt signal) is set to 1. At this point the reading of the data could begin and when it finishes, Conversion Ready and the enable bits becomes 0.

In Normal mode the signals accessible off-chip are listed in *Table 11* External pins of ADC macro in Normal mode.

Table 11. External pins of ADC macro in Normal mode

Signal	Direction	Description
AID[15:0]	Input	Analog channels

Test mode

Test mode is set by assigning the following logic state to the test pins:

TEST0 → 0

TEST1 → 1

TEST2 → 0

TEST3 → 1

In this mode ST-ADC8MUX16 is accessible for the testing procedure and its signals are switched to the following pins:

Table 12. External pads of ADC macro in Test mode

SIGNAL	PIN	DIRECTION	DESCRIPTION
TEST_OUT	TEST_OUT	Output	Analog test point output
TEST	TX_EN	Input	Test mode select
START	CRS	Input	Start conversion
EN	COL	Input	Conversion enable
CLK	RXD[0]	Input	Clock
EOC	SCL	Output	End of conversion
D_0	RXD[1]	Output	Data output
D_1	RXD[2]	Output	Data output
D_2	RXD[3]	Output	Data output
D_3	RX_DV	Output	Data output
D_4	RX_ER	Output	Data output
D_5	MCD	Output	Data output
D_6	MDIO	Output	Data output
D_7	SDA	Output	Data output
SEL[0 to 3]	TX[0 to 3]	Input	Selection line – input analog mux

6.14 WATCHDOG TIMER

The WdT is based on a programmable 8 bit counter and generates a hot reset (single pulse) when it overflows. The timer should be cleared by the software before it overflows.

The counter is clocked by a slow signal coming from a 21 bit prescaler clocked by the APB clock. So that, as APB Bus has a frequency of 66.5 MHz, the maximum elapsing time is 8.07 second, while the minimum is 31.52 ms.

The WdT is an APB Slave device.

6.15 REAL TIME CLOCK

The Real Time Clock block implements 3 functions:

- time-of-day clock in 24 hour mode
- calendar
- alarm

Time and calendar value are stored in binary code decimal format.

Date and time are stored in dedicated registers, so that the RTC can start to count the time.

An alarm time can be defined and when the value of time and date is equal to the value on alarm registers, an interrupt is generated, if enabled.

For debug the prescaler, that define the seconds, they can be bypassed to obtain a faster counter of the time.

A further option available is that if the seconds are masked, an interrupt for any second is generated. In the same way for minutes, hours, days, months or years.

The RTC provides also a self-isolation mode, which allows it working even if power isn't supplied to the rest of the device.

The RTC is an APB Bus.

6.16 GENERAL POURPOSE TIMER

SPEAr Head has 4 GPTs, connected as APB Bus slaves.

A GPT is constituted by 2 channels and each one consists of a programmable 16 bit counter and a dedicated 8 bit timer clock prescaler. The programmable 8 bit prescaler unit performs a clock division by 1, 2, 4, 8, 16, 32, 64, 128, and 256, allowing a frequency range from 3.96 Hz to 66.5 MHz.

Two modes of operation are available for each GPT:

- **Auto Reload Mode.** When the timer is enabled, the counter is cleared and starts incrementing. When it reaches the compare register value, an interrupt source is activated, the counter first is automatically cleared and then restarts incrementing.
  The process is repeated until the timer is disabled.
- **Single Shot Mode.** When the timer is enabled, the counter is cleared and starts incrementing. When it reaches the compare register value, an interrupt source is activated, the counter stopped and the timer disabled.
  The current timer counter value could be read from a register.

6.17 CUSTOMIZABLE LOGIC

6.17.1 OVERVIEW

The Customizable Logic consists of an embedded macro where it is possible to map up to 200K equivalent ASIC gates.

The logic is interfaced with the rest of the system so that it is possible to implement:

- AHB sub-systems with masters and slaves (via 1 AHB full master, 1 AHB full slave, 1 AHB master lite, 2 AHB slave ports)
- AHB master lite connected to DRAM controller
- AHB memories (via AHB slave ports) implemented by configuring the logic cells as SRAM elements.
- I/O protocol handlers (via the 112 dedicated GPIO connections)
- 8 interrupt channels
- 8 DMA requests
- 4 independent SRAM data channels (via dedicated connection to on-chip 16 KByte SRAM)

All of the above configuration scenarios can be mixed together in the same user-defined logic.

6.17.2 CUSTOM PROJECT DEVELOPMENT

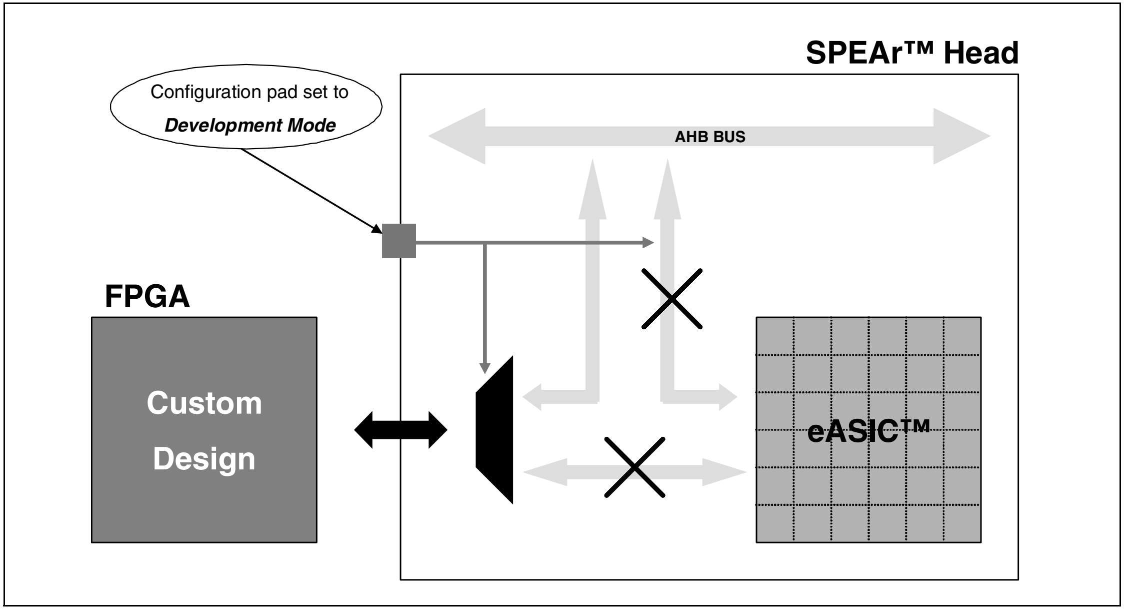
The custom project to design in the customizable logic can be implemented on an external FPGA, which emulates eASIC logic cells. The purpose of this characteristic is allowing the user to develop his project both under real-time constraints and compliant to eASIC MacroCell features.

This mode is enabled by using the GPIO interface, which is internally configured to support full-master and full-slave AHB ports. The *Figure 13* highlights the described behavior. In order to enable the "Development mode", the configuration pin has to be set to state logic 1. After this configuration the logic implemented in the external FPGA

- can completely interact with the following scenarios:
  - AHB sub-systems with masters and slaves connected to the main system bus (full masters and full slaves peripherals)
  - I/O protocol handlers (via 112 dedicated FPGA I/Os)
  - 4 interrupt channels
  - 4 DMA requests

  All the above scenarios can be mixed in the same FPGA configuration
- can be tested in order to verify the accordance with eASIC MacroCell features, by running the ARM926EJ-S software debugger on a PC connected to SPEAr Head.
  Once this test has been completed successfully, then the user-defined logic is ready to be moved without any additional changes within the on-chip eASIC configurable logic

Figure 13. Emulation with external FPGA



6.17.3 CUSTOMIZATION PROCESS

The customization process requires two separate steps, executed at different times:

1. Programming layer fabrication (single VIA-mask).
2. Bitstream download.

The step 1 defines the interconnection between the customizable logic cells and is executed at fabrication level on top of the silicon wafers stored in the fab.

The step 2 defines the logic function for each customizable logic cell and is executed after that the system has been powered up by dedicated software routines running on the ARM926 microprocessor.

Both Bitstream and VIA-mask realize the user-defined customization for the entire device.

The eASIC mapping flow starts from the RTL description of the user-defined customization, with the purpose to generate the VIA-mask and configuration Bitstream.

6.17.4 POWER ON SEQUENCE

Once the system is powered-on, the eASIC logic has to be properly configured before its usage. In order to accomplish this task, two main operations have to be performed (both using dedicated software routines running on the ARM9 microprocessor):

1. Bitstream download
2. Startup of connection between the eASIC MacroCell and the rest of the device

Both steeps are driven by a control register programmable via APB Bus.

6.17.5 BITSTREAM DOWNLOAD

The bitstream download operation is responsible for the eASIC logic initialization, since each configurable cell of the customizable logic is loaded with a data stream that represents the mapped logic function. Each operation of this download is performed by a dedicated software routine that read and writes data across the Control register.

The bitstream is a 32 KByte data that is stored in the external non-volatile memory of the SPEAr device.

6.17.6 CONNECTION STARTUP

Once the eASIC logic is up and running due to the Bitstream initialization, next steep is its reset, in order to allow connections to the other IPs of the chip. The reset routine is activated by programming the Control register.

Last steep is the enabling of needed connections, by setting the Status register.

6.17.7 PROGRAMMING INTERFACE

In order to achieve the Bitstream download and the reset routine, a dedicate logic has been embedded in the SPEAr Head: the Programming Interface, which also includes the Control register.

7 Electrical Characteristics

7.1 ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages; however it is advisable to take normal precaution to avoid application of any voltage higher than the specified maximum rated voltages.

Table 13. Absolute maximum rating values

Symbol	Parameter	Value	Unit
VDD core	Supply voltage core	2.1	V
VDD I/O	Supply voltage I/O	6.4	V
VDD PLL	Supply voltage PLL	6.4	V
VDD SDR	Supply voltage SDRAM	6.4	V
VDD DDR	Supply voltage DDR	5.4	V
VDD RTC	Supply voltage RTC	2.1	V
Vi TTL	Input voltage TTL (3.3 and 5 V tollerant)	6.4	V
Vi SRAM	Input voltage SDRAM	6.4	V
Vi DDR	Input voltage DDR	5.4	V
Vi USBds	Input voltage USB (Host and Device) data signal interfaces	6.4	V
Vi USBrr	Input voltage USB reference resistor	6.4	V
Vi AN	Analog input voltage ADC	6.4	V
Tj	Junction temperature	-40 to 125	°C
Tstg	Storage temperature	-55 to 150	°C

The average chip-junction temperature, Tj, can be calculated using the following equation:

$$T_j = T_A + (P_D \cdot \Theta_{JA})$$

where :

- T_A is the ambient temperature in °C
- Θ_{JA} is the package Junction-to-Ambient thermal resistance, which is 34 °C/W
- $P_D = P_{INT} + P_{PORT}$
  - P_{INT} is the chip internal power
  - P_{PORT} is the power dissipation on Input and Output pins ; user determined

If P_{PORT} is neglected, an approximate relationship between P_D is:

$$P_D = K / (Tj + 273\ °C)$$

And, solving first equations:

$$K = P_D \cdot (T_A + 273\ °C) + \Theta_{JA} \times P_D^2$$

K is a constant for the particular, which can be determined through last equation by measuring P_D at equilibrium, for a know T_A

Using this value of K, the value of P_D and T_J can be obtained by solving first and second equation, iteratively for any value of T_A.

7.2 DC ELETTRICAL CHARACTERISTICS

7.2.1 SUPPLY VOLTAGE SPECIFICATIONS

The recommended operating conditions are listed in the following table:

Table 14. Recommended operating conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VDD core	Supply voltage core	1.14	1.2	1.26	V
VDD I/O	Supply voltage I/O	3	3.3	3.6	V
VDD PLL	Supply voltage PLL	3	3.3	3.6	V
VDD SDR	Supply voltage SDRAM	3	3.3	3.6	V
VDD DDR	Supply voltage DDR	2.3	2.5	2.7	V
VDD RTC	Supply voltage RTC	1.14	1.2	1.26	V
Top	Operating temperature	-40		85	°C

7.2.2 I/O VOLTAGE SPECIFICATIONS

7.2.2.1 LVTTL I/O (C0MPLIIANT WITH EIA/JEDEC STANDARD JESD8-B)

For LVTTL (3.3 and 5 V tolerant) pins, the allowed I/O voltages are:

Table 15. Low Voltage TTL DC input specification (3 < VDD < 3.6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Vil	Low level input voltage			0.8	V
Vih	High level input voltage		2		V
Vhyst	Schmitt trigger hysteresis		0.495	0.620	V

Table 16. Low Voltage TTL DC output specification (3 < VDD < 3.6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Vol	Low level output voltage	Iol = X mA *		0.15	V
Voh	High level output voltage	Ioh = X mA *	VDD - 0.15		V

* X is the source / sink current under worst case conditions and it is reflected in the name of the I/O cell according to the drive capability.

Table 17. Pull-up and Pull-down characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Ipu	Pull-up current	Vi = 0 V	40	60	110	µA
Ipd	Pull-down current	Vi = VDD	30	60	133	µA
Rup	Equivalent Pull-up resistance	Vi = 0 V	32	50	75	KOhm
Rpd	Equivalent Pull-down resistance	Vi = VDD	27	50	100	KOhm

7.2.2.2 LVCMOS/SSTL I/O

If the I/Os are set as LVCMOS (for SDRAM memories), the DC electrical characteristics are the following:

Table 18. LVCMOS DC input specification (3 < VDD < 3.6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Vil	Low level input voltage	Vout ≥ Voh (min) or Vout ≤ Vol (max)	-0.3	0.8	V
Vih	High level input voltage		2	VDD+0.3	V
Iin	Input Current	Vin = 0 or Vin =VDD		±5	µA

Table 19. LVCMOS DC output specification (3 < VDD < 3.6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Vol	Low level output voltage	VDD = min, Iol = 100 µA		0.2	V
Voh	High level output voltage	VDD = min, Ioh = -100 µA	VDD - 0.2		V

Instead when they are set as (for DDR memories), refer to following tables:

Table 20. DC input specification of bidirectional SSTL pins (2.3 < VDD DDR < 2.7)

Symbol	Parameter	Min.	Max.	Unit
Vil	Low level input voltage	-0.3	SSTL_VREF – 0.15	V
Vih	High level input voltage	SSTL_VREF + 0.15	VDD DDR – 0.15	V

Table 21. DC input specification of bidirectional differentialSSTL pins (2.3 < VDD DDR < 2.7)

Symbol	Parameter	Min.	Max.	Unit
Vil	Low level input voltage	-0.3	VDD DDR + 0.3	V
Vih	High level input voltage	0.36	VDD DDR – 0.6	V

8 Package information

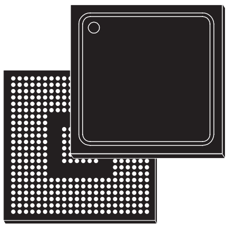
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

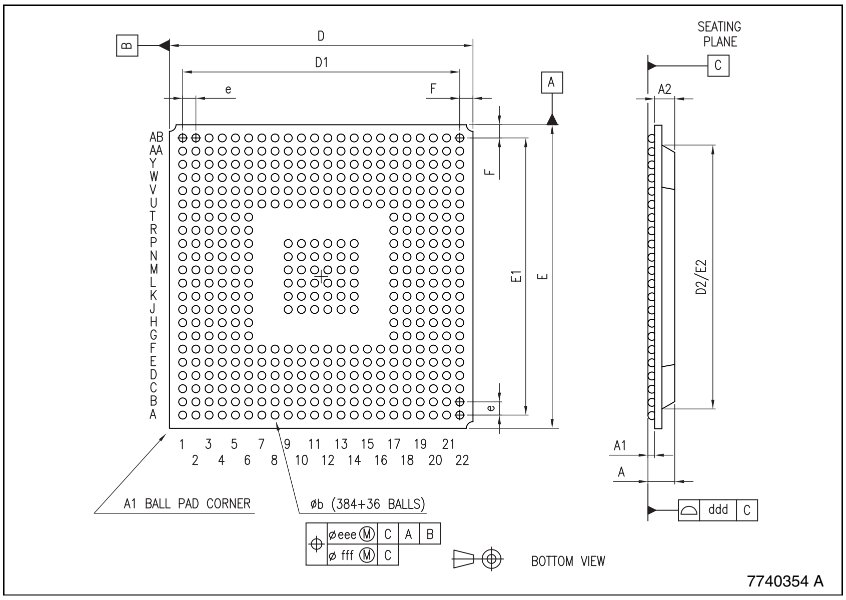
Figure 14. PBGA420 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.16			0.085
A1	0.30			0.012		
A2		1.53			0.060	
b	0.50	0.60	0.70	0.020	0.024	0.027
D	22.80	23.00	23.20	0.8976	0.905	0.913
D1		21.00			0.827	
D2		20.00			0.787	
E	22.80	32.00	23.20			
E1		21.00				
E2		20.00				
e		1.00			0.039	
F		1.00			0.039	
ddd			0.20			0.008
eee			0.25			0.010
fff			0.10			0.004

OUTLINE AND MECHANICAL DATA



PBGA420 (23x23x2.16mm) Ball Grid Array Package



9 Revision history

Date	Revision	Changes
17-Oct-2005	1	Initial release.
1-Dec-2005	2	Changed the Part Number from SPEAR-09-H020 to SPEAR-09-H022. Modified/added some dates in the Chapter 7.

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