VV5500 & VV6500

Mono and Colour Digital Video CMOS Image Sensors

PRELIMINARY RELEASE

The VV5500/VV6500 are multi format digital output imaging devices based on STMicroelectronics's unique CMOS sensor technology. Both sensors require minimal support circuitry.

VV5500 (monochrome) and VV6500 (colourised) produce digital video output. The video streams from both devices contain embedded control data that can be used to enable frame grabbing applications as well as providing input data for the external exposure controller.

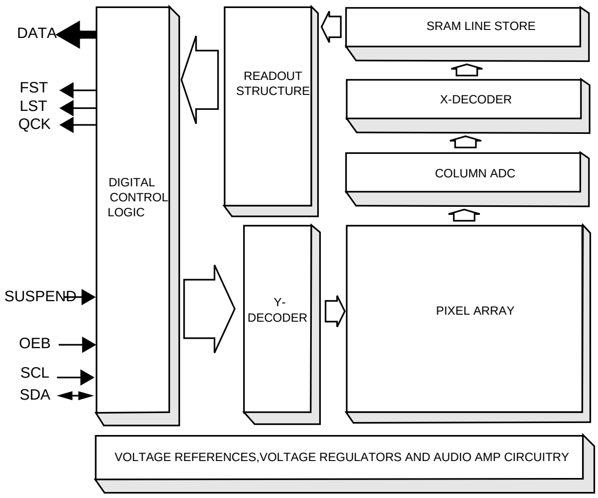
The pixel array in VV6500 is coated with a Bayer colour pattern. This colourised sensor can interface to a range of STMicroelectronics co-processors. A chipset comprising VV6500 and STV0657 will output 8bit YUV or RGB digital video. A USB camera can be realised by partnering VV6500 with STV0672. Finally a high quality digital stills camera can be produced by operating VV6500 with STV0680B-001. Please contact STMicroelectronics for ordering information on all of these products.

Both VV5500 and VV6500 are initialised in a power saving mode and must be enabled via I2C control before they can produce video. The I2C allows the master coprocessor to reconfigure the device and control exposure and gain settings.

USB systems are catered for with an ultra low power, pin driven, suspend mode.

The on board regulator can supply sufficient current drive to power external components, (e.g. the video coprocessor).

Functional block diagram



Key Features

- 3.3V operation
- Multiple video formats available
- Pan tilt image feature
- Sub sampled image full FOV feature
- On board 10 bit ADC
- On board voltage regulator
- Suspend for USB systems
- Automatic black and dark calibration
- LVDS clock input
- On board audio amplifier
- I2C communications

Applications

- PC camera
- Personal digital assistant
- Mobile video phones
- Digital stills cameras

Specifications

Effective image sizes after colour processing	640 x 480 (VGA) 352 x 288 (CIF) 320 x 240 (QVGA)
Pixel resolution	644 x 484 (VGA) 356 x 292 (CIF) 324 x 244 (QVGA)
Pixel size	7.5µm x 7.5µm
Array size	4.89mm x 3.66mm
Exposure control	+81dB
Analogue gain	+12dB (recommended max)
Signal/Noise ratio	57dB
Supply voltage	3.3V-6.0V DC +/– 5%
Supply current	42mA (max,VGA@30fps) 74µA (suspend clock disabled)
Operating temperature (ambient)	0^{o}C - 40^{o}C (for extended temp. info please contact STMicroelectronics)
Package type	48LCC

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1. Document Revision History

Revision	Date	Comments
1.0	11/05/2000	• Original release
2.0	22/08/2000	• Package drawing and pin description updated • Optical characterisation data added • Audio description extended • Pixel defect specification added • Product numbering updated • Gain ceiling recommendation • Documentation errors corrected
2.1	29/08/2000	• Sensor power up sequence clarified and updated
2.2	28/09/2000	• Product order codes updated • Package pinout updated

Table 1 : Document Revision History

2. Introduction

2.1 Overview

VV5500/VV6500 is a VGA format CMOS image sensor. The VV5500 sensor is the basic monochrome device and VV6500 is the colourised variant. The operation of VV5500 and VV6500 is very similar but any differences will be identified and explained. VV5500 and VV6500 contain the same basic video timing modes. Table 2 summarises these video modes and Section 3. will discuss the these modes in more detail.

Important: VV5500 and VV6500's output video data stream only contains raw data. A master co-processor is required to generate a video waveform that can be displayed on a VDU.

Mode	Input Clock (MHz)	System Clock Divisor	Image Size	Line Time (µs)	Lines per Frame	Frame Rate (fps)
pantiltCIF	16.00	4	356 x 292	104.00	320	30.0481
pantiltCIF[1]	24.00	6	356 x 292	104.00	320	30.0481
VGA	24.00	2	644 x 484	63.50	524	30.0535
pantiltQVGA	24.00	8	324 x 244	127.00	262	30.0535
sub sampledQVGA	24.00	8	324 x 244	127.00	262	30.0535

Table 2 : Video Modes

[1] **The user can also provide a 24 MHz clock, rather than a 16 MHz clock, for the pantiltCIF mode, which the sensor then internally divides by 1.5, (see data_format[22]), to give an effective input clock frequency of 16 MHz.**

2.2 Exposure Control

VV5500/VV6500 does not include any form of automatic exposure and/or gain control. Thus to produce a correctly exposed image the integration period for the pixels, in the sensor array, an exposure control algorithm must be implemented externally. The new exposure values are written to the sensor via the serial interface.

2.3 Digital Interface

The sensor's offers a very flexible digital interface, the main components of which are listed below:

1. A tri-stateable 5-wire data bus (D[4:0]) for sending both video data and embedded timing references.
2. 4-wire and 8-wire data bus alternatives available. If the 8-wire option is selected then the FST/LST pins are reconfigured to output data information.
3. A data qualification clock, QCK, which can be programmable via the serial interface to behave in a number of different ways (Tri-stateable).
4. A line start signal, LST (Tri-stateable).
5. A frame start signal, FST (Tri-stateable).
6. OEB tri-states all 5 data bus lines, D[4:0], the qualification clock, QCK, LST and FST.
7. A 2-wire serial interface (SDA,SCL) for controlling and setting up the device.

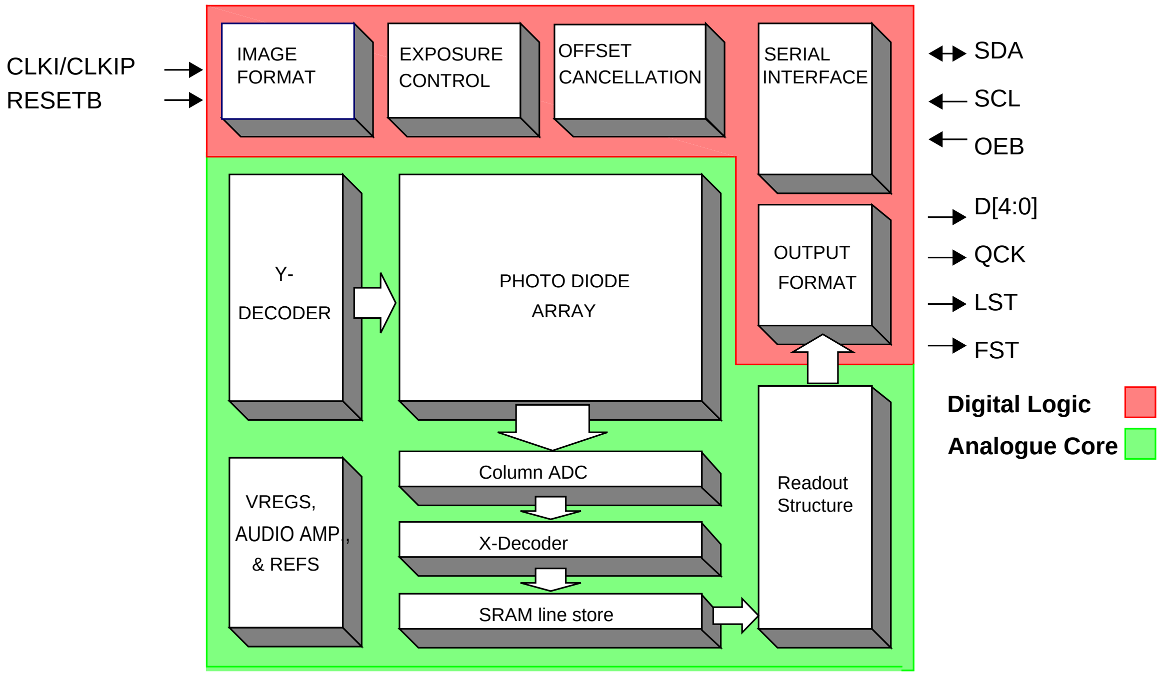


Figure 1 : Block Diagram of VV5500/VV6500 Image Sensor (5-wire output)

2.3.1 Digital Data Bus

Along with the pixel data, codes representing the start and end of fields and the start and end of lines are embedded within the video data stream to allow a co-processor to synchronise with video data the camera module is generating. Section 8. defines the format for the output video data stream.

2.3.2 Frame Grabber Control Signals

To complement the embedded control sequences the data qualification clock (QCK), the line start signal (LST) and the field start signal (FST) signals can be independently set-up as follows:

1. Disabled
2. Free-running.
3. Qualify only the control sequences and the pixel data.
4. Qualify the pixel data only

There is also the choice of two different QCK frequencies where one is twice the frequency of the other.

1. Fast QCK: the falling edge of the clock qualifies every 8, 5 or 4 bit blocks of data that makes up a pixel value.
2. Slow QCK: the rising edge qualifies 1st, 3rd, 5th, etc. blocks of data that make up a pixel value while the falling edge qualifies the 2nd, 4th, 6th etc. blocks of data. For example in 4-wire mode the rising edge of the clock qualifies the most significant nibbles while the falling edge of the clock qualifies the least significant nibbles.

2.3.3 2-wire Serial Interface

The 2-wire serial interface provides complete control over sensor setup and operation. Two serial interface broadcast addresses are supported. One allows all sensors to be written to in parallel while the other allows all sensors and co-processors to be written to in parallel.

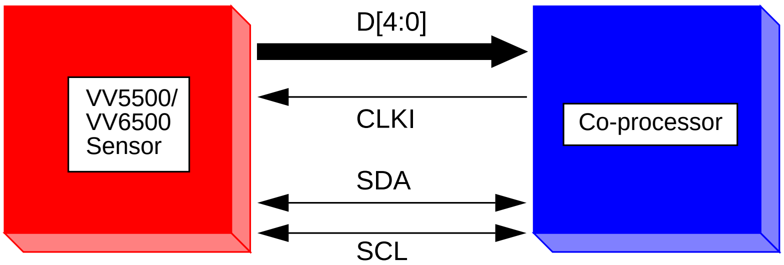
Section 9. defines the serial interface communications protocol and the register map of all the locations which can be accessed via the serial interface.

2.3.4 Sensor/Co-processor Interface Options

There are 3 main ways of interfacing to the VV5500/VV6500 sensor based on the above signals:

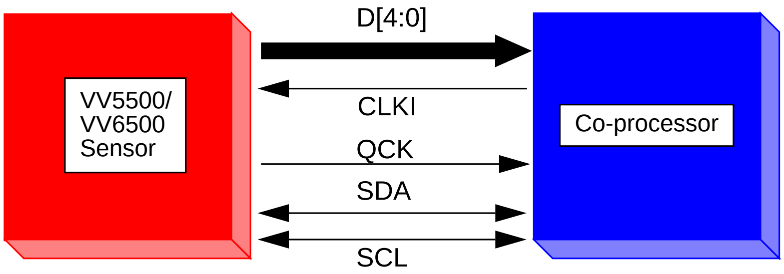
1. The colour co-processor supplies the sensor clock, CLKI, and uses the embedded control sequences to synchronise with the frame and line level timings. Thus the video processor and sensor are running off derivatives of the same fundamental clock. To allow the co-processor to determine the best sampling position of the video data, during its power-up sequence the sensor outputs a 101010... sequence on each of its data bus lines for the video processor to lock on to.

1.



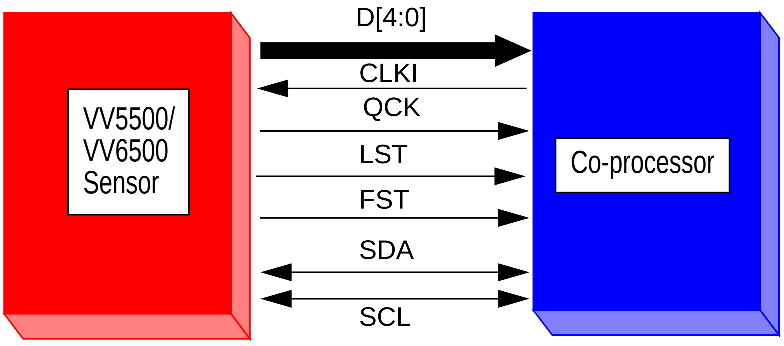
2. The colour co-processor supplies the sensor clock, CLKI, and uses a free-running QCK supplied by the sensor to sample the incoming video data stream. The embedded control sequences are used to synchronise the frame and line level timings.

2.



3. The colour co-processor supplies the sensor clock, CLKI, and uses FST, LST and the data only mode for QCK to synchronise to the incoming video data. Primarily intended for interfacing to frame grabbers.

3.



2.4 Other Features

2.4.1 Audio Amplifier

Pins AIN and AOUTP & AOUTN are the input and outputs respectively for an audio amplifier. A simple microphone is connected across the AIN pin.

2.4.2 Voltage Regulator

The on-chip voltage regulator requires only a few external components to form a fully functional voltage regulator to 3.3V.

2.4.3 Serial Interface Programmable Pins

The FST and QCK pins are re-configurable to follow the state of 2-bits in a serial register. The user could then use these control bits to control a peripheral device, a motor or shutter mechanism for example.

3. Operating Modes

3.1 Video Timing

The video format mode on power-up is pantiltCIF by default. After power-up the mode can be changed by a serial interface to write to Setup0[16]. Please note that the sensor can exit low power in ANY of the available video modes.

Table 3 details the setup for each of the video timing modes. A serial write to serial register [16] will force the contents of other registers in the serial interface to change to the appropriate values, regardless of their present state. If for example a different data output mode is required than the default for a particular video mode, a write to the appropriate register after the mode has changed will restore the desired value..

Video Mode	Clock (MHz)	System Clock Divisor	Video Data	Line Length	Field Length	Data Output Mode
CIF	24.00	6	356 x 292	416	320	5-wire
VGA	24.00	2	644 x 484	762	524	5-wire
QVGA[1]	24.00	8	324 x 244	381	262	5-wire

Table 3 : Video Timing Modes

1. **Both QVGA modes are configured in this way**

3.1.1 Arbitration registers

When the operating video mode is changed a number of serial registers are forced into new states. The complete list is as follows:

Arbitrated feature	Video mode selected/value automatically programmed[1]			
	pantiltCIF	VGA	pantiltQVGA	subsampledQVGA
line length	415	761	380	380
field length	319	523	261	261
system clock division	4	2	8	8
extra black lines[2]	no	yes	yes	yes

Table 4 : Arbitration registers

1. **Remember that the line length and field length values programmed are always 1 less than the actual line and field lengths as the internal line and field length counters count from 0.**
2. **The contents of the extra black lines are enabled on to the data bus by setting bit [5] of serial register [17]. If bit [0] of serial register [24] is reset, indicating that the preferred coprocessor device is not the VP3 device, (a STMicroelectronics coprocessor), then the extra black lines are enabled by default regardless of the basic video mode selected. The VGA, pantiltQVGA or subsampledQVGA video modes have the extra black lines always selected regardless of the state of the lsbit of serial register[24].**

The registers that control the image position within the pixel array and also the order in which the pixels are read out have not been included in the table as their values are subject to a secondary series of registers. We will discuss the former in sections 2.2 and 2.3.

3.1.2 Input Clock Frequencies

It is recommended that a 16 MHz clock is used to generate 30fps pantiltCIF and a 24MHz clock used to generate 30fps VGA, pantiltQVGA and subsampledQVGA. The sensor can adapt to a range of other input frequencies and still generate the required frame rates. For example, a 24 MHz clock can be used to generate CIF-30fps. By setting bit [7] of serial register [22] the sensor can automatically divide the incoming clock by 1.5 by setting bit [7] of serial register [22], such that the internal clock generator logic will still receive a 16 MHz clock.

Note that the clock division register is internally an 8 bit value, although the user may only program the lower nibble. The upper nibble is reserved for setting the clock divisor as we change between primary video modes. The lower nibble can be programmed to reduce the effective frame rate within each video mode and also increase the overall exposure time which may be useful when controlling exposure in low light conditions.

The system clock divisor column in Table 5 assumes that the programmable pixel clock divisor is set to the default of 0, implementing a divide by 1 of the internal pixel clock. Consider the following scenario where a user requires 15 fps CIF resolution image. As can be seen there are a wide range of options to achieve the same result.

clk in (MHz)	Divide by 3/2 enabled?	System clock divisor	Pixel clock divisor	pclk (MHz)	Field Rate
8	no	4	1	2	15
12	yes	4	1	2	15
16	no	4	2	2	15
24	yes	4	2	2	15

Table 5 : System clock divisor options

3.2 Pixel Array

The physical pixel array is 652 x 488 pixels. The pixel size is 7.5 µm by 7.5 µm. The image size for VGA is 644 x 484 pixels, for pantiltQVGA and subsampledQVGA modes the image size is 324 x 244 pixels and, finally, the pantiltCIF mode image size is 356 x 292.

The 4 physical columns on each side of the VGA image prevent columns 1 and 2 in VGA modes from being distorted by the edge effects which occur when a pixel is close to the outer edge of the physical pixel array.These columns can be enabled as part of the visible image if the user is operating the sensor in the pantiltQVGA or pantiltCIF modes.

Figure 3 shows how the 356 x 292 and 324 x 244 sub-arrays are aligned within the full size 652 x 488 pixel array. The Bayer colourisation pattern requires that the top-left corner of the pixel sub-array is always a Green 1 pixel. Note that the pantiltQVGA and pantiltCIF sub-arrays are centrally orientated within the full size array.

Image read-out is very flexible. Sections 3.3.2 - describe the options available to the user. By default the sensor read out is configured to be horizontally 'shuffled' non-interlaced raster scan. The horizontally 'shuffled' raster scan order differs from a conventional raster in that the pixels of individual rows are re-ordered, with the odd pixels within a row read-out first, followed by the even pixels. This 'shuffled' read-out within a line, groups pixels of the same colour (according to the Bayer pattern - Figure 2) together, reducing cross talk between the colour channels. This option is on by default and is controllable via the serial interface. The horizontal shuffle option would normally only be selected with the colour sensor variant, VV6500.

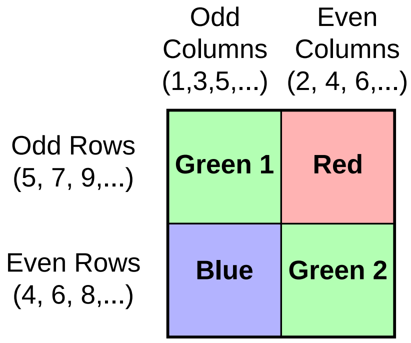
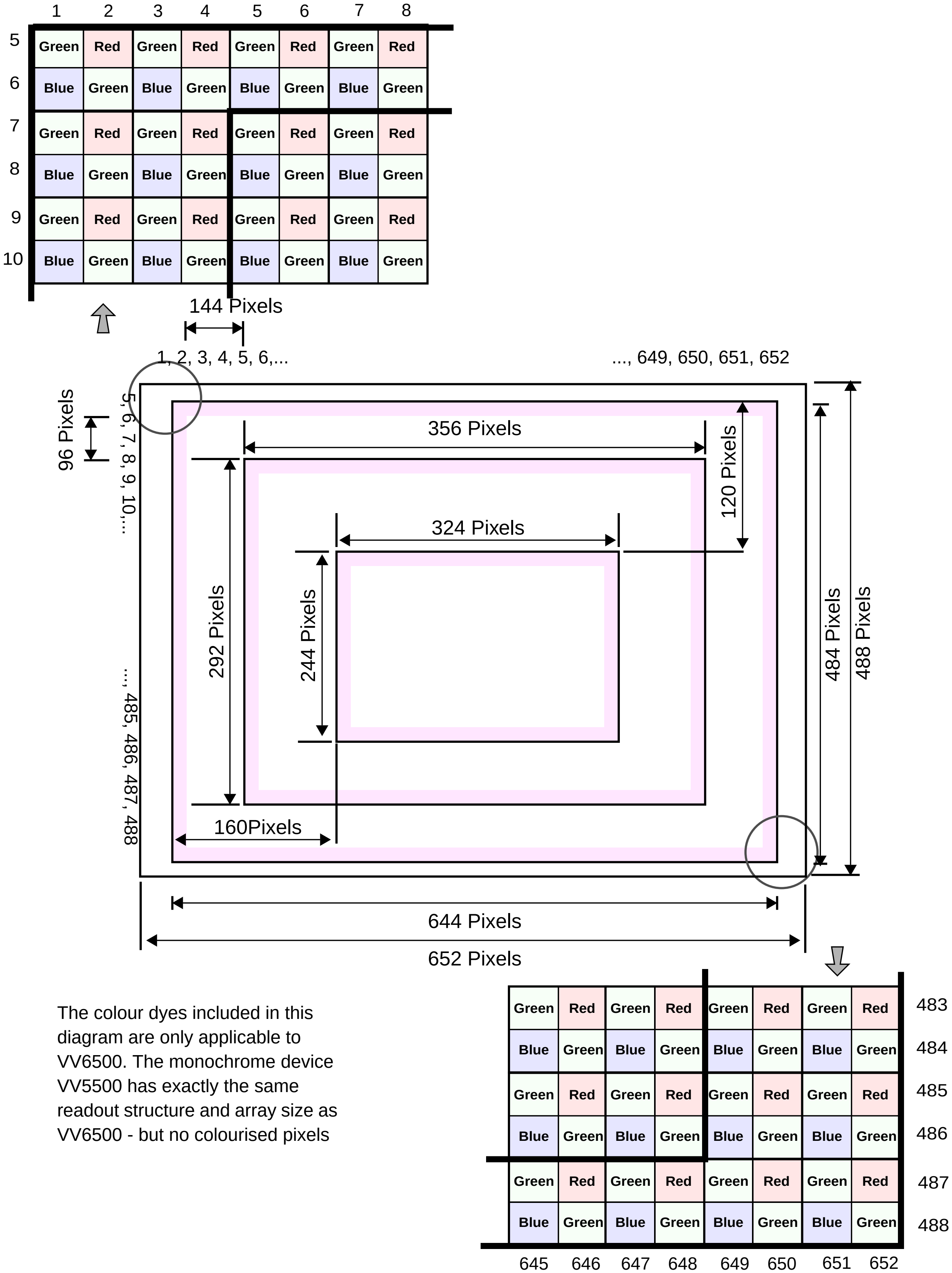


Figure 2 : Bayer Colourisation Pattern (VV6500 only)



	1	2	3	4	5	6	7	8
5	Green	Red	Green	Red	Green	Red	Green	Red
6	Blue	Green	Blue	Green	Blue	Green	Blue	Green
7	Green	Red	Green	Red	Green	Red	Green	Red
8	Blue	Green	Blue	Green	Blue	Green	Blue	Green
9	Green	Red	Green	Red	Green	Red	Green	Red
10	Blue	Green	Blue	Green	Blue	Green	Blue	Green

645	646	647	648	649	650	651	652	
Green	Red	Green	Red	Green	Red	Green	Red	483
Blue	Green	Blue	Green	Blue	Green	Blue	Green	484
Green	Red	Green	Red	Green	Red	Green	Red	485
Blue	Green	Blue	Green	Blue	Green	Blue	Green	486
Green	Red	Green	Red	Green	Red	Green	Red	487
Blue	Green	Blue	Green	Blue	Green	Blue	Green	488

The colour dyes included in this diagram are only applicable to VV6500. The monochrome device VV5500 has exactly the same readout structure and array size as VV6500 - but no colourised pixels

Figure 3 : Image Formats

3.3 X-offset and Y-offset

The image information is retrieved from the pixel array via a 2 dimensional address. The x and y address busses count from a starting point described by x-offset, y-offset up to a maximum count in x and y that is determined by the image size. The order of this count and the count step size is dependent upon the special image format parameters described below. The detailed control of the x and y address counters is entirely handled by the sensor logic.

As can be seen in Figure 3 the visible array size is 652 columns by 488 rows. The VGA image is sized, 644 columns by 484 rows, thus we have a “border” of visible pixels that we do not read when this mode is selected.

The images that are read out of the sensor are always “centred” on the array, therefore we allow a border of 4 columns at either end of the image in the x-direction and a border of 2 rows at the top and bottom of the image in the y-direction. The pantilt CIF and pantiltVGA images are similarly centred within the full size array.

The x and y offset coordinates are fixed for the VGA mode but if the user selects the pantiltCIF or pantiltQVGA modes then they may specify x and y-offsets for pantiltCIF in the range:

- (xoffset >= 1) and (xoffset <= 297)
- (yoffset >= 5) and (yoffset <= 197)

and x and y-offsets for pantiltQVGA in the range:

- (xoffset >= 1) and (xoffset <= 329)
- (yoffset >= 5) and (yoffset <= 245)

The sensor will automatically clip values outwith the specified ranges. The y addresses less than 5 are reserved for the sensor black lines and the y address greater than 492 are reserved for the sensor dark lines. Neither the black lines nor the dark lines contain visible image data.

3.3.1 Image readout parameters

The following parameters are available to process the sensor readout:

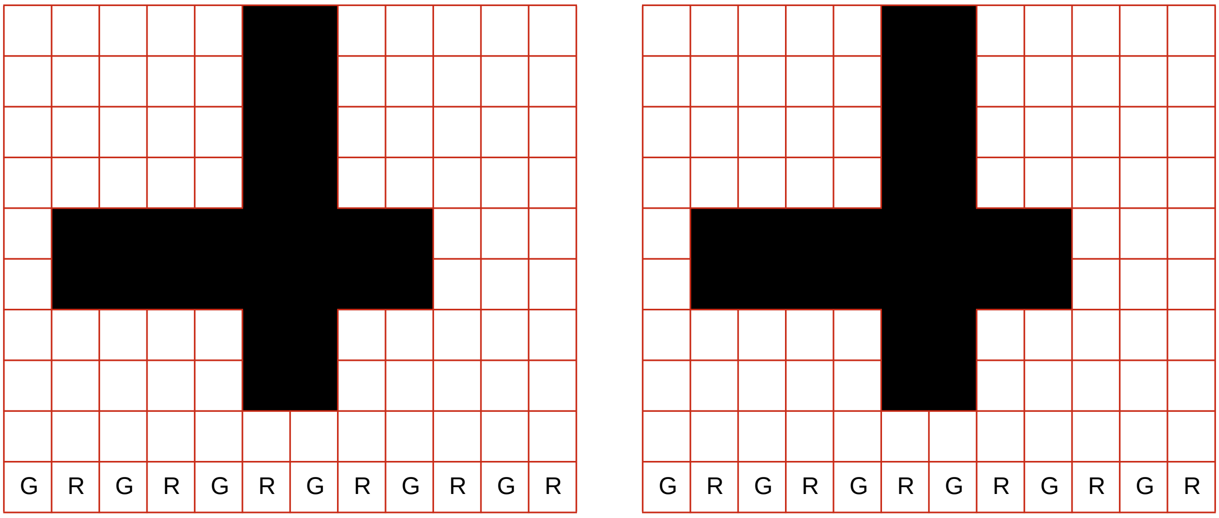
- Shuffle horizontal readout, enabled by setting bit [7] of serial register [17]
- Mirror horizontal readout, enabled by setting bit [3] of serial register [22]
- Shuffle vertical readout, enabled by setting [2] or serial register [22]
- Mirror vertical readout, enabled by setting [4] of serial register [22]

The effect of each of these parameters is probably best described via a series of diagrams, see sections 3.3.2 - below.

Although all the above features may be used in conjunction with one another we will only display one special image readout parameter at any one time.

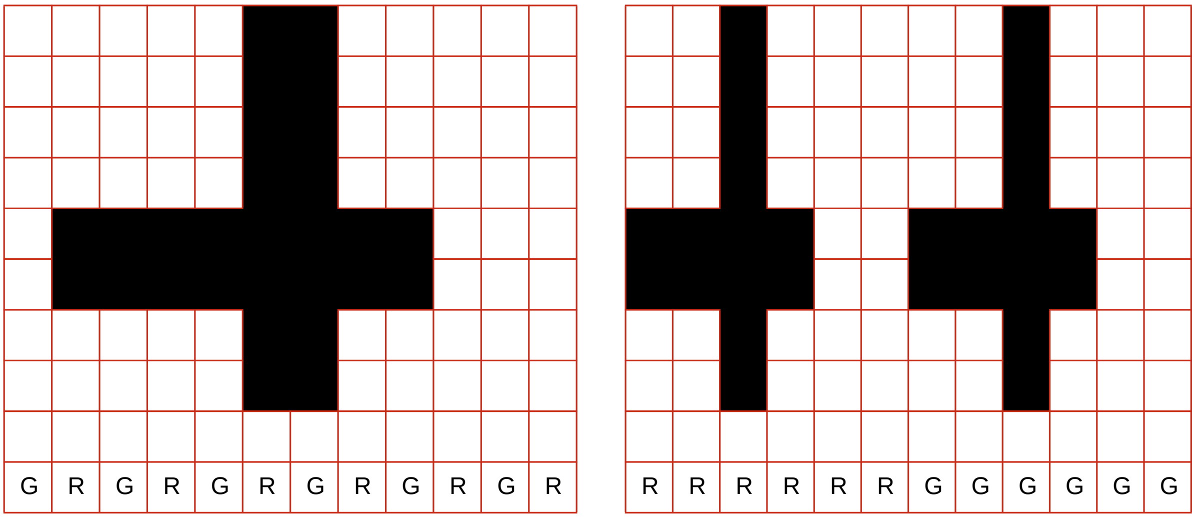
3.3.2 Horizontal shuffle

Figure 5 is the reference figure that shows the image readout without any of the optional image parameters, shuffle or mirror, selected. Figure 5 shows how the image will appear if the horizontal shuffle bit has been selected. Note that the even columns, (column 2,4,6 etc), are read out first followed by the odd columns, (1,3,5,7 etc).‘



Where G - Green and R - Red

Figure 4 : Standard Image Readout



Where G - Green and R - Red

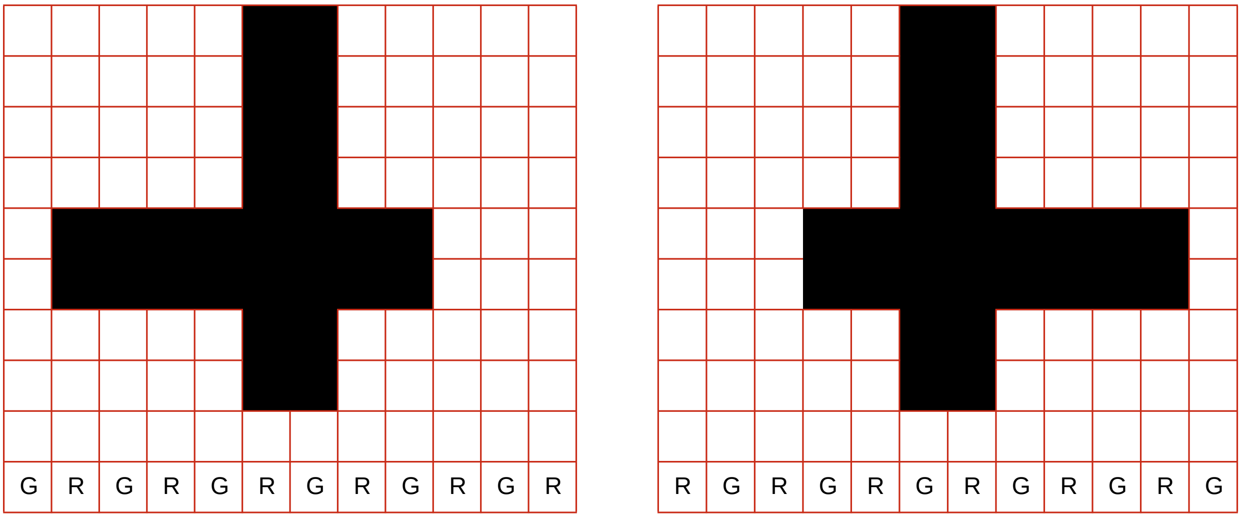
Figure 5 : Horizontal Shuffle Enabled

3.3.3 Horizontal mirror

Figure 6 shows the output image with the horizontal mirror feature enabled. Note that the columns are read out in reverse order.

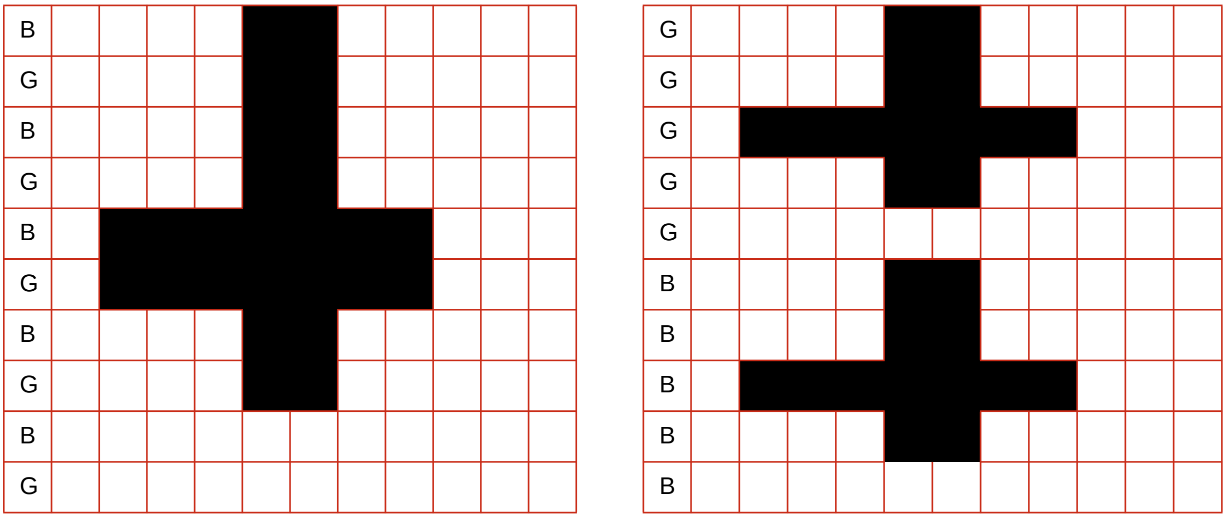
3.3.4 Vertical shuffle

Figure 7 shows the output image with the vertical shuffle feature enabled. Note that the even rows (rows 2,4,6 etc), are read out first followed by the odd rows, (rows 1,3,5 etc)



Where G - Green and R - Red

Figure 6 : Horizontal mirror enabled

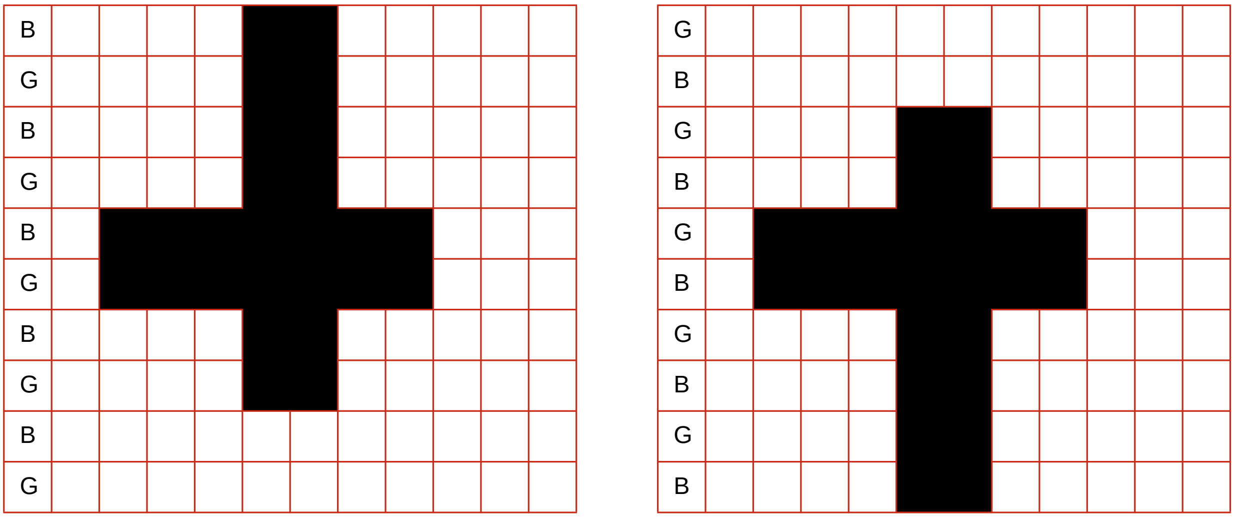


Where G - Green and B - Blue

Figure 7 : Vertical Shuffle enabled

3.3.5 Vertical mirror

Figure 8 shows the output image with the vertical mirror feature enabled. Note that the rows are read out in reverse order.



Where G - Green and B - Blue

Figure 8 : Vertical Mirror enabled

3.4 Sub Array Output Modes

VV5500/VV6500 has two sub-array output modes, pan/tiltCIF (ptCIF) and pantiltVGA (ptVGA).

3.4.1 Pan/Tilt CIF and Pan/TIlt QVGA

In this mode the CIF/QVGA image is generated by outputting a cropped portion of the VGA image as illustrated in Figure 9. When the pan-tilt modes are initially selected the image will be horizontally and vertically justified in the within the full size array. The coordinates which define the top left corner of the QVGA portion of the array to be output are defined by the x-offset & y-offset parameters in serial registers 88 - 91 inclusive.

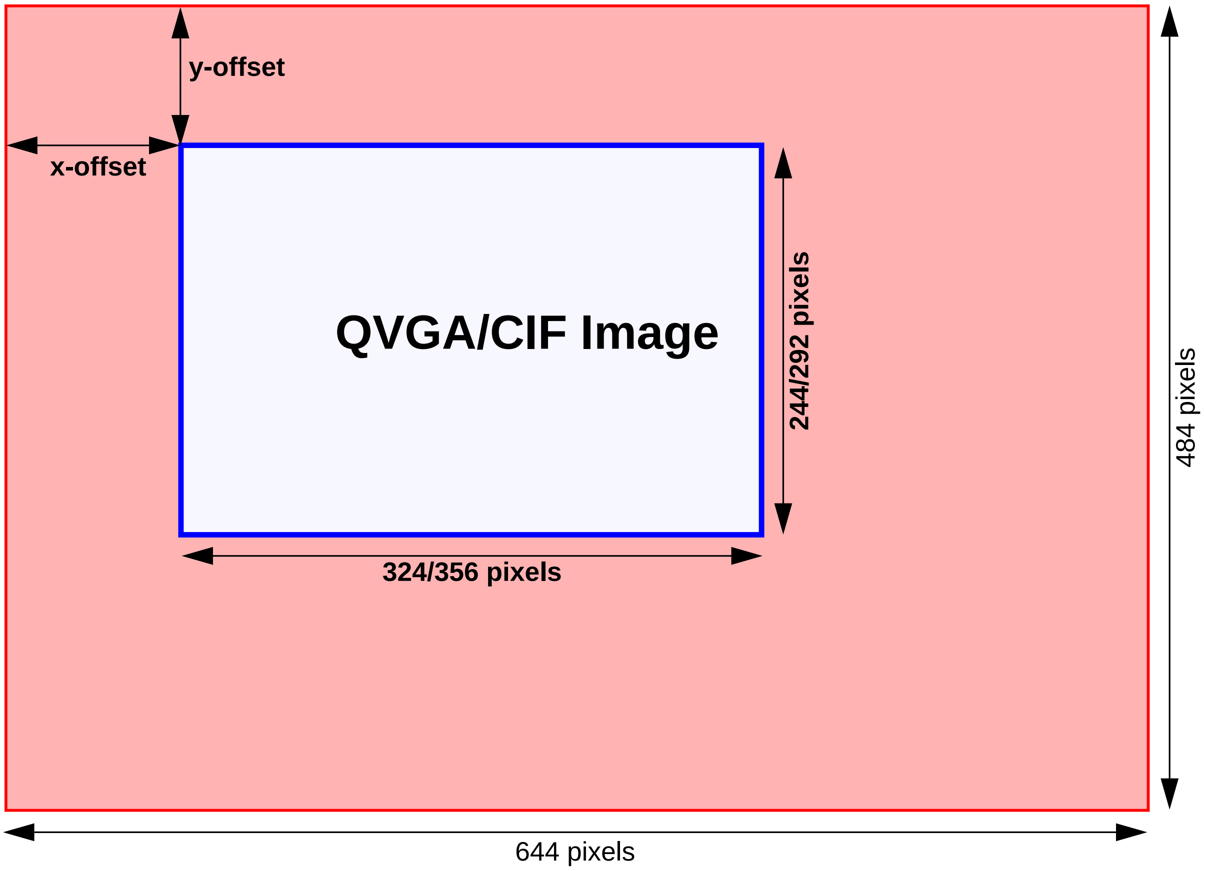
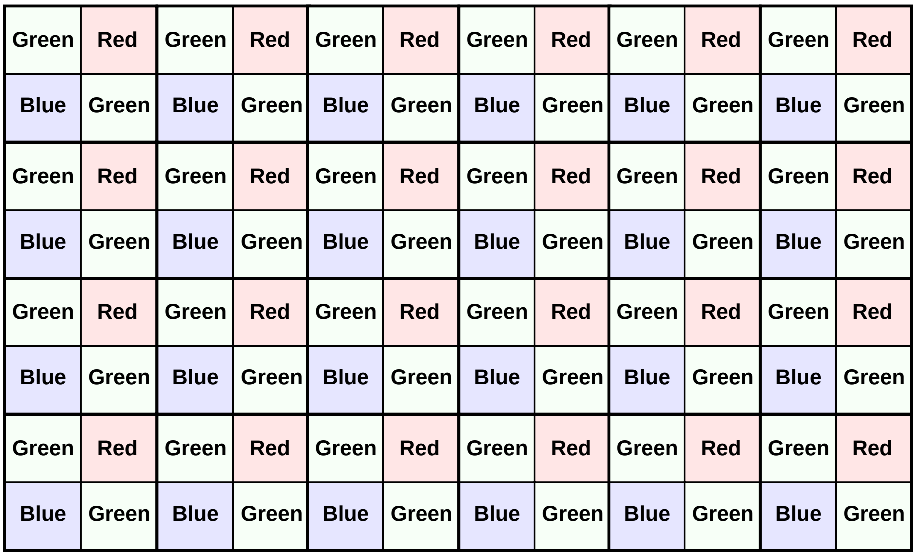


Figure 9 : Pan/Tilt CIF, Pan/Tilt QVGA Image Format

The x-offset and y-offset parameters are subject to minimum and maximum values which are set according to the video output mode (horizontal shuffle etc). Any clipping (against a maximum) or clamping (against a minimum) will be automatically controlled by the sensor logic. Regardless of whether any of the shuffle/mirror modes have been selected the user should always identify the top left corner coordinates as the x-offset and y-offset. To preserve the Bayer pattern at the sensor output the first pixel image of the image should always be green followed by red. If the x or y offsets are adjusted by a single step, i.e. adjust the x-offset from n to n+1, then this pattern will be corrupted. The user should always write an **odd** number to the x and y offset registers and this will preserve the Bayer pattern. The 5500, monochrome sensor is unaffected by such an adjustment to the x-offset coordinate, as the pixels do not contain any colour information.

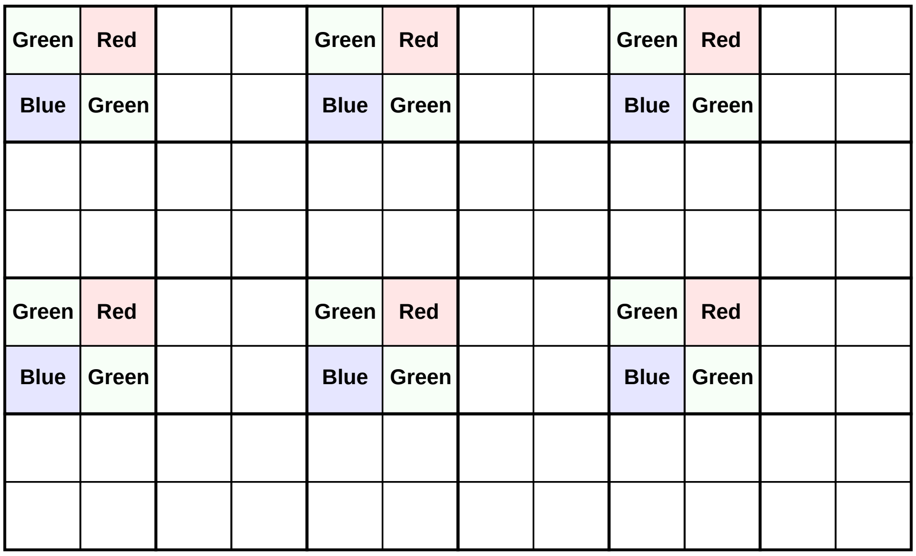
3.4.2 Sub-Sampled QVGA

In this mode the QVGA image is generated by sub-sampling the VGA image in groups of 4 to preserve the Bayer pattern with every second group of pixels & lines skipped as illustrated in Figure 10. Although the former would not necessarily apply to a monochrome sensor the same address sequence is preserved. VV5500 users should ignore the colour references in Figure 10. Due to the crude nature of the sub-sampling, the resultant output image will be of inferior quality but contains full field of view and is intended for use in gesture recognition applications or perhaps as a preview option before switching to ptQVGA or ptCIF modes to view the required scene region in more detail.



Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green

Bayer Colourised Pixel Array



Green	Red			Green	Red			Green	Red		
Blue	Green			Blue	Green			Blue	Green		
Green	Red			Green	Red			Green	Red		
Blue	Green			Blue	Green			Blue	Green		

Sub-Sampled Bayer Colourised Pixel Array

Figure 10 : Sub-Sampled QVGA Image Format

4. Black Offset Cancellation

In order to produce a high quality output image from VV5500/VV6500 it is important to accurately control the video signal black level. Within the sensor array of VV5500/VV6500 there are a number of lines that are specified as black, that is they are exposed to incident light but are always held in minimum exposure. VV5500/VV6500 also has a number of dark lines, that is lines that are integrated for the same length of time as the visible lines but the pixels within these dark lines are shielded from incident light by an opaque material (e.g. metal 3). The diagram below shows where the different types of lines that appear within the full array.

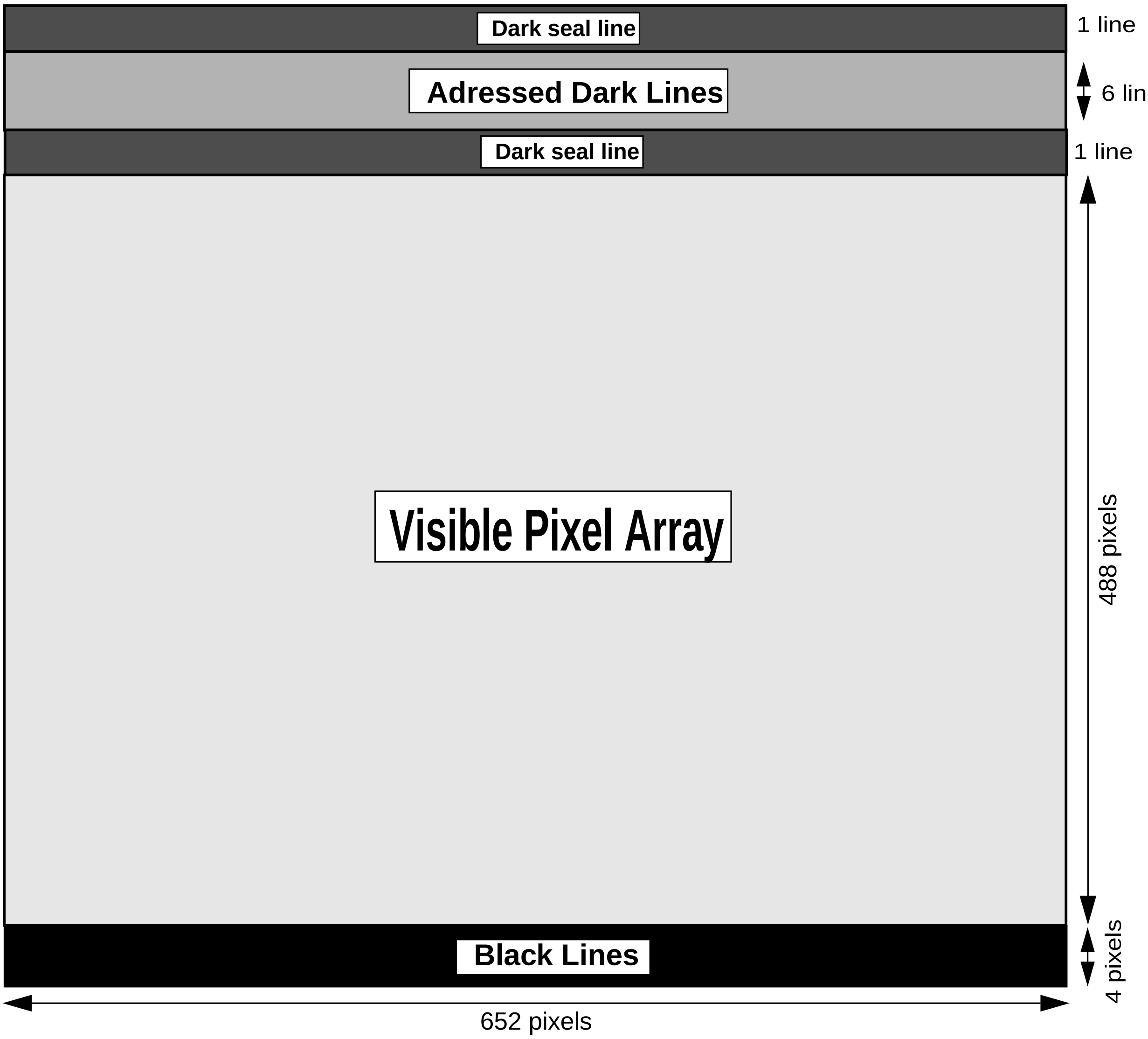


Figure 11 : Physical position of Black and Dark Lines

VV5500/VV6500 can perform automatic black offset cancellation that will optimise the video black level. VV5500/VV6500 contains an algorithm that monitors the level of the black pixels and applies a correction factor, if required, to provide an ideal black level for the video stream.

The user can control the application of the offset cancellation parameter. The internally calculated offset can be applied to the video stream or alternatively an externally calculated offset can be applied or finally there is the option of applying no offset at all. Details of how to select the aforementioned modes can be found in subsubsection 9.5.5.

The black offset cancellation algorithm accumulates data from the centre 2 of the 4 physical black lines. The table below describes all the variable black offset cancellation parameters. The internal cancellation algorithm uses a leaky integrator model to control the size of the calculated offset. The leaky integrator model takes as input the current offset plus a shifted version of the error between the ideal black level and the current offset. The magnitude of the shift in the error is programmable. It is also possible to control the range of pixel values that will inhibit a change in the calculated offset. A narrow band (128 +/- 2 codes) or a wide band (128 +/- 4 codes) can be selected. If the latter is selected and the pixel average returned in the current field lies between 124 and 132 then the offset cancellation will remain unchanged.

Following a gain change, or when exiting low-power, sleep or suspend modes, the internal (19bit) offset register will be reset to the default resulting in an automatic black offset of -64.

5. Dark Offset Cancellation

VV5500/VV6500 performs dark line offset cancellation as well as black line offset cancellation. A dark line is shielded from incident light by an opaque material such as metal 3 (as an example) but these lines will be exposed to incident light for the same length of time as the visible pixels. If the dark pixels are completely shielded from light then no incident light should reach the pixels and the pixels will produce the same digital code as the black pixels, i.e. 128 internally (therefore 64 externally). The algorithm used to calculate the dark offset cancellation is identical to that used to calculate the black offset cancellation, however the dark algorithm does assume that the dark pixels have already been black corrected therefore the target dark average is 64 thus the dark offset cancellation is 0 by default.

The dark offset cancellation algorithm is configured by the dark offset cancellation setup register, [46], see subsubsection 9.5.3. The only parameter in this that is different from the corresponding table that configures the black offset cancellation algorithm is the control bit, [bit2], that determines the number of dark lines that are to be used by the cancellation algorithm. It is possible to select half of the total number of available dark lines to be used to calculate the dark offset cancellation setting. When the former is selected the dark lines used by the algorithm are always preceeded by another dark line, thereby giving extra immunity from damaging edge effects that may occur on lines close to the edge of the shield material.

It should be noted that the black and dark offset cancellation are completely independent. For example it is possible for the user to select internal automatic black offset cancellation but to opt for no dark offset cancellation or indeed choose to perform the dark offset cancellation externally.

6. Exposure Control

6.1 Calculating Exposure Period

The exposure time, comprising coarse and fine components, for a pixel and the analogue gain are programmable via the serial interface.

The coarse exposure value sets the number of complete lines a pixel exposes for, while the fine exposure sets the number of additional pixel clock cycles a pixel integrates for. The sum of the two gives the overall exposure time for the pixel array.

Exposure Time = ((Coarse setting x Line Period) + (Fine setting)) x (CLKI clock period) x Clock Divider Ratio$_{\text{note1}}$

note1: Clock Divider Ratio = 1/(Basic Clock Division * Optional Pixel Clock Divisor)

Default Clock Divder Ratio as follows: (Optional Pixel Clock Divisor = 1)

- VGA - 1/2
- ptCIF - 1/4
- ptQVGA/ssQVGA - 1/8

The maximum coarse and fine exposure settings are a function of the field and line lengths respectively. The maximum coarse exposure is current field length - 1 and the the maximum fine exposure is current line length - fixed offset, see below. If an exposure value is requested that is beyond the maximum then the applied exposure setting will be clipped to the current maximum.

Video Mode	Fine Exposure Offset (pck's)
VGA	49
ptCIF	53
ptQVGA	110
ssQVGA	110

Table 6 : Fine Exposure Offset

6.2 Gain Components

The analogue gain in VV5500/VV6500 is programmed via the 8 bit gain register[36]. The analogue gain comprises 2 components, capacitive gain, (set by the ms nibble), and current gain, (set by the ls nibble). It is strongly recommended that the capacitive gain setting is left at the default value of 4'b1111. Table 7 details the available gain settings. We assume that mode_select[24], bit1 is 0. gain[7:0] is the value programmed in register[36]. The ls nibble of the gain value is limited to 4'he, with 4'hf not permitted.

10bit ADC mode			
gain[7:0]	igain[3:0]	cgain[5:0]	Overall Gain
8'hfe	1 (0001_2)	63	4.000
8'hfd	2 (0010_2)	63	2.6667
8'fc	3 (0011_2)	63	2.0000

Table 7 : Analogue Gain Settings

10bit ADC mode			
gain[7:0]	igain[3:0]	cgain[5:0]	Overall Gain
8'hfb	4 (0100_2)	63	1.6000
8'hfa	5 (0101_2)	63	1.3333
8'hf9	6 (0110_2)	63	1.1429
8'hf8	7 (0111_2)	63	1.0000
8'hf7	8 (1000_2)	63	0.8889
8'hf6	9 (1001_2)	63	0.8000
8'hf5	10 (1010_2)	63	0.7273
8'hf4	11 (1011_2)	63	0.6667
8'hf3	12 (1100_2)	63	0.6154
8'hf2	13 (1101_2)	63	0.5714
8'hf1	14 (1110_2)	63	0.5333
8'hf0	15 (1111_2)	63	0.5000

Table 7 : Analogue Gain Settings

note: The relationship between the programmed gain value as written to register[36] and the igain (current gain) and cgain (capacitive gain) is as follows:

igain

If mode_select[24], bit 1 is set then igain[3:0] is the inverse of gain[3:0], i.e. if gain[3:0] = 6, igain[3:0] = 9.

If mode_select[24], bit 1 is reset then igain[3:0] is the inverse of the mirror of gain[3:0], i.e. bit 3 of igain is the inverse of bit 0 of gain, i.e. gain = 4 and igain = 13.

cgain

cgain is a 6 bit value therefore we have to pad the 4 bits of the gain register. In 10bit modes cgain[1:0] is fixed at 2'b11 and cgain[5:2] is set to gain[7:4]. In the 9bit modes cgain[1:0] is also set to 2'b11, however cgain[5:2] is set to gain[7:4] divided by 2, thus gain[7:4] = 4'b1111 gives cgain[5:0] = 6'b011111.

6.3 Clock Division

Although the clock divisor register is an 8 bit register the user only has write access to the lower 4 bits as described above. The upper 4 bits of the register are altered automatically when the video mode is changed by writing to Setup0[16] register. The upper 4 bits are pre-programmed as follows:

Video mode	Register[37], bits[7:4]	Additional divide by 1.5 enabled	Effective system clock divisor
VGA	4'b0000	no	Divide CLKI/CLKIP by 2
CIF (16 Mhz input clock)	4'b0001	nos	Divide CLKI/CLKIP by 4
CIF (24 Mhz input clock)	4'b0001	yes	Divide CLKI/CLKIP by 6

Table 8 : System Clock Divisor Options

Video mode	Register[37], bits[7:4]	Additional divide by 1.5 enabled	Effective system clock divisor
QVGA	4’b0011	no	Divide CLKI/CLKIP by 8

Table 8 : System Clock Divisor Options

6.4 Updating Exposure,Gain and Clock Division Settings

Although the user can write a new exposure, gain or clock division parameter at any point within the field the sensor will only consume these new external values at a certain point. The exceptions to this behaviour are when the user has selected immediate update of gain and clock division. If the user has selected the former then the new gain or clock division value will be applied as soon as the serial interface message has completed. The fine and coarse exposure values are always written in a “timed” manner. There are a number of “update pending” flags available to the user (see Status0 reg[2] for details) that allows the user to detect when the sensor has consumed one of the timed parameters. In the next section of this document we will detail all the timed parameters and describe when they are updated.

It is important to realise that there is a 1 frame latency between a new exposure value being applied to the sensor array and the results of this new exposure value being read-out. The same latency does not exist for the gain value. To ensure that the new exposure and gain values are aligned up correctly the sensor delays the application of the new gain value by approximately one frame relative to the application of the new exposure value.

If the user is using the autoincrement option in the serial interface when writing a new series of exposure/gain and clock division parameters then it is important to ensure that the sensor receives the complete message bunch before updating any of the parameters. It is also important that the timed parameters are updated in the correct order, we will discuss this fully in the next section. If an autoincrement message sequence is in progress but we have reached the point in the field timing where the gain value would normally be updated, we actually inhibit the update. We inhibit the update to ensure that the gain change is not passed to the sensor before a change in the exposure is still pending.

7. Timed Serial Interface Parameters

The previous section, Exposure Control, introduced the concept of a “timed parameter”, that is information that is written via the serial interface but will not be used immediately by the sensor, rather there will be a delay before the information is passed to the internal registers (referred to as the working registers) from the serial interface registers (referred to as the shadow registers). It is the contents of the working registers that will determine sensor behaviour.

The architecture of VV5500/6500 requires that many of the programmable registers are handled in such a manner. This section will identify all these registers, describe what they are all used for and then go on to explain when they are all updated.

7.1 Listing and Categorizing the Parameters

The timed parameters are split into 6 categories as follows:

- fine exposure
- coarse exposure
- clock division
- gain
- pan parameter
- tilt parameter
- video timing

There is a “pending” flag for each of the above categories. These flags are stored in Status0 Register[2]. If one of the flags is high this indicates that the working register/s controlled by that flag have yet to be updated from the according shadow register/s. This feedback information could be useful if a user is, for example, attempting to write an exposure controller. The status of the pending flags allows accurate timing of the serial interface communications.

7.1.1 Fine Exposure

The fine exposure category simply comprises registers[32,33].

7.1.2 Coarse Exposure

The coarse exposure category simply comprises registers[34,35].

7.1.3 Clock Division

The clock division category simply comprises register[37].

7.1.4 Gain

The gain category simply comprises register[36].

7.1.5 Pan Parameter

The pan parameter category comprises the following registers:

- Setup0[16] (The “pan_pend” flag is set unconditionally)
- Setup1[17] (The “pan_pend” flag will only be set if the hshuffle control bit is changing state)
- Data_format[22] (The “pan_pend” flag will only be set if the hmirror control bit is changing state)
- X-offset[87,88] (The “pan_pend” flag set unconditionally)

7.1.6 Tilt Parameter

The tilt parameter category comprises the following registers:

- Setup0[16] (The “tilt_pend” flag will is set unconditionally)
- data_format[22] (The “tilt_pend” flag will be set if the hshuffle control bit or the hmirror control bit is changing state)
- Y-offset[89,90] (The “tilt_pend” flag is set unconditionally)

7.1.7 Video Timing Parameter

The video timing parameter category comprises all the other shadow/working register pairs. The video timing parameter update pending flag will be unconditionally set if any of the following registers are written to:

- Setup0[16]
- Setup1[17]
- fg_mode[20]
- data_format[22]
- op_format[23]
- mode_select[24]
- Dark Pixel Offset[44,45]
- Dark Pixel Cancellation Setup Register
- Black Pixel Offset[44,45]
- Black Pixel Cancellation Setup Register
- Line Length[82,83]
- Field Length[97,98]

7.2 Timed Parameter Update Points

The timed parameter categories are updated as follows:

note: We refer to odd and even fields in the table below. In a video mode like CIF or QVGA the fields are all identical in length, we still have to be able to differentiate between fields to enable correct updating of register parameters.

Timed parameter category	Updated when?
fine exposure	Conditional on a change pending in the line length register. ***Line length change pending***: update fine exposure at the odd to even field transition ***Line length change not pending***: update fine exposure during the start of active video (SAV) region of the end of frame (EOF) line (the line that follows the last line of active video) in the odd field.
coarse exposure	Updated during the SAV region of the first dark line in an odd field
clock division	Updated at the odd to even field transition
gain	Updated during the SAV region of the EOF line in the odd field
pan parameter	Updated during the SAV region of the EOF line in the odd field
tilt parameter	Updated during the SAV region of the first visible line in an odd field
video timing	Updated at the odd to even field transition

Table 9 : Timed Parameter Update Points

The order that the above timed parameters are updated is critical. Let us assume that all the pending flags are set, i.e. we have written to at least one register in each category. The working registers will be updated in the following order:

1. Coarse exposure
2. Tilt parameters

3. Gain, Pan parameters and conditionally the fine exposure (see Table 9 for details)
4. Clock division, video timing parameters and conditionally the fine exposure (see Table 9 for details)

8. Digital Video Interface Format

8.1 General description

The video interface consists of a bidirectional, tri-stateable 5-wire data bus. The nibble transmission is synchronised to the rising edge of the system clock (Figure 26).

<table>
<tr><td>Read-out Order</td><td colspan="4">Progressive Scan (Non-interlaced)</td></tr>
<tr><td>Form of encoding</td><td colspan="4">Uniformly quantised, PCM, 8/10 bits per sample</td></tr>
<tr><td rowspan="4">Correspondence between video signal levels and quantisation levels:</td><td colspan="4">The internal10-bit pixel data is clipped to ensure that 0_H and $3FF_H$ (5 Wire) or FF_H (4/8 Wire) values do not occur when pixel data is being output on the data bus.</td></tr>
<tr><td colspan="2">10-Bit Data</td><td colspan="2">8-Bit Data</td></tr>
<tr><td>Pixel Values</td><td>1 to 1022</td><td>Pixel Values</td><td>1 to 254</td></tr>
<tr><td>Black Level</td><td>64</td><td>Black Level</td><td>16</td></tr>
</table>

Table 10 : Video encoding parameters

Digital video data may be either 8 or 10 bits per sample, and can be transmitted in one of the following ways:

10-bit data

1. A series pair of 5-bit nibbles, most significant nibble first, on 5 wires.
2. An 8-bit number e.g. line code. line numbers and status line data is padded with 00 in the least significant two bits to make up a 10-bit value.

8-bit data

1. A single 8 bit byte over 8 output wires$_{note}$.
2. A series pair of 4-bit nibbles, most significant nibble first, on 4 wires.
3. The top 8-bits of a 10-bit value e.g. pixel data or line averages is used as the 8-bit equivalent.

=

note: if the 8-wire output mode has been selected then the normal FST/LST pin function is sacrificed as these pins are required to output data information

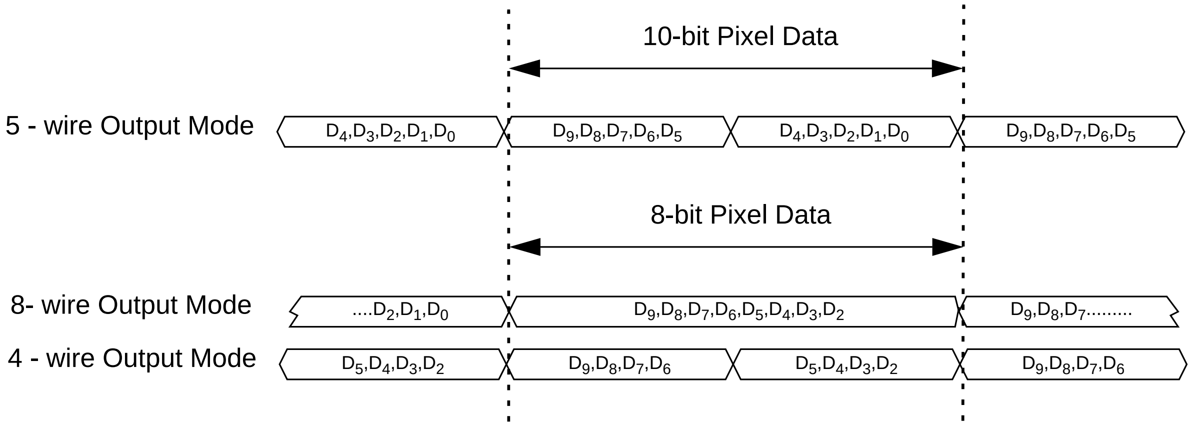


Figure 12 : Possible Output Modes

In the following description the 4-wire mode is used as an example. The 5-wire mode can be viewed as a variant of the 4-wire mode. Data is output on the least significant data wires available. e.g. in 4-wire mode, data is output on data wires D[3:0] while in

5-wire mode data is output on D[4:0].

Multiplexed with the sampled pixel data is control information including both video timing references and sensor status/ configuration data.

Video timing reference information takes the form of field start characters, line start characters, end of line characters and a line counter.

Where hexadecimal values are used, they are indicated by a subscript H, such as FF_H; other values are decimal.

8.2 Embedded control data

To distinguish the control data from the sampled video data all control data is encapsulated in embedded control sequences. These are 6 bytes long and include a combined escape/sync character, 1 control byte (the ‘command byte’) and 2 bytes of supplementary data.

To minimise the susceptibility of the embedded control data to random bit errors redundant coding techniques have been used to allow single bit errors in the embedded control words to be corrected. However, more serious corruption of control words or the corruption of escape/sync characters cannot be tolerated without loss of sync to the data stream. To ensure that a loss of sync is detected a simple set of rules has been devised. The four exceptions to the rules are outlined below:

1. Data containing a command word that has two bit errors.
2. Data containing two ‘end of line’ codes that are not separated by a ‘start of line’ code.
3. Data preceding an ‘end of field’ code before a start of frame’ code has been received.
4. Data containing line that do not have sequential line numbers (excluding the ‘end of field’ line).

If the video processor detects one of these violations then it should abandon the current field of video

8.2.1 The combined escape and sync character

Each embedded control sequence begins with a combined escape and sync character that is made up of three words. The first two of these are FF_H FF_H- constituting two words that are illegal in normal data. The next word is 00_H - guaranteeing a clear signal transition that allows a video processor to determine the position of the word boundaries in the serial stream of nibbles. Combined escape and sync characters are always followed by a command byte - making up the four byte minimum embedded control sequence.

8.2.2 The command word

The byte that follows the combined escape/sync characters defines the type of embedded control data. Three of the 8 bits are used to carry the control information, four are ‘parity bits’ that allow the video processor to detect and correct a certain level of errors in the transmission of the command words, the remaining bit is always set to 1 to ensure that the command word never has the value 00_H. The coding scheme used allows the correction of single bit errors (in the 8-bit sequence) and the detection of 2 bit errors The three data bits of the command word are interpreted as shown in Figure 13.The even parity bits are based on the following relationships:

1. An even number of ones in the 4-bit sequence (C_2, C_1, C_0 and P_0).
2. An even number of ones in the 3-bit sequence (C_2, C_1, P_1).
3. An even number of ones in the 3-bit sequence (C_2, C_0, P_2).
4. An even number of ones in the 3-bit sequence (C_1, C_0, P_3).

Table 13 shows how the parity bits maybe used to detect and correct 1-bit errors and detect 2-bit errors.

8.2.3 Supplementary Data

The last 2 bytes of the embedded control sequence contains supplementary data. Three options:

1. The last 2 bytes of the SAV 6 byte sequence contain the current 12-bit line number. The 12-bit line number is packaged up by splitting it into two 6-bit values. Each 6-bit value is then converted into an 8-bit value by adding a zero to the start and an odd word parity bit at the end.
2. The 5th byte of the EAV sequence contains a pixel average for that line either based upon the middle 256 pixels of the line. The final byte is FF_H.

Note: in 5-wire mode, the embedded control data is calculated as detailed above and output as the most significant 8-bits. The least significant 2-bits are padded with zero.

Line Code	Nibble X_H (1 C_2 C_1 C_0)	Nibble Y_H (P_3 P_2 P_1 P_0)
End of Line	1000_2 (8_H)	0000_2 (0_H)
Blank Line (BL)	1001_2 (9_H)	1101_2 (D_H)
Black line (BK)	1010_2 (A_H)	1011_2 (B_H)
Visible Line (VL)	1011_2 (B_H)	0110_2 (6_H)
Start of Even Field (SOEF)	1100_2 (C_H)	0111_2 (7_H)
End of Even Field (EOEF)	1101_2 (D_H)	1010_2 (A_H)

Table 11 : Embedded Line Codes

The table below shows how the 8 bit control codes are mapped onto the output data bits in the 5 wire mode.

Line Code	Most significant nibble Data[4:0]	Least significant nibble Data[4:0]
End of Line	1_0000_2 (10_H)	0_0000_2 (00_H)
Blank Line (BL)	1_0011_2 (13_H)	1_0100_2 (14_H)
Black line (BK)	1_0101_2 (15_H)	0_1100_2 ($0C_H$)
Visible Line (VL)	1_0110_2 (16_H)	1_1000_2 (18_H)
Start of Even Field (SOEF)	1_1000_2 (18_H)	1_1100_2 ($1C_H$)
End of Even Field (EOEF)	1_1011_2 ($1B_H$)	0_1000_2 (08_H)

Table 12 : Mapping 8bit control codes to 5 wire output mode

Parity Checks				Comment
P_3	P_2	P_1	P_0	
✔	✔	✔	✔	Code word un-corrupted
✔	✔	✔	✘	P_0 corrupted, line code OK
✔	✔	✘	✔	P_1 corrupted, line code OK
✔	✘	✔	✔	P_2 corrupted, line code OK
✘	✔	✔	✔	P_3 corrupted, line code OK
✘	✘	✔	✘	C_0 corrupted, invert sense of C_0
✘	✔	✘	✘	C_1 corrupted, invert sense of C_1
✔	✘	✘	✘	C_2 corrupted, invert sense of C_2
All other codes				2-bit error in code word.

Table 13 : Parity Check

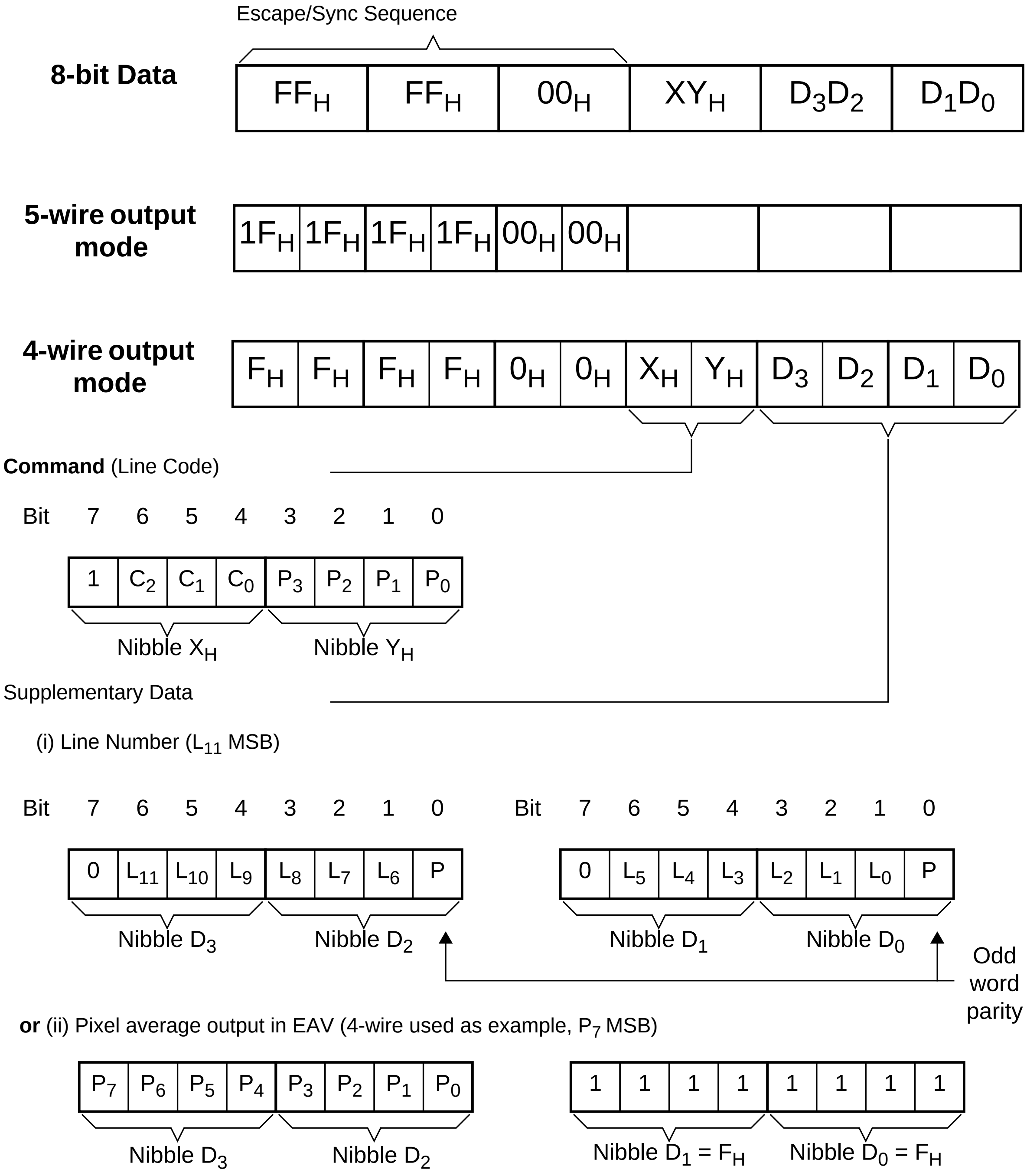


Figure 13 : Embedded Control Sequence

8.3 Video timing reference and status/configuration data

Each frame of video sequence is made up of 2 fields. Each field of data is constructed of the following sequence of data lines.

1. A start of field line

2. A number of black lines
3. A number of blank (or dark) lines
4. A number active video lines
5. An end of field line
6. A number of blank or black lines

s

Video Format	**VGA**	**QVGA**	**CIF**		
VP3 Mode	N/A	N/A	Off	On	
Extra Black Lines	N/A	N/A	N/A	On	Off
1st Field					
Start of Field Line	1	1	1	1	1
Black Lines	18	10	20	8	2
Blanking Lines	0	0	0	1	7
Dark Lines	6	6	6	0	0
Active Video lines	484	244	292	292	292
End of Field Line	1	1	1	1	1
Blanking Lines	0	0	0	0	17
Black Lines	14	0	0	17	0
Total	524	262	320	320	320
2nd Field					
Start of Field Line	1	1	1	1	1
Black Lines	18	10	20	8	2
Blanking Lines	0	0	0	1	7
Dark Lines	6	6	6	0	0
Active Video lines	484	244	292	292	292
End of Field Line	1	1	1	1	1
Blanking Lines	0	0	0	0	17
Black Lines	14	0	0	17	0
Total	524	262	320	320	320

Table 14 : Field Format

Table 14 details the number of each type of data lines for VGA, QVGA and CIF output formats. Each line of data starts with an embedded control sequence that identifies the line type (as outlined in Table 3). The control sequence is then followed by two bytes that, except in the case of the end-of-frame line, contain a coded line number. The line number sequences starts with the start-of-frame line at 00_H and increments one per line up until the end-of-frame line. Each line is terminated with an end-of-line embedded control sequence. The line start embedded sequences must be used to recognise visible data lines as a number of null bytes may be inserted between successive data lines.

There are a series of figures (Figure 14 - Figure 18) on the following pages that show line type construction of the fields in each of the available video modes in VV5500/VV6500

8.3.1 Blank lines

In addition to padding between data lines, actual blank data lines may appear in the positions indicated above. These lines begin with start-of-blank-line embedded control sequences and are constructed identically to active video lines except that they will contain only blank bytes, 07_H, (expressed as $01C_H$ in 10bit form).

8.3.2 Black line timing

The black lines (which are used for black offset calculation) are identical in structure to valid video lines except that they begin with a start-of-black line code and contain either information from the sensor black lines or blanking data.

By default VP3 mode (see mode_select[24] for details) is selected. It is an option in any of the VP3 modes to select the additional black lines to be output (line 3-8). If the VP3 mode is not selected then all the black lines are enabled - no blank lines are output.

Internally there is the concept of dark lines - to be used for dark offset cancellation (see following diagrams to identify their position within the frame timing model), however externally the dark lines share the same line type code as the black lines.

8.3.3 Padding Lines and Fields

The user may choose to extend the inter-field period by increasing the field length by writing to serial registers 97 & 98. In this event, the appropriate number of additional black or blank lines is inserted between the End Of Field (EOF) line and the Start Of Field (SOF) line. This means that the distance between SOF and EOF will remain constant.

The user can also extend the line length by writing to serial registers 82 and 83. The line length padding is inserted after the EAV sequence, ensuring that the distance between the SAV and EAV sequences will remain constant.

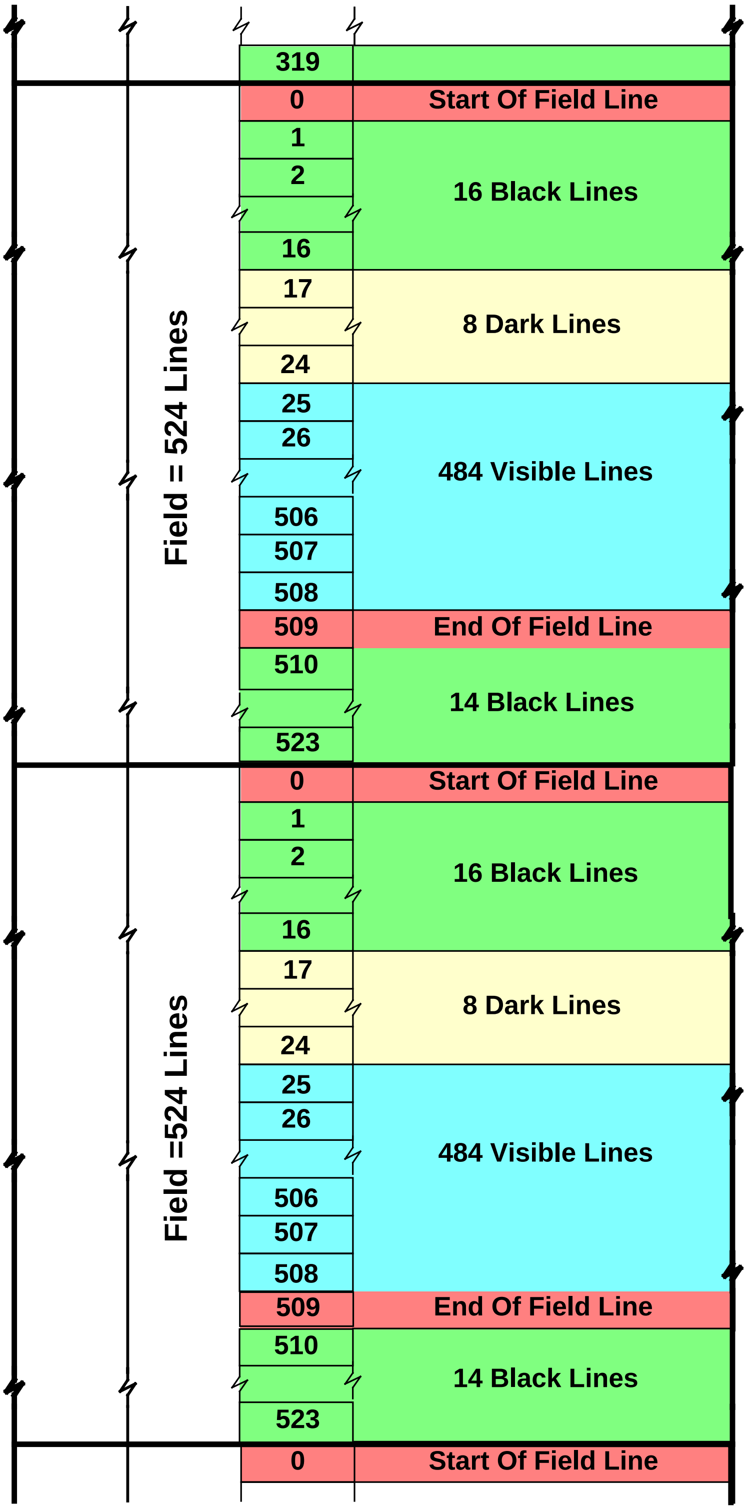


Figure 14 : VGA Field Format

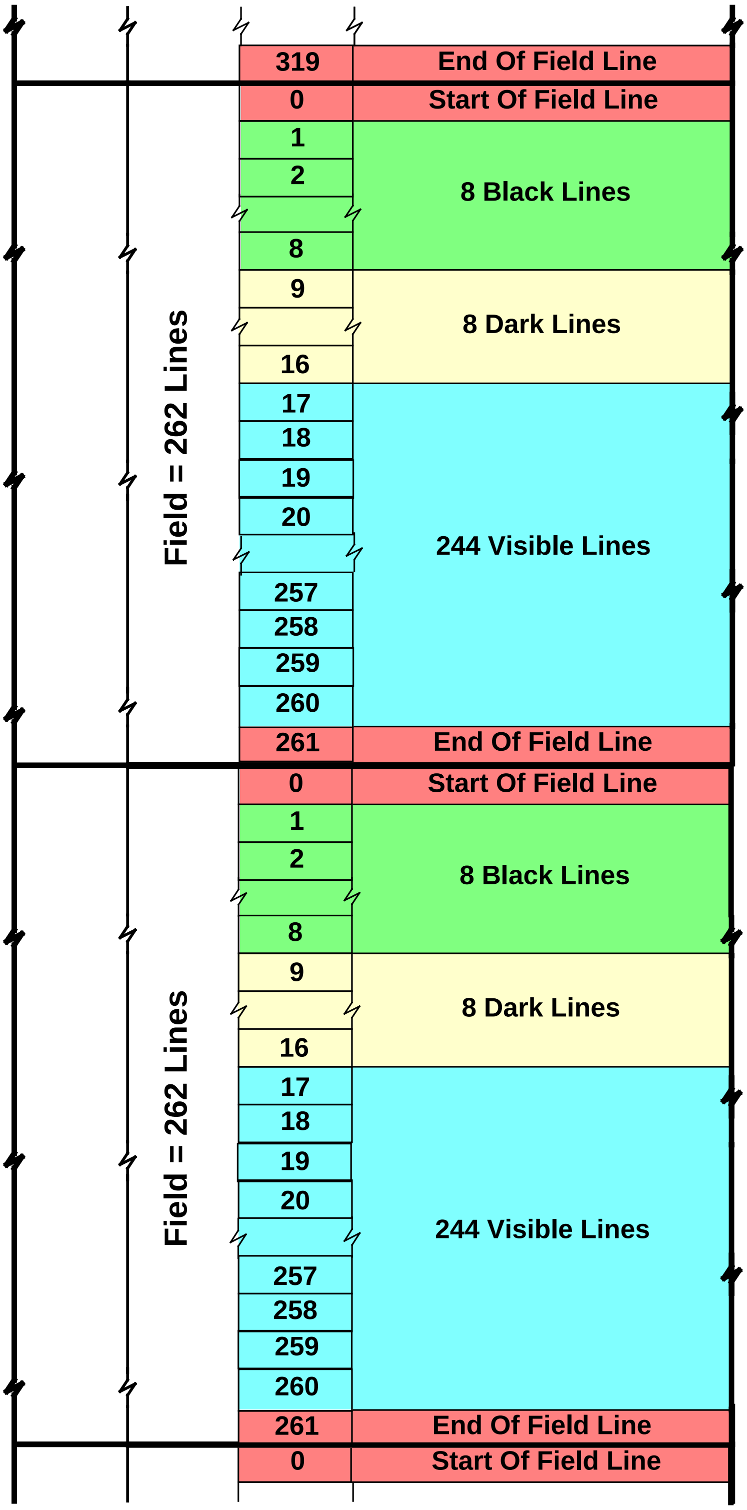


Figure 15 : QVGA Field Format

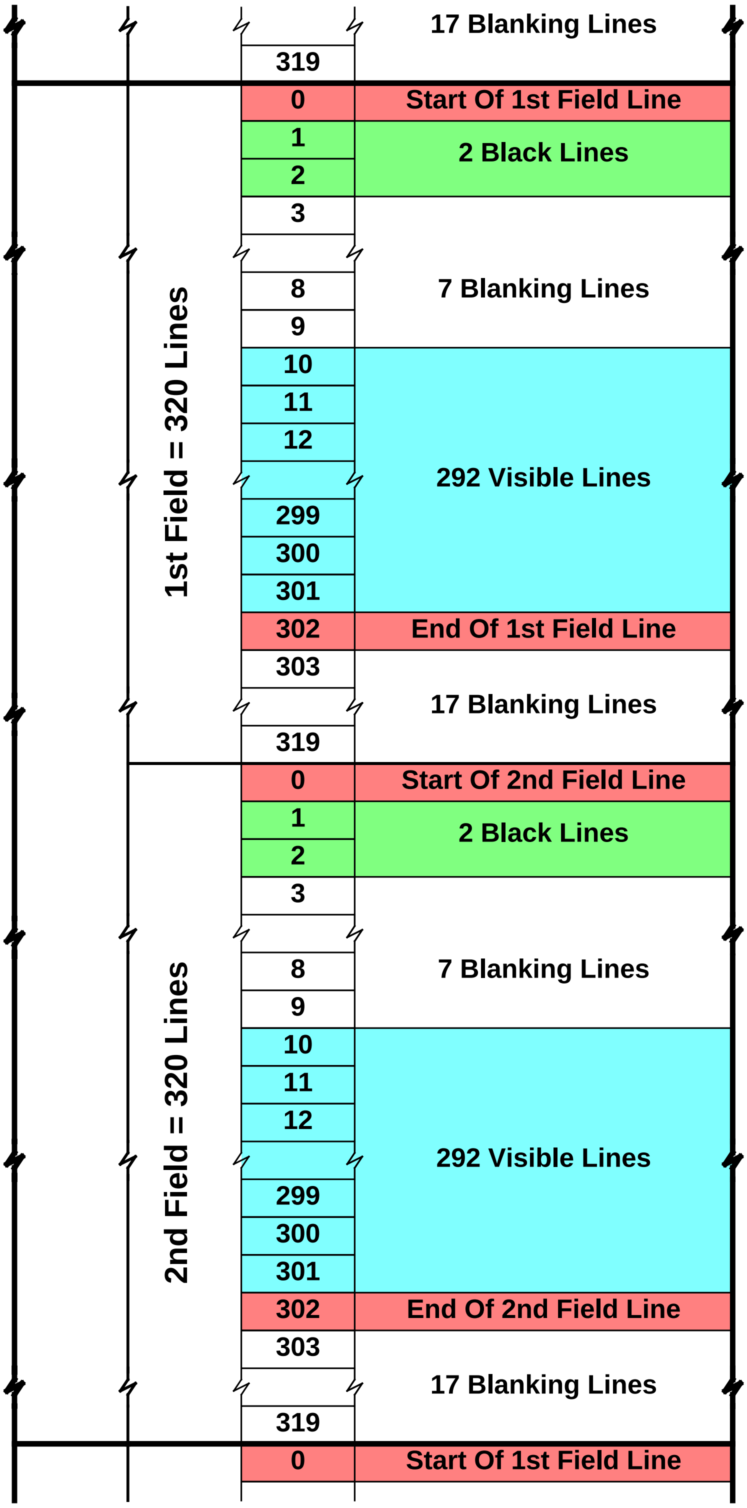


Figure 16 : CIF Field Format - VP3 Mode On, Extra Black Lines Off

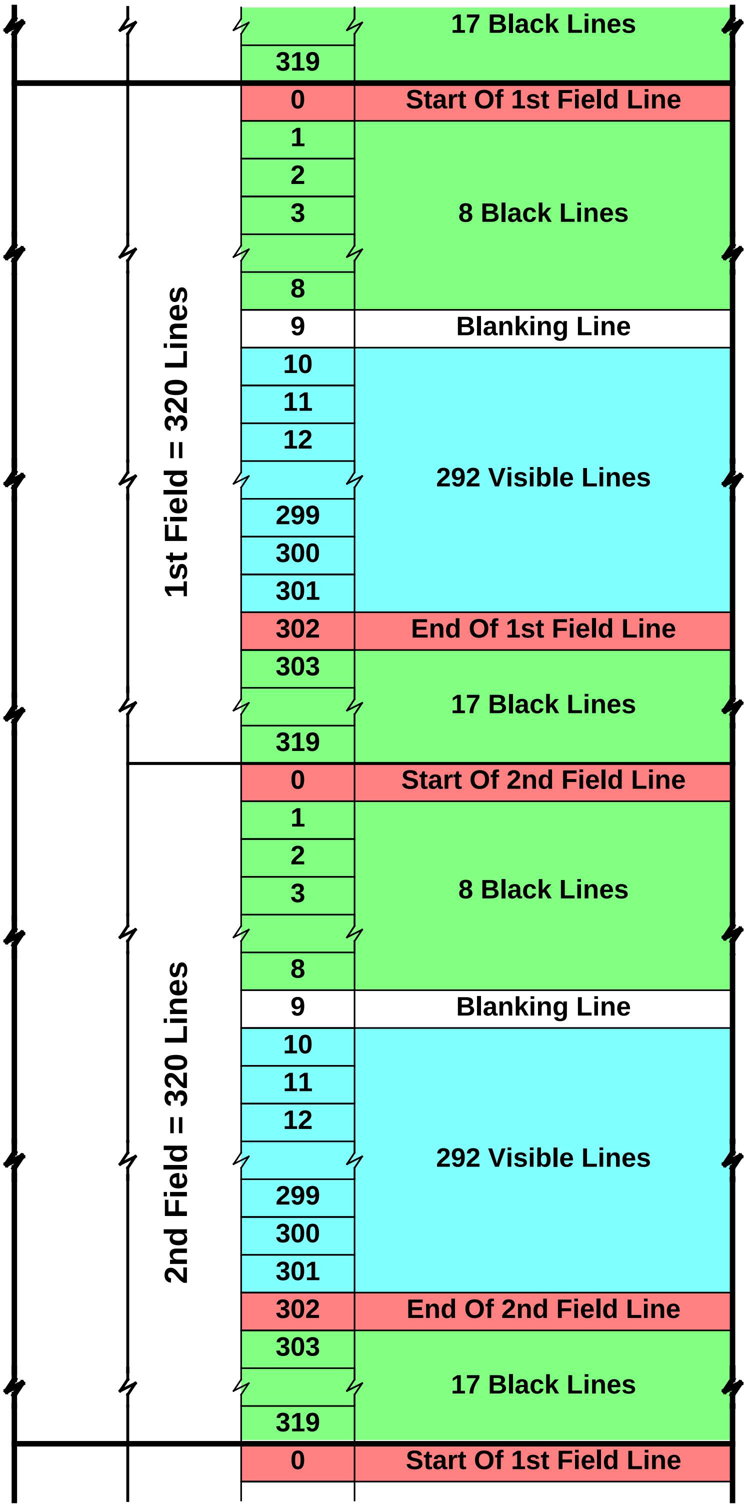


Figure 17 : CIF Field Format - VP3 Mode On, Extra Black Lines On

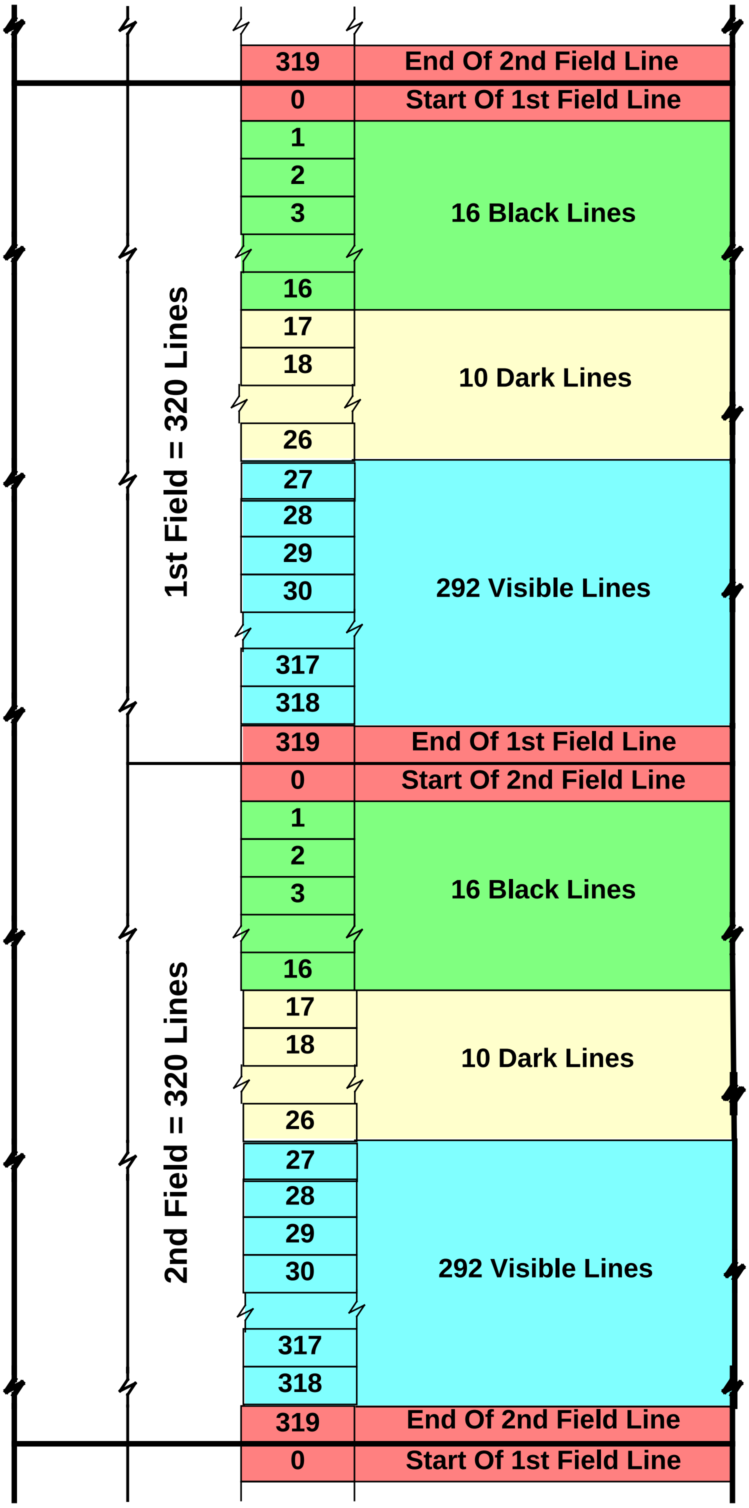
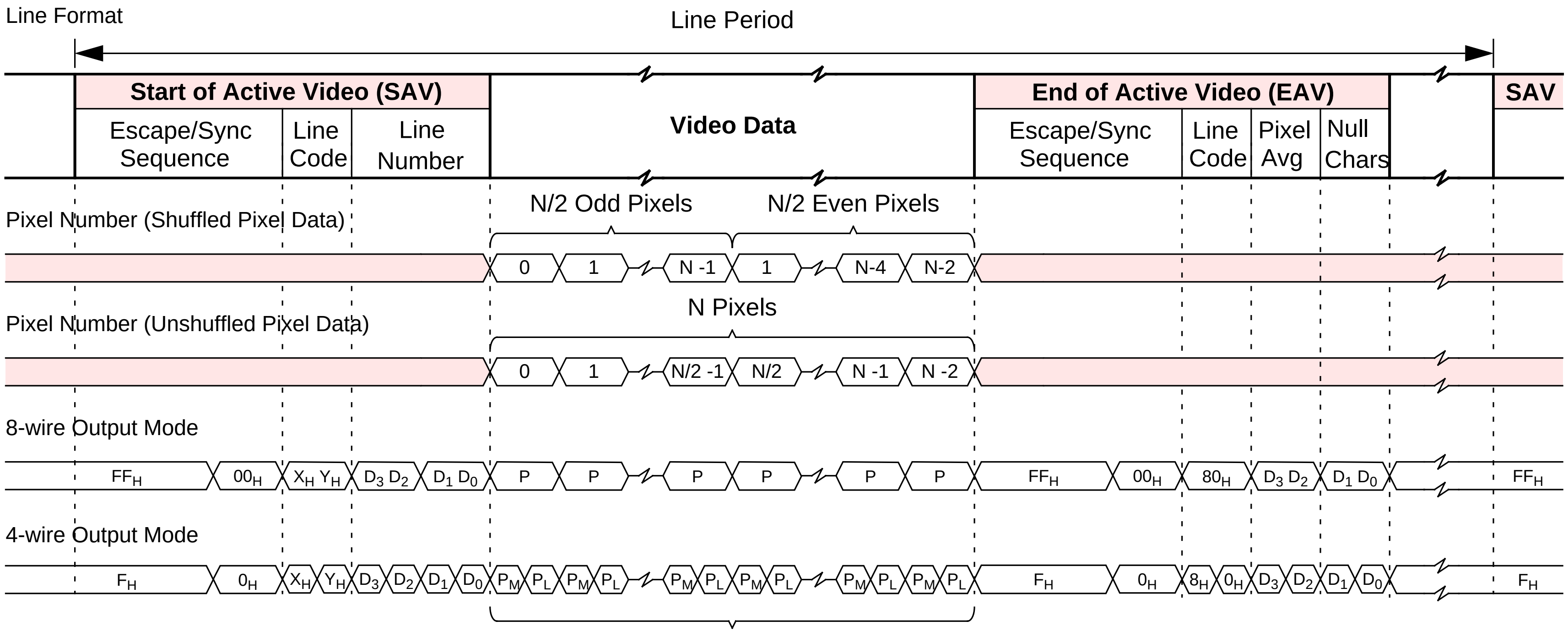


Figure 18 : CIF Field Format - VP3 Mode Off



(i)	Blanking Line (BL)	P = Blanking Level (07_H)
(ii)	Black Line (BK)	P = Valid Black Pixel Data
(iii)	Visible Line (VL)	P = Valid Pixel Data
(iv)	Start of Frame (SOF)	P = Sensor Status Data, data at pixel position 0 and 1 set to blanking level, 07_H.
(v)	End of Frame (EOF)	P = Blanking Level (07_H)

Figure 19 : Line Data Format.

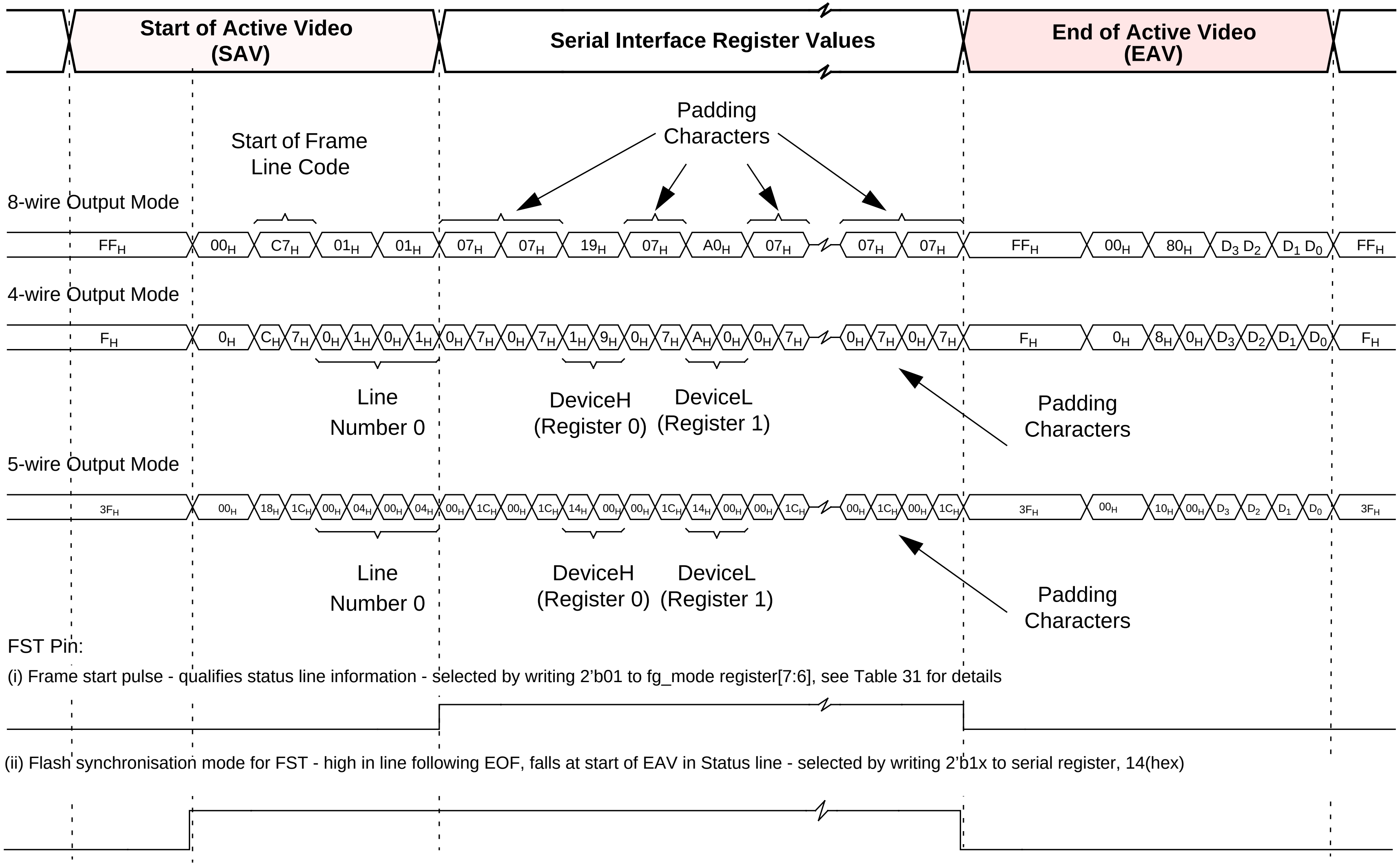


Figure 20 : Status Line Data Format and FST Signals

8.3.4 Valid video line timing

All valid video data is contained on active video lines. The pixel data appears as a continuous stream of bytes within the active lines. The pixel data may be separated from the line header and end-of-line control sequence by a number of ‘blank’ bytes (07_H).

8.3.5 Start of frame line timing

The start of frame line which begins each video field contains no video data but instead contains the contents of the serial interface register map. Immediately following the SAV sequence there are 2 padding pixels, (see Figure 20), output as blanking levels, (07_H). There will be more blanking codes output after all the serial interface registers have been output . The padding pixels continue to be output until terminated by an end-of-line control sequence. To ensure that no escape/sync characters, (the reserved FF,FF,00 sequence), appear in the sensor status/configuration information the code 07_H is output after each serial interface value.

If a serial interface register location is unused then a default value, the DeviceH register, is output. The read-out order of the registers is independent of whether the pixel read-out order is shuffled or un-shuffled.

8.3.6 End of frame line timing

The end of frame line contains no video data. Its sole purpose is to indicate the end of a frame.

8.4 Detection of sensor using data bus state

On power-up a sensor will pull all data lines high and these lines will remain high while the device is in the power up default, low power state. The device is removed from this low power mode by the I2C host writing to sensor register, setup0 [address 10_{16}]. When the device exits the low power mode it will follow a defined power up sequence, please see Figure 22 for more details. Upon completion of the power up sequence the sensor will begin streaming video.

8.5 Resetting the Sensor Via the Serial Interface

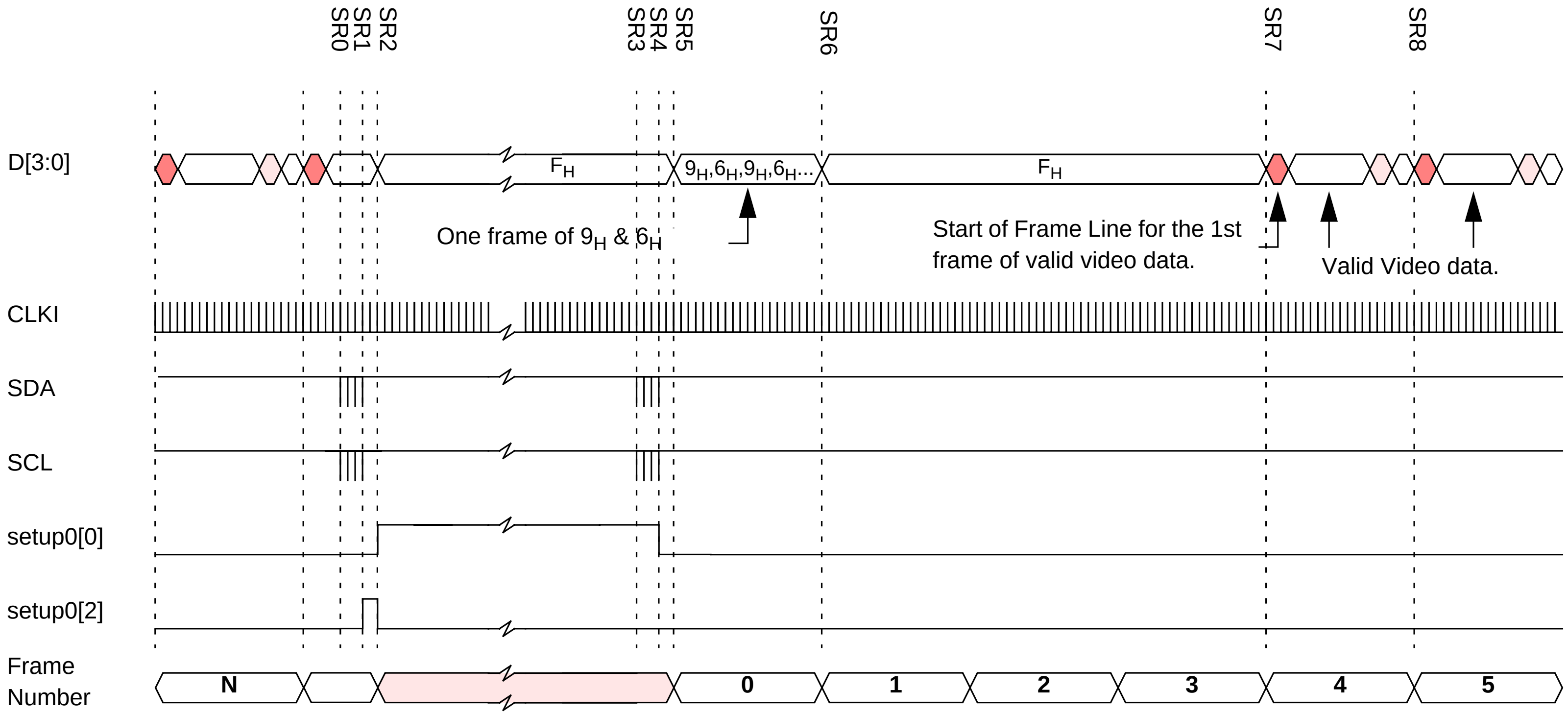
Bit 2 of setup0 register allows the VV5500/VV6500 sensor to be reset to its power-on state via the serial interface. Setting this “Soft Reset” bit causes all of the serial interface registers including the “Soft Reset” bit to be reset to their default values. This “Soft Reset” leaves the sensor in low-power mode.

8.6 Resetting the Sensor Via the RESETB pin

On power-up the RESETB pin is configured as an active low system reset which has the same effect as a soft reset issued via the serial interface as described above.

8.7 Resynchronising the Sensor Via the RESETB pin configured as SINB

Bit 5 of the pin mapping register [21] allows the RESETB pin to be re-configured as an active low (edge triggered) system synchronisation signal which will reset the video timing to the beginning of a field but will NOT reset the serial registers therefore the host does not have to reconfigure the sensor following a resynchronisation.



SR0-SR1	“Soft-Reset” Command. At the end of the command the sensor is reset and enters low-power mode.
SR2	The sensor enters low-power mode.
SR3-SR4	“Exit Low Power Mode” Command. Powers-up analog circuits and initiates the VM6500 sensor’s 4-frame start-up sequence
SR5-SR6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the video processor to determine the best sampling phase for the nibble data (D[3:0]).
SR7-SR8	4 Frames after the “Exit Low-Power mode” command, the sensor starts outputting valid video data.

Figure 21 : Resetting the VV5500/VV6500 Sensor via the Serial Interface.

8.8 Power-up, Low-power and Sleep modes

Please note that the following descriptions of low power and sleep modes assumes that the user has selected the optional 4 wire output mode, that is D[3:0] will transmit the digital video data. If the 5-wire or 8-wire modes are selected the same basic behaviour is followed however the contents of the data bus will differ slightly.

PU0	System Power Up
PU1	Sensor enters low power mode and databus bits driven high.
PU2	Host enables the sensor clock, CLKI.
PU3-PU4	The host sends a “Soft-Reset” command to the sensor via the serial interface. This ensures that the sensor is in low-power mode.
PU5	Host issues command to remove sensor from low-power mode.
PU6-PU7	Sensors begins execution 4 frame start sequence.
PU8-PU9	One frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best sampling phase for video data.
PU10-PU11	4 Frames after the “Exit Low-Power Mode” serial comms, the sensor starts outputing valid video data.

Table 15 : Typical System Power-Up

8.8.1 Power-Up/Down (Figure 22)

The sensor enters low-power mode on power-up. On power-up all of the data bus lines are driven high immediately and the device is in low-power mode (Section 8.8.2).

The sensor will remain in the low power mode until the external host sends the appropriate message over I2C to clear the low power bit - bit0 of serial reguister, setup0, index 10_{16}.

After the “Exit Low-Power Mode” command has been sent the sensor will output for one frame, a continuous stream of alternating 9_H and 6_H values on D[3:0] The patterns generated in 5 and 8 wire modes are given in Table 16 below. By locking onto the resulting 0101/1010 patterns appearing on the data bus lines the host can determine the best sampling position for the nibble data. After the last 9_H 6_H pair has been output the data bus returns to F_H,($1F_H$ in 5 wire mode), until the start of fifth frame. At this point the first active video frame will be output. After the host has determined the correct sampling position for the data, it should then wait for the next start of frame line (SOF).

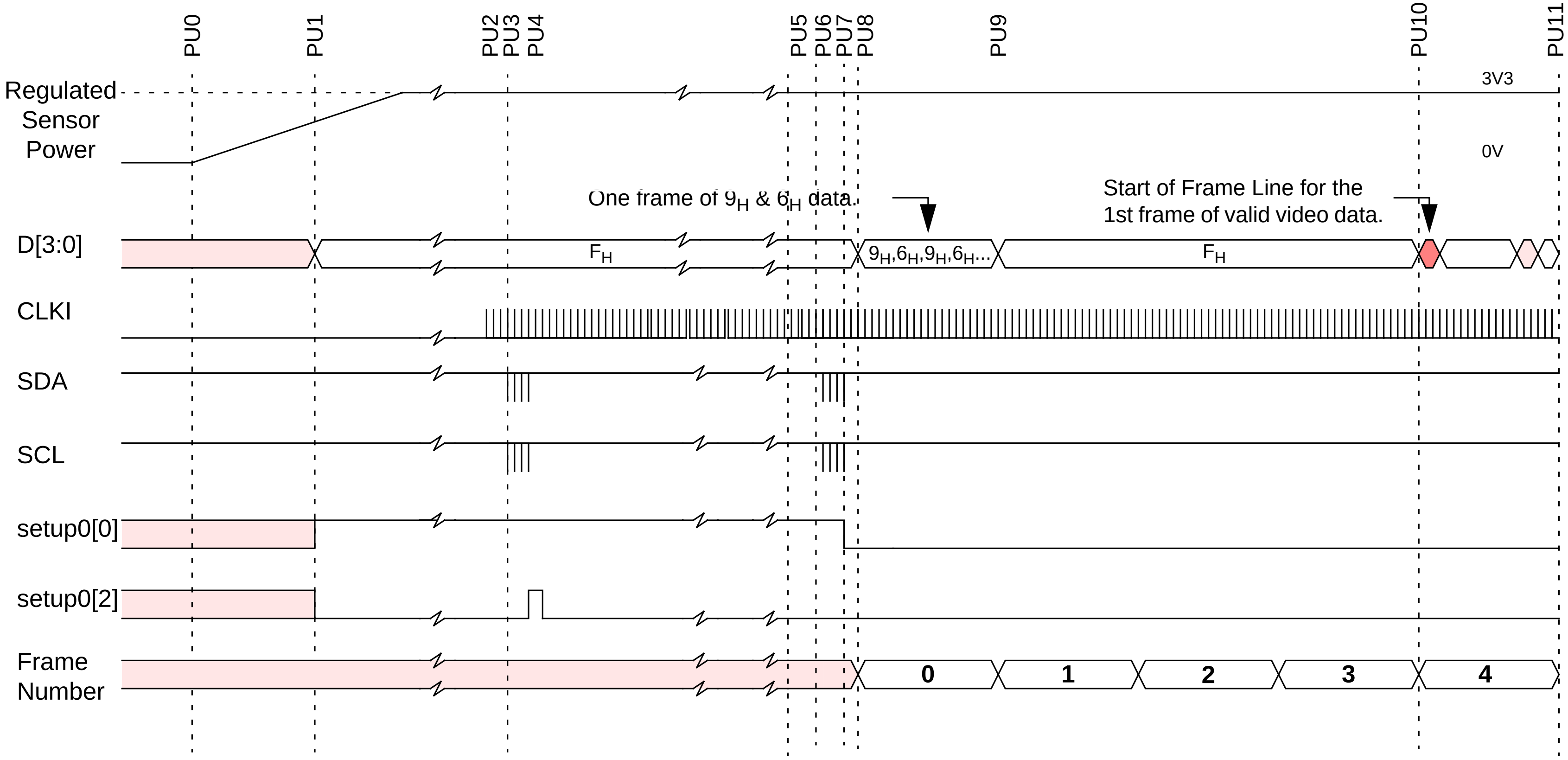


Figure 22 : Typical System Power-Up Procedure

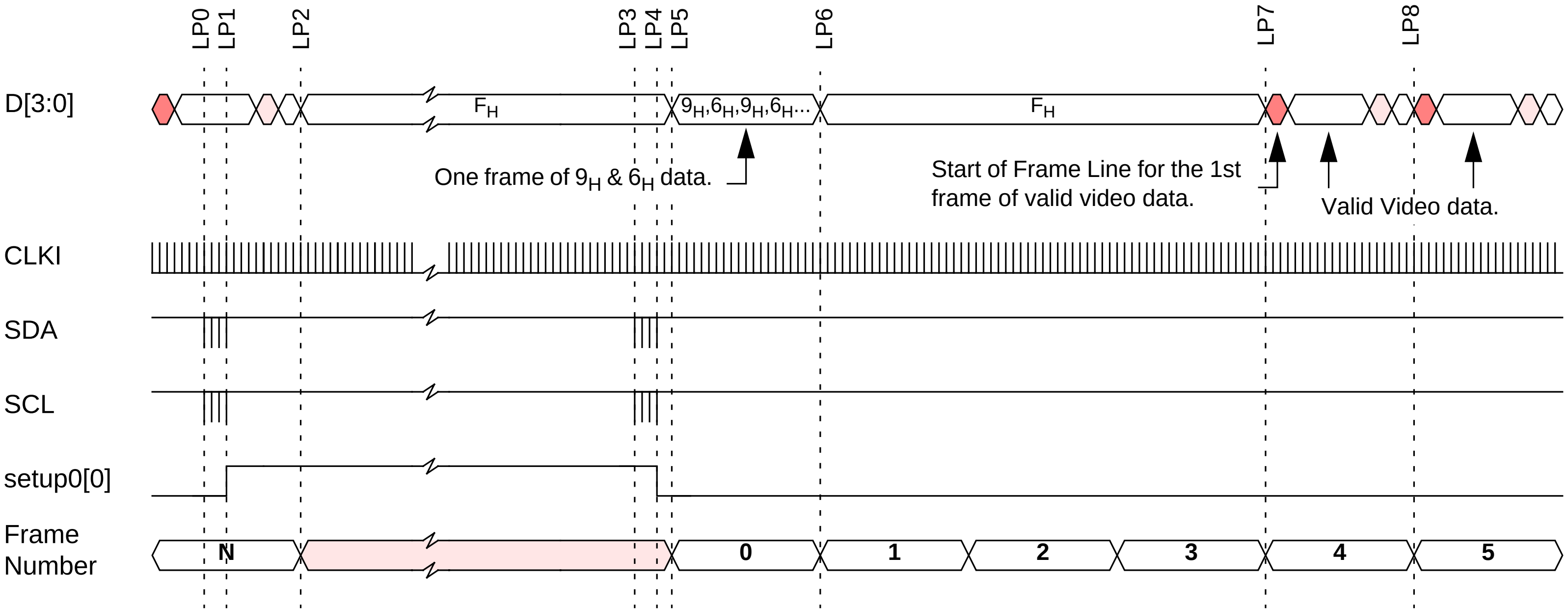
Mode	10-bit Value	Output Data Bus Pattern
4-Wire	258_H	$9_H/6_H$ ($1001_2/0110_2$)
5-Wire	136_H	$09_H/16_H$ ($01001_2/10110_2$)
8-Wire	096_H / 069H	$25_H/1A_H$ ($00100101_2/00011010_2$)

Table 16 : Output Data Bus Patterns for determination of Best Sampling Position

8.8.2 Low-Power Mode (Figure 23)

Under the control of the serial interface the sensor analog circuitry can be powered down and then repowered. When the low-power bit is set via the serial interface, all the data bus lines will go high at the end of the end of frame line of the current frame. At this point the analog circuits in the sensor will power down. The system clock must remain active for the duration of low power mode.

During low power mode only the analog circuits are powered down, the values of the serial interface registers e.g. exposure and gain are preserved. The internal frame timing is reset to the start of a video frame on exiting low-power mode. In a similar manner to the previous section, the first frame after the serial comms contains a continuous stream of alternating 9_H and 6_H - or equivalent for the alternative ouput databus widths - to allow the host to re-confirm its sampling position. Then three frames later the first start of frame line is generated.



LP0-LP1	“Enter Low Power Mode” Command.
LP2	At end of current frame, the sensor will enter the low power mode and the databus will be driven high.
LP3-LP4	“Exit Low Power Mode” Command sent to sensor - sensor begins power up sequence.
LP5-LP6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best sampling phase for the nibble data (D[3:0]).
LP7-LP8	4 Frames after the “Exit low Power Mode” command, the sensor starts outputing valid video data.

Figure 23 : Entering and Exiting Low Power Mode (example is 4wire mode).

8.8.3 Sleep Mode

Sleep mode is similar to the low-power mode, except that analog circuitry remains powered. When the sleep command is received via the serial interface the pixel array will be put into reset and the data lines all will go high at the end of the current frame. Again the system clock must remain active for the duration of sleep mode.

When sleep mode is disabled, the CMOS sensor’s frame timing is reset to the start of a frame. During the first frame after exiting from sleep mode the data bus will remain high, while the exposure value propagates through the pixel array. At the start of the second frame the first start of field line will be generated.

8.8.4 System clock status during sensor low-power modes

To allow the sensor to enter and exit the low power and sleep modes the system clock, CLKI, must be active.

8.9 Suspend mode

Under the control of the SUSPEND pin VV5500/VV6500 can be forced into an ultra low power mode. We refer to this mode as suspend mode. The sensor will consume less than 80uA of current while suspended. While the sensor is in this mode video output is turned off and no serial communications will be possible. The sensor will enter the suspend mode when a high state on the SUSPEND pin has been sampled by the system clock, CLKI, and certain critical analogue timing clocks are deemed to be in a “safe” state. This safety check is included so that the analogue circuits can be powered down in a state that preserves the critical phase relationships between the key analogue timing clocks, thus ensuring that when the sensor exits the suspend mode no reconfiguration of any sensor circuits is necessary for the device to become functional. The number of clocks that the USB host device has to send to the sensor after the SUSPEND pin has been driven high will depend upon how the clock management logic in VV5500/VV6500 has been configured. Table 17 below explains how many clocks are required by the sensor to safely enter the suspend mode. Note that where the calculation to determine the number of clocks yields a fraction of a clock period, i.e. 4.5 clocks we will round up to the next whole number of clocks, 5 clocks in this example.

Clock division		Clocks required per Video Mode		
programmed clock divisor [serial register ‘h25, bits0..3]	extra 1.5 divide	VGA	pantiltCIF	QVGA
0	✔	2	5	9
	✘	2	3	6
1	✔	5	9	18
	✘	3	6	12
2	✔	7	14	27
	✘	5	9	18
3	✔	9	18	36
	✘	6	12	24
4	✔	12	23	45
	✘	8	15	30
5	✔	14	27	54
	✘	9	18	36
6	✔	16	32	63
	✘	11	21	42

Table 17 : CLKI periods required by sensor to enter suspend mode

Clock division		Clocks required per Video Mode		
programmed clock divisor [serial register ‘h25, bits0..3]	extra 1.5 divide	VGA	pantiltCIF	QVGA
7	✔	18	36	72
	✘	12	24	48
8	✔	21	41	81
	✘	14	27	54
9	✔	23	45	90
	✘	15	30	60
10	✔	25	50	99
	✘	17	33	66
11	✔	27	54	108
	✘	18	36	72
12	✔	30	59	117
	✘	20	39	78
13	✔	32	63	126
	✘	21	42	84
14	✔	34	68	135
	✘	23	45	90
15	✔	36	72	144
	✘	24	48	96

Table 17 : CLKI periods required by sensor to enter suspend mode

The detailed timing and behaviour of the suspend mode is given in Figure 24 and Figure 25 on the following pages.

The sensor video timing machine will be reset to a video field start upon exiting suspend mode. The first video field after exiting the suspend mode will not contain valid video data as the exposure reading will have been corrupted. However the next video field and all subsequent fields will contain valid video data.

When the SUSPEND pin is driven low, removing the sensor from suspend mode, CLKI should be re-enabled. In a similar manner to exiting low-power mode, the first frame upon exiting the suspend mode contains a continuous stream of alternating 9_H & 6_H in 4-wire mode, 09_H & 16_H in 5-wire mode and 69_H & 96_H in 8-wire mode to allow the video processor to re-confirm its sampling position.

Once the host has restored the sustem clock to the sensor I2C communications can also resume. It should be noted that the serial interface register contents are maintained during the suspend mode.

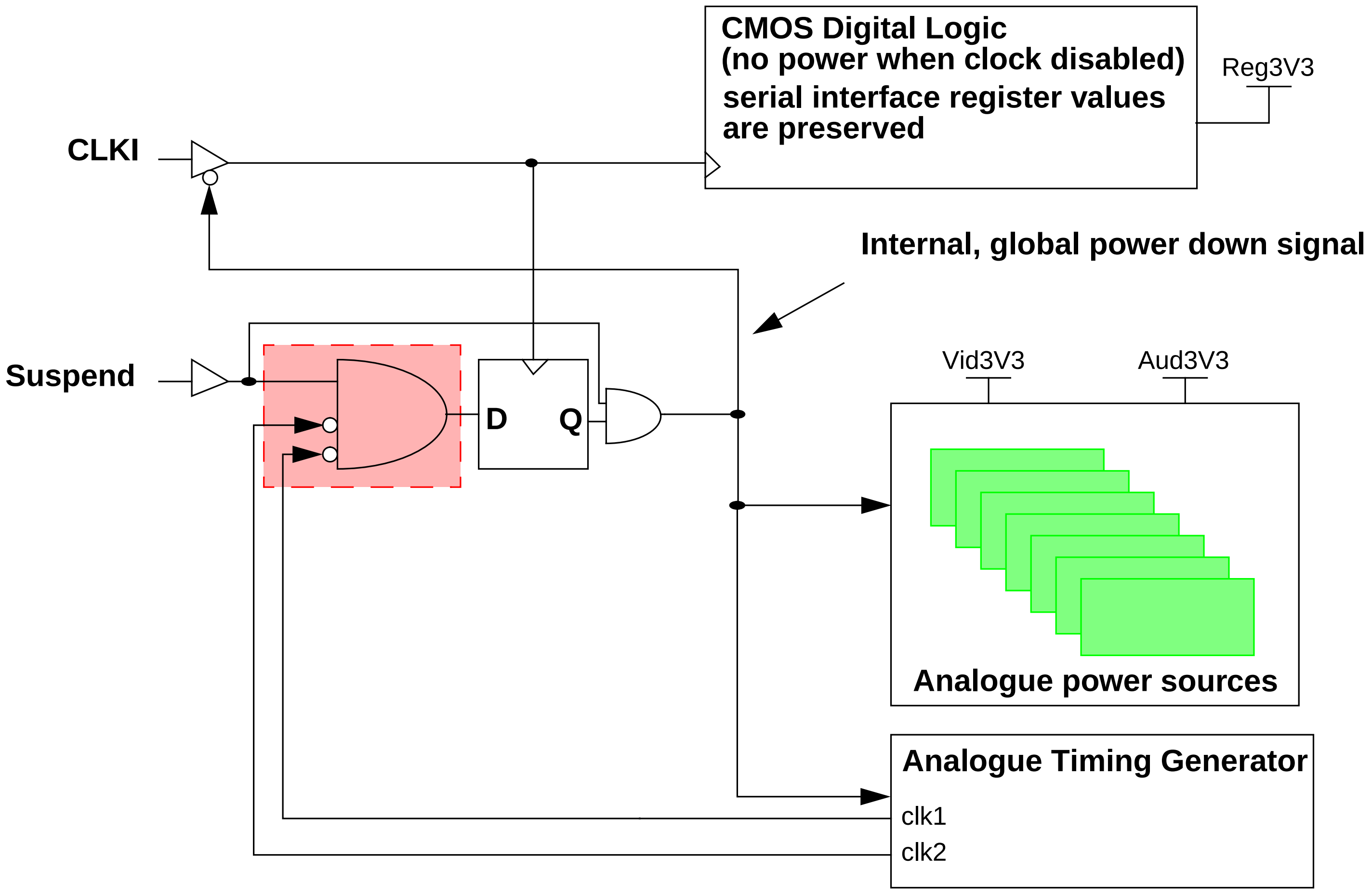
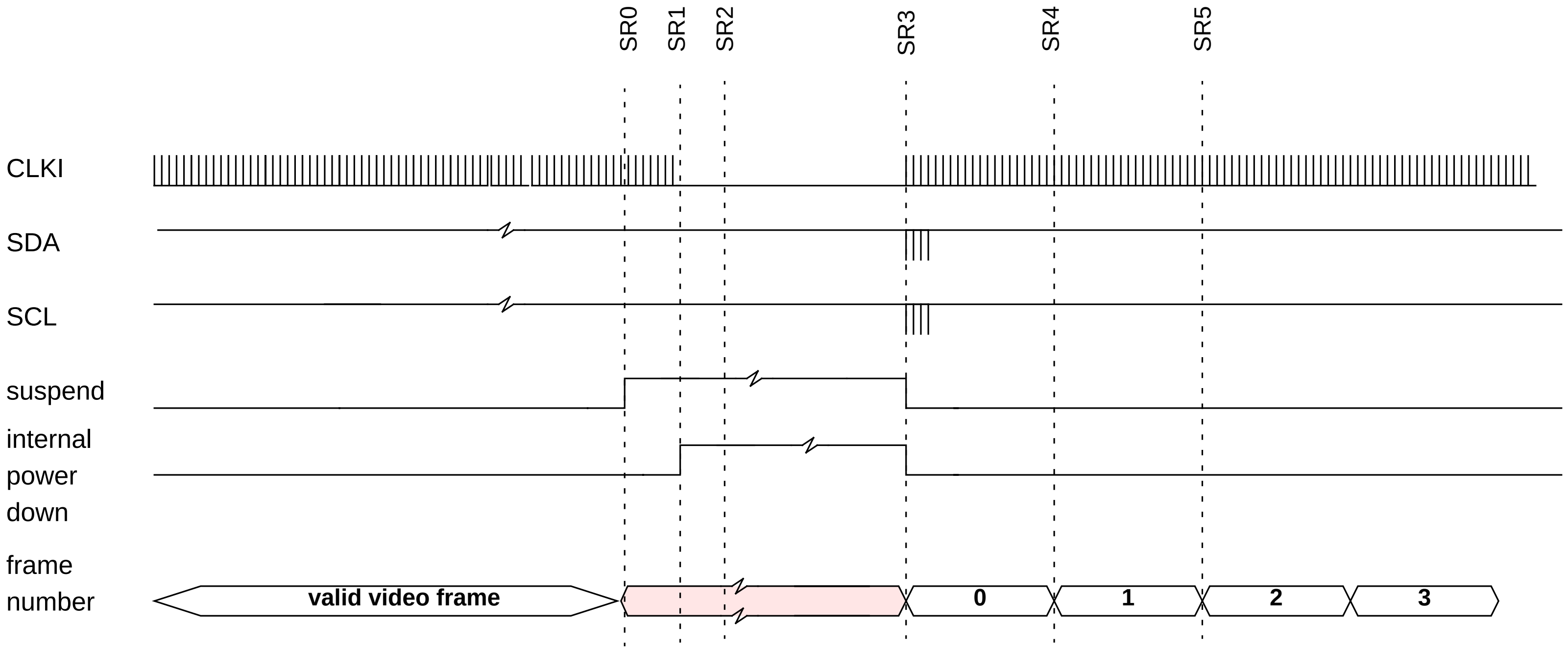


Figure 24 : Block diagram of Suspend Behaviour

The internal global power down signal disables the clock input pad. It also forces the analogue timing generator into a passive state. Finally it powers down all the analogue power sources, audio amp regulator, cab regulator, VCCS, SRAM comparator etc.

The AND gate logic that takes Suspend pin as an input also has 2 analogue timing signals as inputs. It is these signals that determine the “safe” point to enter suspend mode. Note that suspend being driven low will clear the internal power down signal.



SR0-SR1	Variable number of clock periods required to force sensor to enter suspend mode - see Table 17 Clock may be removed after this point has been reached.
SR2	Sensor will consume less than 80uA less than 7msecs after the suspend pin has been driven high (as required by meet USB1.1)
SR3	The sensor is removed from low power when the suspend pin is driven low again. The clock is applied to the sensor again. The serial interface communications can be resumed also.
SR3-SR4	1 Frame of non valid video
SR4-SR5	The first valid video frame after exiting suspend - all subsequent frames will contain valid video

Figure 25 : Entering and exiting Suspend Mode

8.9.1 Using the External Clock signal applied to CLKI

The data on the output data bus changes on the rising edge of CLKI. The delay between the video processor supplying a rising clock edge and the data on the data bus becoming valid, depends on the length of the cable between the sensor and the video processor to re-confirm its sampling position. Then one frame later the first start of frame line is generated.

8.10 Qualification of Output Data

There are two distinct ways to qualify the data nibbles appearing of the output data bus.

8.10.2 Data Qualification Clock, QCK

VV5500/VV6500 provides a data qualification clock, (see Figure 26), for the output bus There are two frequencies for the qualification clock: one runs at the nibble rate and the other at the pixel read-out rate. The falling edge of the fast QCK qualifies every nibble irrespective of whether it is most or least significant nibble. For the slow QCK, the rising edge qualifies the most significant nibbles in the output data stream and the falling edge qualifies the least significant nibbles in the output data stream.

There are 4 modes of operation of QCK.

1. Disabled (Always low - default mode of operation)
2. Free running - qualifies the entire output data stream.
3. Qualify embedded control sequences, status data, (from the SOF line), and pixel data.
4. Qualify pixel data only, (this will include data from the black lines).

The operating mode for QCK is set via the serial interface. The QCK output is tri-stated either when OEB is driven high or via the appropriate control bit in the serial interface, (see data_format register[22]).

The QCK pin can also be configured to output the state of a serial interface register bit. This feature allows the sensor to control external devices, e.g. stepper motors, shutter mechanisms.

Full details of how to configure the QCK output pin can be found in 2 registers, fg_mode[20] and pin_mapping[21].

8.10.3 Line Start Signal, LST

There are 4 modes of operation for the LST pin programmable via the serial interface, (see fg_mode[20]):

1. Disabled (Always Low- Default).
2. Free running - LST signal occurs once at the beginning of every line.
3. All lines except blanking lines are qualified by LST.
4. Only Black and Visible Lines are qualified by LST.

The LST is tri-stated either when OEB is driven high or via the appropriate control bit in the serial interface, (see data_format register[22]). The table below details the LST timing for the different video modes, (see Figure 28 for specification of t1 and t2). We assume a 24Mhz input clock.

Video Mode	t1		t2	
	pck's	us	pck's	us
VGA	48	4.003	22	1.834
pantiltCIF	19	4.75	15	3.75
pantiltQVGA/ssQVGA	12	4.003	23	7.673

8.10.4 Frame Start Signal, FST

There are 3 modes of operation for the FST pin programmable via the serial interface:

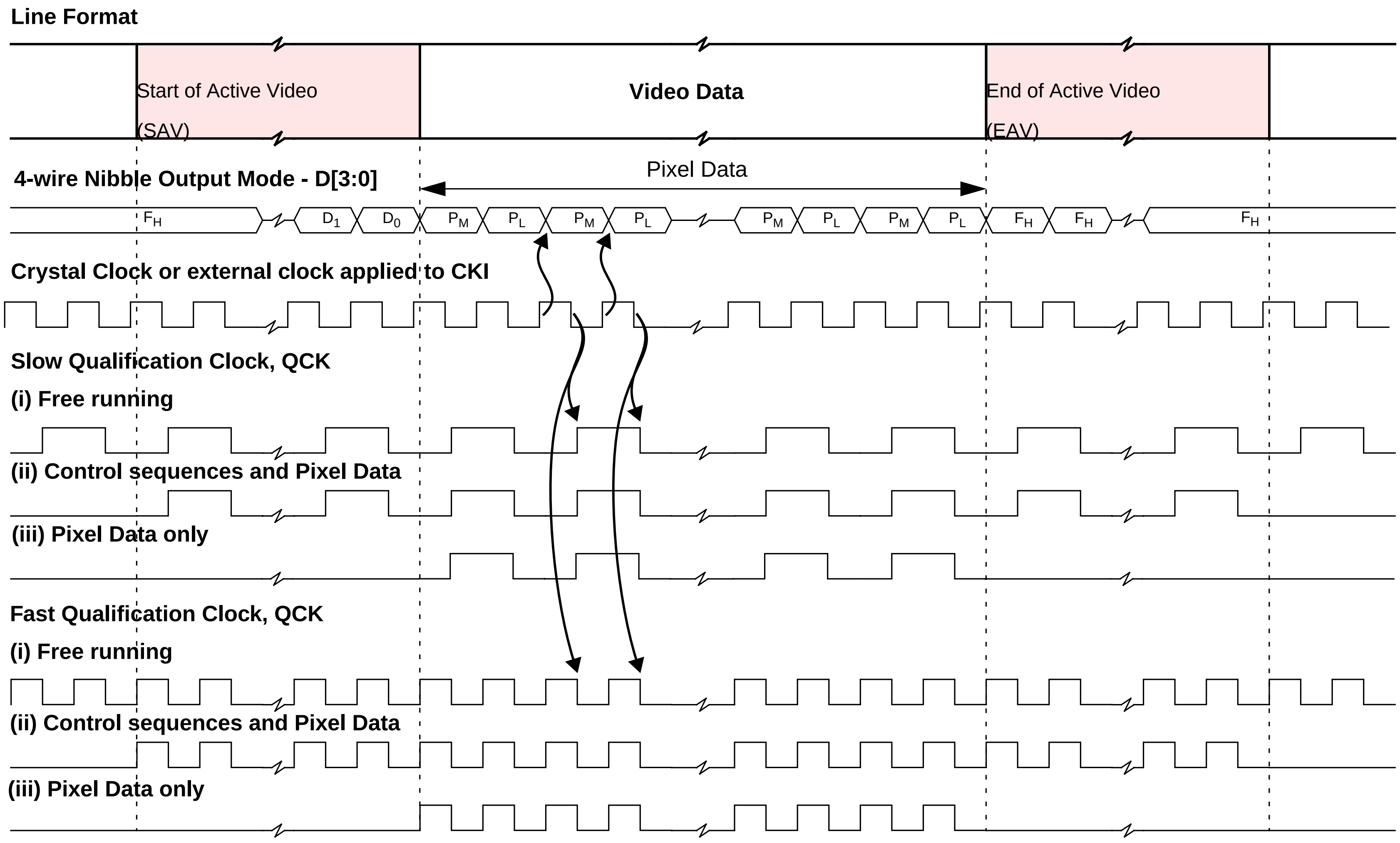
1. Disabled (Always Low- Default).
2. Frame start signal. The FST signal occurs once frame, is high for 644 pixel periods in VGA mode, (356 pixel periods in pan-

tilt CIF mode and 324 pixel periods in either QVGA mode), and qualifies the data in the start of frame line.

3. Shutter/Electronic Flash Synchronisation Signal - FST rises at the start of the video data in the first black/blank line after the EOF line and falls at the end of data in the SOF line.

The FST output is tri-stated either when OEB is driven high or via the appropriate control bit in the serial interface, (see data_format register[22]).

The configuration details for FST can be found in fg_mode register[20].



P_M = Pixel Value - Most Significant Nibble, P_L = Pixel Value - Least Significant Nibble, P = 8-bit Pixel Value

Figure 26 : Qualification of Output Data (Border Rows and Columns Enabled).

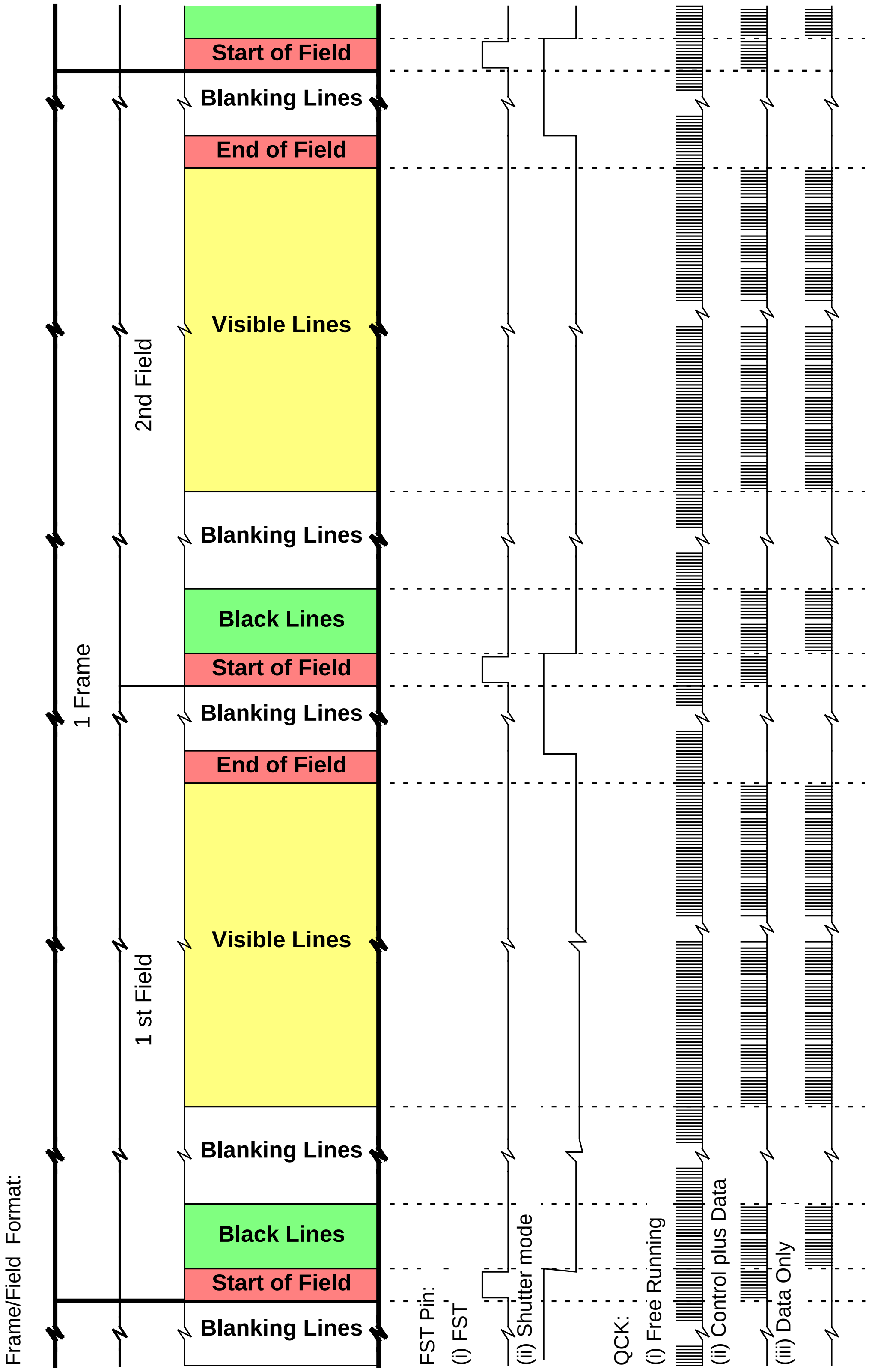


Figure 27 : Frame/Field Level Timings for FST and QCK.

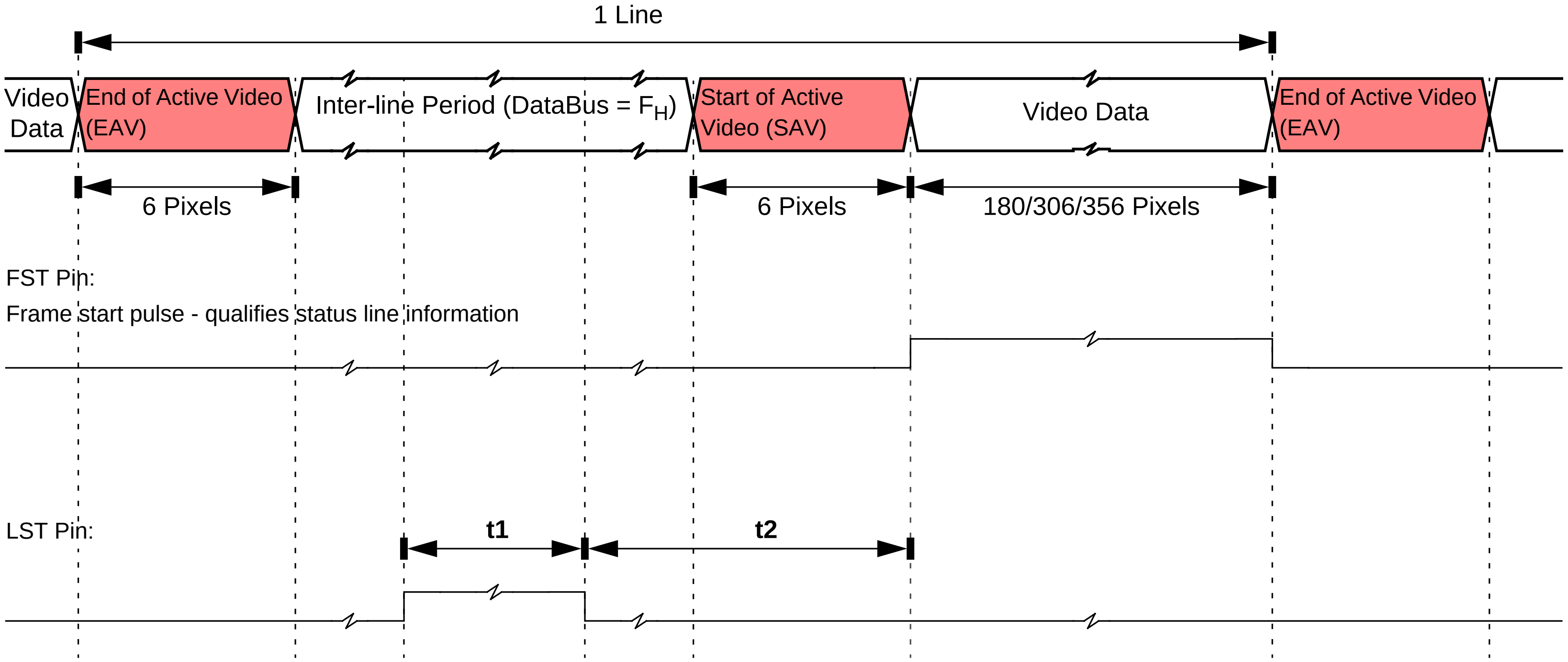


Figure 28 : Line Level Timings for FST and LST.

9. Serial Control Bus

9.1 General Description

Writing configuration information to the video sensor and reading both sensor status and configuration information back from the sensor is performed via the 2-wire serial interface.

The serial interface allows the user to communicate with a number of registers internal to the sensor. These registers store sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the receiving equipment to change their contents. Others (such as the chip id) are read only.

The main features of the serial interface include:

- Variable length read/write messages.
- Indexed addressing of information source or destination within the sensor.
- Automatic update of the index after a read or write message.
- Message abort with negative acknowledge from the master.
- Byte oriented messages.

The contents of all internal registers accessible via the serial control bus are encapsulated in each start-of-field line - see Section 8.3.5.

9.2 Serial Communication Protocol

The co- processor or host must perform the role of a communications master and the camera acts as either a slave receiver or transmitter.The communication from host to camera takes the form of 8-bit data with a maximum serial clock video processor frequency of up to 100 kHz. Since the serial clock is generated by the bus master it determines the data transfer rate. Data transfer protocol on the bus is illustrated in Figure 29.

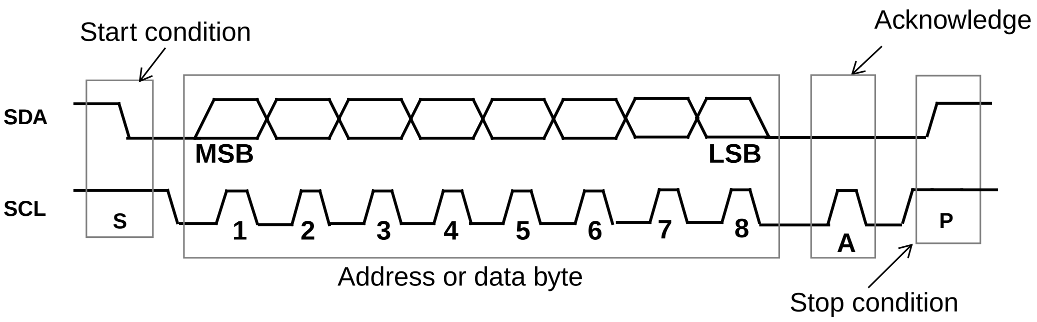


Figure 29 : Serial Interface Data Transfer Protocol

9.3 Data Format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling *sda* at a rising edge of *scl*. The external data must be stable during the high period of *scl*. The exceptions to this are *start* (S) or *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

A message contains at least two bytes preceded by a *start* condition and followed by either a *stop* or *repeated start, (Sr)* followed by another message.

The first byte contains the device address byte which includes the data direction *read,* (r), *~write*, (~w), bit. The lsb of the address byte indicates the direction of the message. If the lsb is set high then the master will read data from the slave and if the lsb is reset low then the master will write data to the slave. After the *r, ~w* bit is sampled, the data direction cannot be changed, until the next address byte with a new *r, ~w* bit is received.

0	0	1	0	0	0	0	R/W

Figure 30 : VV5500/VV6500's Serial Interface Address

The byte following the address byte contains the address of the first data byte (also referred to as the *index*). The serial interface can address up to 128, byte registers. If the msb of the second byte is set the automatic increment feature of the address index is selected.

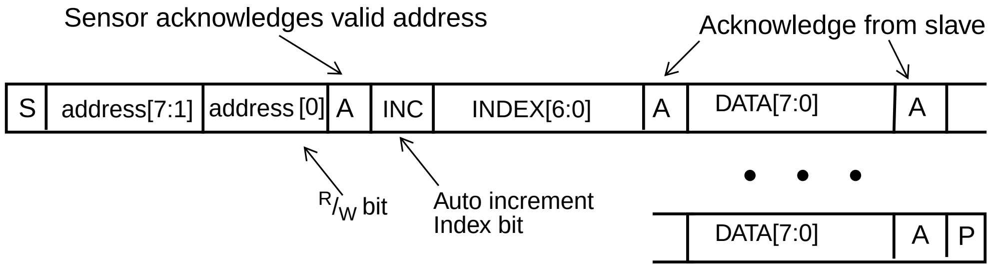


Figure 31 : Serial Interface Data Format

9.4 Message Interpretation

All serial interface communications with the sensor must begin with a *start* condition. If the *start* condition is followed by a valid address byte then further communications can take place. The sensor will acknowledge the receipt of a valid address by driving the *sda* wire low. The state of the *read/~write* bit (lsb of the address byte) is stored and the next byte of data, sampled from *sda,* can be interpreted.

During a write sequence the second byte received is an address index and is used to point to one of the internal registers. The msbit of this second byte is the *index auto increment* flag. If this flag is set then the serial interface will automatically increment the index address by one location after each slave acknowledge. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition or sends a *repeated start*, *(Sr)*. If the auto increment feature is used the master does *not* have to send address indexes to accompany the data bytes.

As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the current index is read out in the byte following the device address byte. The next byte read from the slave device are the contents of the register addressed by the current index. The contents of this register are then parallel loaded into the serial/parallel register and clocked out of the device by *scl.*

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. Although VV5500/VV6500 is always considered to be a slave device, it acts as a transmitter when the bus master requests a read from the sensor.

At the end of a sequence of incremental reads or writes, the terminal index value in the register will be one *greater* the last location read from or written to. A subsequent read will use this index to begin retrieving data from the internal registers.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

9.5 The Programmers Model

There may be up to 128, 8-bit registers within the camera, accessible by the user via the serial interface. They are grouped according to function with each group occupying a 16-byte page of the location address space. There may be up to eight such groups, although this scheme is purely a conceptual feature and not related to the actual hardware implementation, The primary categories are given below:

- Status Registers (Read Only).
- Setup registers with bit significant functions.
- Exposure parameters that influence output image brightness.
- System functions and analog test bit significant registers.

Any internal register that can be written to can also be read from. There are a number of read only registers that contain device status information, (e.g. design revision details).

Names that end with H or L denote the most or least significant part of the internal register. Note that unused locations in the H byte are packed with zeroes.

Vision sensors that include a 2-wire serial interface are designed with a common address space. If a register parameter is unused in a design, but has been allocated an address in the generic design model, the location is referred to as ***reserved***. If the user attempts to read from any of these ***reserved or unused*** locations a default byte will be read back. In VV5500/VV6500 this data is 1F$_H$. A write instruction to a reserved (but unused) location is illegal and would not be successful as the device would not allocate an internal register to the data word contained in the instruction.

A detailed description of each register follows. The address indexes are shown as decimal numbers in brackets [....] and are expressed in decimal and *hexadecimal* respectively.

Index$_{10}$	Index$_{16}$	Name	Length	R/W	Default	Comments
Status Registers - [0-15]						
0	0	deviceH	8	RO	0001_1111_2	Chip identification number including revision indicator
1	1	deviceL	8	RO	0100_0000_2	
2	2	status0	8	RO	0001_0000_2	User can determine whether timed serial interface data has been consumed by interrogating flag states
3	3	line_countH	8	RO	n/a	Current line count
4	4	line_countL	8	RO	n/a	
5	5	xendH	1	RO	503	End x coordinate of image
6	6	xendL	8	RO		
7	7	yendH	1	RO	393	End y coordinate of image
8	8	yendL	8	RO		
9	9	dark_avgH	4	RO	0	This is the average pixel value returned from the dark line offset cancellation algorithm (2's complement notation)
10	A	dark_avgL	8	RO	0	
11	B	black_avgH	4	RO	0	This is the average pixel value returned from the black line offset cancellation algorithm (2's complement notation)
12	C	black_avgL	8	RO	0	
13	D	status1	2	RO	00	Flags to indicate whether the x or y image coordinates have been clipped
14-15	E-F	unused				
Setup Registers - [16-31]						

Table 18 : Serial Interface Address Map.

Index$_{10}$	Index$_{16}$	Name	Length	R/W	Default	Comments
16	10	setup0	8	R/W	0000_1001$_2$	Low-power/sleep modes & video timing
17	11	setup1	8	R/W	1100_0000$_2$	Various parameters
18	12	sync_value	8	R/W	0001_1111$_2$	Contains pixel counter reset value used by external sync
19	13	reserved				
20	14	fg_modes	8	R/W	0000_0000$_2$	Frame grabbing modes (FST, LST and QCK)
21	15	pin_mapping	7	R/W	000_1000$_2$	FST and QCK mapping modes.
22	16	data_format	8	R/W	0000_0001$_2$	Data resolution
23	17	op_format	7	R/W	001_1000$_2$	Output coding formats
24	18	mode_select	2	R/W	01$_2$	Various mode select bits
25 - 31	19-1F	unused				
Exposure Registers - [32-47]						
32	20	fineH	2	R/W	0	Fine exposure.
33	21	fineL	8	R/W		
34	22	coarseH	2	R/W	302	Coarse exposure
35	23	coarseL	8	R/W		
36	24	analog gain	8	R/W	1111_0000	Analog gain setting
37	25	clk_div	4	R/W	0	Clock division
38-43	26-2B	reserved				
44	2C	dark offsetH	3	R/W	0	dark line offset cancellation value (2's complement notation)
45	2D	dark offsetL	8	R/W		
46	2E	dark offset setup	7	R/W	0110 0001$_2$	dark line offset cancellation enable
47	2F	reserved				
Colour Registers - [48-79]						
48 - 79	30-4F	reserved	8	R/W		
Video Timing Registers - [80-103]						
81 - 80	50-51	reserved				
82	52	line_lengthH	2	R/W	415	Line Length (Pixel Clocks)
83	53	line_lengthL	8	R/W		
84 - 86	54-56	reserved				
87	57	x-offsetH	1	R/W	149	x-co-ordinate of top left corner of region of interest (x-offset)
88	58	x-offsetL	8	R/W		
89	59	y-offsetH	1	R/W	103	y-co-ordinate of top left corner of region of interest (y-offset)
90	5A	y-offsetL	8	R/W		
91 - 96	5B-60	reserved				
97	61	field_lengthH	2	R/W	319	Field length (Lines)
98	62	field_lengthL	8	R/W		
102 - 99	63-66	reserved				
103	67	unused		R/W		
Text Overlay Registers - [104-107]						
104 - 105	68-69	reserved				
106 - 107	6A-6B	unused				

Table 18 : Serial Interface Address Map.

Index$_{10}$	Index$_{16}$	Name	Length	R/W	Default	Comments
Serial Interface Registers - [108-111]						
108 - 109	6C-6D	reserved				
110 - 111	6E-6F	unused				
System Registers - [112-127]						
112	70	black offsetH	3	R/W	- 64	black offset cancellation default value (2's complement notation)
113	71	black offsetL	8	R/W		
114	72	black offset setup	6	R/W	$0011\ 0001_2$	black offset cancellation setup
115	73	unused				
116	74	reserved				
117	75	cr0	8	R/W	$0000\ 0000_2$	Analog Control Register 0
118	76	cr1	8	R/W	$0000\ 0000_2$	Analog Control Register 1
119	77	as0	8	R/W	$0101\ 1010_2$	ADC Setup Register
120	78	at0	8	R/W	$1010\ 0000_2$	Analog Test Register
121	79	at1	8	R/W	$0000\ 0001_2$	Audio Amplifier Setup Register
122 - 125	7A-7D	unused				
126	7E	reserved				
127	7F	reserved				

Table 18 : Serial Interface Address Map.

9.5.1 Status Registers - [0 - 15],*[0-F]*

[0-1],*[0-1]* - DeviceH and DeviceL

These registers provide read only information that identifies the sensor type that has been coded as a 12bit number and a 4bit mask set revision identifier. The device identification number for VV5500/VV6500 is 500 i.e. $0001\ 1111\ 0100_2$**.** The initial mask revision identifier is 0 i.e. 0000_2**.**

Bits	Function	Default	Comment
7:0	Device type identifier	$0001\ 1111_2$	Most significant 8 bits of the 12 bit code identifying the chip type.

Table 19 : [0],*[0]* - DeviceH

Bits	Function	Default	Comment
7:4	Device type identifier	1000_2	Least significant 4 bits of the 12 bit code identifying the chip type.
3:0	Mask set revision identifier	0000_2	

Table 20 : [1],*[1]* - DeviceL

2],*[2]* - Status0

Bit	Function	Default	Comment
0	Fine exposure value update pending	0	Fine exposure value sent but not yet consumed by the sensor
1	Coarse exposure value update pending	0	Coarse exposure value sent but not yet consumed by the sensor
2	Gain value update pending	0	Gain value sent but not yet consumed by the sensor
3	Clock division update pending	0	Clock divisor sent but not yet consumed by the sensor
4	Odd/even frame	1	The flag will toggle state on alternate frames
5	Pan image parameters pending	0	Pan image parameters sent but not yet consumed by the sensor
6	Tilt image parameters pending	0	Tilt image parameters sent but not yet consumed by the sensor
7	Video timing parameter update pending flag	0	Video timing parameters sent but not yet consumed by sensor

Table 21 : [2],*[2]* - Status0

[3-4],*[3-4]* - Line_countH & Line_countL

Register Index	Bits	Function	Default	Comment
3	0	Current line count MSB	-	Displays current line count
4	7:0	Current line count LSB	-	

Table 22 : [3-4],*[3-4]* - Current Line Counter Value.

[5-6],*[5-6]* - XendH & XendL

Register Index	Bits	Function	Default	Comment
5	0	Xend msb’s	503	These registers contain the end x coordinate of the read out image size, (the x offset register contains the start x coordinate)
6	7:0	Xend ls byte		

Table 23 : [5-6],*[5-6]* - Xend

[7-8],*[7-8]* - YendH & YendL

Register Index	Bits	Function	Default	Comment
5	0	Yend ms bits	393	These registers contain the end y coordinate of the read out image size, (the y offset register contains the start y coordinate)
6	7:0	Yend ls byte		

Table 24 : [7-8],*[7-8]* - Yend

[9-12],*[9-C]* - Black_Avg & Dark_Avg

Register Index	Bits	Function	Default	Comment
9	3:0	Dark avg ms bits	0	The calculated pixel average over a series of dark lines (1,2 or 4 lines). The pixel sample size from each dark line will be image size dependent up to a maximum of 256 The average value is a signed 12 bit number
10	7:0	Dark avg ls byte	0	
11	3:0	Black avg ms bits	0	The calculated pixel average over a series of black lines (4 or 8 lines). The pixel sample size from each black line will be image size dependent up to a maximum of 256 The average value is a signed 12 bit number
12	7:0	Black avg ls byte	0	

Table 25 : [9-12],*[9-C]* - Black & Dark Averages

[13],*[D]* - Status1 Register

Bit	Function	Default	Comment
0	X image parameters clipped	0	If this bit is set then the current x offset parameter requested has caused the x coordinates to be clipped
1	Y image parameters clipped	0	If this bit is set then the current y offset parameter requested has caused the y coordinates to be clipped
7:2	unused	000000	

Table 26 : [13],*[D]* - Status1

[14-15],*[E-F]* - unused

9.5.2 Setup Registers - [16 - 31],*[10-1F]*

[16],*[10]* - Setup0

[

Bit	Function	Default	Comment
0	Low Power Mode: Off / **On**	1	Powers down the sensor array. The output data bus goes to F_H. On power-up the sensor enters low power mode.
1	Sleep Mode: **Off** / On	0	Puts the sensor array into reset. The output data bus goes to F_H.

Table 27 : [16],*[10]* - Setup0

Bit	Function	Default	Comment
2	Soft Reset **Off** / On	0	Setting this bit resets the sensor to its power-up defaults. This bit is also reset.
5:3	reserved	001	
7:5	Video Timing Mode Select	000	**000 - pantilt CIF Timing Mode** 001 - VGA Timing Modes 100 - pan/tilt/QVGA Timing Modes *If this mode is selected a QVGA size image will be output. The coordinates which define the top left corner of the QVGA portion of the array to be output are defined by the parameters in registers 88 - 91 inclusive. By default the x- and y-sizes of the output image are180 & 148 respectively.* 110 - sub-sampled QVGA Timing Modes *If this mode is selected a QVGA size image will be output. The CIF image is sub-sampled in groups of 4 to preserve the Bayer pattern with every second group of pixels & lines skipped.*

Table 27 : [16],*[10]* - Setup0

setup0 [7:5]	System Clock Divisor	Video Data	Line Length	Field Length	Data Format	Comment
000	2	356 x 292	416	320	5-wire	pan/tilt CIF
001	2	644 x 484	762	524	5-wire	VGA
010	-	-	-	-	-	reserved
011	-	-	-	-	-	reserved
100	8	324 x 244	381	262	5-wire	pan/tilt QVGA 30fps
101	-	-	-	-	-	reserved
110	8	324 x 244	381	262	5-wire	sub-sampled QVGA 30fps
111	-	-	-	-	-	reserved

Table 28 : Video Timing Modes

[17],*[11]* - Setup1

Bit	Function	Default	Comment
2:0	reserved	000	
3	Enable immediate clock division update. **Off**/On	0	Allow manual change to clock division to be applied immediately
4	Enable immediate gain update. **Off**/On	0	Allow manual change to gain to be applied immediately

Table 29 : [17],*[11]* - Setup1

Bit	Function	Default	Comment
5	Enable additional black lines (lines 3-8) **Off**/On	0	If enabled this bit will also enable the lines immediately following the end of frame line. This bit can only set/reset if the VP3 mode (ON) has been selected. In VP3 mode (OFF) operation all possible black lines are always output.
6	reserved	1	
7	Pixel read-out order (hshuffle) Unshuffled or **Shuffled**	1	It is recommended to use shuffled horizontal read-out with VV6500 sensor.

Table 29 : [17],*[11]* - Setup1

[18],*[12]* - sync_reset

Bit	Function	Default	Comment
7:0	Pixel counter reset value	31	During synchronisation the pixel counter can be reset to the known value or offset by up to 255 pck's into the pixel count sequence.

Table 30 : [18],*[12]* - sync_reset

[19],*[13]* - reserved

[20],*[14]* - fg_modes

It is likely that the user will require the QCK signal to qualify the digital video output. The folowing table describes how to this signal as well as the FST and LST outputs. Note that the slow QCKoption is selected by default.

Bit	Function	Default	Comment
1:0	FST/QCK pin modes	00	See Table 32 below for details
3:2	QCK modes	00	See Table 33 below for details
5:4	LST modes	00	See Table 34 below for details
7:6	FST modes	00	See Table 35 below for details

Table 31 : [20],*[14]* - fg_modes

fg_mode[1:0]		FST pin	QCK pin
0	0	FST	Slow QCK
0	1	FST	Fast QCK
1	0	Fast QCK$_{\textbf{note1}}$	Slow QCK
1	1	Invert of Fast QCK$_{\textbf{note1}}$	Fast QCK

Table 32 : FST/QCK Pin Selection

note1: The FST pin will always output the free running version of QCK (either inverted or normal)

fg_mode[3:2]		QCK state
0	0	Off

Table 33 : QCK Modes

fg_mode[3:2]		QCK state
0	1	Free Running
1	0	Valid during data and control period of line
1	1	Valid only during data period of line

Table 33 : QCK Modes

fg_mode[5:4]		LST pin
0	0	Off
0	1	Free Running
1	0	Output for black, video data and status lines
1	1	Output only for black and video data lines.

Table 34 : LST Modes

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fg_mode[7:6]		FST pin
0	0	Off
0	1	Normal behaviour, FST will qualify the visible pixels in the status line
1	x	Special digital stills mode. FST will be asserted at the beginning of valid data on the line following the EOF line. FST will be cleared at the end of the visible pixels in the following status line.

Table 35 : FST Modes

The option to enable the qclk during the data and control period of the line ***must not be selected if monochrome (shuffled or unshuffled) video has been selected.***

[21],*[15]* - pin_mapping

Bit	Function	Default	Comment
0	Map serial interface register bits values on to the QCK and FST pins **Off**/On	0	
1	Serial Interface Bit for QCK pin	0	
2	Serial Interface Bit for FST pin	0	
4:3	Output driver strength select	00	Default setting selects 2mA driver

Table 36 : [21],*[15]* - pin_mapping

Bit	Function	Default	Comment
5	Enable RESETB pin as SIN **Off** / On	0	On power up the RESETB pin is configured as an active low system reset which will synchronise the video timing logic and reset all serial registers to their default state. Setting this bit configures the RESETB pin as an active high system synchronisation signal (SIN) which will synchronise the video timing but will NOT reset the serial registers.
7:6	unused	0	

Table 36 : [21],*[15]* - pin_mapping

Mapping Enable	FST pin	QCK pin
0	FST	QCK
1	pin_mapping[2]	pin_mapping[1]

Table 37 : FST/QCK Pin Selection

oeb_composite	pin_map[4]	pin_map[3]	Comments
0	0	0	Drive strength = 2mA (Default)
0	0	1	Drive strength = 4mA
0	1	0	Drive strength = 6mA
0	1	1	unallocated
1	x	x	Outputs are not being driven therefore driver strength is irrelevant

Table 38 : Output driver strength selection

OEB pin	setup0[4]	oeb_composite	Comments
0	0	0	Data outputs enabled.
0	1	1	Data outputs are tri-stated by op_format[5].
1	0	1	Data outputs are tri-stated by OEB pin.
1	1	1	Data outputs are tri-stated.

Table 39 : oeb_composite generation

Note: **oeb_composite is the logical OR of setup0[4] and the OEB pin.**

[22],*[16]* - data_format

Bit	Function	Default	Comment
1:0	Unused	1	

Table 40 : [22],*[16]* - data_format

Bit	Function	Default	Comment
2	Line read-out order (vshuffle) **Unshuffled** or Shuffled	0	If the line read out is shuffled then all the even address rows will be read out first followed by all the odd address rows
3	Pixel read-out order (hmirror) **Normal** or Mirrored	0	If the pixel read out is horizontally mirrored then the columns are read out in reverse order, that is the column on the right of the sensor array will appear on the left of the displayed image and vice versa
4	Line read-out order (vmirror) **Normal** or Mirrored	0	If the line read out is vertically mirrored then the rows are read out in reverse order, that is the row at the bottom of the array will appear at the top of the displayed image and vice versa.
5	FST/LST **Enable**/Disable	0	The FST/LST digital outputs can be tri-stated but are enabled as outputs by default. The enabling/disabling of FST/LST can be retimed to a field boundary. The current state of this control bit is always available via a serial interface read, i.e. it does not have to wait to change state at a field boundary
6	QCK **Enable**/Disable	0	The QCK output can be tri-stated independently. The enabling/disabling of QCK can be retimed to a field boundary. The current state of this control bit is always available via a serial interface read, i.e. it does not have to wait to change state at a field boundary.
7	Pre clock generator divide On/**Off**	0	The CIF video mode will generate 30fps given a 16Mhz input clock. However the system will also generate 30fps if the user supplies a 24Mhz clock and enables this bit to perform an additional divide of the system clock by 1.5.

Table 40 : [22],*[16]* - data_format

[23],*[17]* - op_format

Bit	Function	Default	Comment
1:0	Data format select.	0	**00 - 5 wire parallel output** 01 - 4 wire parallel output 1x - 8 wire parallel output *Note: If the 8 wire output option has been selected then the FST and LST pins will output data bits 5 and 6 respectively, normal FST and LST function is not available*
2	Embedded SAV/EAV Escape Sequences **On /** Off	0	0 - Insert Embedded Control Sequences e.g Start and End of Active Video into Output Video data 1 - Pass-through mode. Output Video data equals ADC data.
4:3	reserved	11	
5	Tri-state output data bus **Outputs Enabled** / Tri-state	0	On power up the data bus pads are enabled by default. This bit is ORed with the OEB pin to generate the enable signal for the data pins as detailed in Table 39
6	Re-time tri-state update. **Off** / On	0	Re-time new tri-state value to a field boundary.
7	unused	0	

Table 41 : [23],*[17]* - op_format

[24],*[18]* - mode_select

This register allows the user to configure the sensor to operate with the present generation of coprocessors as well as anticipated future devices.

Bit	Function	Default	Comment
0	Coprocessor device is VP3 No/**Yes**	1	By default the sensor expects the coprocessor to be a VP3 device. If the sensor is not being used with a VP3 device then this bit should be reset. This bit controls the arrangement of black/dark/visible lines within the field. It does not alter timing.
1	Retro mode for gain application **Off**/On	0	The gain passed to the CAB comprises 2 components, IDAC[3:0] and CDAC[5:0]. If the user selects the retro mode then the IDAC value will be the inverse of the ls gain nibble. The user is barred from writing to the ms gain nibble. In the non retro mode all 8 bits are available to program. The 2 ls bits of CDAC[5:0] are fixed at 2'b11.
2	Select log CDAC ramp **Off**/On	0	By default the same CDAC value is applied for the duration of every line of every field. Setting this bit causes the CDAC value to be varied during the line.
3	Reverse CDSSIG & CDSBCK on all lines **Off**/On	0	When set, this bit causes CDSSIG & CDSBCK to be reversed on alternate lines and a chop signal to be toggled. Chop is high by default and when pulse on CDSSIG precedes CDSBCK.
4	Reverse CDSSIG & CDSBCK during black lines only **Off**/On	0	When set, this bit causes CDSSIG & CDSBCK to be reversed every 2/4 black lines (see bit [6] below).
5	Clamp CDSSIG & CDSBCK during black lines **Off**/On	0	When set, this bit causes CDSSIG & CDSBCK to be generated from the ORed versions of their default signals.
6	Number of black lines over which to loop **2 lines**/4 lines	0	
7	Inhibit capsimp operation	0	Inhibits the grounded sample and hold storage capacitor in the columns.

Table 42 : [24],*[18]* - Mode Select

[25-31],*[19-1F]* - unused

9.5.3 Exposure Control Registers [32 - 47],*[20-2F]*

There is a set of programmable registers which controls the sensitivity of the sensor. The registers are as follows:

1. Fine exposure.
2. Coarse exposure.
3. Analog gain.
4. Clock division

Note: As we know from an explanation earlier in this document (see Section 6. for further details) the exposure control registers are not updated immediately, rather they are timed to be updated at a precise point in the field timing.

The range of some parameter values is limited and any value programmed out-with this range will be clipped to the maximum currently permitted, (the fine and coarse maximum allowable settings are set by the current line and field length respectively).

Index_{10}	Index_{16}	Bits	Function	Default	Comment
32	20	0	Fine MSB exposure value	0	The maximum fine exposure is line length dependent. The expressions used to calculate the maximum fine exposure for each of the default video modes, that can be selected via Setup0 register, are as follows VGA= line length - 110 CIF = line length - 53 QVGA = line length - 49
33	21	7:0	Fine LSB exposure value		
34	22	0	Coarse MSB exposure value	318	The maximum allowable coarse exposure setting is filed length dependent. We provide the maximum coarse exposure settings for each of the standard video modes. VGA = 522 CIF = 318 QVGA = 260
35	23	7:0	Coarse LSB exposure value		
36	24	7:0	Analog gain value	1111_0000	Bits [7:4] CDAC gain control CDAC default = 63 (10-bit modes) CDAC default = 31 (9-bit modes) Bits[3:0] IDAC control, max IDAC value = 14.
37	25	3:0	Clock divisor value	0	The user can opt to slow the internal clocks down form their default settings and extend the effective exposure period. Table 10 describes the range of clock divisors that may be selected.

Table 43 : Exposure Reated Registers

Clock Divisor Setting	Pixel Clock Divisor
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7

Table 44 : Clock Divisor Values

Clock Divisor Setting	Pixel Clock Divisor
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

Table 44 : Clock Divisor Values

[38-43],*[26-3B]* - reserved

[44 - 45] - Dark Pixel Offset

Bit	Function	Default	Comment
2:0	MS Dark line pixel offset	0	This register contains a fixed offset that can be applied to the digitised pixels in the digital output coding block. The offset is a 2's complement number, giving an offset range -1024,+1023. If this external offset cancellation is to be applied then it register[46], bits[1:0] should be reprogrammed to 2'b1x.
7:0	LS Dark line pixel offset		

Table 45 : [44 - 45],*[3C-3D]* - Dark Pixel Offset

[46],*[3E]* - Dark Pixel Cancellation Setup Register

Bit	Function	Default	Comment
1:0	Dark line offset cancellation	01	x0 - Accumulate dark pixels, calculate dark pixel average and report, but don't apply anything to data stream **01** - Accumulate dark pixels, calculate dark pixel average and report and apply internally calculated offset to data stream 11 - Accumulate dark pixels, calculate dark pixel average and report, but apply an externally calculated offset
2	Number of dark lines used **All dark lines**/Use half the number of dark lines.	0	The number of dark lines form the sensor array used to calculate the dark offset cancellatiuon varies from video mode to video mode, the user can opt to only select half of these lines on which to base the algorithm.
5:3	reserved		
6	Use narrow dark offset deadband **Yes**/No	1	The deadband describes a range of dark pixel averages that will force the leaky integrator algorithm to hold it's current value. 0 - Target +/- 4 codes 1 - Target +/- 2 codes
7	unused	0	

Table 46 : [46],*[3E]* - Dark Pixel Cancellation Setup Register

47],*[3F]* - reserved

[48-79],*[30-4F]* - reserved

9.5.4 Video Timing Registers [80 - 103],*[50-67]*

Indexes in the range [80 - 103] control the generically named video timing registers, including the image pan/tilt parameters and line & field length of the sensor. The registers are as follows:

1. line length.

2. x-offset of region of interest.
3. y-offset of region of interest.
4. frame length.

The length of a line is specified in a number of pixel clocks, whereas the length of a field is specified in a number of lines.

The range of some parameter values is limited and any value programmed out-with this range will be clipped to the maximum allowed. The x-offset and y-offset are only programmable if the user has selected the pan tilt QVGA mode. If the other video modes are selected then the x-offset and y-offset registers will have pre-programmed values applied, but they cannot be changed. The x-offset and y-offset default values are chosen such that the output image, regardless of video mode selected, will be centered within the pixel array, (see Section 3.2 for details).

Index_{10}	Index_{16}	Bit	Function	Default	Comment
81 - 80	50-51		reserved		
82	52	1:0	Line Length MSB value	415	Minimum mode dependent Maximum = 1023 Actual line duration in pixel periods is line length programmed +1.
83	53	7:0	Line Length LSB value		
84 - 86	54-56		reserved		
87	57	0	x-offset MSB value	149	Minimum (positive) value = 1
88	58	7:0	x-offset LSB value		
89	59	0	y-offset MSB value	103	Minimum (positive) value = 1
90	5A	7:0	y-offset LSB value		
91 - 96	5B-60		reserved		
97	61	1:0	Field Length MSB value	319	Minimum mode dependent Maximum = 1023 Actual field duration in line periods is field length programmed +1.
98	62	7:0	Field Length LSB value		
102 - 99	63-66		reserved		

Table 47 : Video Timing Registers

[103],*[67]* - unused

[104-105],*[68-69]* - reserved

[106-107],*[6A-6B]* - unused

[108-109],*[6C-6D]* - reserved

[110-111],*[6E-6F]* - unused

9.5.5 System Registers -Addresses [112 - 127],*[70-7F]*

This page of the serial interface I2C address space comprises a wide range of registers including the registers required to control the black offset cancellation algorithm, enable test modes and also control various aspects of the analogue behavior of the sensor.

[112 - 113],*[70-71]* - Black Pixel Offset

Bit	Function	Default	Comment
2:0	MS Black line pixel offset	- 64	This register contains a fixed offset that can be applied to the digitised pixels in the digital output coding block.The offset is a 2's complement number, giving an offset range -1024,+1023. If this external offset cancellation is to be applied then it register[114], bits[1:0] should be reprogrammed to 2'b1x.
7:0	LS Black line pixel offset		

Table 48 : [112 - 113],*[70-71]* - Black Pixel Offset

[114],*[72]* - Black Pixel Cancellation Setup Register

Bit	Function	Default	Comment
1:0	Black line offset cancellation	01	00 - Accumulate black pixels, calculate black pixel average and report, but don't apply anything to data stream **01** - Accumulate black pixels, calculate black pixel average and report and apply internally calculated offset to data stream 1x - Accumulate black pixels, calculate black pixel average and report, but apply an externally calculated offset
4:2	reserved	100	The time constant controls the rate at which a change in the black level is corrected for.
5	Use narrow black offset deadband **Yes**/No	1	The deadband describes a range of pixel averages that will cause the leaky integrator algorithm to hold it's current value. 0 - Target +/- 4 codes 1 - Target +/- 2 codes
7:6	Black offset to be applied	00	00 - Apply offset during all black and image lines 01 - Apply offset during image lines only 10 - Apply additional offset of 64 during black lines only. Apply offset as normal during image lines. 11 - Apply additional offset of 128 during black lines only. Apply offset as normal during image lines.

Table 49 : [114],*[72]* - Black offset cancellation setup

[115],*[73]* - unused

[116],*[74]* - reserved

[117 - 118],*[75-76]* - Control Registers 0 and 1- CR0 and CR1

Although we give the user access to the following 5registers it is not anticipated that the contents of these registers will have to be altered. If the user does wish to alter any of the register bits then they are strongly advised to contact VIBU before doing so.

Bit	Function	Default	Comment
0	Enable bit line clamp **Off**/On	0	
1	Enable bit line test **Off**/On	0	
3:2	Bit line white reference **1.5 V** / 1.1 V / 0.7V / Ext.	00	00 - 1.5V 01 - 1.1V 10 - 0.7V 11 - External
4	Enable anti blooming **Off**/On	0	
5	Power Down - LVDS input comparator **Off**/On	0	Powers down LVDS input. CMOS clock input may still be used.
6	Power Down - SRAM **Off**/On	0	Powers down SRAM comparator
7	Power Down - VCCS **Off**/On	0	Powers down voltage controlled current source

Table 50 : [117],*[75]* - Control Register CR0

Bit	Function	Default	Comment
0	Stand-by **Off**/On	0	Powers down ALL analog circuitry with the exception of the band gap
1	Power Down - Internal Ramp Generator **Off**/On	0	
2	Power Down - Column ADC **Off**/On	0	Powers down preamp and comparators
3	Power Down - CAB regulator **Off**/On	0	Referred to in figures as pd_creg
4	Power Down - Audio Amplifier regulator **Off**/On	0	Referred to in figures as pd_areg
5	Power Down - VRT Amplifier **Off**/On	0	Allows external VRT to be applied
6	Ramp common mode voltage **VRT-vtn**/1.5V	0	0 - VRT-vtn ramp common mode voltage 1- 1.5V ramp common mode voltage
7	Current boost to column comparator **75uA**/50uA	0	0 - 75uA 1- 50uA

Table 51 : [118],*[76]* - Control Register CR1

119]*[77]* - ADC Setup Register AS0

Bit	Function	Default	Comment
1:0	reserved	10	
2	Enable voltage doubler **Off**/On	0	It is recommended that this bit is set if the sensor is being used in a 3.3V supply environment
3	Differential ramp enable Off/**/On**	1	Ramp generator signal bpramp
4	view column/view vcmtcas **vcmtcas**/column	1	0 - view column voltage Vx[651] 1- view vcmtcas
5	ramp viewing/column comparator test **ramps**/test comparator	0	0 -view ramps on CPOS/CNEG 1- input to test comparator 652
6	Stepped Ramp Enable Off/**On**	1	Setting this bit enables a stepped ramp. Clearing this bit enables a continuous ramp.
7	unused	0	

Table 52 : [119],*[77]* - ADC Setup Register AS0

[120],*[78]* - Analog Test Register AT0

Bit	Function	Default	Comment
0	SRAM test enable **Off**/On	0	
2:1	VRT Voltage **2.2 V** / 2.6 V / 3.0V / Ext.	00	**00** - VRT = 2.2V 01 - VRT = 2.6V 10 - VRT = 3.0V 11 - External (must bond VRTref)
4:3	LineInt & ReadInt phasing	00	**00**- 0 degree phase delay 01 - 90 degree phase delay 10 - 180 degree phase delay 11 - 270 degree phase delay
7:5	reserved	101	

Table 53 : [120],*[78]* - Analog Test Register AT0

[121],*[79]* - Audio Amplifier Setup Register AT1

Bit	Function	Default	Comments
0	First stage gain	1	0 - 0dB 1 - 30dB
1	Second stage gain[1]	0	gain[1] gain[0] - gain(dB) 0 0 - 0dB 0 1 - 6dB 1 0 - 12dB 1 1 - 18dB
2	Second stage gain[0]	0	
3	Power Down	0	0 - Powered up 1 - Power down
4	Output Select	0	0 - Single ended 1 - Differential
5	Current Boost	0	0 - 1mA output drive in output buffers 1 - 2mA output drive in output buffers
7:6	Unused	00	

Table 54 : [121],*[79]* - Audio Amplifier Setup Register AT1

[122-125],*[7A-7D]* - unused

[126-127],*[7E-7F]* - reserved

9.6 Types of messages

This section gives guidelines on the basic operations to read data from and write data to the serial interface.

The serial interface supports variable length messages. A message may contain no data bytes, one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available are detailed below.

- Write no data byte, only sets the index for a subsequent read message.
- Single location data write or read for monitoring (real time control)
- Multiple location read or write for fast information transfers.

Examples of these operations are given below. A full description of the internal registers is given in the previous section. For all examples the slave address used is 32_{10} for writing and 33_{10} for reading. The write address includes the read/write bit (the lsb) set to zero for device writes and set to one for device reads.

9.6.1 Single location, single data write.

When a random value is written to the sensor, the message will look like this:

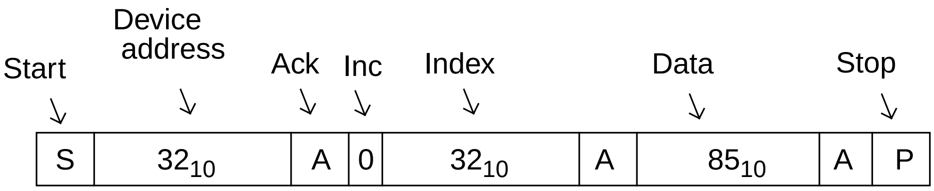

Figure 32 : Single location, single write.

In this example, the *fineH* exposure register (index = 32_{10}) is set to 85_{10}. The r/w bit is set to zero for writing and the *inc* bit (msbit of the index byte) is set to zero to disable automatic increment of the index after writing the value. The address index is preserved and may be used by a subsequent read. The write message is terminated with a stop condition from the bus master.

9.6.2 Single location, single data read.

A read message always contains the index used to get the first byte.

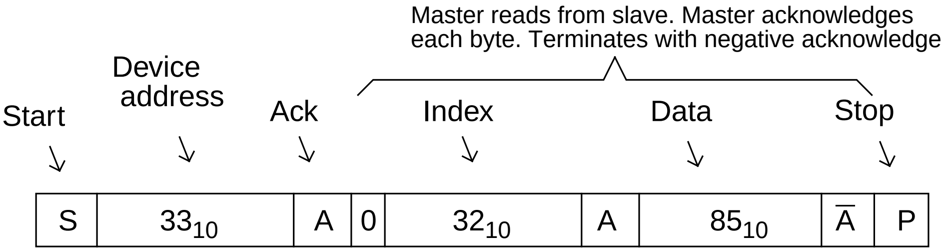

Figure 33 : Single location, single read.

This example assumes that a write message has already taken place and the residual index value is 32_{10}. A value of 85_{10} is read from the *fineH* exposure register. Note that the read message is terminated with a negative acknowledge ($\overline{A}$) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the *sda* line cannot rise, which is part of the stop condition.

9.6.3 No data write followed by same location read.

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master a repeated start condition is asserted between the write and read messages, i.e. no stop condition is asserted. In this example, the *gain* value (index = 36_{10}) is read as 15_{10}:

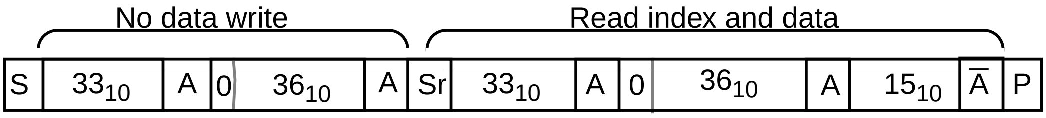

Figure 34 : No data write followed by same location read.

As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

9.6.4 Same location multiple data write.

It may be desirable to write a succession of data to a common location. This is useful when the status of a bit (e.g. auto-load) must be toggled.

The message sequence indexes *sf_setup* register 108. If bit 0 is toggled high, low this will initiate a fresh auto-load. This is achieved by writing two consecutive data bytes to the sensor. There is no requirement to re-send the register index before each data byte.

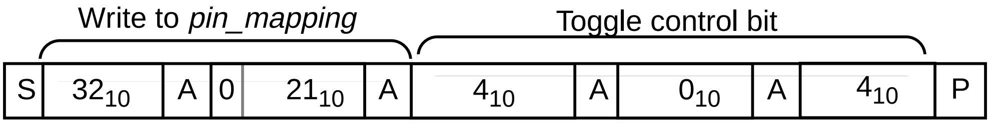

Figure 35 : Same location multiple data write.

9.6.5 Same location multiple data read

When an exposure related value (*fineH, fineL, coarseH, coarse* L, *gain or clk_div*) is written, it takes effect on the output at the beginning of the next video frame, (remember that the application of the *gain* value is a frame later than the other exposure parameters). To signal the consumption of the written value, a flag is set when any of the exposure or gain registers are written and is reset at the start of the next frame. This flag appears in *status0* register and may be monitored by the bus master. To speed up reading from this location, the sensor will repeatedly transmit the current value of the register, as long as the master acknowledges each byte read.

In the below example, a *fineH* exposure value of 0 is written, the status register is addressed (no data byte) and then constantly read until the master terminates the read message.

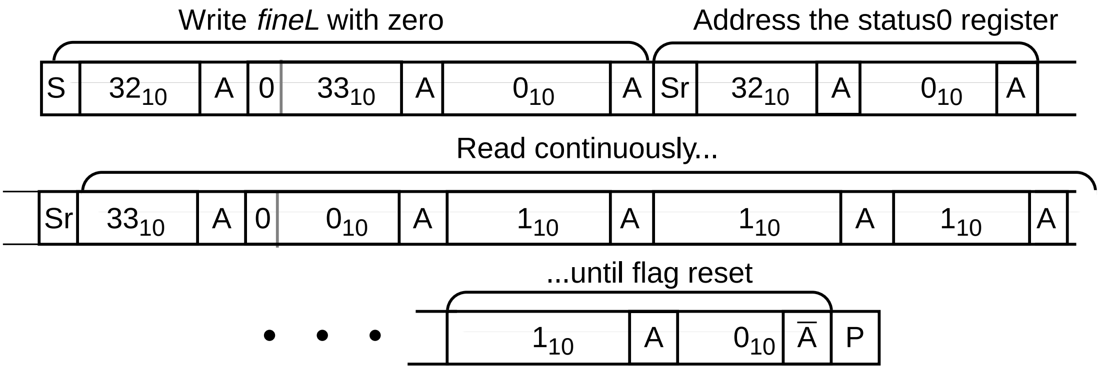

Figure 36 : Same location multiple data read.

9.6.6 Multiple location write

If the automatic increment bit is set (msb of the index byte), then it is possible to write data bytes to consecutive adjacent internal registers, (i.e. 23,24,25,26 etc), without having to send explicit indexes prior to sending each data byte. An auto-increment write to the exposure registers with their default values is shown in the following example, where we write 17_{10} to the pin_mapping register[21] and 193_{10} to the data format register[22].

.

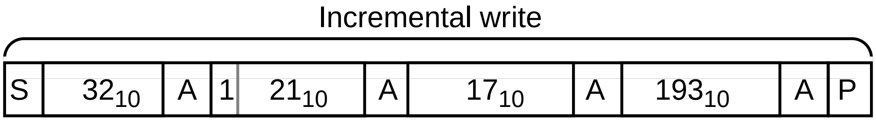

Figure 37 : Multiple location write.

9.6.7 Multiple location read

In the same manner, multiple locations can be read with a single read message. In this example the index is written first, to ensure the exposure related registers are addressed and then all six are read.

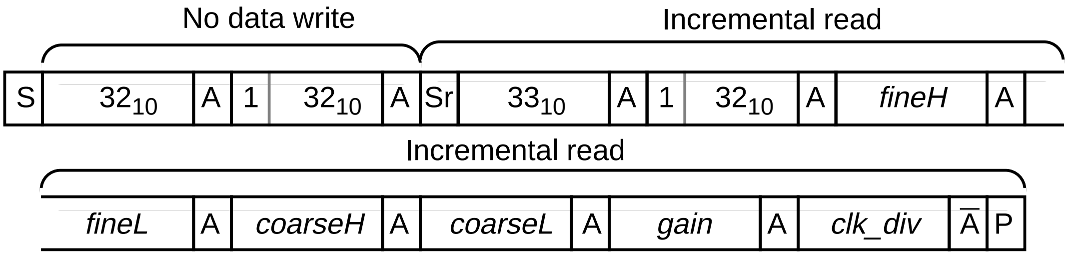

Figure 38 : Multiple location read.

Note that a stop condition is not required after the final negative acknowledge from the master, the sensor will terminate the communication upon receipt of the negative acknowledge from the master.

9.7 Serial Interface Timing

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	fscl	0	100	kHz
Bus free time between a ***stop*** and a ***start***	tbuf	2	-	us
Hold time for a repeated ***start***	thd;sta	80	-	ns
LOW period of SCL	tlow	320	-	ns
HIGH period of SCL	thigh	160	-	ns
Set-up time for a repeated ***start***	tsu;sta	80	-	ns
Data hold time	thd;dat	0	-	ns
Data Set-up time	tsu;dat	0	-	ns
Rise time of SCL, SDA	tr	-	300	ns
Fall time of SCL, SDA	tf	-	300	ns
Set-up time for a ***stop***	tsu;sto	80	-	ns
Capacitive load of each bus line (SCL, SDA)	Cb	-	200	pF

Table 55 : Serial Interface Timing Characteristics

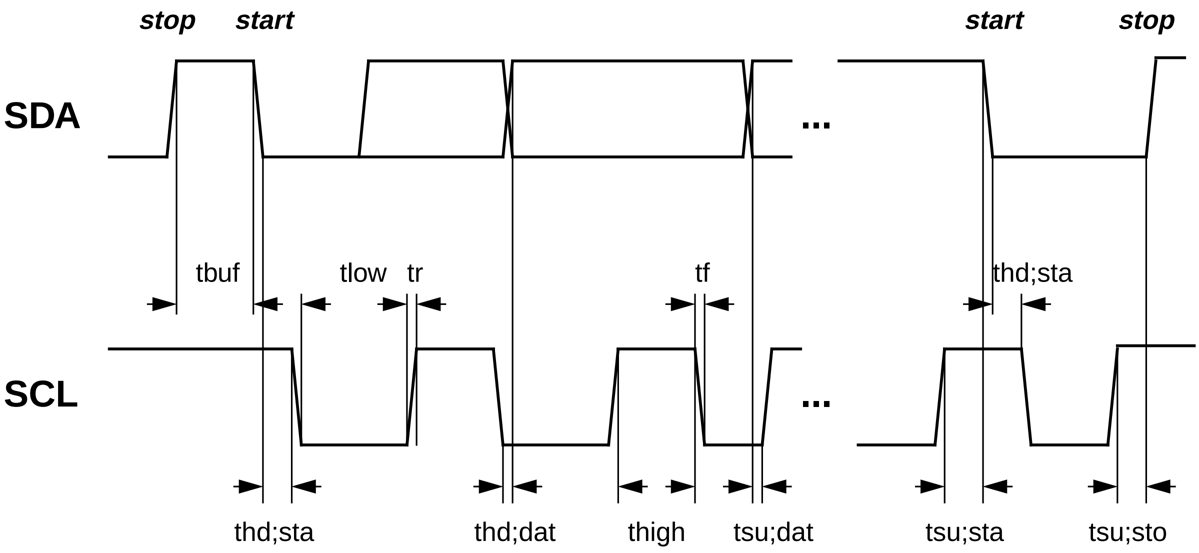

Figure 39 : Serial Interface Timing Characteristics

10. Clock Signal

VV5500/VV6500system clock is supplied from an external clock source directly driving the CLKI pin. The clock pad has an integral Schmitt buffer to filter noise from the clock source. Please note that there is no support for an external resonator circuit.

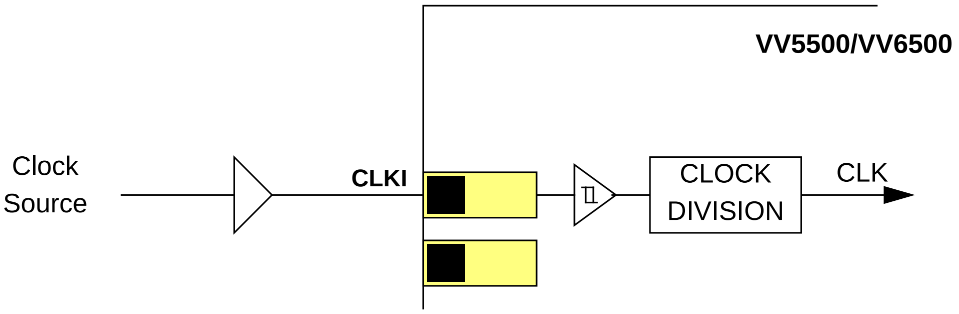

Figure 40 : CMOS Clock Source

I

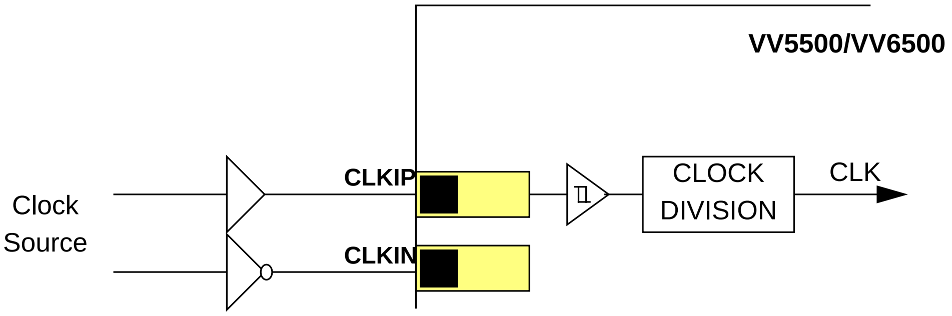

Figure 41 : LVDS Clock Source

The clock signal must be a square wave with, ideally a 50% (10%) mark:space ratio, although a non-ideal mark:space ratio can be tolerated, please contact STMicroelectronics for details. The maximum input clock frequency for the module is 24.0 MHz. If the 24MHz crystal is preferred then the user must select the pre-clock divide by 1.5 option such that the bulk of the internal logic is driven by a 16MHz clock, see serial interface, register 16_{10}, data_format.

11. Other Features

11.1 Audio Amplifier

VV5410/VV6410 contains an on-chip audio amplifier which can be configured via the serial interface. The amplifier may also be powered down via the serial interface.

The following document outlines the implementation of audio circuitry on the VV5410/VV6410 sensor.

11.1.1 Audio Amplifier Configuration

The audio circuit is controlled through a single eight bit register on the VV5410/VV6410. This includes bits for power down, output select, first and second stage gains and current boosting. Table 56 describes the functionality of the control register bits.

The first stage provides a gain of 0dB or 30dB using a low noise amplifier design.

The reference is provided from the on-chip bandgap voltage. This is buffered by a cut down version of the low-noise amplifier used in the first gain stage.

Bit	Function	Default	Comments
0	First stage gain	1	0 - 0dB 1 - 30dB
1	Second stage gain[1]	0	gain[1] gain[0] - gain(dB) **0 0 - 0dB** 0 1 - 6dB 1 0 - 12dB 1 1 - 18dB
2	Second stage gain[0]	0	
3	Power Down	0	**0 - Powered up** 1 - Power down
4	Output Select	0	**0 - Single ended** 1 - Differential
5	Current Boost	0	**0 - 1mA output drive in output buffers** 1 - 2mA output drive in output buffers
7:6	Unused		

Table 56 : Control register summary for VV5410/VV6410 audio circuit.

The output of the first gain stage is fed to two output amplifiers. These can be configured with a 1mA or 2mA output drive current. The inverting gain stage provides an additional gain between 0dB and 18dB.

The output of the inverting gain stage may be routed through the other output buffer to provide two single ended outputs. Otherwise, the inverted and non-inverted outputs provide a fully differential output signal.

Some more circuit specifications may be found in Table 57.

11.1.2 AUD3V3 (Audio Supply Regulator)

Symbol	Parameter	Min	Typical	Max	Units
AUD3V3	Regulated supply (No external load)	3.13	3.3	3.46	V
AUD3V3_Ld	Regulated supply Vdrop (Current Load 20mA)		-50		mV
AUD3V3_sus	Regulated supply (Suspend mode)		Off		V
ZAUD3V3_sus	Output impedance in Suspend mode		TBC		KΩ
PSRR	Power Supply Rejection versus Vin		-48		dB

Table 57 : Audio Circuit Specification

11.1.3 Audio Amplifier Parameters

Symbol	Parameter	Min	Typical	Max	Units
VAin	Audio Regulator Input Voltage		V_{bg}		V
R_{IN}	Input impedance		100		kΩ
Gain1	Ist stage (28dB) gain accuracy		+/-0.5		dB
Gain2	2nd stage (0,6,12,18dB) gain accuracy[1]		+/-0.2		dB
Gmatch	Differential output mode gain matching (0dB) (28dB)(		0.2 0.5		dB
Out_max	Output Clipping Level[2]	1.6	2.2		Vpp
OUT_DC	Output DC Voltage	1.1	1.22	1.3	V
D-OUT_DC	Differential DC Offset (AoutN-AoutP)		20	100	mV
Rout	Output Impedance		2		kΩ
THD	THD (includes noise) Vin = 20mVpp, f-1KHz, Gain =28dB		0.2		%
SNR	Signal to Noise ratio (1KHz) (10KHz)[3]		65 75		dB
PSRR	Power supply rejection ratio from Vin		-55		dB
LFc	Low frequency cutoff (Cin=100nF)		15		Hz
Xtalk	Video crosstalk to audio outputs (gain = 28dB)		-56		dB

Table 58 : Audio Amplifier Parameters

1. **2nd stage gain is only available on AoutN with the audio amplifier in differential mode**

2. **Minimum dynamic range includes dcout (i.e. Vclip- OUT_DC is greater than Vppmin/2)**
3. **Assumes 10µF bypass capacitors on all supplies and well separated supplies and grounds**

11.1.4 Audio Amplifier Bandwidth[1]

The audio circuit can be bandwidth limited to a first order, through the use of minimum external circuitry. The two outputs, AoutP and AoutN, require compensation capacitors that may also be used to define the bandwidth of the circuit.

Compensation Capacitor (nF)	3dB Bandwidth	Units
1	175	kHz
10	41	kHz
100	4.2	kHz

Table 59 : Compensation capacitor values

In addition, the inclusion of a resistor (microphone biasing) and decoupling capacitor at the input allows a first order high pass filter to be realised. This can easily be designed to remove frequencies below 50Hz/60Hz (mains electricity noise).

11.2 Voltage Regulators

VV5410/VV6410 contains three on-chip voltage regulators, two of which are capable of being powered-down via the serial interface. The third regulator, controlling the band gap references is never powered down. The band gap circuitry is extremely low power consuming only 30µA.

11.2.1 Regulator for Digital System

The output of the regulator, Reg3V3, powers the digital logic and can power an external co-processor. The regulator is powered up by default. The regulator has its own discrete power supply and can source a load of 300µA -> 150mA and will regulate to 3.0V 10% from an input range of 4-6V. When VV5410/VV6410 is in the USB compatible suspend mode, the clocks to the digital logic are removed to limit power consumption to approximately 80µA. If an external 3.3V supply is available, this regulator may be overdriven by an external 3.3V supply to directly power the logic. This voltage regulator is never powered down.

11.2.2 Regulator for Audio Amplifier

The output of the regulator for the audio amplifier, Aud3V3, drives the load resistor for the microphone and the audio pre-amplifier. As this regulator is capable of being powered-down via the serial interface, all control signals from the digital logic are low during low power/standby. This regulator will be powered up by default.

11.2.3 Regulator for Video Supply/Analogue Core

The output of the regulator for the video supply,Vid3V3, powers the analog core. This regulator is capable of being powered-down via the serial interface but will be powered up by default. Note that the sensor will be in low power mode initially and therefore

11.3 Valid Supply Voltage Configurations

The power supplies to the VV5410 and VV6410 sensors can be configured such that the sensor will operate in a number of systems:

- USB system (sensor will regulate the nominal 5V supply to 3V3 internally) with optional BJT to provide power for a companion chip.
- Direct drive the sensor with 3V3 (internal voltage regulators will be powered down in this mode).

The next 2figures will detail the options described above:

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[1] Each audio output must have a capacitor (Ccomp) connected to ground to avoid any oscillation

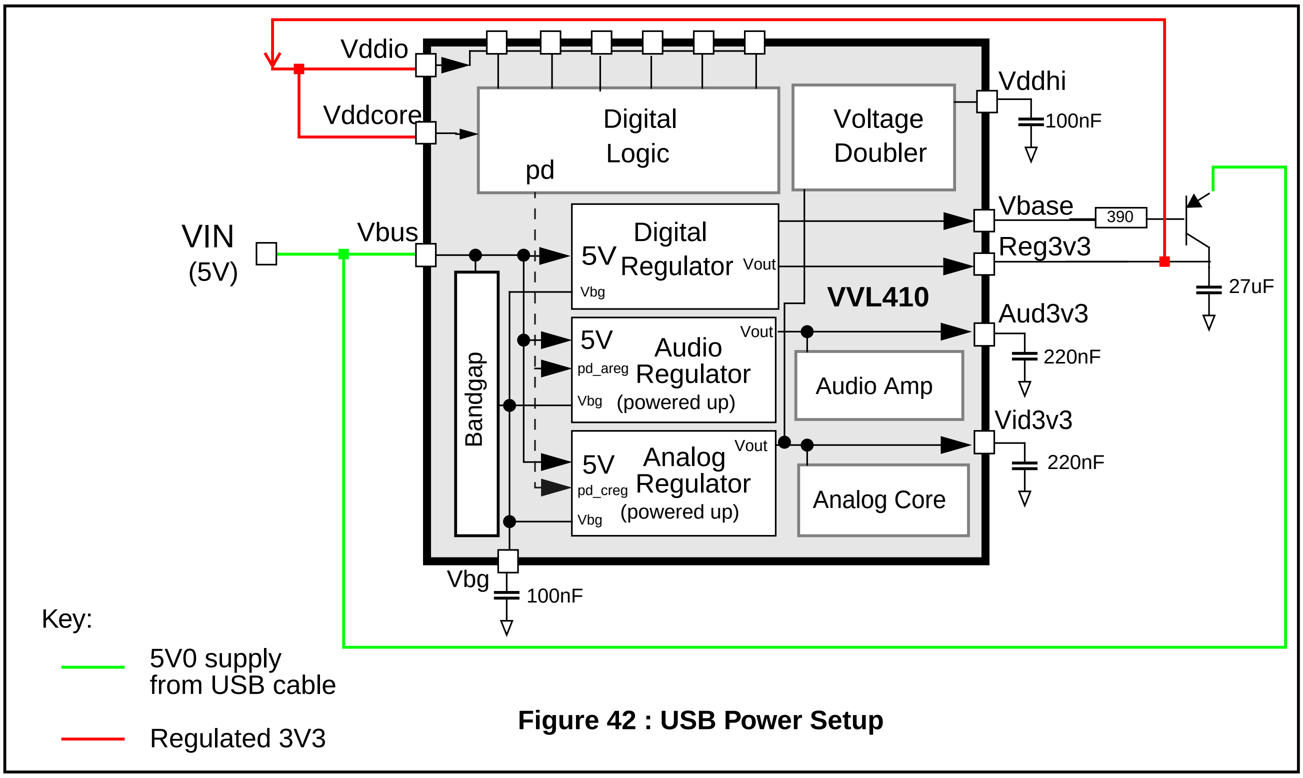


Figure 42 : USB Power Setup

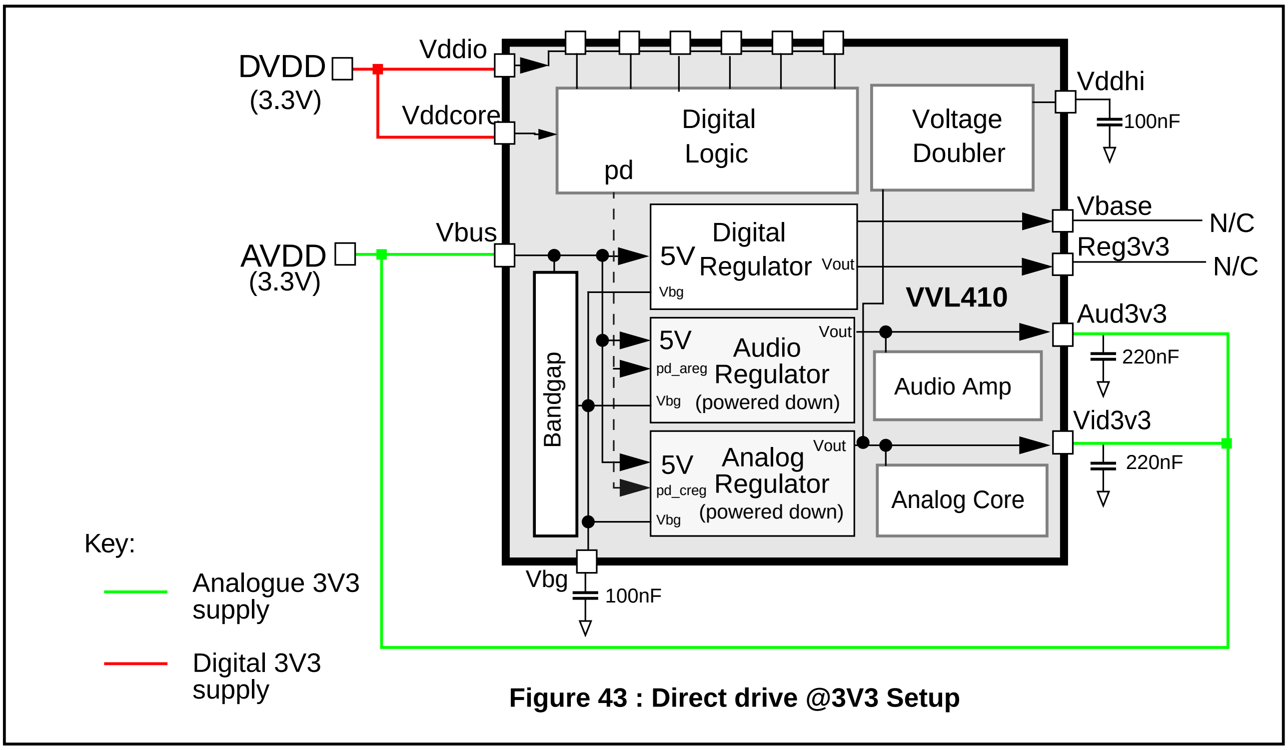


Figure 43 : Direct drive @3V3 Setup

Supply	USB System	3.3V-only System
Vbus	Supply from USB cable	3.3V direct drive
Vddio	connect to Vreg3v3	3.3V direct drive
Vddcore	connect to Vreg3v3	3.3V direct drive
Vreg3v3	optionally populate external BJT for added drive	BJT not populated
Vid3v3	generated by internal regulator	internal regulator powered down
Aud3v3	generated by internal regulator	internal regulator powered down

Table 60 : Sensor Voltage Supply summary

11.4 Programmable Pins

The FST and QCK pins can be re-configured to follow the values of bits 1 and 2 in the serial interface.register *pin_mapping*. This is to allow remote control of a electro-mechanical system, maybe two different crop settings, in a remote camera head via the serial interface.

12. Characterisation Details

12.1 VV5500/VV6500 AC/DC Specification

Parameter	Comment	Units
Image Format	644 x 484 pixels (VGA) 356 x 292 pixels (CIF) 324 x 244 pixels (QVGA)	-
Pixel Size	7.5 x 7.5	µm
Technology	0.5µm 3 level metal CMOS	-
Array Format	CIF	-
Exposure control range	81 (minimum exposure period 3µs and maximum exposure period is 33ms)[1]	db
Supply Voltage	3.0-6.0 DC +/-10%	V
Operating Temp. range	0 - 40	^oC
V_{OL_max}[2]	0.527	V
V_{OH_min}[3]	2.34	V
V_{ILI_max}[4]	1.16	V
V_{IH_min}[5]	2.1	V
Serial interface frequency range	0-100kHz	

1. **We assume CIF (30fps) mode, input clock of 16MHz and internal clock divisor of 1.**
2. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
3. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
4. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**
5. **This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 2V7**

Table 61 : VV5500/VV6500 DC specification

12.2 VV5500/VV6500 Optical Characterisation Data

Optical Parameter	Min	Typical	Max	Units
Dark Current	-	TBA	-	mV/sec
Average Sensitivity	-	TBA	-	V/lux.sec
Fixed Pattern Noise (FPN)	-	TBA	-	mV
Vertical Fixed Pattern Noise (VFPN)	-	TBA	-	mV
Random Noise	-	TBA	-	mV
Sensor SNR	-	TBA	-	dB
Shading (Gross)	-	TBA	-	mV

Table 62 : VV5500/VV6500 Optical Characterisation Data

12.2.1 Noise Parameters and Dark Current

Various noise parameters are measured on the 500 device as follows:

- Fixed Pattern Noise (FPN)
- Vertical Fixed Pattern Noise (VFPN)
- Random Noise
- Fine Shading
- Gross Shading

The parameters will be described in more detail below along with the data produced by the characterisation programme.

12.2.2 Blooming

Blooming is a phenomenon that does not affect CMOS sensors in the same way as CCD imagers are afflicted. With a CCD blooming can cause an entire column/columns to flood and saturate.

CMOS imagers are however affected by a different type of saturation. If an intense light source, (e.g. Maglite torch), is shone at very close proximity to the image sensor the pixel sampling mechanism will break down and rather than displaying a saturated white light a black image will occur.

The 500 pixel architecture uses Correlated Double Sampling (CDS) to help reduce noise in the system. The pixel is read normally first, yielding the true integrated signal information, then the pixel is reset and very quickly read for a second time. This normally yields black information - as the pixel has had no exposure time - that can be subtracted from the signal from the first read. This subtraction will remove much of the noise from the pixel leaving only the useful signal information.

In an example where a pixel has saturated in both the first and the second reads due to an intense light source. When the noise cancellation subtraction operation is then performed the result is close to zero signal from the pixel therefore resulting in the displayed black image.

We do not perform any test measurements for this phenomenon.

12.2.3 Dark Current

This is defined as the rate at which the average pixel voltage increases over time with the device not illuminated. The dark current will be measured at a gain setting of 4 and a clock divisor of 16 at a fixed temperature and will be expressed in mV.

12.2.4 Fixed Pattern Noise

The FPN of an image sensor is the average pixel non-temporal noise divided by the average pixel voltage. The illumination source will be white light that has been IR filtered, producing a diffuse uniform illumination at the surface of the sensor package. The FPN will be calculated at coarse exposure settings of 0,10,150,250 and 302 with gain set to 1. 10 frames are grabbed and averaged to produce a temporally independent frame before each calculation. FPN will be expressed in mV.

12.2.5 Vertical Fixed Pattern Noise

VFPN describes the spatial noise in an image sensor related to patterns with a vertical orientation. The VFPN is defined as the standard deviation over all columns of the average pixel voltage for each column determined at zero exposure and zero illumination. VFPN will be expressed in mV.

12.2.6 Random Noise

Random noise is the temporal noise component within the image. Random noise will be expressed in mV.

12.2.7 Shading

This describes how average pixel values per “block” change across the image sensor array. For fine shading calculations the image sensor array is split into 30 pixel by 30 pixel blocks. An average value is then calculated for each block and the averages are then compared across the whole device. The blocks are increased in size to 60 pixels by 60 pixels for the gross shading calculation. Shading will be expressed in mV.

12.3 VV5500/VV6500 Power Consumption

Operating Condition	Current Consumption
Low power mode current consumption	7.6mA
Sleep mode current consumption[1]	18mA
Suspend mode current consumption (with CLKIP disabled)	74uA
Normal operating mode current consumption[2]	42mA (max)

1. **Estimated figures - this parameter was not measured during final characterisation**
2. **Measured while device is clocked at 24MHz and streaming VGA video at 30fps**

Table 63 : VV5500/6500 Current consumption in different modes

12.4 Digital Input Pad Pull-up and Pull-down Strengths

Pad Type	Pads	Min current	Max Current
Library pulldown	suspend	35uA	52uA
Library pullup	scl, sda, oeb	25uA	42uA
Custom pullup	resetb	66uA	250uA

Table 64 : Pad Pull-up/Pull-down Strengths

13. Pixel Defect Specification

13.1 Pixel Fault Definitions

Please find the pixel notation described in Figure 44 below. For the purposes of the test the 3x3 array describes 9 bayer pixels of a common colour, i.e. ALL the pixels will either be Red, Green or Blue. The pixel under test is **X**.

[0]	[1]	[2]
[7]	**X**	[3]
[6]	[5]	[4]

Figure 44 : Pixel Numbering Notation

13.2 Stuck at White Pixel Fault

A pixel is said to be “stuck at white” - it can also be referred to as “hot” - if it is saturated (pixel output at maximum) even with no incident light and exposure set to zero.

13.3 Stuck at Black Pixel Fault

A pixel is said to be “stuck at black” - it can also be referred to as “dead” - if the pixel output is zero even if the pixel is fully exposed to incident light.

13.4 Column / Row Faults

A line of continuous pixel fails of length > 3 will be described as a row fault in the x-direction and a column fault in the y-direction.

If the array contains more than 1 row or column fault and the defective pixels overlap as shown in Figure 45 then this fault is described as a double row or double column fault respectively. The minimum overlap is 1 pixel. A defective pixel is indicated by **X** and a good pixel by ‘p’.

n	n+1
X	‘p’
X	‘p’
X	p
X	**X**
‘p’	**X**
‘p’	**X**
‘p’	**X**

Figure 45 : Double Column Fault

In Figure 46 there are 2 column faults however there is no overlap between the 2 columns therefore there are 2 single column faults but no double column faults.

n	n+1
X	‘p’
X	‘p’
X	p
X	‘p’
‘p’	**X**
‘p’	**X**
‘p’	**X**
‘p’	**X**

Figure 46 : Single Column Faults

13.5 Image Array Blemishes

The automatic test programme rejects any sensors that contain blemishes referred to as blobs and clusters (please see below for definitions of these terms) as they cannot be successfully defect corrected by ST coprocessor devices. Up to 120 single pixel faults can be corrected and sensors meeting this criteria will PASS this part of the test programme.

13.5.1 Cluster Definition

A failing pixel at **X** with a failing pixel at position [0] or [1] or [2] or [3] or [4] or [5] or [6] or [7] or any combination of these 8 positions except the case where all positions are defective. This is a special case and is described below. In the example in Figure 47 there are additional pixel fails in positions [3] and [7].

[0]	[1]	[2]
[X]	**X**	[X]
[6]	[5]	[4]

Figure 47 : Cluster Example

Blob (special case of cluster):- a failing pixel at position **X** with failing pixels at position [0],[1],[2],[3],[4],[5],[6] and [7] as in Figure 48 below:

[X]	[X]	[X]
[X]	**X**	[X]
[X]	[X]	[X]

Figure 48 : Blob Example

Single pixel:- a failing pixel with no immediate failing same colour neighbours. Pixels at position [0],[1],[2],[3],[4],[5],[6] and [7] are all valid pixels. Please see Figure 49 below.

[0]	[1]	[2]
[7]	**X**	[3]
[6]	[5]	[4]

Figure 49 : Isolated pixel fail

13.5.2 Summary Pass Criteria

Clusters	Blobs	Row Fails (inc doubles)	Column Fails (inc doubles)	Single pixel fails	Notes[1]
0	0	0	0	<=120	Pass

Table 65 : Sensor Pixel Defect Pass Criteria

[1] **If there is a non-zero number of clusters, blobs or row/column faults and greater than 120 single pixel defects then the device will be rejected and classed as a fail.**

14. Pinout and pin descriptions (48pin LCC package)

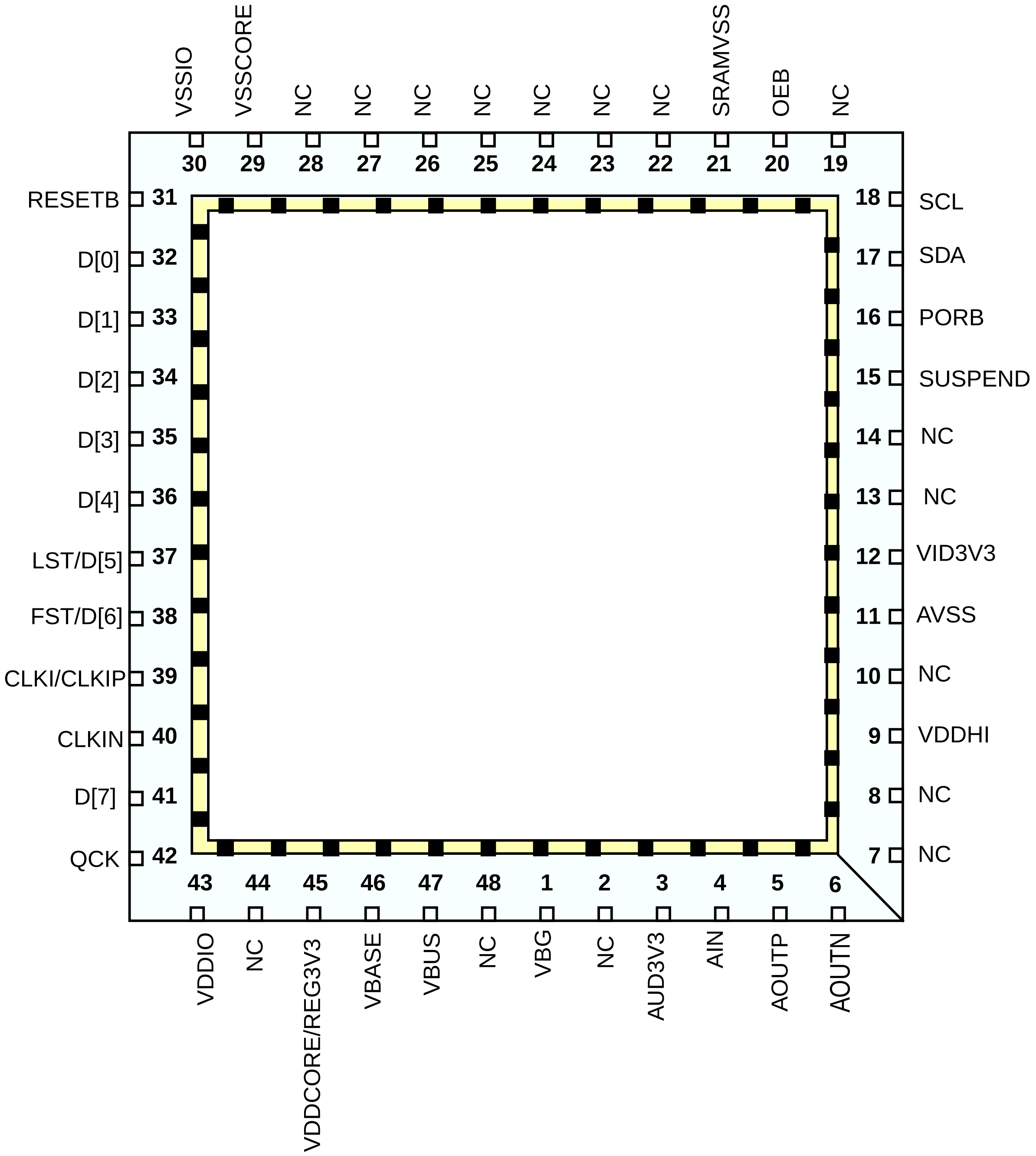


Figure 50 : 48 pin LCC package pin assignment

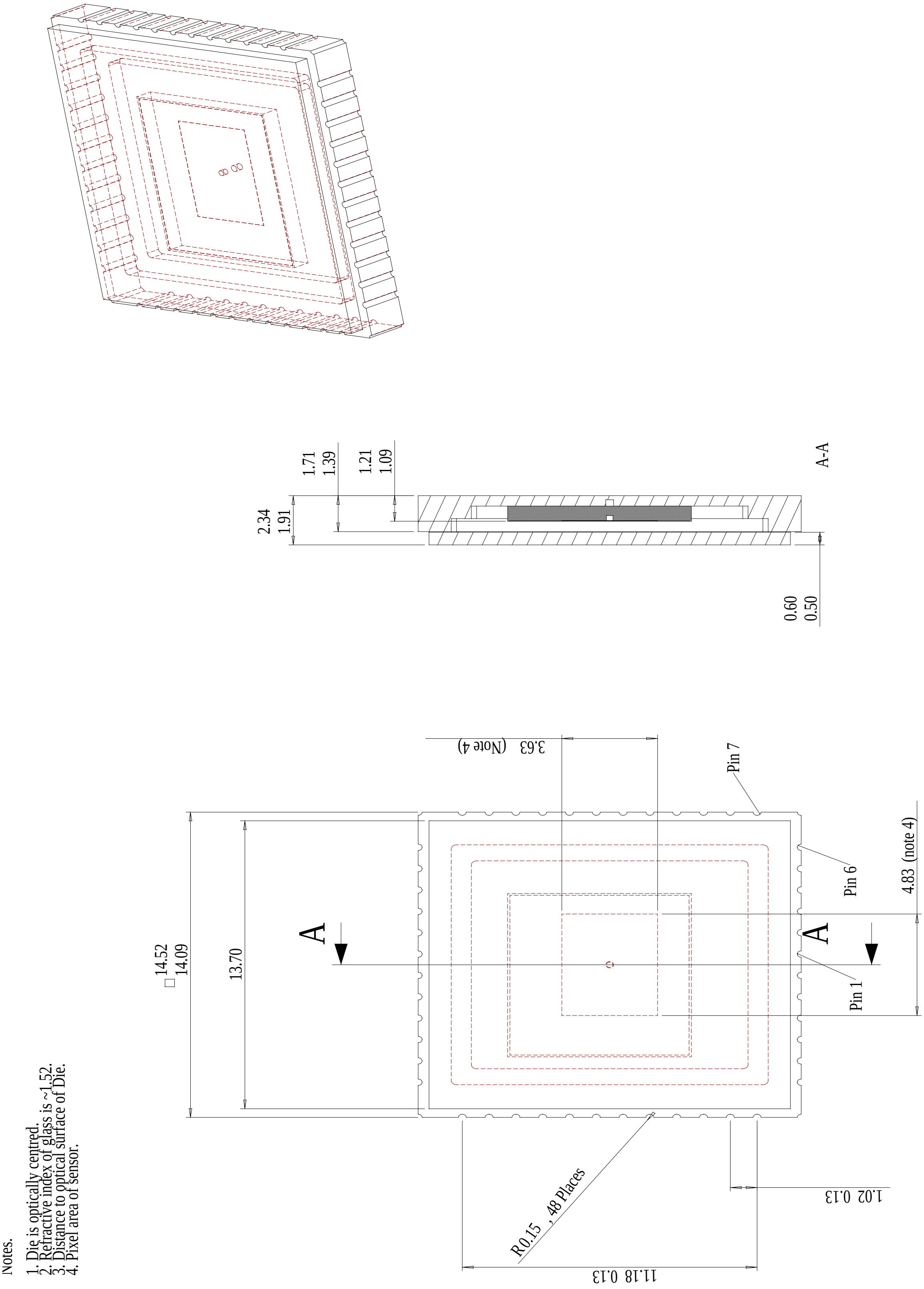
Name	Pin Number	Type	Description
POWER SUPPLIES			
AVSS	11	GND	Core analog ground and reference supplies.

Name	Pin Number	Type	Description
SRAMVSS	21	GND	In-column SRAM analog ground.
VDDCORE/ REG3V3	44	PWR	Digital logic power.
VDDIO	43	PWR	Digital pad ring power.
VSSCORE	29	GND	Digital logic ground.
VSSIO	30	GND	Digital pad ring ground.
SRAMVSS	21	GND	In-column SRAM analogue ground.
ANALOG SIGNALS			
VBG	1	OA	Internally generated bandgap reference voltage 1.22V
AIN	4	IA	Analog input to Audio Amplifier
AOUTP	5	OA	Analog output of Audio Amplifier (positive)
AOUTN	6	OA	Analog output of Audio Amplifier (negative)
VDDHI	9	OA	Output from voltage doubler, 4.6V -> 4.8V
VBASE	46	OA	Drive for base of external bipolar
VBUS	47	IA	Incoming power supply 4.1V-> 6V
AUD3V3	3	OA	On-chip Audio Amplifier Voltage Regulator Output
VID3V3	12	OA	On-chip Video Supply Voltage Regulator Output
PORB	16	OA	Power-on Reset (Bar) Output.
DIGITAL VIDEO INTERFACE			
D[4] D[3] D[2] D[1] D[0]	36 35 34 33 32	ODT	Tri-stateable 5-wire output data bus. - D[4] is the most significant bit. - D[4:0] have programmable drive strengths 2, 4 and 6 mA
QCK	42	ODT	Tri-stateable data qualification clock.
CLKIN	40	BI↑	LVDS negative Clock input
LST/D[5]	37	ODT	Tri-stateable Line start output May be configured as tri-stateable output data bit 5 D[5].
FST/D[6]	38	ODT	Tri-stateable Frame start signal. May be configured as tri-stateable output data bit 6 D[6].
D[7]	41	ODT	Tri-stateable Data wire (ms data bit). May be configured as tri-stateable output data bit 7 D[7].
OEB	20	ID↓	Digital output (tri-state) enable.

Name	Pin Number	Type	Description
DIGITAL CONTROL SIGNALS			
RESETB	31	ID↑	System Reset. Active Low. May be configured as System Sync. Active Low.
SUSPEND	15	ID↑	USB Suspend Mode Control signal. Active High If this feature is not required then the support circuit must pull the pin to ground. The combination of an active high signal and pull up pad was chosen to limit current drawn by the device while in suspend mode.
SERIAL INTERFACE			
SCL	18	BI↑	Serial bus clock (input only).
SDA	17	BI↑	Serial bus data (bidirectional, open drain).
SYSTEM CLOCKS			
CLKI/CLKIP	39	ID↓	Schmitt Buffered Clock input or LVDS positive Clock input
CLKIN	40	ID↑	LVDS negative Clock input

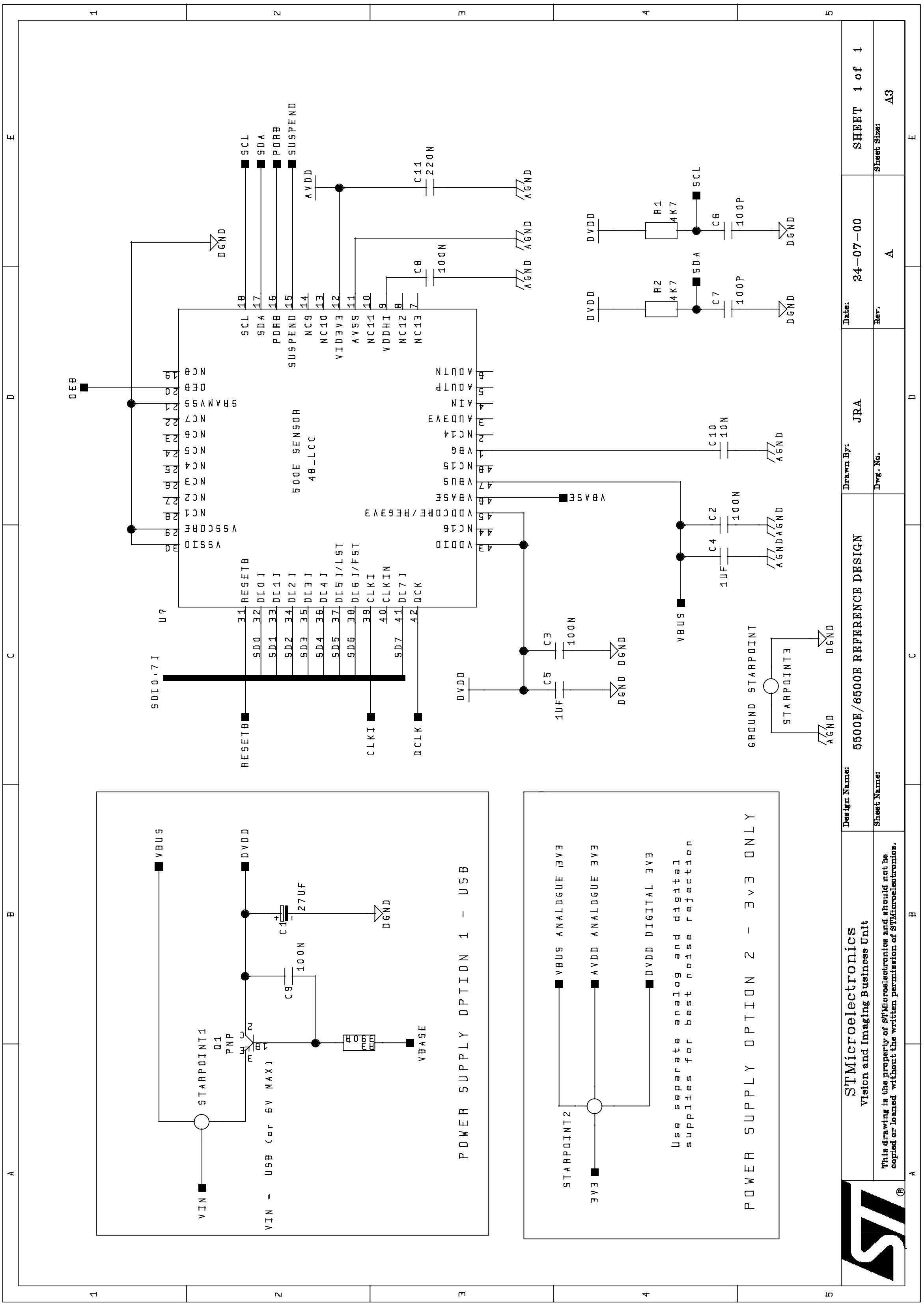
Key			
A	Analog Input	D	Digital Input
OA	Analog Output	ID↑	Digital input with internal pull-up
BI	Bidirectional	ID↓	Digital input with internal pull-down
BI↑	Bidirectional with internal pull-up	OD	Digital Output
BI↓	Bidirectional with internal pull-down	ODT	Tri-stateable Digital Output

15. Package Details (48 pin LCC)



Notes.
1. Die is optically centred.
2. Refractive index of glass is ~1.52.
3. Distance to optical surface of Die.
4. Pixel area of Sensor.

16. Recommended VV5500/6500 support circuit



17. Evaluation kits (EVK's)

There are a number of evaluation kits available that demonstrate the 5500 and 6500 sensors.

The monochrome 5500 sensor can be demonstrated using the PCI card based standard evaluation kit, STV-5500-E01, (see next page for ordering details on this and all the other evaluation kits).

The colourised 6500 sensor may also be demonstrated using a PCI based evaluation kit, STV-6500-E01. There are two further evaluation kits that can demonstrate the 6500 sensor. These kits use two ST coprocessor designs. The first of these coprocessors, STV0657, can output either YUV 4:2:2 or RGB data, evaluation kit STV-YUV/VGA-E01. The second of these coprocessors, STV0672, allows direct interface to a PC via the USB port., evaluation kit STV-USB/VGA-R01.

18. Ordering details

Part Number	Description
VV5500C001	48pin CLCC packaged, microlensed VGA monchrome sensor
VV6500C001	48pin CLCC packaged, microlensed VGA ColourMOS sensor
STV0672	USB companion CoProcessor
STV0680B-001	Digital stills companion CoProcessor
STV-5500-R01	Reference design board for 5500
STV-6500-R01	Reference design board for 6500
STV-USB/VGA-R01	Reference design board for VV6500C001 & STV0672
STV-YUV/VGA-E01	Evaluation kit for VV6500C001 & STV0657
STV-DCA/VGA-E01	Reference design board for VV6500C048 & STV0680B-001
STV-5500-E01	Sensor only evaluation kit for VV6410C036 & VV6500C048
STV-6500-E01	Sensor only evaluation kit for VV6410C036 & VV6500C048

Table 66 : VV6500/VV5500 Ordering Details

Imaging Division

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