M48ST59W

3.0V, 64 Kbit (8 Kbit x 8) SUPERVISORY TIMEKEEPER® SRAM

PRELIMINARY DATA

FEATURES SUMMARY

- 2.7V TO 3.6V OPERATING VOLTAGE
- INTEGRATED ULTRA-LOW POWER SRAM, REAL TIME CLOCK (RTC), POWER-FAIL CONTROL CIRCUIT, CRYSTAL, and BATTERY
- 1.25V REFERENCE (FOR PFI/$\overline{PFO}$)
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES
  V_{PFD} = Power-fail Deselect Voltage:
  – M48ST59W: V_{CC} = 2.7 to 3.6V
  $2.50V \leq V_{PFD} \leq 2.70V$
- MICROPROCESSOR POWER-ON RESET (Valid even during battery back-up mode)
- PROGRAMMABLE ALARM and INTERRUPT FUNCTION
  (Valid even during battery back-up mode)
- BYTEWIDE™, RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES, and SECONDS
- FREQUENCY TEST OUTPUT FOR RTC CALIBRATION
- BATTERY LOW FLAG
- PROGRAMMABLE t_{REC}
- PACKAGING INCLUDES A 44-LEAD SOIC and SNAPHAT® TOP (to be ordered separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP WHICH CONTAINS THE BATTERY and CRYSTAL

Figure 1. 44-pin SOIC Package

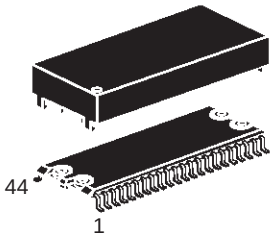


TABLE OF CONTENTS

SUMMARY DESCRIPTION 4
Logic Diagram (Figure 2.) 4
Signal Names (Table 1.) 4
44-pin SOIC Connections (Figure 3.) 5
Block Diagram (Figure 4.) 5

MAXIMUM RATING 6
Absolute Maximum Ratings (Table 2.) 6

DC AND AC PARAMETERS 7
DC and AC Measurement Conditions (Table 3.) 7
AC Testing Load Circuit (Figure 5.) 7
Capacitance (Table 4.) 7
DC Characteristics (Table 5.) 8

OPERATING MODES 9
Operating Modes (Table 6.) 9
READ Mode 10
READ Mode AC Waveforms (Figure 6.) 10
READ Mode AC Characteristics (Table 7.) 10
WRITE Mode 11
WRITE Mode AC Waveforms (Figure 7.) 11
Chip Enable Controlled, WRITE Mode AC Waveforms (Figure 8.) 11
WRITE Mode AC Characteristics (Table 8.) 12
Data Retention Mode 13
Power Down/Up Mode AC Waveforms (Figure 9.) 13
Power Down/Up Trip Points DC Characteristics (Table 9.) 14
Power Down/Up AC Characteristics (Table 10.) 14

CLOCK OPERATIONS 15
Reading the Clock 15
Setting the Clock 15
Stopping and Starting the Oscillator 15
Register Map (Table 11.) 16
Calibrating the Clock 17
Setting Alarm Clock 17
Programmable Interrupts 18
Alarm Repeat Mode (Table 12.) 18
Back-up Mode Alarm Waveform (Figure 10.) 18
Interrupt Reset Waveforms (Figure 11.) 19
Watchdog Timer 19
Power-on Reset 19
Battery Low Flag 19
Century Bit 20
Initial Power-On Defaults 20
Default Values (Table 14.) 20
TREC Bit 20
tREC Definitions POWER-ON (Table 13.) 20
Power-Fail Comparator 21
Adding Hysteresis (Figure 12.) 21
Hysteresis on Rising VIN (Figure 13.) 22
Power Supply Decoupling and Undershoot Protection 22
Supply Voltage Protection (Figure 14.) 22
Crystal Accuracy Across Temperature (Figure 15.) 23
Clock Calibration (Figure 16.) 23

PART NUMBERING 24

PACKAGE MECHANICAL INFORMATION 25

REVISION HISTORY 28

SUMMARY DESCRIPTION

The M48ST59W SUPERVISORY TIMEKEEPER® RAM is an 8Kbit x 8 non-volatile static RAM and real time clock. The monolithic chip is available in a surface mount package to provide a highly integrated battery backed-up memory and real time clock solution. The 44-pin, 330mil SOIC package provides sockets with gold-plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be attached after the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion. The SOIC and battery/crystal packages are shipped separately in plastic, anti-static tubes or in Tape & Reel form (see Table 15, page 24 for the part numbering scheme.)

The battery/crystal package (e.g., SNAPHAT) part number is “M4T28-BR12SH” or “M4T32-BR12SH” (see Table 16, page 24).

Caution: Do not place the SNAPHAT battery/crystal package “M4TXX-BR12SH” in conductive foam, as this will drain the lithium button-cell battery.

Figure 2. Logic Diagram

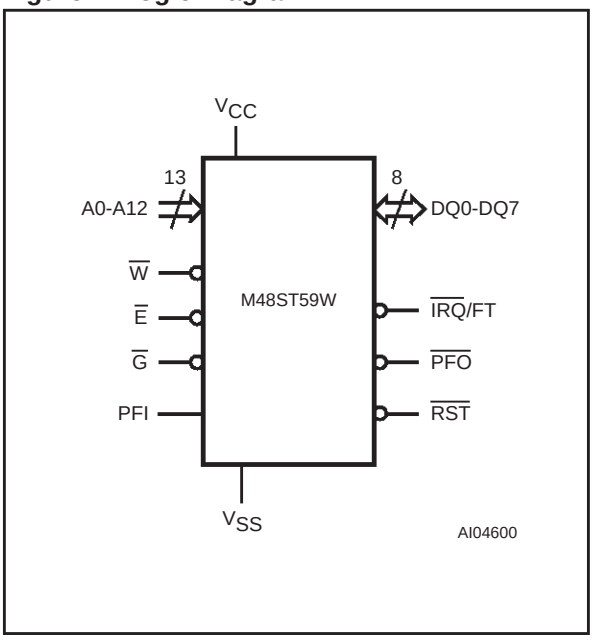


Table 1. Signal Names

A0-A12	Address inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{IRQ}$/FT	Interrupt/Frequency Test Output (Open Drain)
$\overline{RST}$	Reset Output (Open Drain)
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable Input
$\overline{W}$	WRITE Enable Input
$\overline{PFO}$	Power Fail Output
PFI	Power Fail Input
V_{CC}	Supply Voltage Input
V_{SS}	Ground

Figure 3. 44-pin SOIC Connections

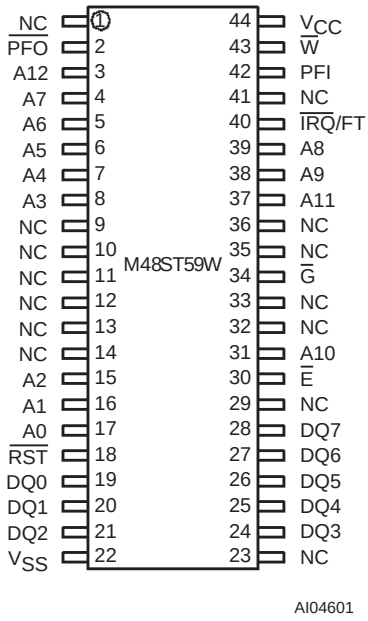
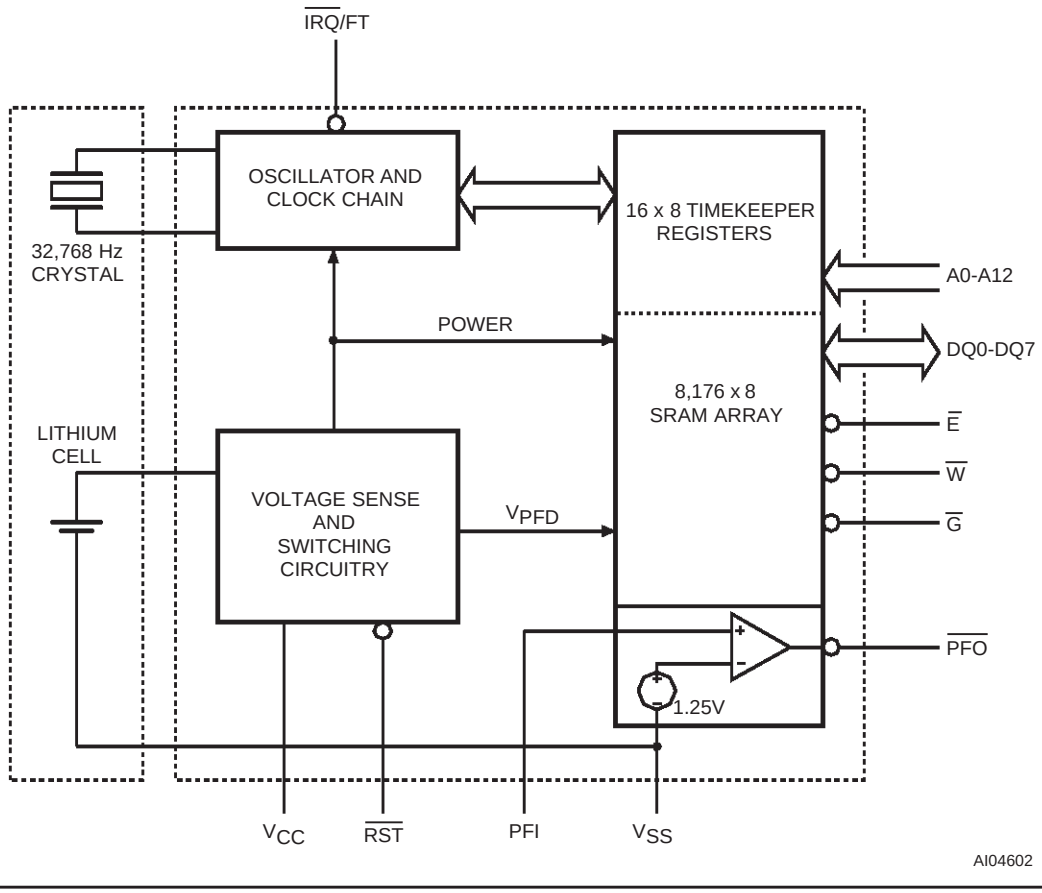


Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Operating Temperature	Grade 1	0 to 70	°C
		Grade 6	–40 to 85	°C
T_{STG}(1)	Storage Temperature (V_{CC}, Oscillator Off)	SNAPHAT®	–40 to 85	°C
		SOIC	–55 to 125	°C
T_{SLD}	Lead Solder Temperature for 10 seconds		260	°C
V_{CC}	Supply Voltage (on any pin relative to Ground)		–0.3 to 4.6	V
V_{IO}	Input or Output Voltages		–0.3 to 4.6	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: 1. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

CAUTION! *Negative undershoots below -0.3V are not allowed on any pin while in the Battery Back-up Mode.*
CAUTION! *Do NOT wave-solder the SOIC to avoid damaging the SNAPHAT sockets.*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. DC and AC Measurement Conditions

Parameter		M48ST59W
V_{CC} Supply Voltage		2.7 to 3.6V
Ambient Operating Temperature	Grade 1	0 to 70°C
	Grade 6	–40 to 85°C
Load Capacitance (C_L)		50pF
Input Rise and Fall Times		≤ 5ns
Input Pulse Voltages		0 to 3V
Input and Output Timing Ref. Voltages		1.5V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Load Circuit

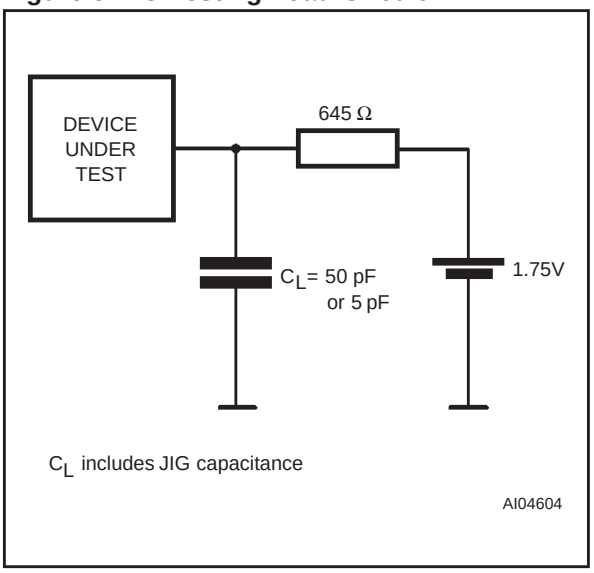


Table 4. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance		10	pF
C_{IO}[3]	Input / Output Capacitance		10	pF

Note: 1. Effective capacitance measured with power supply at 3.6V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs were deselected.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition(1)	M48ST59W			Unit
			–70 / –100			
			Min	Typ	Max	
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±1	µA
	Input Leakage Current (PFI)	$0V \le V_{IN} \le V_{CC}$	–25	2	25	
I_{LO}(2)	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}	Supply Current	Outputs open			30	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$			2	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$			1	mA
V_{IL}(3)	Input Low Voltage		–0.2		0.8	V
V_{IH}	Input High Voltage		2		V_{CC} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4	V
	Output Low Voltage ($\overline{IRQ}$/FT and $\overline{RST}$)(4)	I_{OL} = 10mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4			V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. Outputs deselected.
3. Negative spikes of –1V allowed for up to 10ns once per cycle.
4. The $\overline{IRQ}$/FT and $\overline{RST}$ pins are Open Drain.

OPERATING MODES

The static memory array and the quartz-controlled clock oscillator of the M48ST59W are integrated on one silicon chip (see Figure 4, page 5). The memory locations used to provide user accessible BYTEWIDE™ clock information are in the bytes with addresses 1FFFh-1FF9h (see Table 11, page 16). These clock locations contain the century, year, month, date, day, hour, minute, and second in 24 hour, BCD format. Corrections for 28, 29 (leap year - compliant until the year 2100), 30, and 31 day months are made automatically.

Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ READ/WRITE memory cells. The M48ST59W includes a clock control circuit which updates the clock bytes with current information approximately once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48ST59W also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single V_{CC} supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit writes protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below the Battery Back-up Switchover Voltage, (V_{SO}), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Table 6. Operating Modes

Symbol	V_{CC}	E	G	W	DQ7 – DQ0	Power
Deselect	2.7 to 3.6V	V_{IH}	X	X	Hi-Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	Hi-Z	CMOS Standby
Deselect	$\leq V_{SO}$(1)	X	X	X	Hi-Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.

1. See Table 9, page 14.

READ Mode

The M48ST59W is in the READ Mode whenever WRITE Enable ($\overline{W}$) is high and Chip Enable ($\overline{E}$) is low. The unique address specified by the 13 Address Inputs defines which one of the 8,176 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access Time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and Output Enable ($\overline{G}$) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold Time (t_{AXQX}) but will be indeterminate until the next Address Access.

Figure 6. READ Mode AC Waveforms

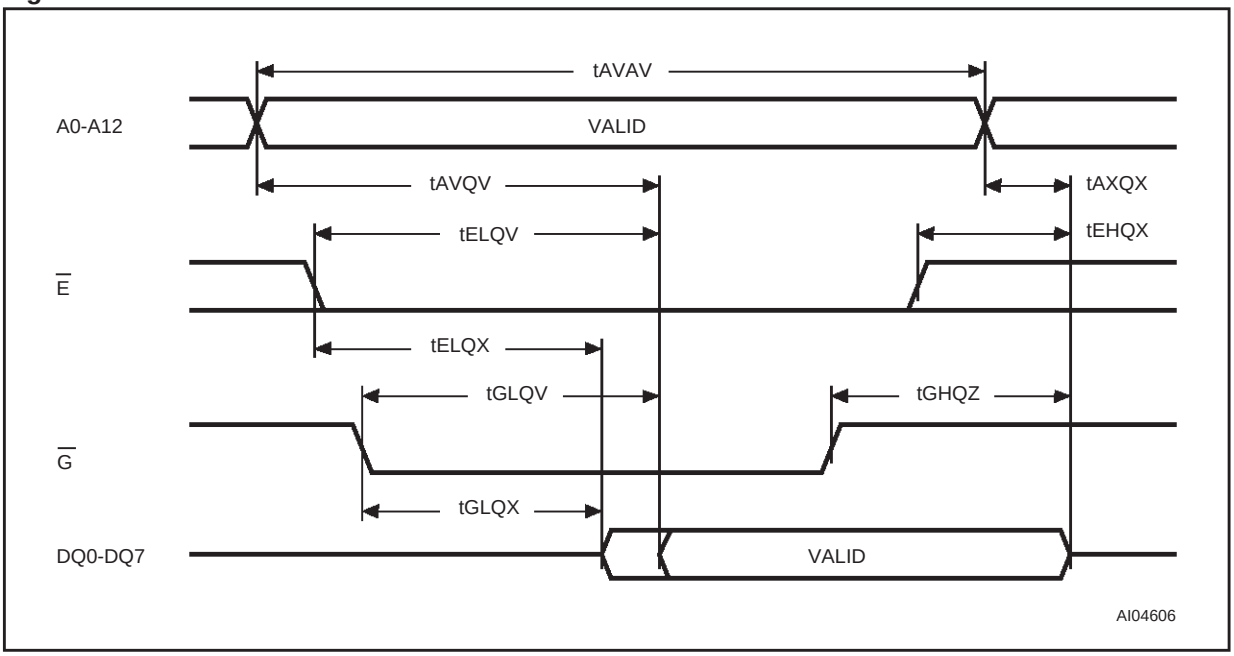


Table 7. READ Mode AC Characteristics

Symbol	Parameter[1]	M48ST59W –70 / –100		Unit
		Min	Max	
t_{AVAV}	READ Cycle Time	70		ns
t_{AVQV}	Address Valid to Output Valid		70	ns
t_{ELQV}	Chip Enable Low to Output Valid		70	ns
t_{GLQV}	Output Enable Low to Output Valid		35	ns
t_{ELQX}[2]	Chip Enable Low to Output Transition	5		ns
t_{GLQX}[2]	Output Enable Low to Output Transition	5		ns
t_{EHQZ}[2]	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ}[2]	Output Enable High to Output Hi-Z		25	ns
t_{AXQX}	Address Transition to Output Transition	10		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. C_L = 5 pF.

WRITE Mode

The M48ST59W is in the WRITE Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. WRITE Mode AC Waveforms

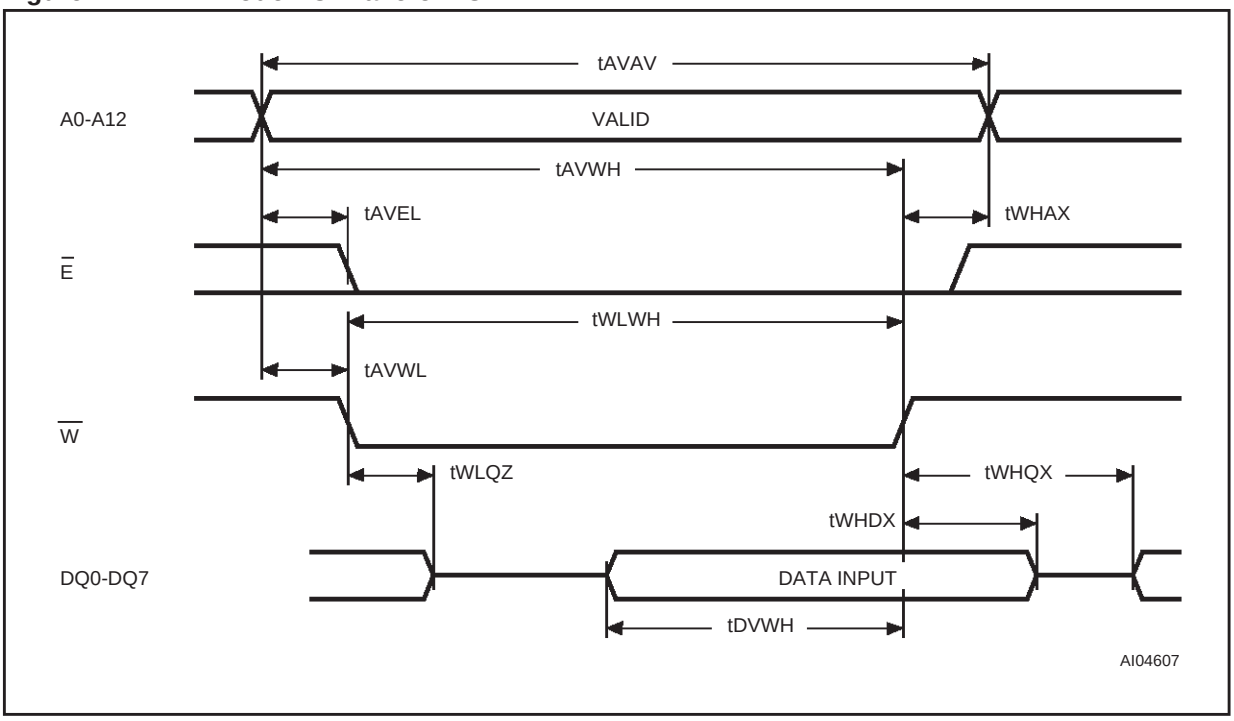


Figure 8. Chip Enable Controlled, WRITE Mode AC Waveforms

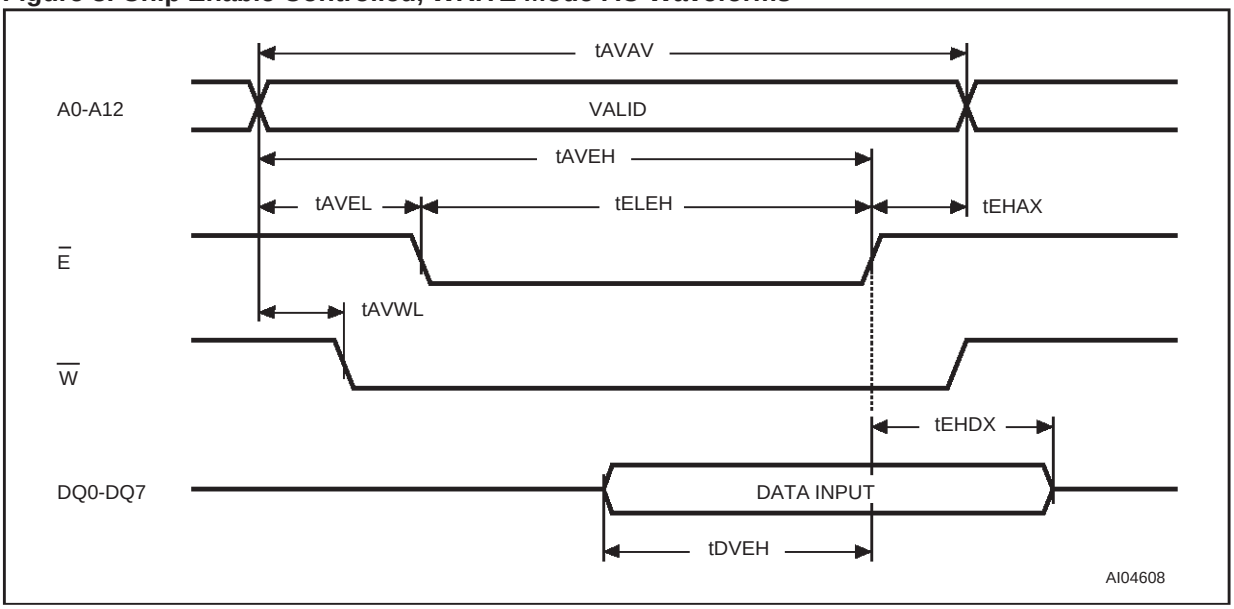


Table 8. WRITE Mode AC Characteristics

Symbol	Parameter[1]	M48ST59W		Unit
		–70 / –100		
		Min	Max	
t_{AVAV}	WRITE Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	WRITE Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	WRITE Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to WRITE Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	WRITE Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ}[2,3]	WRITE Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to WRITE Enable High	60		ns
t_{AVE1H}	Address Valid to Chip Enable High	60		ns
t_{WHQX}[2,3]	WRITE Enable High to Output Transition	5		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. C_L = 5pF (see Figure 5, page 7).
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Data Retention Mode

With valid V_{CC} applied, the M48ST59W operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “don’t care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM’s content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48ST59W may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48ST59W for an accumulated period of t_{DR} (at room temperature when V_{CC} is less than V_{SO}; see Table 9, page 14). As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Normal RAM operation can resume t_{REC} after V_{CC} reaches V_{PFD}(max).

For more information on Data Retention Storage Life refer to the Application Note AN1012.

Figure 9. Power Down/Up Mode AC Waveforms

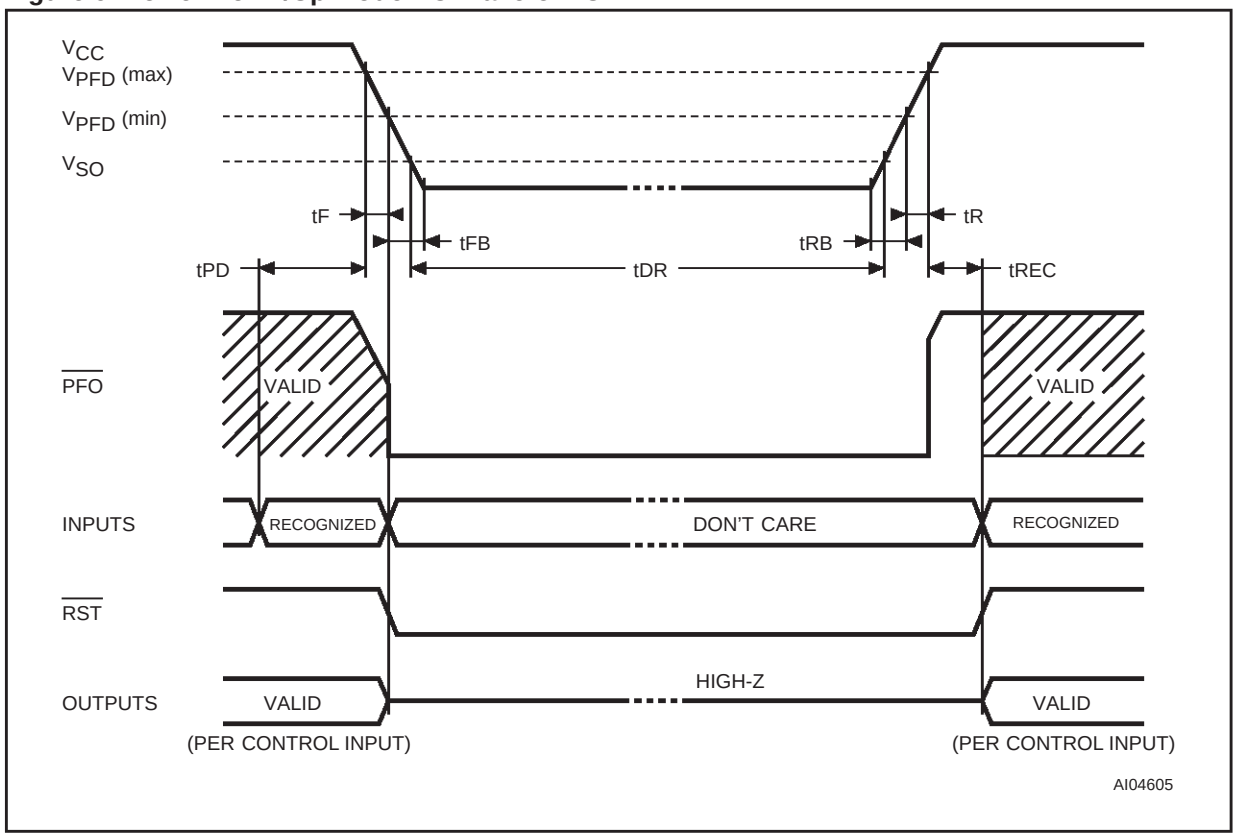


Table 9. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter[1,2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage		2.5	2.6	2.7	V
V_{SO}	Battery Back-up Switchover Voltage			V_{PFD} –100mV		mV
V_{PFI}	PFI Input Threshold		1.225	1.250	1.275	V
t_{DR}	Expected Data Retention Time (at 25 °C)	Grade 1	7			Years
		Grade 6[3]	10			Years

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. All voltages referenced to V_{SS}.
3. Using larger M4T32-BR12SH6 SNAPHAT top (recommended for Industrial Temperature Range - Grade 6 device).

Table 10. Power Down/Up AC Characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at VIH before Power Down	0			µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} Fall Time	10			µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	10			µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time	1			µs
t_{PFD}	PFI to $\overline{PFO}$ Propagation Delay		15	25	µs
t_{REC}[4]	V_{PFD} (max) to $\overline{RST}$ High		Note 4		ms

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) Fall Time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} Fall Time of less than t_{FB} may cause corruption of RAM data.
4. t_{REC} is undefined at initial power-up. Refer to Table 13, page 20.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER® registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT™ TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ Bit, D6 in the Control register (1FF8h). As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating occurs within a second after the bit is reset to a '0.'

Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE Bit. Setting the WRITE Bit to a '1,' like the READ Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 11, page 16).

Resetting the WRITE Bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE Bit is reset, the next clock update will occur within approximately one second.

Note: Upon power-up following a power failure, both the WRITE Bit and the READ Bit will be reset to '0'.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. When reset to a '0', the M48ST59W oscillator starts within one second.

Note: It is not necessary to set the WRITE Bit when setting or resetting the FREQUENCY TEST Bit (FT), the STOP Bit (ST) or the CENTURY ENABLE Bit (CEB).

Table 11. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	TR	FT	CB	CEB	0	Day			Century/ Day	00-01/ 01-07
1FFBh	0	0	10 Hours		Hours				Hours	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	
1FF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
1FF6h	AFE	Y	ABE	Y	Y	Y	Y	Y	Interrupts	
1FF5h	RPT4	Y	Al. 10 Date		Alarm Date				Alarm Date	01-31
1FF4h	RPT3	Y	Al. 10 Hours		Alarm Hours				Alarm Hours	00-23
1FF3h	RPT2	Alarm 10 Minutes			Alarm Minutes				Alarm Minutes	00-59
1FF2h	RPT1	Alarm 10 Seconds			Alarm Seconds				Alarm Seconds	00-59
1FF1h	Y	Y	Y	Y	Y	Y	Y	Y	Unused	
1FF0h	WDF	AF	Z	BL	Z	Z	Z	Z	Flags	

Keys: S = SIGN Bit
FT = FREQUENCY TEST Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'
Y = '1' or '0
Z = '0' and are Read only
AF = Alarm Flag
BL = Battery Low
WDS = Watchdog Steering Bit
BMB0-BMB4 = Watchdog Multiplier Bits
RB0-RB1 = Watchdog Resolution Bits
AFE = Alarm Flag Enable
ABE = Alarm in Battery Back-up Mode Enable
RPT1-RPT4 = Alarm Repeat Mode Bits
WDF = Watchdog Flag
CEB = Century Enable Bit
CB = Century Bit
TR = TREC Bit

Calibrating the Clock

The M48ST59W is driven by a quartz controlled oscillator with a nominal frequency of 32,768Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48ST59W improves to better than +1/–2 ppm at 25°C.

The oscillation rate of any crystal changes with temperature (see Figure 15, page 23). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48ST59W design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage (see Figure 16, page 23). The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five-bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control register (1FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles; for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48ST59W may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT pin. The pin will toggle at 512Hz when the Stop Bit (D7 of 1FF9h) is '0', the FT Bit (D6 of 1FFCh) is '1,' the AFE Bit (D7 of 1FF6h) is '0', and the Watchdog Steering Bit (D7 of 1FF7h) is '1' or the Watchdog Register is reset (1FF7h = 0).

Any deviation from 512Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The $\overline{IRQ}$/FT pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time. The FT Bit is cleared on power-down.

Note: For more information on calibration, see the Application Note AN934, "TIMEKEEPER Calibration."

Setting Alarm Clock

Registers 1FF5h-1FF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific day of the month or repeat every month, day, hour, minute, or second. It can also be programmed to go off while the M48ST59W is in the battery back-up mode of operation to serve as a system wake-up call.

RPT1-RPT4 put the alarm in the repeat mode of operation. Possible configurations are shown in Table 12. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

Note: The user must transition address (or toggle chip enable) to see the Flag Bit change.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT1-RPT4, AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT pin. To disable alarm, write '0' to the Alarm Date register and RPT1-4. The alarm flag and the $\overline{IRQ}$/FT output are cleared by a READ to the Flags Register.

The $\overline{IRQ}$/FT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE Bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48ST59W was in the deselect mode during power-up. Figure 10 illustrates the back-up mode alarm timing.

Programmable Interrupts

The M48ST59W provides two programmable interrupts; an alarm and a watchdog. When an interrupt condition occurs, the M48ST59W sets the appropriate flag bit in the Flag Register 1FF0h. The interrupt enable Bits (AFE and ABE) in 1FF6h and the Watchdog Steering Bit ($\overline{WDS}$) in 1FF7h allow the interrupt to activate the $\overline{IRQ}$/FT pin.

The interrupt flags and the $\overline{IRQ}$/FT output are cleared by a READ to the Flags Register. An interrupt condition reset will not occur unless the addresses are stable at the flag location for at least 15ns while the device is in the READ Mode (see Figure 11, page 19).

The $\overline{IRQ}$/FT pin is an open drain output and requires a pull-up resistor (10kΩ recommended) to V_{CC}. The pin remains in the high impedance state unless an interrupt occurs or the frequency test mode is enabled.

Table 12. Alarm Repeat Mode

RPT4	RPT3	RPT2	RPT1	Alarm Activated
1	1	1	1	Once per Second
1	1	1	0	Once per Minute
1	1	0	0	Once per Hour
1	0	0	0	Once per Day
0	0	0	0	Once per Month

Figure 10. Back-up Mode Alarm Waveform

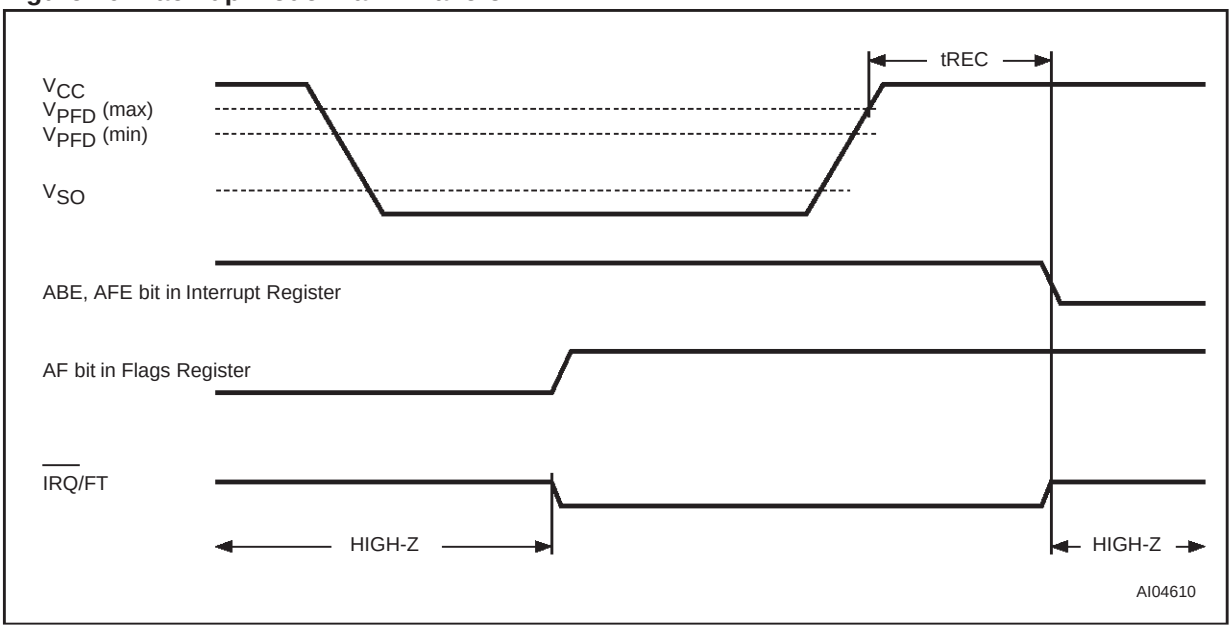
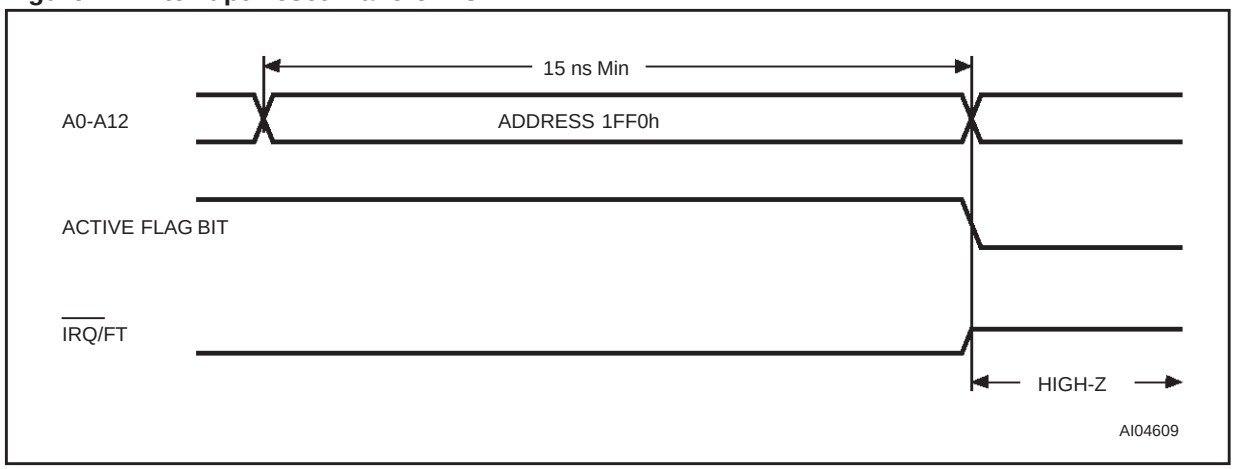


Figure 11. Interrupt Reset Waveforms



Watchdog Timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the eight-bit Watchdog Register (Address 1FF7h). The five bits (BMB4-BMB0) store a binary multiplier and the two lower order bits (RB1-RB0) select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3 x 1 or 3 seconds).

Note: Accuracy of timer is a function of the selected resolution.

If the processor does not reset the timer within the specified period, the M48ST59W sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset. The WDF is reset by reading the Flags Register (Address 1FF0h).

The most significant bit of the Watchdog Register is the Watchdog Steering Bit. When set to a '0,' the watchdog will activate the $\overline{IRQ}$/FT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for a duration of 40ms to 200ms. The Watchdog register and the FT Bit will reset to a '0' at the end of a watchdog time-out when the WDS Bit is set to a '1.'

The watchdog timer resets when the microprocessor performs a re-write of the Watchdog Register. The time-out period then starts over. Should the watchdog timer time-out, a value of 00h needs to be written to the Watchdog Register in order to clear the $\overline{IRQ}$/FT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the Flags Register will reset the Watchdog Flag (D7, Register 1FF0h). The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT pin and the frequency test function is activated, the watchdog or alarm function prevails and the frequency test function is denied.

Power-on Reset

The M48ST59W continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{REC} (see Table 13, page 20) after V_{CC} passes V_{PFD}. The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control rise time.

Battery Low Flag

The M48ST59W automatically performs periodic battery voltage monitoring upon power-up and at factory-programmed time intervals of 24 hours (at day rollover) as long as the device is powered and the oscillator is running. The Battery Low flag (BL), Bit D4 of the Flags Register 1FF0h, will be asserted high if the SNAPHAT® battery is found to be less than approximately 2.5V. The BL Flag will remain active until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery voltage is below 2.5V (approximately), which may be insufficient to maintain data integrity. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data has not been compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, it is recommended that the battery be replaced. The SNAPHAT® top may be replaced while V_{CC} is applied to the device.

Note: This will cause the clock to lose time during the interval the SNAPHAT battery/crystal top is disconnected.

Note: Battery monitoring is a useful technique only when performed periodically. The M48ST59W only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

Century Bit

Bits D5 and D4 of Clock Register 1FFCh contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

Note: The WRITE Bit must be set in order to write to the CENTURY Bit.

Initial Power-On Defaults

Upon application of power to the device, the following register bits are set to a '0' state: WDS; BMB0-BMB4; RB0-RB1; AFE; ABE; W; R; and FT (see Table 14):

TREC Bit

Bit D7 of Clock Register 1FFCh contains the TREC Bit (TR). TREC refers to the automatic continuation of the deselect time after V_{CC} reaches V_{PFD} (max). This allows for a voltage settling time before WRITEs may again be performed to the device after a power-down condition. The TREC Bit will allow the user to set the length of this deselect time as defined by Table 13.

Table 13. t_{REC} Definitions POWER-ON

TREC Bit (TR)	t_{REC} Time(1)
0	40 ms to 200 ms
1	2 ms (max)

Note: 1. Initial default is undefined.

Table 14. Default Values

Condition	W	R	FT	AFE	ABE	WATCHDOG(1) Register
Initial Power-up (Battery Attach for SNAPHAT)(2)	0	0	0	0	0	0
Subsequent Power-up / RESET(3)	0	0	0	0	0	0
Power-down(4)	0	0	0	1	1	0

Note: 1. WDS, BMB0-BMB4, RBO, RB1.
2. State of other control bits undefined.
3. State of other control bits remains unchanged.
4. Assuming these bits set to '1' prior to power-down.

Power-Fail Comparator

The Power-Fail Input (PFI) is compared to an internal reference voltage (independent from the V_{PFD} comparator). If PFI is less than the power-fail threshold (V_{PFI}), the Power-Fail Output ($\overline{PFO}$) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the M48ST59W or the microprocessor drops below the minimum operating voltage.

During battery back-up, the power-fail comparator turns off and $\overline{PFO}$ goes (or remains) low. This occurs after V_{CC} drops below V_{PFD}(min). When power returns, $\overline{PFO}$ is forced high, irrespective of V_{PFI} for the write protect time (t_{REC}), which is the time from V_{PFD} (max) until the inputs are recognized. At the end of this time, the power-fail comparator is enabled and $\overline{PFO}$ follows PFI. If the comparator is unused, PFI should be connected to V_{SS} and $\overline{PFO}$ left unconnected.

Hysteresis may be added to PFI for additional noise margin if desired (see Figure 12). The ratio of R1 and R2 should be selected such that PFI sees V_{PFI} when V_{IN} falls to its trip point (V_{TRIP}). Connecting R3 between PFI and $\overline{PFO}$ provides the hysteresis and should typically be more than ten (10) times the value of R1 or R2. The hysteresis window will extend both above (V_H) and below (V_L) the original trip point (V_t). Connecting an ordinary signal diode in series with R3 causes the lower trip point (V_L) to coincide with the trip point without hysteresis, so the entire hysteresis window occurs above V_{TRIP} (see Figure 13, page 22). This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. The current through R1 and R2 should be at least 1uA to ensure that the 25nA PFI input current does not shift the trip point. R3 should be larger than 82K Ohms to avoid loading down the $\overline{PFO}$ pin. The capacitor C1 is added for noise rejection, but is optional.

Figure 12. Adding Hysteresis

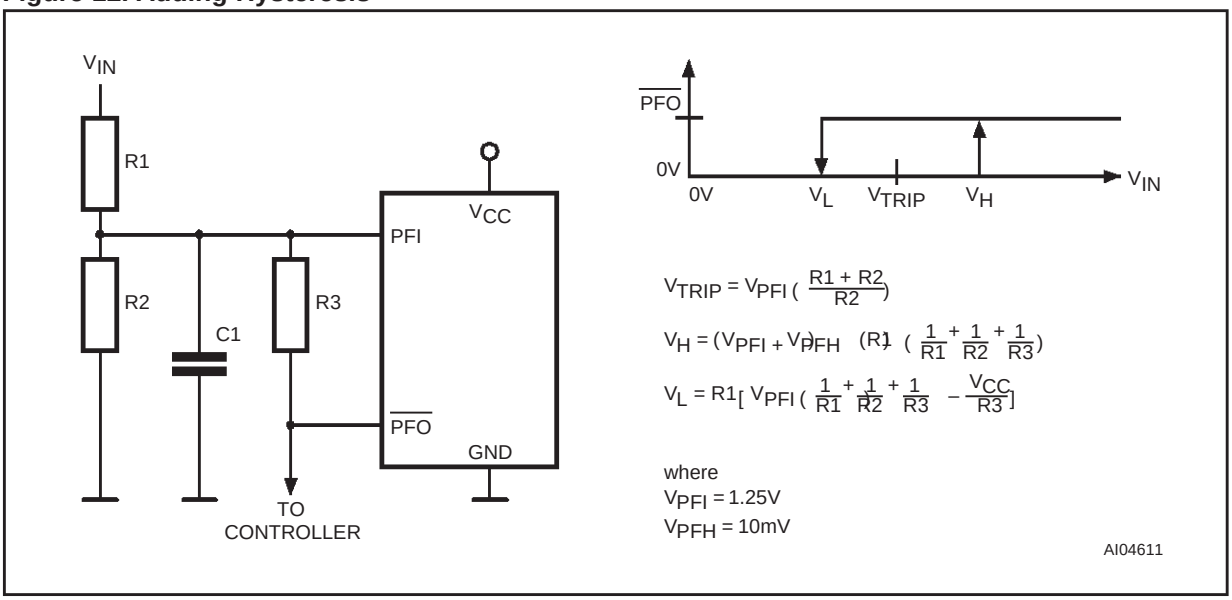
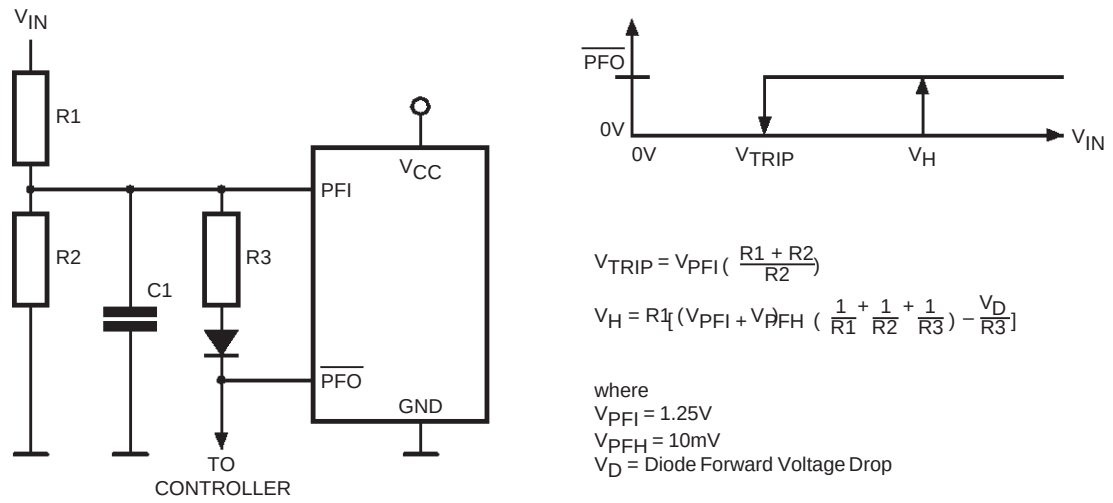


Figure 13. Hysteresis on Rising V_{IN}



Power Supply Decoupling and Undershoot Protection

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (see Figure 14) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 14. Supply Voltage Protection

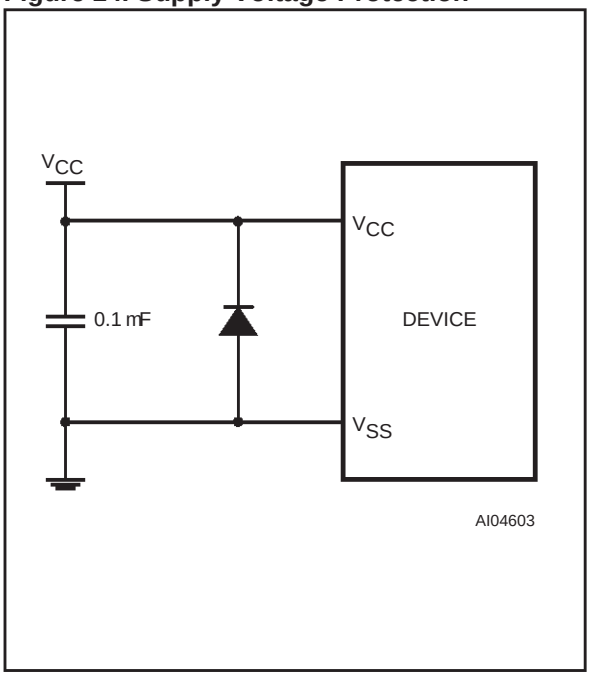


Figure 15. Crystal Accuracy Across Temperature

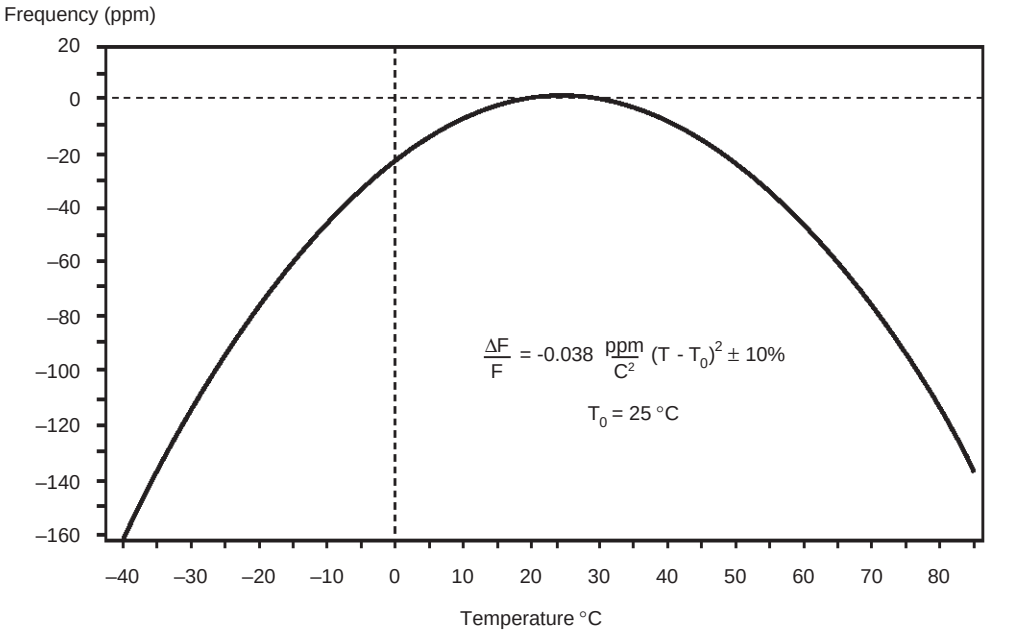
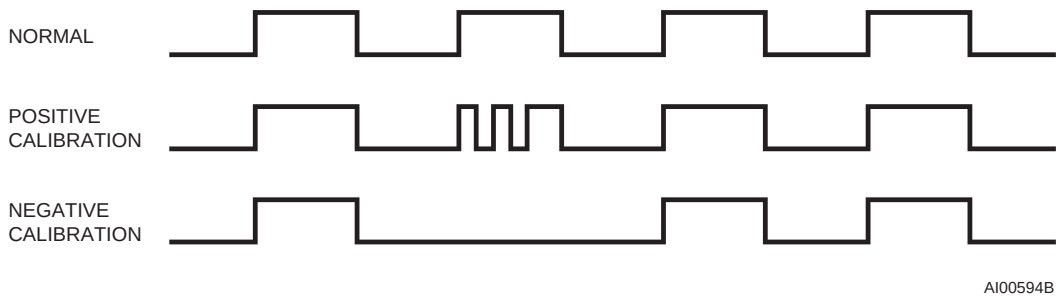


Figure 16. Clock Calibration



PART NUMBERING

Table 15. Ordering Information Scheme

Example: M48ST 59W –70 MH 1 TR

Device Type

M48ST

Supply Voltage and Write Protect Voltage

59W = V_{CC} = 2.7 to 3.6V; V_{PFD} = 2.5 to 2.7V

Speed

–70 = 70ns

–100 = 100ns

Package

MH(1) = SOH44

Temperature Range

1 = 0 to 70°C

6 = –40 to 85°C

Shipping Method for SOIC

blank = Tubes

TR = Tape & Reel

Note: 1. The SOIC package (SOH44) requires the battery crystal package (SNAPHAT®) which is ordered separately under part number "M4TXX-BR12SHX" in plastic tube or "M4TXX-BR12SHXTR" in Tape & Reel form.

Caution: Do not place the SNAPHAT battery/crystal package "M4TXX-BR12SHX" in conductive foam as it will drain the lithium button-cell battery.

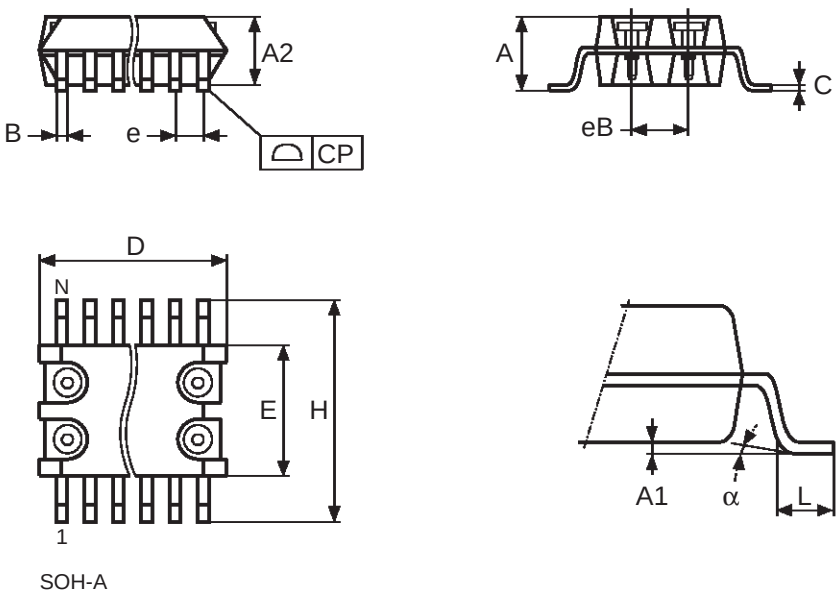
For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 16. SNAPHAT Battery Table

Part Number	Description	Package
M4T28-BR12SH	Lithium Battery (48mAh) SNAPHAT	SH
M4T32-BR12SH	Lithium Battery (120mAh) SNAPHAT	SH

PACKAGE MECHANICAL INFORMATION

Figure 17. SO44 – 44-lead Plastic Small Outline, Package Outline

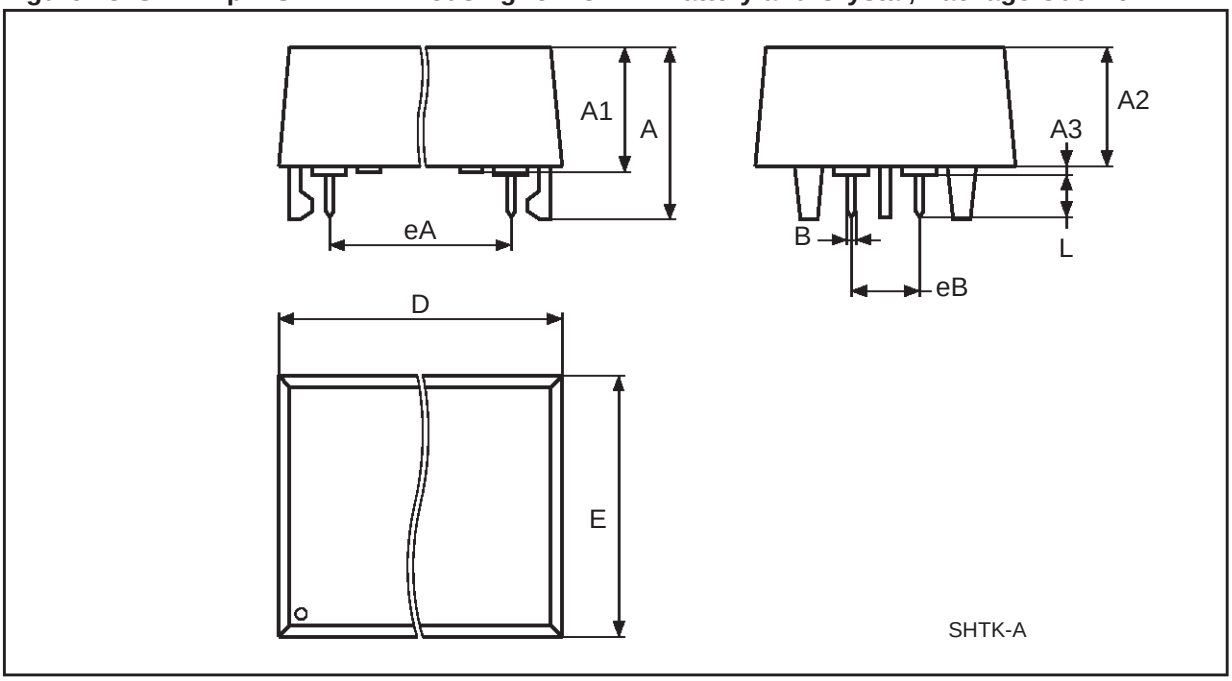


Note: Drawing is not to scale.

Table 17. SOH44 – 44-lead Plastic Small Outline, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05		0	0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.46		0.014	0.018
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	0.81	–	–	0.032	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	44			44		
CP			0.10			0.004

Figure 18. SH – 4-pin SNAPHAT Housing for 48mAh Battery and Crystal, Package Outline

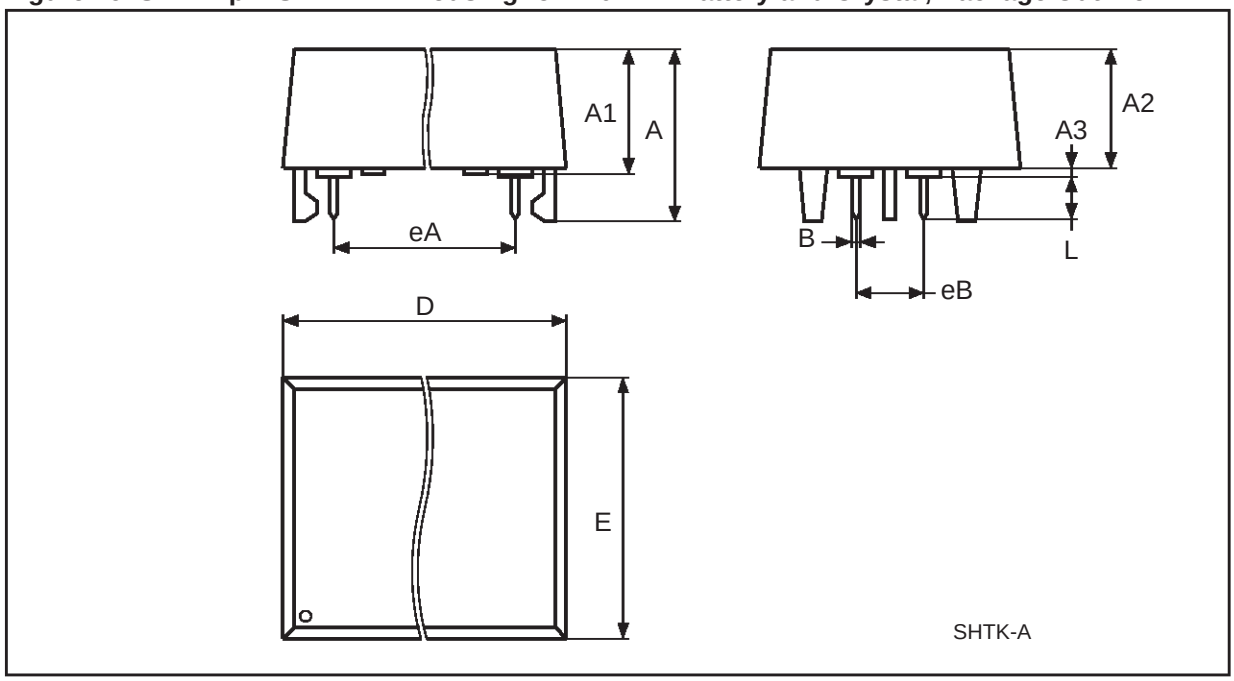


Note: Drawing is not to scale.

Table 18. SH – 4-pin SNAPHAT Housing for 48mAh Battery and Crystal, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78		0	0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38		0	0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA						
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 19. SH – 4-pin SNAPHAT Housing for 120mAh Battery and Crystal, Package Outline



Note: Drawing is not to scale.

Table 19. SH – 4-pin SNAPHAT Housing for 120mAh Battery and Crystal, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54		0	0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38		0	0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

REVISION HISTORY

Table 20. Document Revision History

Date	Revision Details
September 2000	First cut
10/10/00	First markups entered, text added, graphics changed
12/18/00	Reformatted, TOC added, and PFI I_{LI} added (Table 5)
07/31/01	Temp/Voltage information added to tables (Table 4, 5, 7, 8, 9, 10)