

# T6A92

## COLUMN DRIVER LSI FOR A DOT MATRIX LCD

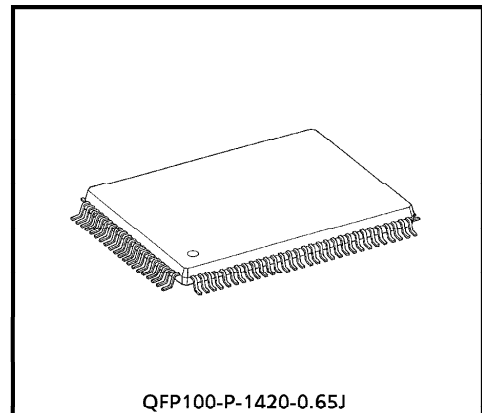
The T6A92 is a column driver with 80 output channels for a medium- or small-scale dot matrix LCD.

The T6A92 realizes low power LCD systems using the CMOS Si-Gate process.

The T6A92 has two types of data flow.

① O<sub>1</sub>→O<sub>80</sub>, ② O<sub>80</sub>→O<sub>1</sub>

The T6A92 can be connected to extension drivers like the T6A39.



Weight: 1.6g (typ.)

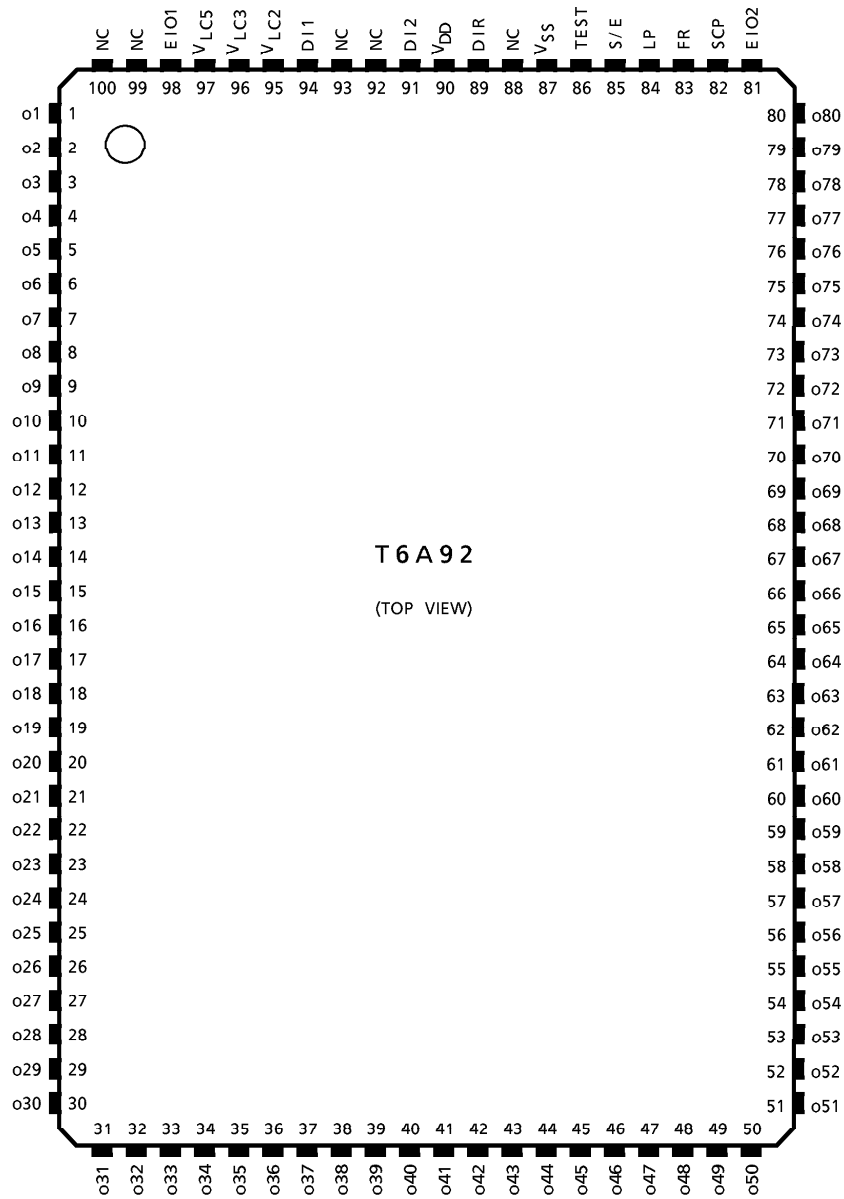
### FEATURES

- 80-output column driver
- Data input format : 1-bit (ENABLE mode)  
: 2-bit (SHIFT mode)
- Two types of data flow :
  - ① O<sub>1</sub>→O<sub>80</sub>
  - ② O<sub>80</sub>→O<sub>1</sub>
- Low power consumption
- Power supply : 5 V ± 10%
- 100-pin plastic flat package

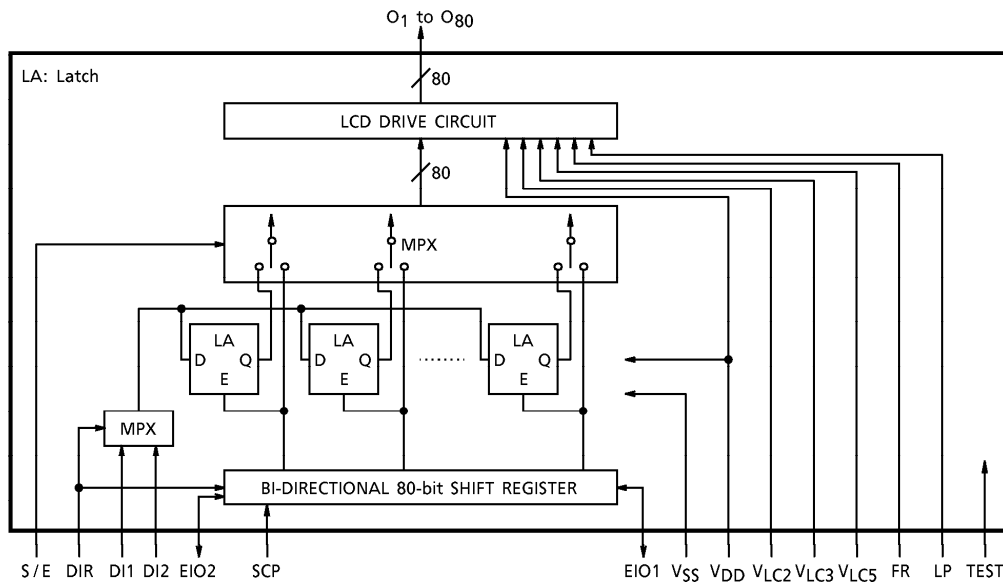
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PIN ASSIGNMENT



BLOCK DIAGRAM



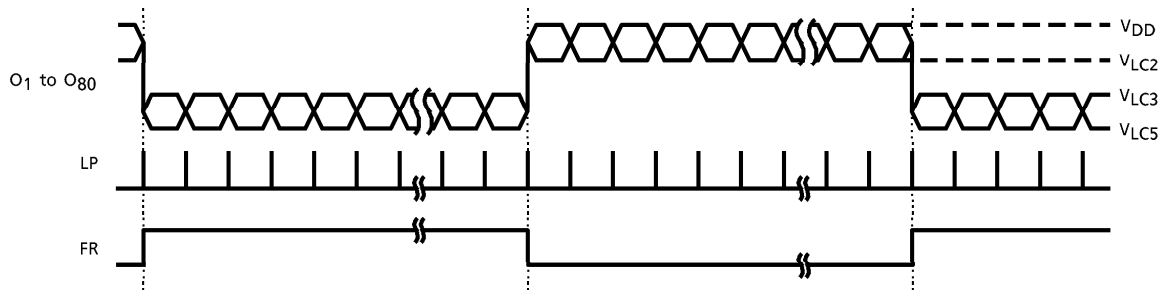
PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1 to O80	Output	LCD drive signal output	$V_{DD}$ to $V_{LC5}$
DI1, DI2	Input	Data signal input	$V_{DD}$ to $V_{SS}$
EIO1, EIO2	I/O	ENABLE signal input/output When S/E = H, this pin is for input.	
SCP	Input	(Shift Clock Pulse) Shift clock pulse input	
FR	Input	(Frame) Frame signal input	
LP	Input	(Latch Pulse) Latch pulse signal input	
S/E	Input	Input for mode selection	
DIR	Input	Input data flow direction select	
TEST	Input	Test pin: usually connected to $V_{SS}$ (0V)	
$V_{LC2, 3, 5}$	—	Power supply for LCD drive	—
$V_{DD}$	—	Power supply (5V)	
$V_{SS}$	—	Power supply (0V)	

**FUNCTION OF DATA AND ENABLE PINS**

S/E DIR	DI1	DI2	EIO1	EIO2	DATA FLOW	FIRST DATA	LAST DATA	MODE
L   L	Open	DATA INPUT	ENABLE signal input	ENABLE signal output	O <sub>80</sub> →O <sub>1</sub>	O <sub>1</sub>	O <sub>80</sub>	ENABLE
L   H	DATA INPUT	Open	ENABLE signal output	ENABLE signal input	O <sub>1</sub> →O <sub>80</sub>	O <sub>80</sub>	O <sub>1</sub>	
H   L	Open	Open	DATA INPUT	DATA OUTPUT	O <sub>1</sub> →O <sub>80</sub>	O <sub>80</sub>	O <sub>1</sub>	SHIFT
H   H	Open	Open	DATA OUTPUT	DATA INPUT	O <sub>80</sub> →O <sub>1</sub>	O <sub>1</sub>	O <sub>80</sub>	

**TIMING DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)**

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V <sub>DD</sub> (Note 1)	-0.3 to 7.0	V
Supply Voltage (2)	V <sub>LC2</sub> , V <sub>LC3</sub> , V <sub>LC5</sub> (Note 1, 2)	-0.3 to 7.0	V
Input Voltage	V <sub>IN</sub> (Note 1)	-0.3 to V <sub>DD</sub> + 0.3	V
Operating Temperature	T <sub>opr</sub>	-20 to 75	°C
Storage Temperature	T <sub>stg</sub>	-55 to 125	°C

(Note 1) Referenced to V<sub>SS</sub> = 0V

(Note 2) Ensure that the following condition is always maintained.

$$V_{DD} \geq V_{LC2} \geq V_{LC3} \geq V_{LC5}$$

**ELECTRICAL CHARACTERISTICS**

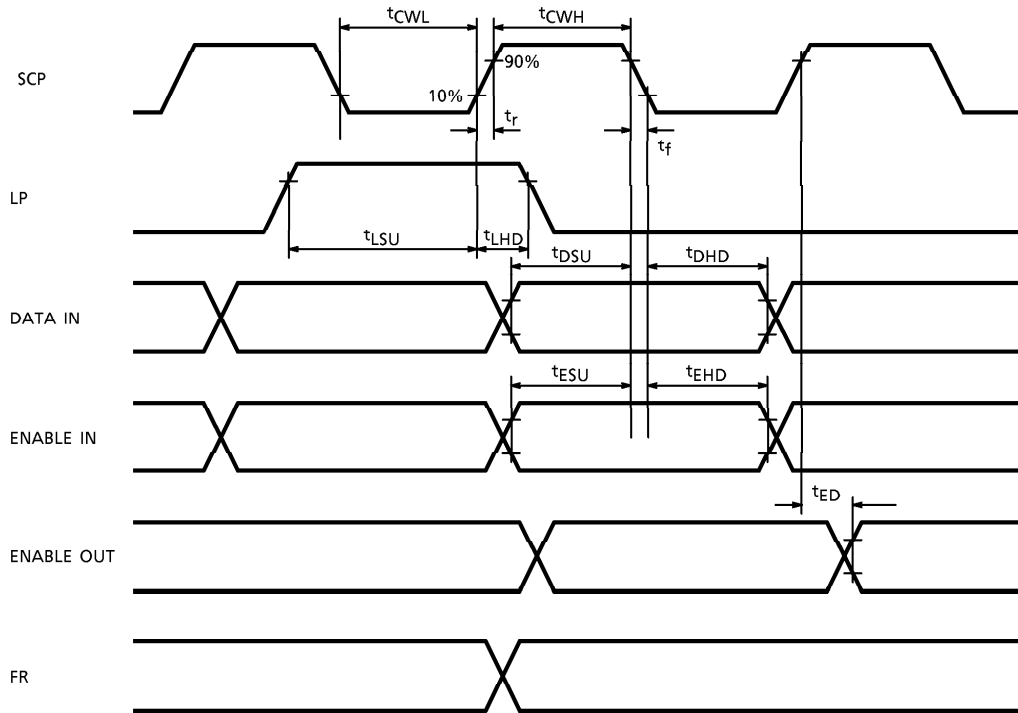
**DC CHARACTERISTICS**

TEST CONDITIONS (Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 5.0V \pm 10\%$ ,  $V_{LC5} = 0V$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM		SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME		
Operating Voltage (1)		—	—	—	4.5	5.0	5.5	V	$V_{DD}$		
Operating Voltage (2)		—	—	—	0	—	$V_{DD} - 3.0$	V	$V_{LC5}$		
Input Voltage	H Level	$V_{IH}$	—	—	$V_{DD} - 1.0$	—	$V_{DD}$	V	(*)		
	L Level	$V_{IL}$	—	—	0	—	1.0	V	(*)		
Output Voltage	H Level	$V_{OH}$	—	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$	—	$V_{DD}$	V	EIO1, EIO2		
	L Level	$V_{OL}$	—	$I_{OH} = 0.4mA$	0	—	0.4	V	EIO1, EIO2		
Output Resistance		$R_{COL}$	—	$I_d = \pm 50\mu A$	—	—	30	$k\Omega$	O <sub>1</sub> to O <sub>80</sub>		
Operating Frequency		$f_{scp}$	—	$T_a = -20$ to $75^\circ C$	—	—	400	kHz	SCP		
Current Consumption	$I_{SS}$	—	—	$V_{DD} = 5.0V$ $V_{LC2} = 3.0V$ $V_{LC3} = 2.0V$ $V_{LC5} = 0.0V$ $f_{FR} = 39Hz$ $f_{scp} = 250kHz$ O <sub>1</sub> to O <sub>80</sub> : No Load	Binary Data Input		—	—	1.0	mA	$V_{SS}$
					Input Data : LOW Constant		—	—	0.4	mA	

(\*) SCP, LP, FR, EIO1, EIO2, DI1, DI2, DIR, S/E, TEST

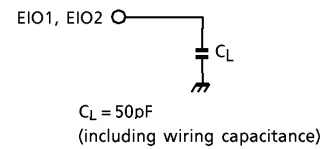
AC CHARACTERISTICS



TEST CONDITIONS ( $V_{SS} = 0V$ ,  $V_{DD} = 5V \pm 10\%$ ,  $V_{LC5} = 0V$ ,  $T_a = -20$  to  $75^\circ C$ )

LOAD CIRCUIT

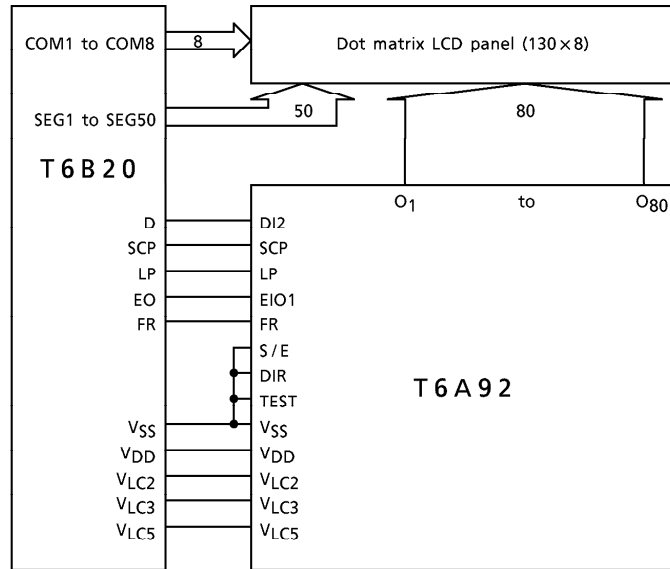
ITEM	SYMBOL	MIN	MAX	UNIT
Operating Frequency	$f_{scp}$	—	400	kHz
SCP Pulse Width	$t_{CWH}, t_{CWL}$	800	—	ns
SCP Rise / Fall Time	$t_r, t_f$	—	200	ns
LP Set-up Time	$t_{LSU}$	500	—	ns
LP Hold Time	$t_{LHD}$	—	10	ns
Data Set-up Time	$t_{DSU}$ (Note 1)	300	—	ns
Data Hold Time	$t_{DHD}$ (Note 1)	300	—	ns
Enable Set-up Time	$t_{ESU}$ (Note 2)	300	—	ns
Enable Hold Time	$t_{EHD}$ (Note 2)	300	—	ns
Enable Delay Time	$t_{ED}$ (Note 3)	—	500	ns



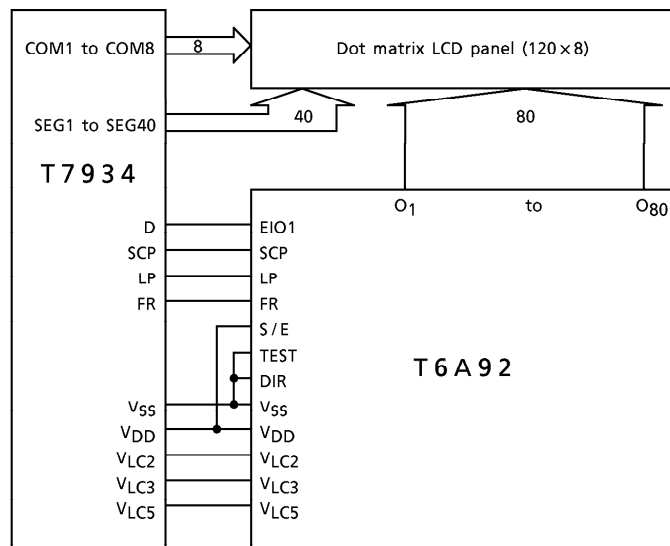
- (Note 1) Applies to DI1 and DI2
- (Note 2) Applies to EIO1 and EIO2
- (Note 3) With load circuit connected

**APPLICATION CIRCUIT**

- S/E=L (ENABLE mode)

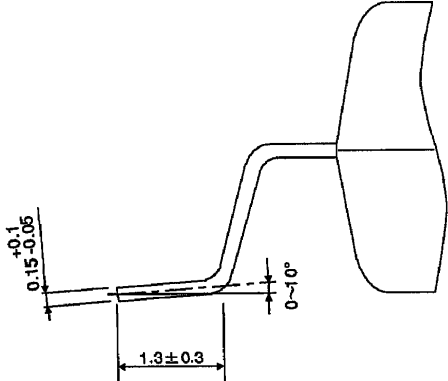
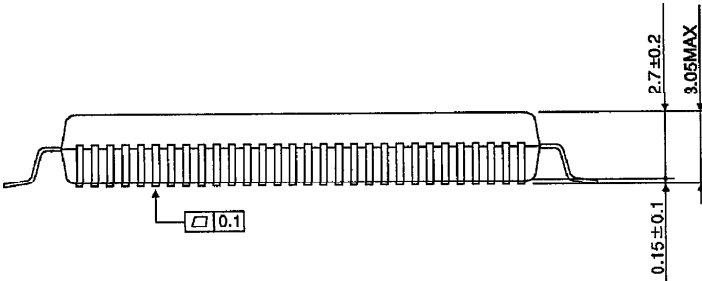
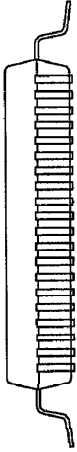
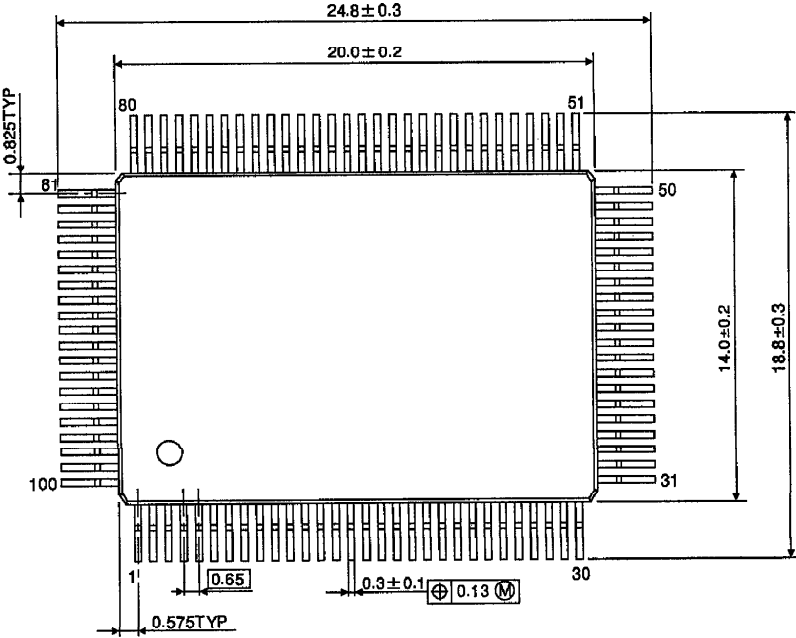


- S/E=H (SHIFT mode)



OUTLINE DRAWING  
QFP100-P-1420-0.65J

Unit : mm



Weight : 1.6g (Typ.)