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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2869

Silicon N Channel MOS FET High Speed Power Switching

RENESAS

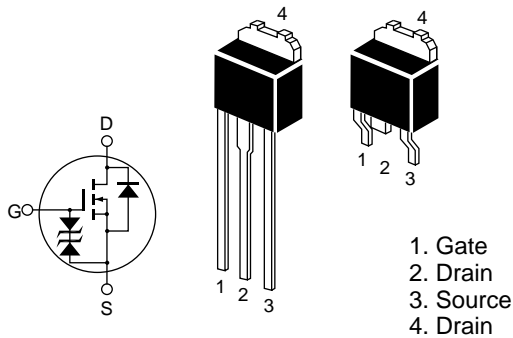
ADE-208-570 (Z)
1st. Edition
Sep. 1997

Features

- Low on-resistance
 $R_{DS} = 0.033 \Omega$ typ.
- High speed switching
- 4V gate drive device can be driven from 5V source

Outline

DPAK-2



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}^{*1}$	80	A
Body to drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP}^{*3}	20	A
Avalanche energy	E_{AR}^{*3}	34	mJ
Channel dissipation	P_{ch}^{*2}	30	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

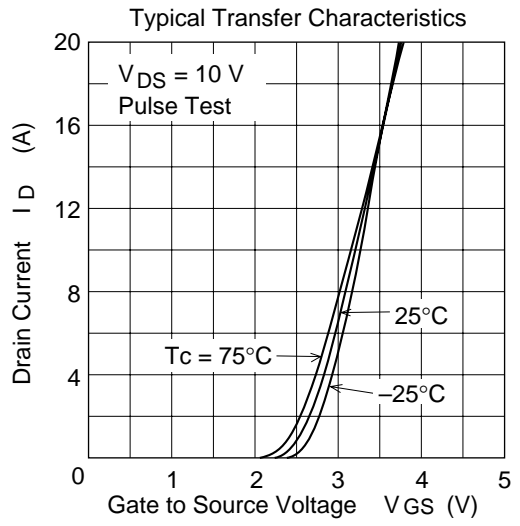
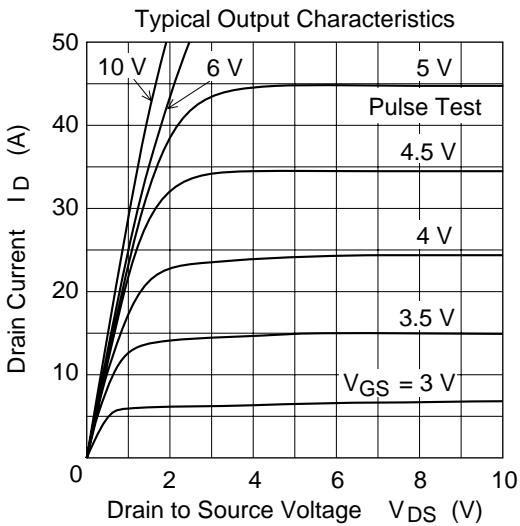
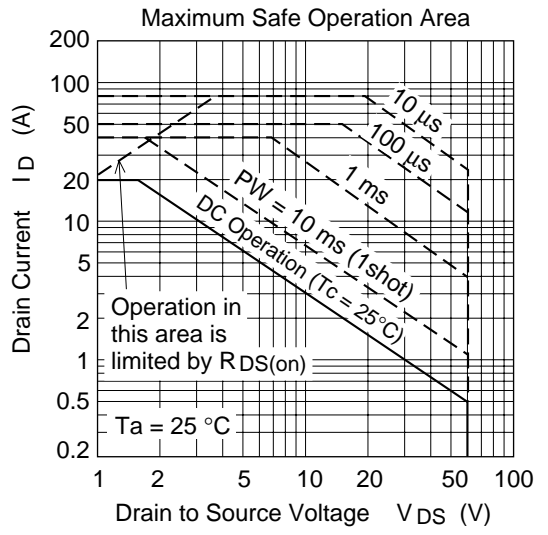
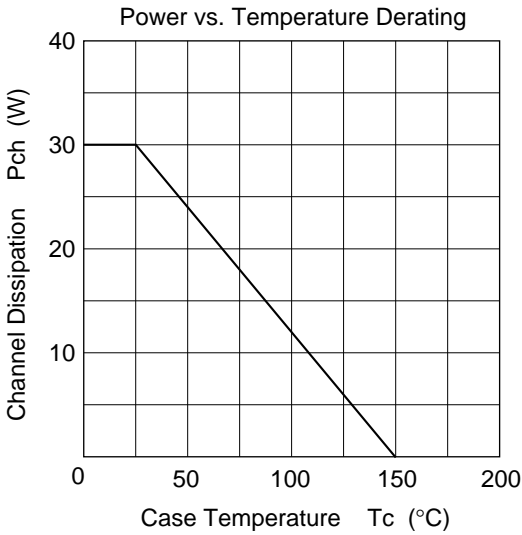
- Notes: 1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ\text{C}$
3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50\Omega$

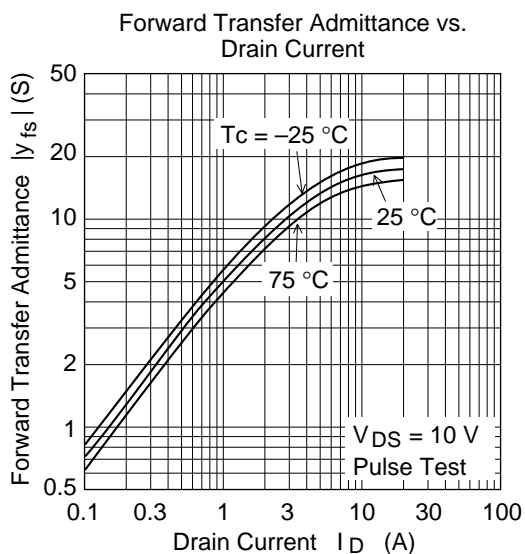
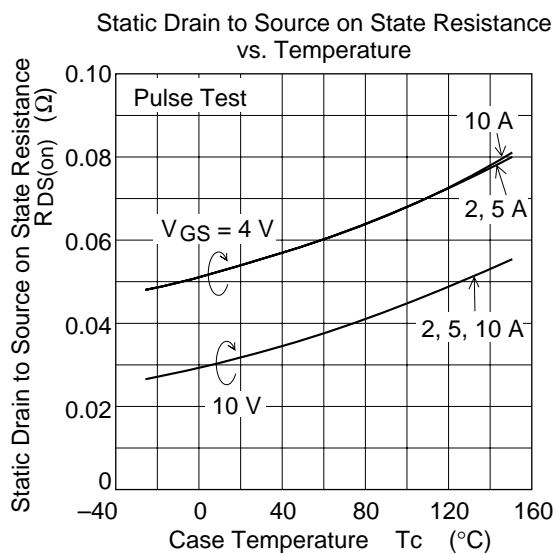
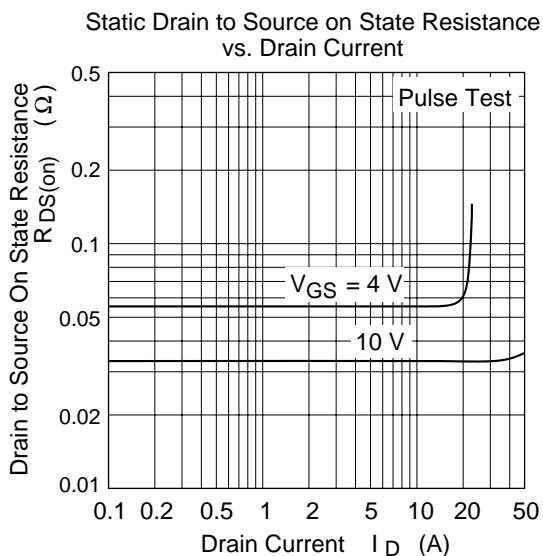
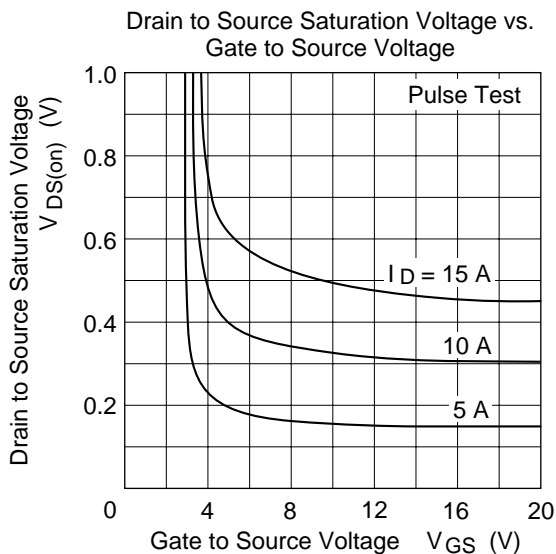
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10mA, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = ±100μA, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = ±16V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1mA, V_{DS} = 10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.045	Ω	$I_D = 10A, V_{GS} = 10V^{*1}$
	$R_{DS(on)}$	—	0.055	0.07	Ω	$I_D = 10A, V_{GS} = 4V^{*1}$
Forward transfer admittance	$ y_{fs} $	10	16	—	S	$I_D = 10A, V_{DS} = 10V^{*1}$
Input capacitance	C_{iss}	—	740	—	pF	$V_{DS} = 10V$
Output capacitance	C_{oss}	—	380	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	140	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = 10A, V_{GS} = 10V$
Rise time	t_r	—	110	—	ns	$R_L = 3Ω$
Turn-off delay time	$t_{d(off)}$	—	105	—	ns	
Fall time	t_f	—	120	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	$I_F = 20A, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	40	—	V	$I_F = 20A, V_{GS} = 0$ $diF/dt = 50A/μs$

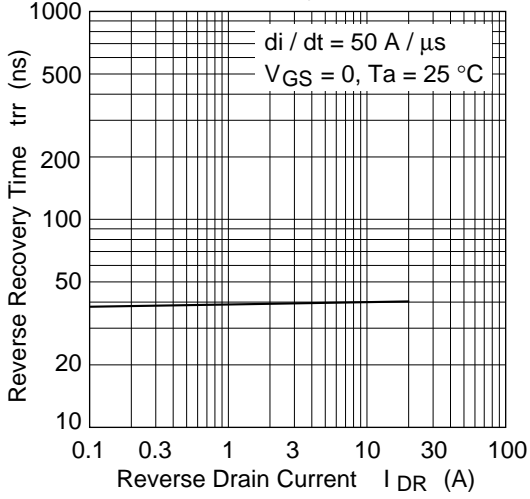
Note: 1. Pulse test

Main Characteristics

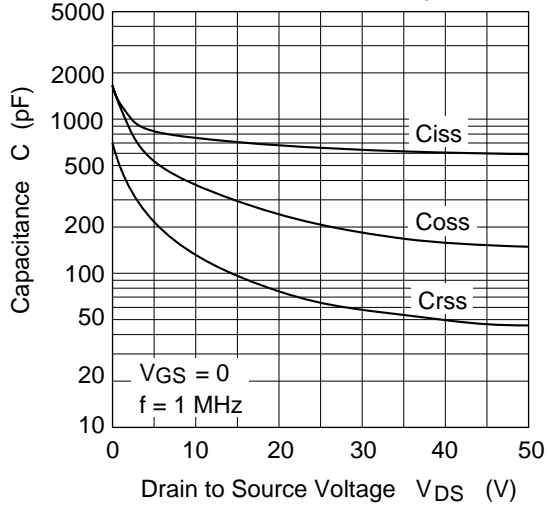




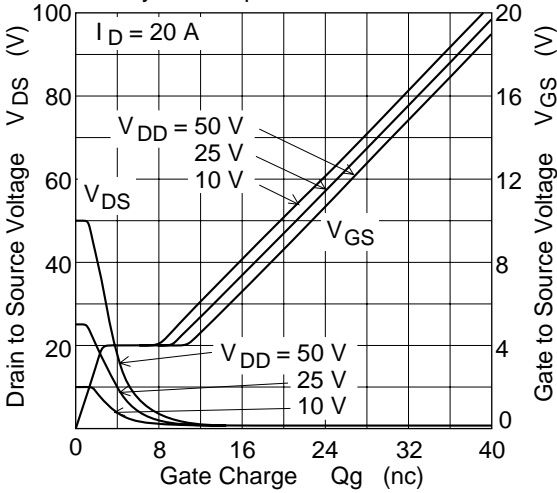
Body to Drain Diode Reverse Recovery Time



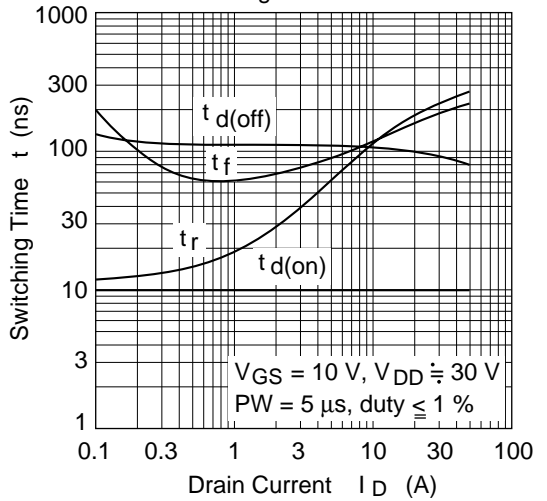
Typical Capacitance vs. Drain to Source Voltage

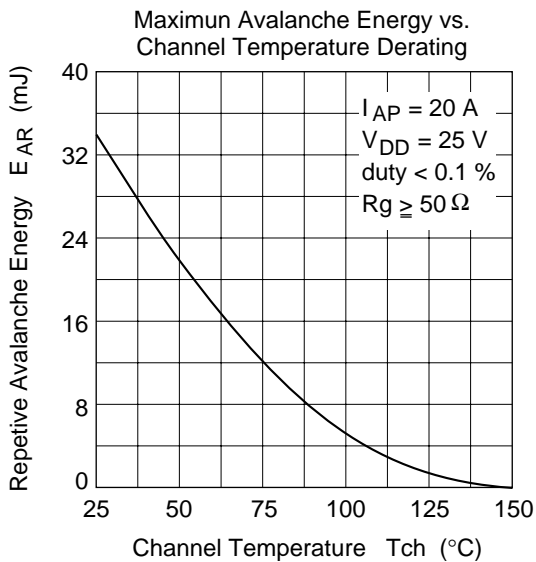
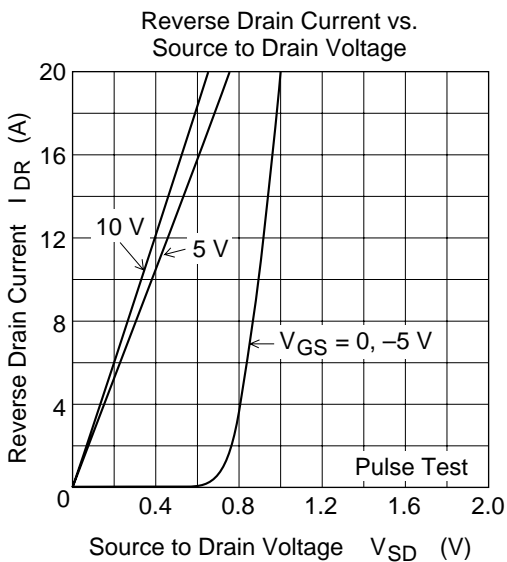


Dynamic Input Characteristics



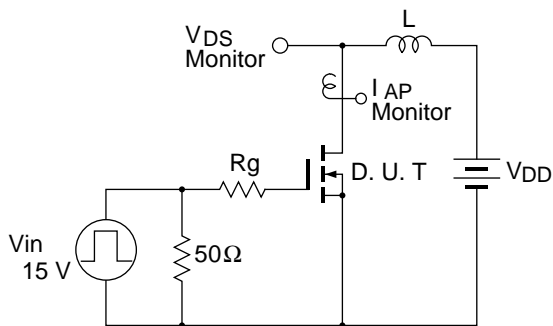
Switching Characteristics



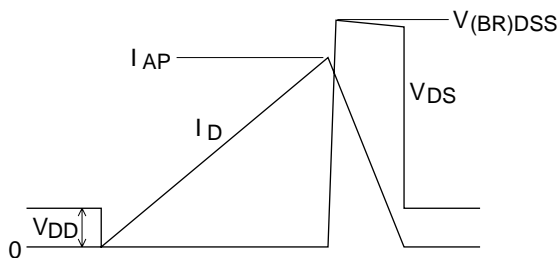


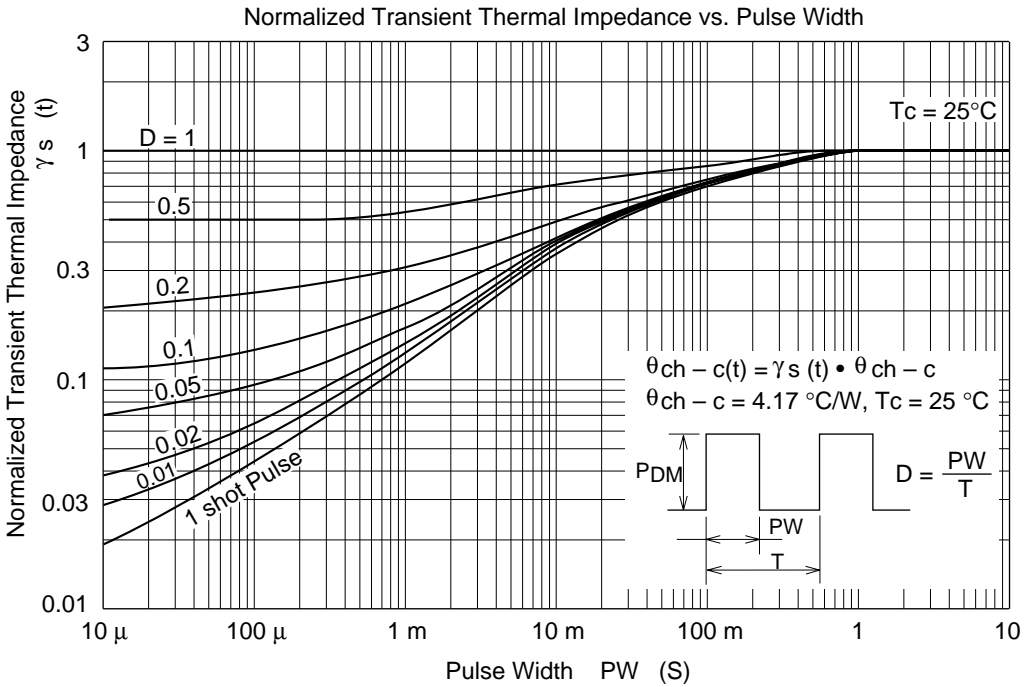
Avalanche Test Circuit

Avalanche Waveform

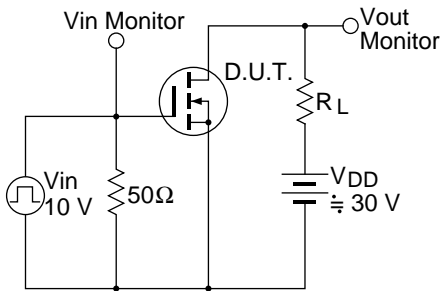


$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

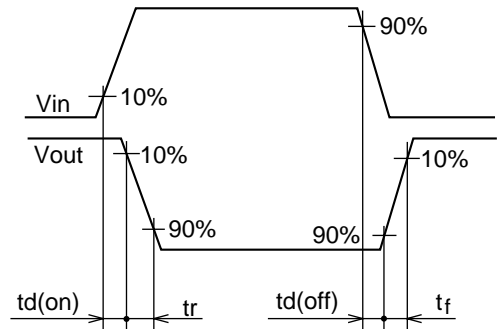




Switching Time Test Circuit



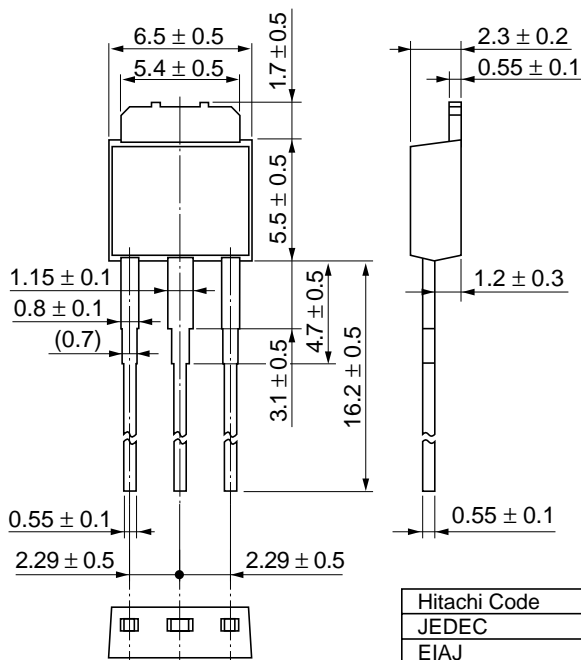
Waveform



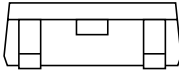
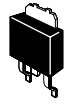
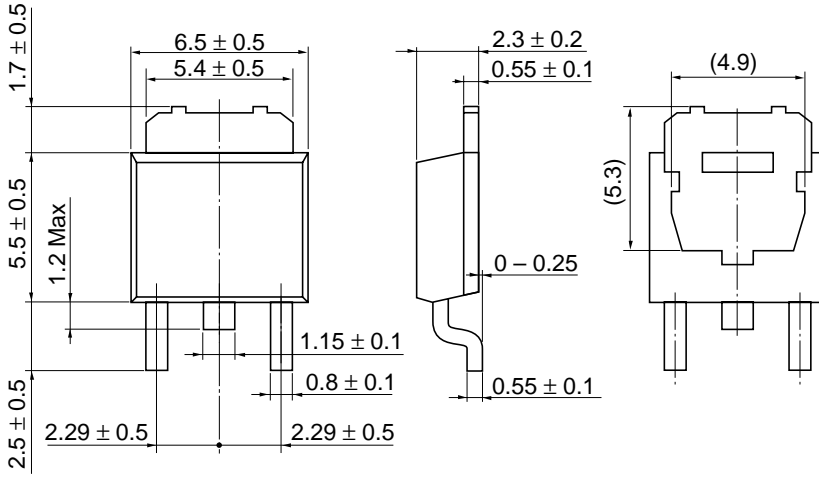
Package Dimensions

As of January, 2001

Unit: mm



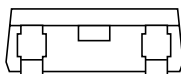
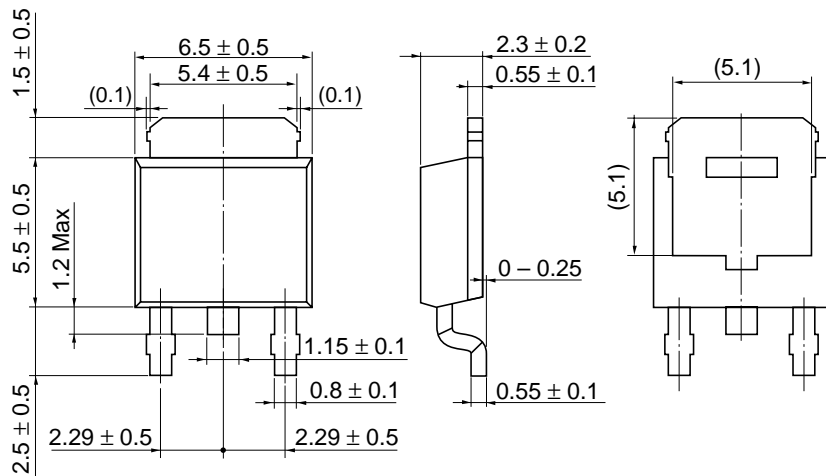
Hitachi Code	DPAK (L)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	0.42 g



Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001

Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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Colophon 2.0