



FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTER

IDT54/74FCT163T/AT/CT

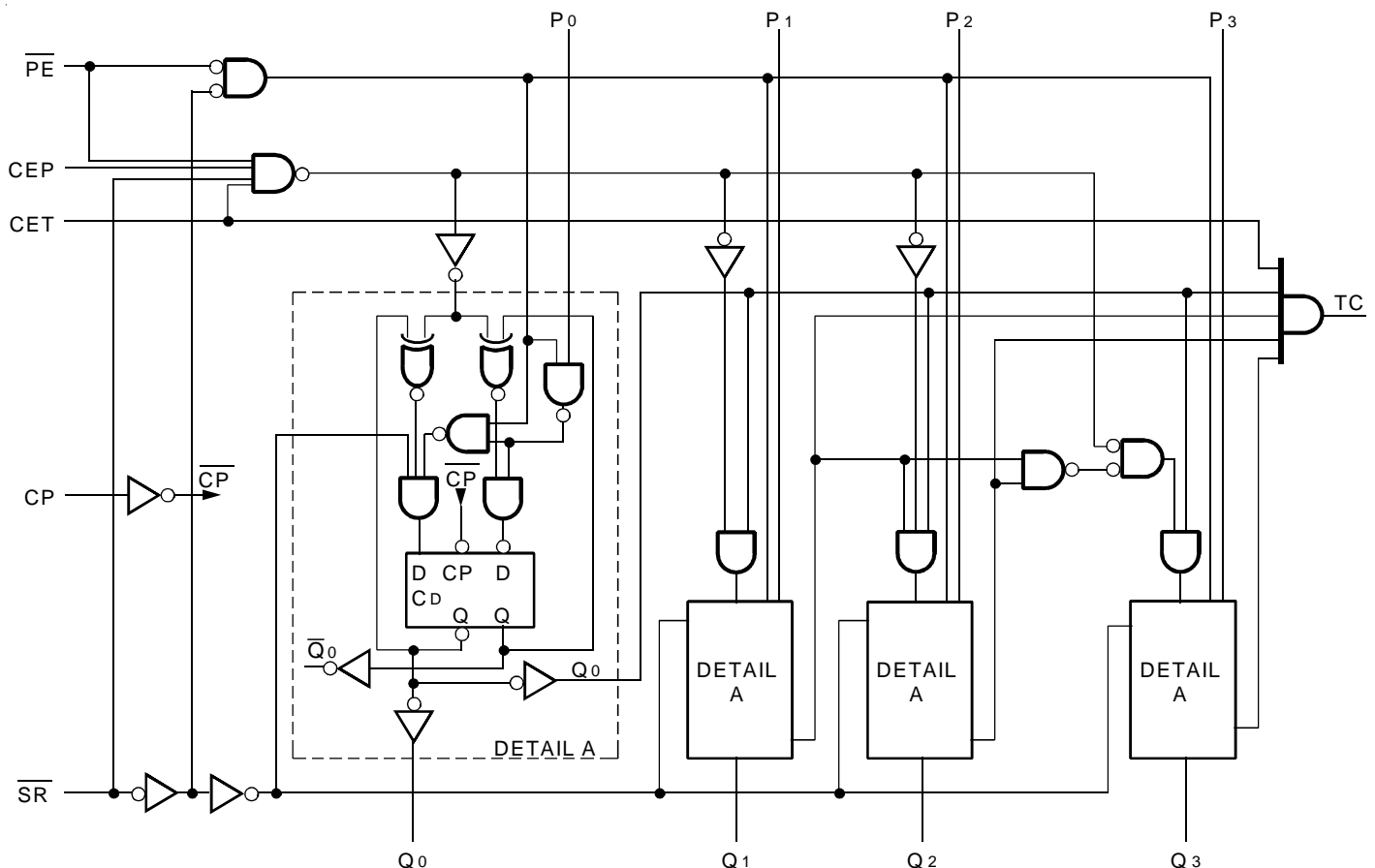
FEATURES:

- Std., A, and C grades
- Low input and output $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- High Drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Power off disable outputs permit "live insertion"
- Available in the following packages:
 - Industrial: SOIC, QSOP
 - Military: CERDIP, LCC

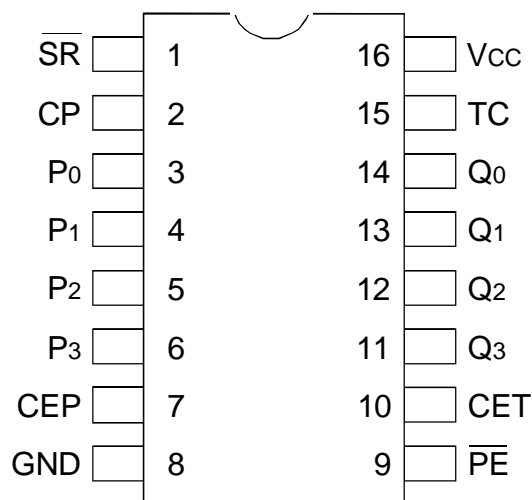
DESCRIPTION:

The FCT163T is a high-speed synchronous modulo-16 binary counter built using an advanced dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The FCT163T has Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

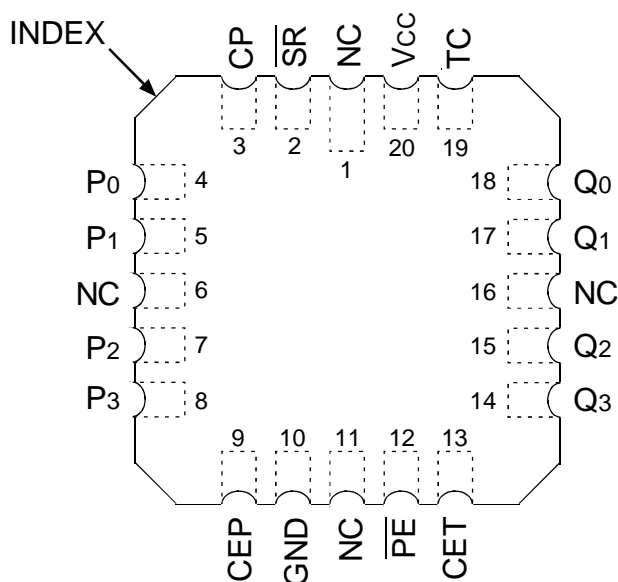
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CERDIP/ SOIC/ QSOP
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by =0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
\overline{SR}	Synchronous Reset Input (Active LOW)
P0-3	Parallel Data Inputs
\overline{PE}	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

FUNCTION TABLE⁽¹⁾

\overline{SR}	\overline{PE}	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P _x →Q _x)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	MIL	2.7	—	—	V
			IND ⁽⁵⁾	2	—	—	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6\text{mA MIL}$ $I_{OH} = -8\text{mA IND}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL}$ $I_{OH} = -15\text{mA IND}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 32\text{mA MIL}$ $I_{OL} = 48\text{mA IND}$	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	μA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
5. Clock pin requires a minimum V_{IH} of 2.5V

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2	mA	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open Load Mode $CEP = CET = \overline{PE} = GND$ $\overline{SR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.15	0.25 mA/ MHz	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $CEP = CET = \overline{PE} = GND$ $\overline{SR} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	2	5.5	
		$V_{CC} = \text{Max.}$, Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $CEP = CET = \overline{PE} = GND$ $\overline{SR} = V_{CC}$ Four Bits Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	3.8	7.3 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	5	12.3 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

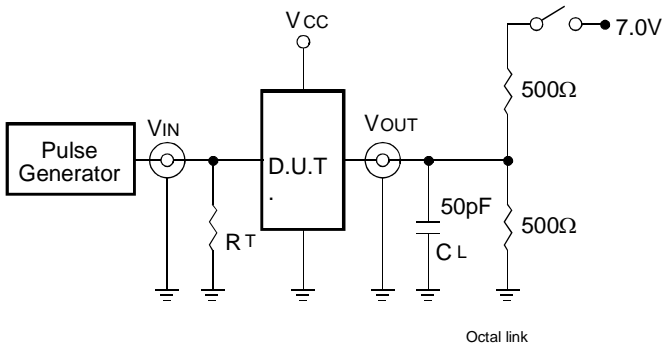
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	54FCT163T		54/74FCT163AT				54/74FCT163CT				Unit
			Mil.		Ind.		Mil.		Ind.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Qx (\overline{PE} input HIGH)	CL = 50pF RL = 500Ω	2	11.5	2	7.2	2	7.5	2	5.8	2	6.3	ns
t _{PLH} t _{PHL}	Propagation Delay CP to Qx (\overline{PE} input LOW)		2	10	2	6.2	2	6.5	2	5.8	2	6.3	ns
t _{PLH} t _{PHL}	Propagation Delay CP to TC		2	16.5	2	9.8	2	10.8	2	7.4	2	8.3	ns
t _{PLH} t _{PHL}	Propagation Delay CET to TC		1.5	9	1.5	5.5	1.5	5.9	1.5	5.2	1.5	5.6	ns
t _{SU}	Set-up Time HIGH or LOW Px to CP		5.5	—	4	—	4.5	—	4	—	4.5	—	ns
t _H	Hold Time HIGH or LOW Px to CP		2	—	1.5	—	2	—	1.5	—	2	—	ns
t _{SU}	Set-up Time HIGH or LOW \overline{PE} or \overline{SR} to CP		13.5	—	9.5	—	11.5	—	9.5	—	11.5	—	ns
t _H	Hold Time HIGH or LOW \overline{PE} or \overline{SR} to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _{SU}	Set-up Time HIGH or LOW CEP or CET to CP		13	—	9.5	—	11	—	9.5	—	11	—	ns
t _H	Hold Time HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	0	—	ns
t _w	CP Pulse Width (load) HIGH or LOW	5	—	4 ⁽³⁾	—	4 ⁽³⁾	—	4 ⁽³⁾	—	4 ⁽³⁾	—	ns	
t _w	CP Pulse Width (count) HIGH or LOW	8	—	6	—	7	—	6	—	7	—	ns	

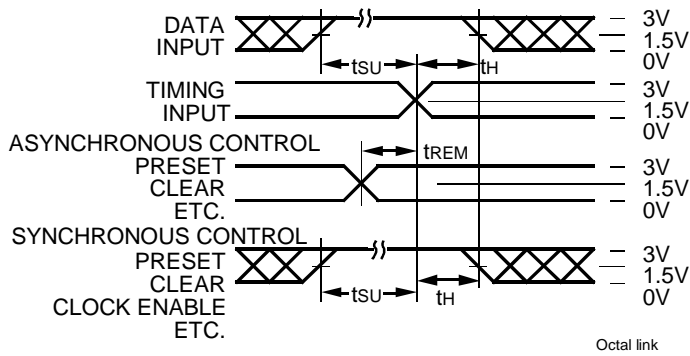
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

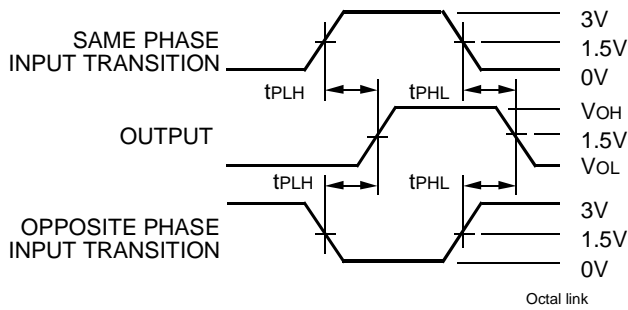
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



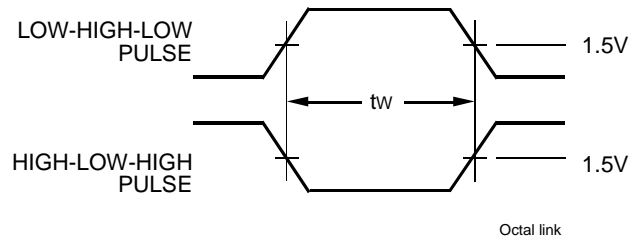
Propagation Delay

SWITCH POSITION

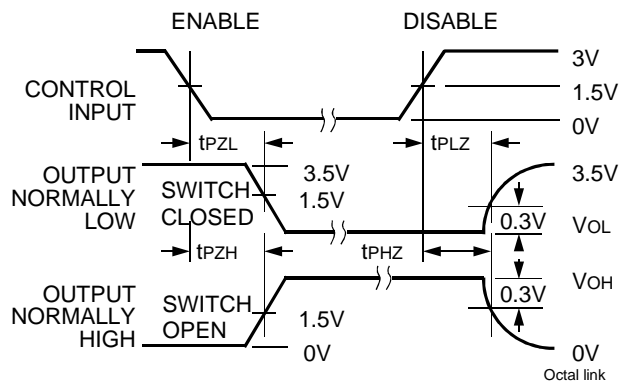
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

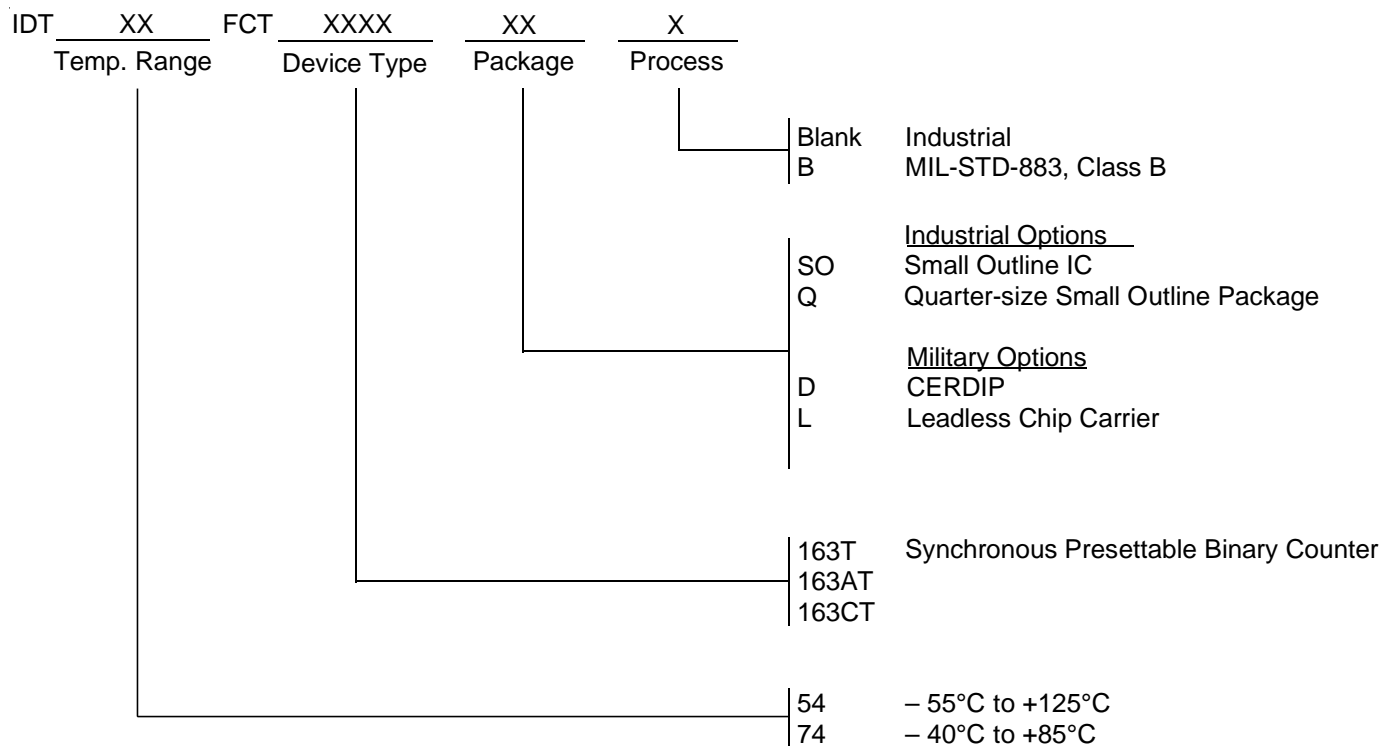


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/20/2002 Updated as per PDNs Logic-00-07 and Logic-01-04



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