

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# H5N2508DL, H5N2508DS

Silicon N Channel MOS FET  
High Speed Power Switching

**RENESAS**

ADE-208-1377 (Z)

1st. Edition

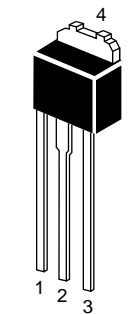
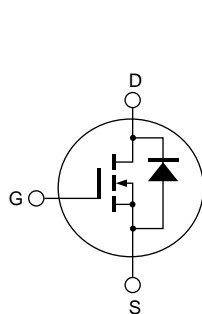
Mar. 2001

## Features

- Low on-resistance:  $R_{DS(on)} = 0.48 \Omega$  typ.
- Low leakage current:  $IDSS = 1 \mu A$  max (at  $V_{DS} = 250 V$ )
- High speed switching:  $t_f = 11 ns$  typ (at  $V_{GS} = 10 V$ ,  $V_{DD} = 125 V$ ,  $I_D = 3.5 A$ )
- Low gate charge:  $Q_g = 13 nC$  typ (at  $V_{DD} = 200 V$ ,  $V_{GS} = 10 V$ ,  $I_D = 7 A$ )
- Avalanche ratings

## Outline

DPAK-2



H5N2508DL



H5N2508DS

1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	250	V
Gate to source voltage	$V_{GSS}$	$\pm 30$	V
Drain current	$I_D$	7	A
Drain peak current	$I_{D (pulse)}^{Note1}$	28	A
Body-drain diode reverse drain current	$I_{DR}$	7	A
Body-drain diode reverse drain peak current	$I_{DR (pulse)}^{Note1}$	28	A
Avalanche current	$I_{AP}^{Note3}$	7	A
Channel dissipation	$P_{ch}^{Note2}$	30	W
Channel to case Thermal Impedance	$\theta_{ch-c}$	4.17	°C/W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. Value at  $T_c = 25^\circ C$

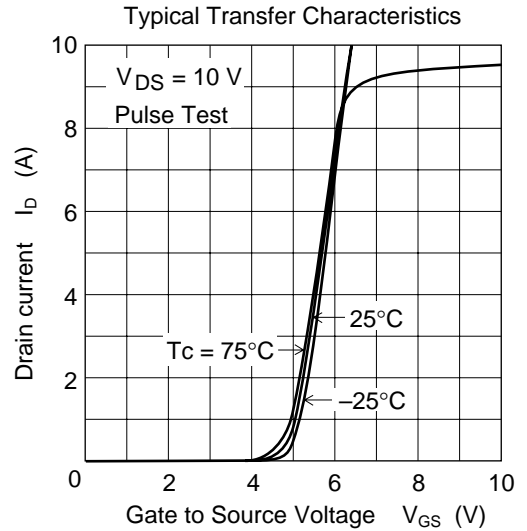
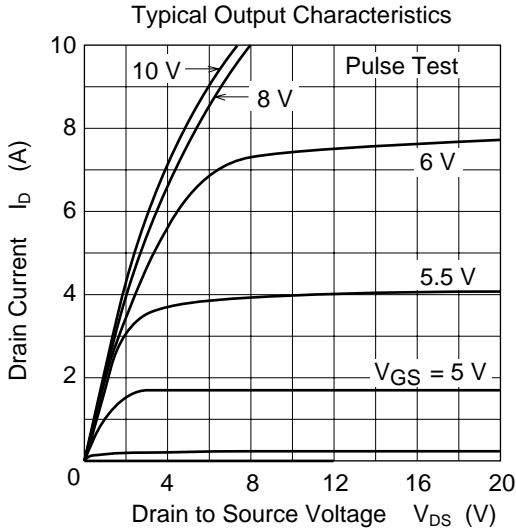
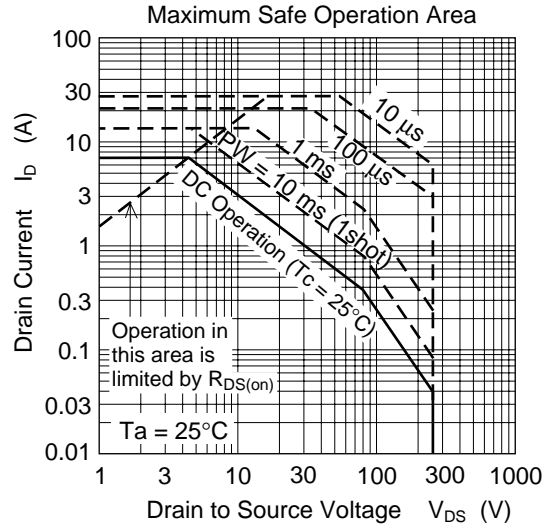
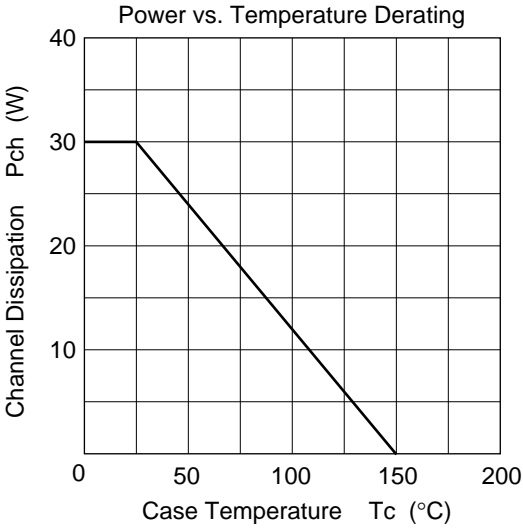
3.  $T_{ch} \leq 150^\circ C$

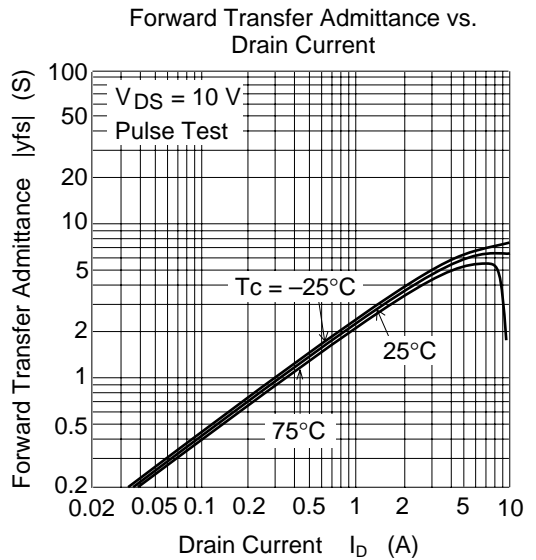
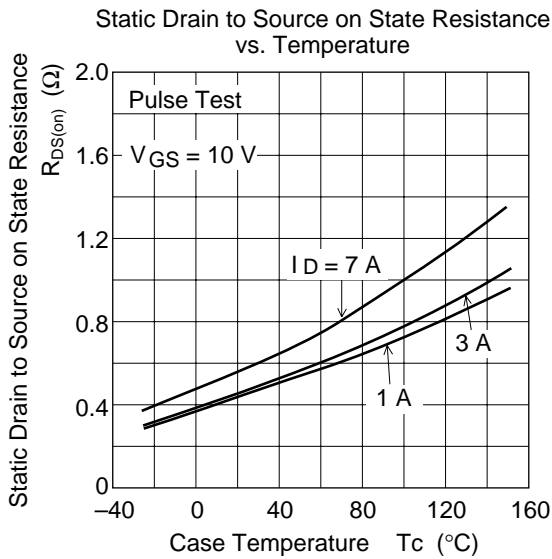
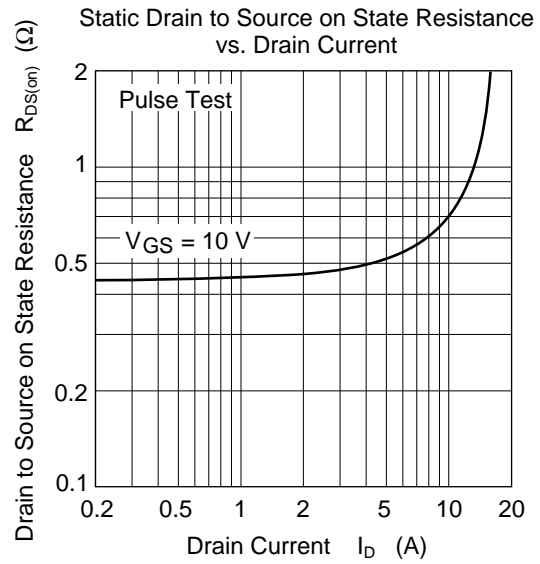
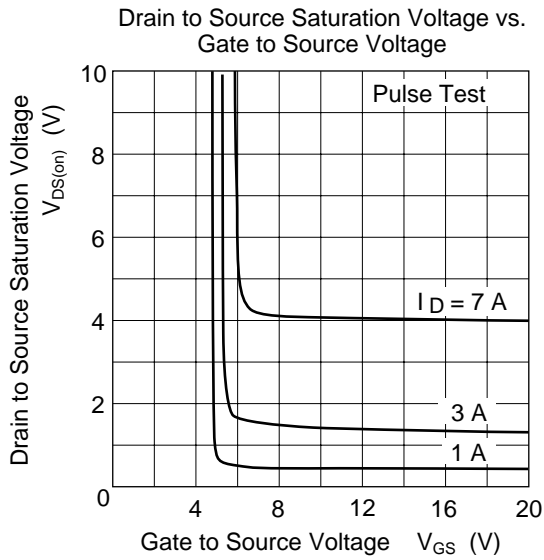
**Electrical Characteristics (Ta = 25°C)**

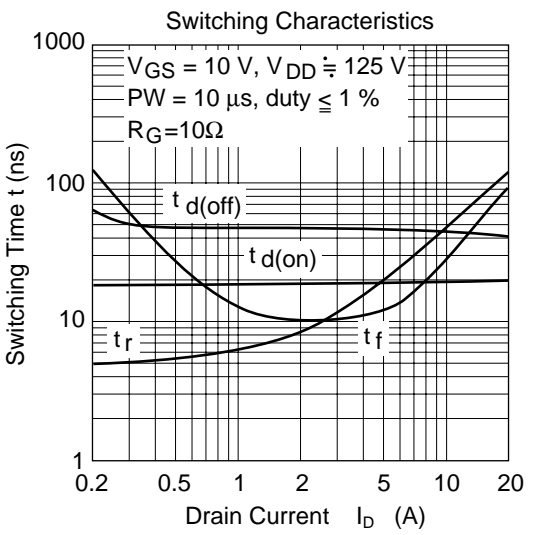
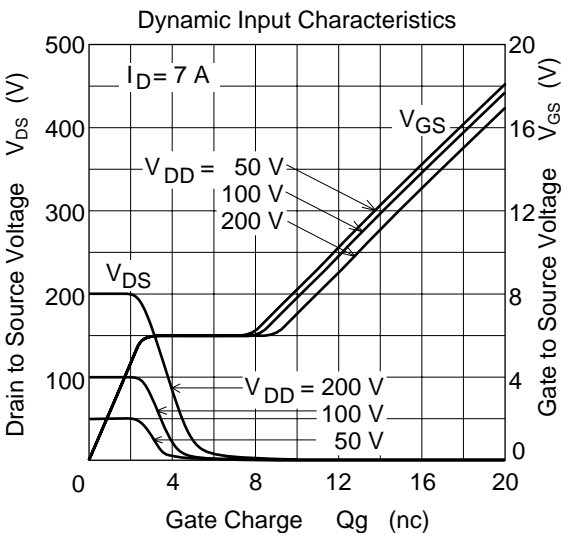
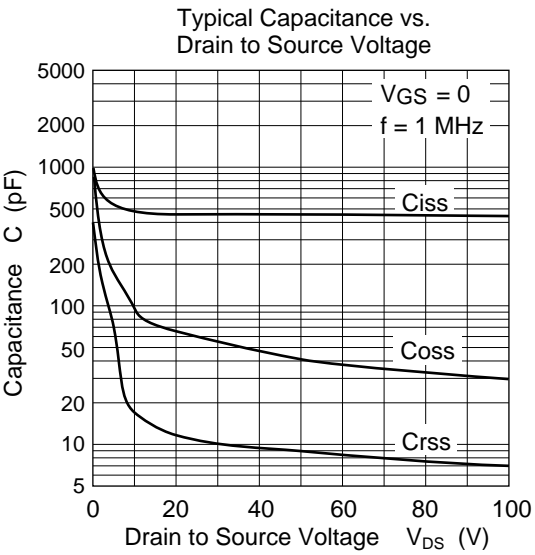
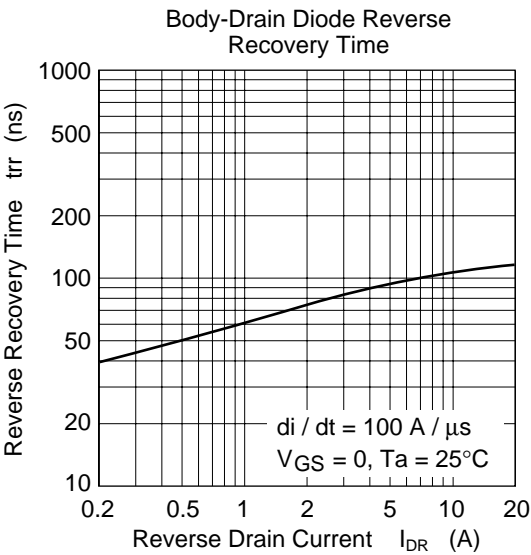
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 250 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.48	0.63	$\Omega$	$I_D = 3.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	3.0	5.0	—	S	$I_D = 3.5 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	450	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	$C_{oss}$	—	60	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	12	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	19	—	ns	$V_{DD} = 125 \text{ V}$ , $I_D = 3.5 \text{ A}$
Rise time	$t_r$	—	14	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	47	—	ns	$R_L = 35.7 \Omega$
Fall time	$t_f$	—	11	—	ns	$R_g = 10 \Omega$
Total gate charge	$Q_g$	—	13	—	nC	$V_{DD} = 200 \text{ V}$
Gate to source charge	$Q_{gs}$	—	2.5	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	6	—	nC	$I_D = 7 \text{ A}$
Body-drain diode forward voltage	$V_{DF}$	—	0.9	1.4	V	$I_F = 7 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	100	—	ns	$I_F = 7 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery charge	$Q_{rr}$	—	0.38	—	$\mu\text{C}$	$diF/dt = 100 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

Main Characteristics

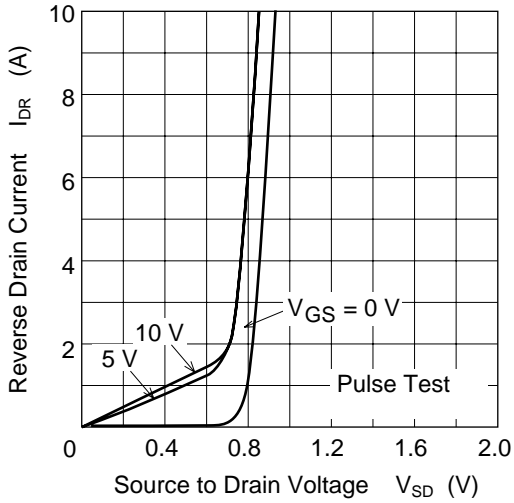




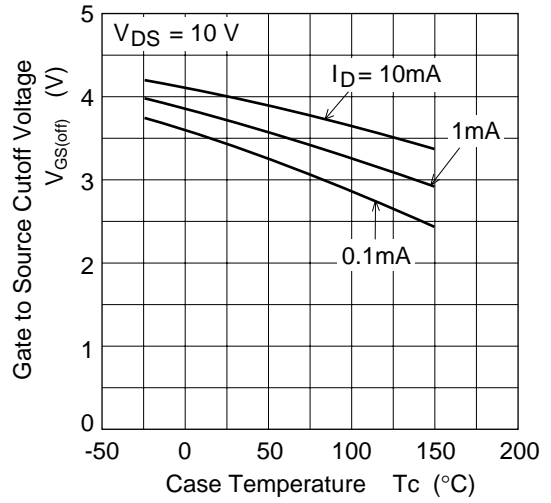




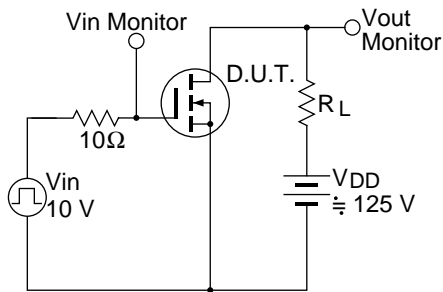
Reverse Drain Current vs.  
Source to Drain Voltage



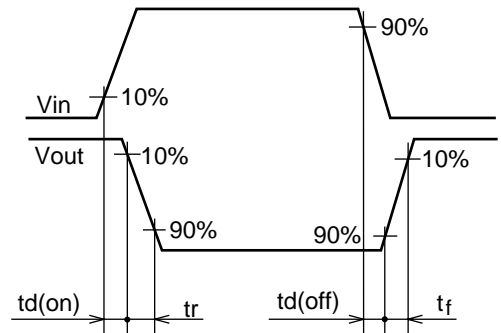
Gate to Source Cutoff Voltage  
vs. Case Temperature

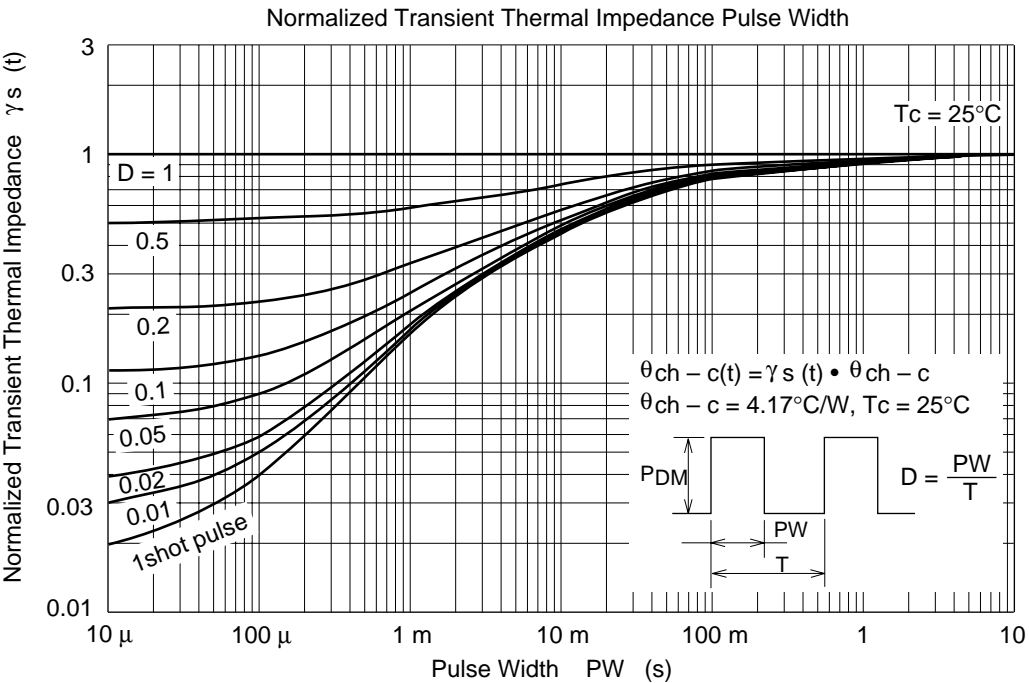


Switching Time Test Circuit



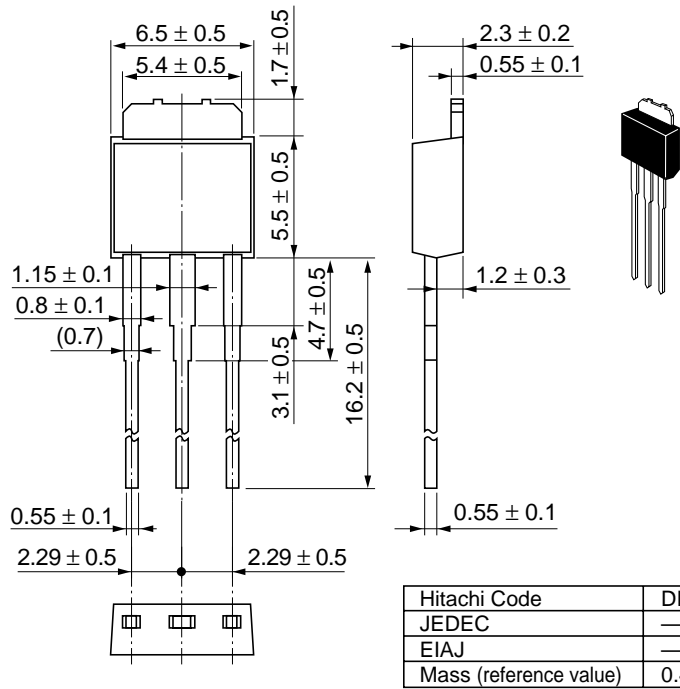
Waveform



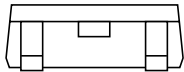
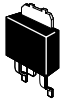
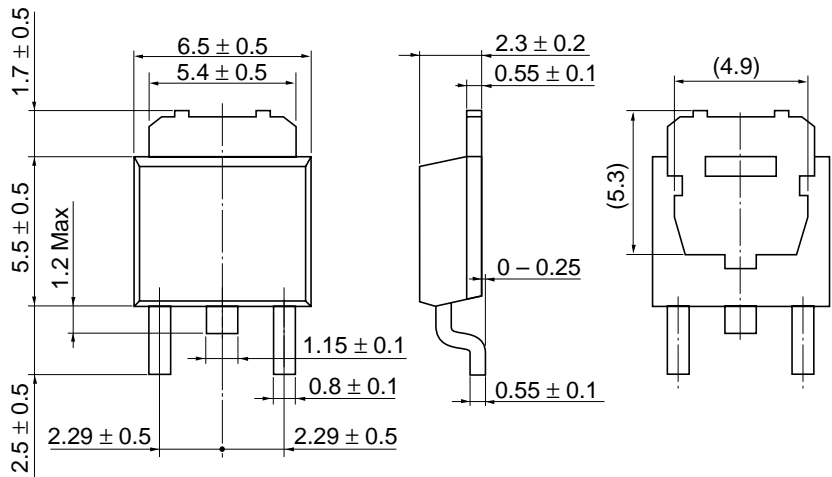


Package Dimensions

As of January, 2001  
Unit: mm



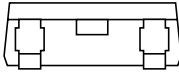
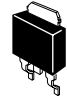
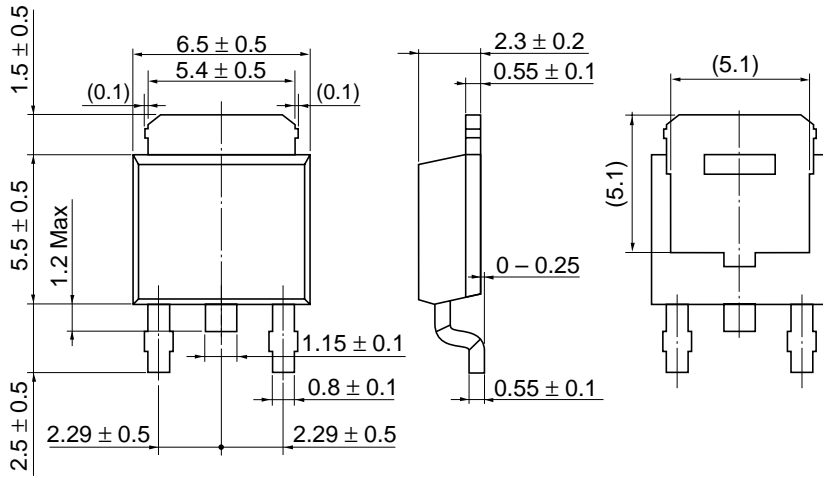
As of January, 2001  
Unit: mm



Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001

Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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