To all our customers

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Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H5N2510DL, H5N2510DS

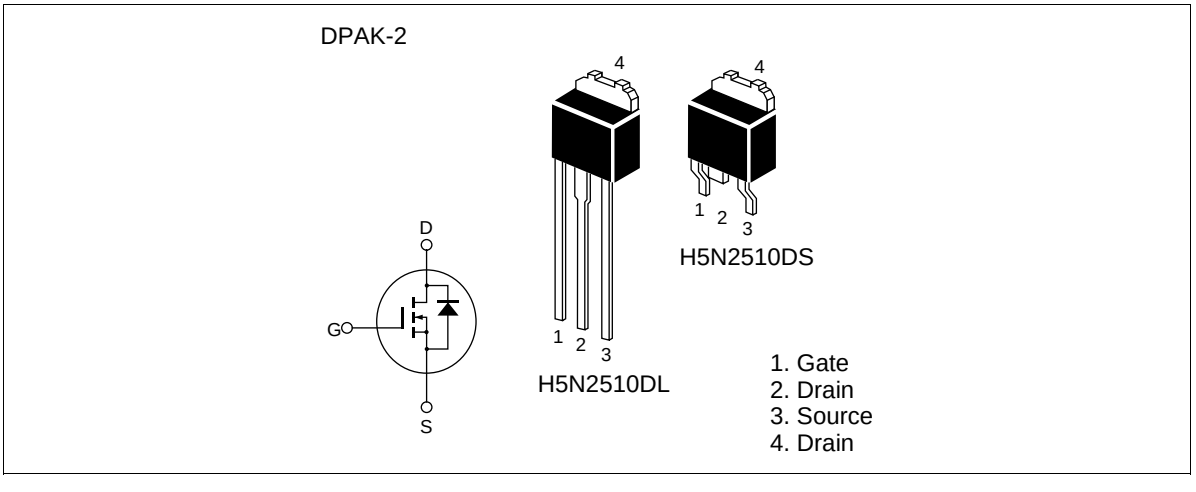
Silicon N Channel MOS FET
High Speed Power Switching

ADE-208-1379 (Z)
Target Specification 1st. Edition
Mar. 2001

Features

- Low on-resistance
- Low drive current
- High speed switching

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	(5)	A
Drain peak current	$I_{D\ (pulse)}$ Note1	(20)	A
Body-drain diode reverse drain current	I_{DR}	(5)	A
Body-drain diode reverse drain peak current	$I_{DR\ (pulse)}$ Note1	(20)	A
Channel dissipation	Pch Note2	25	W
Channel to case Thermal Impedance	θ ch-c	5	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C

Electrical Characteristics (Ta = 25°C)

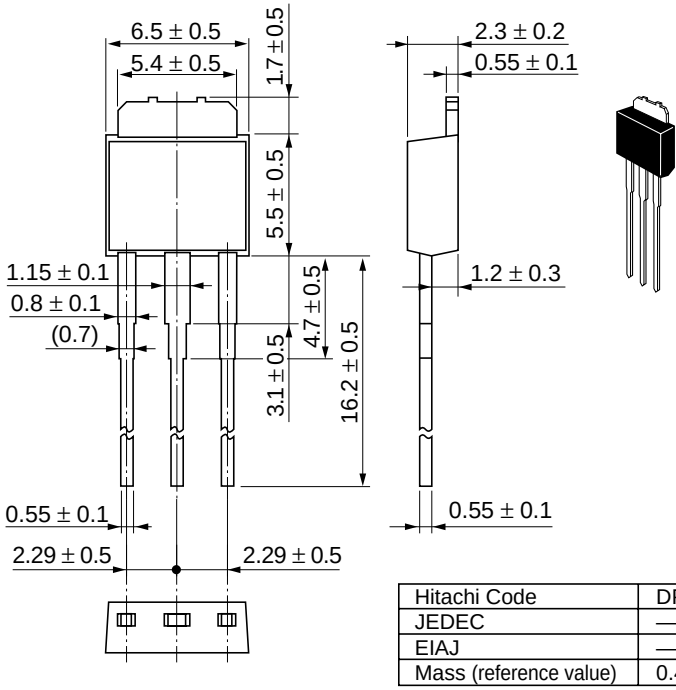
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 250 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	(1.0)	—	(2.5)	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.68)	(0.89)	Ω	I_D = 2.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	(0.72)	(0.97)	Ω	I_D = 2.5 A, V_{GS} = 10 V Note4
Forward transfer admittance	$\|y_{fs}\|$	(3.2)	(5.3)	—	S	I_D = 2.5 A, V_{DS} = 4 V Note4
Input capacitance	Ciss	—	(390)	—	pF	V_{DS} = 25 V
Output capacitance	Coss	—	(45)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(13)	—	pF	f = 1 MHz
Total gate charge	Qg	—	(15.2)	—	nC	V_{DD} = 200 V
Gate to source charge	Qgs	—	(1.3)	—	nC	V_{GS} = 10 V
Gate to drain charge	Qgd	—	(5.1)	—	nC	I_D = 5 A
Turn-on delay time	td(on)	—	(12)	—	ns	I_D = 2.5 A
Rise time	tr	—	(14)	—	ns	V_{GS} = 10 V
Turn-off delay time	td(off)	—	(66)	—	ns	R_L = 50 Ω
Fall time	tf	—	(11)	—	ns	Rg = 10 Ω
Body-drain diode forward voltage	V_{DF}	—	(1.0)	(1.5)	V	I_F = 5 A, V_{GS} = 0
Body-drain diode reverse recovery time	trr	—	(100)	—	ns	I_F = 5 A, V_{GS} = 0
Body-drain diode reverse recovery charge	Qrr	—	(320)	—	nC	diF/dt = 100 A/µs

Note: 4. Pulse test

Package Dimensions

As of January, 2001

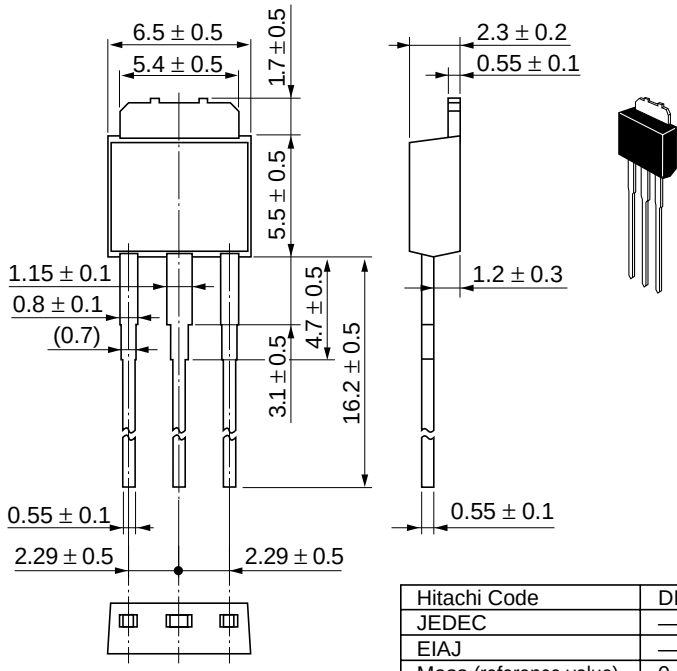
Unit: mm



Hitachi Code	DPAK (L)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	0.42 g

As of January, 2001

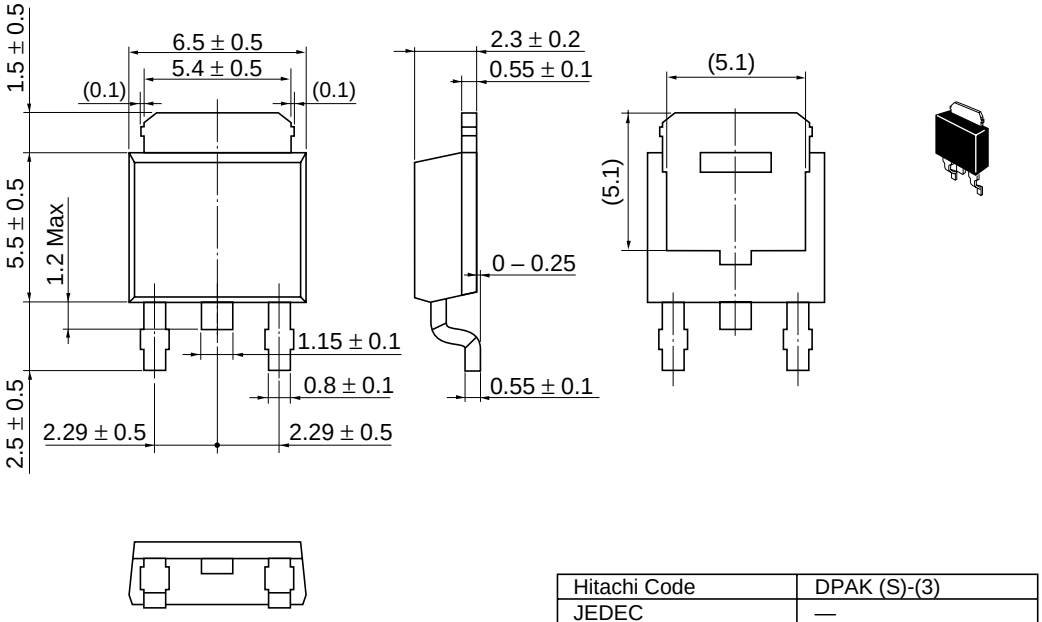
Unit: mm



Hitachi Code	DPAK (L)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	0.42 g

As of January, 2001

Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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