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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H7N0311LD, H7N0311LS, H7N0311LM

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

ADE-208-1423C (Z)

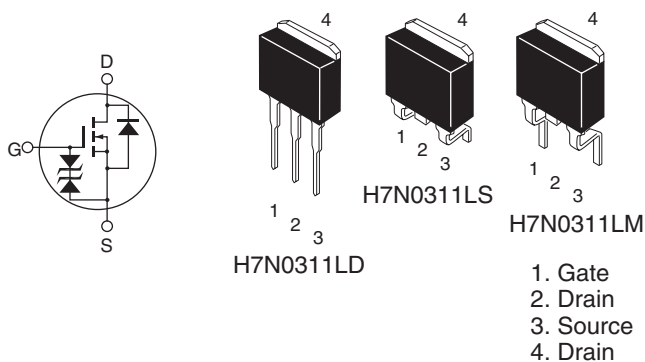
4th. Edition
Aug. 2002

Features

- Low on-resistance
- $R_{DS(on)} = 7.0 \text{ m}\Omega$ typ.
- Low drive current

Outline

LDBPAK



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	45	A
Drain peak current	I _{D(pulse)} ^{Note 1}	180	A
Body-drain diode reverse drain current	I _{DR}	45	A
Channel dissipation	Pch ^{Note 2}	60	W
Channel to Case Thermal Impedance	θch-c	2.08	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1 \%$
2. Value at Tc = 25°C

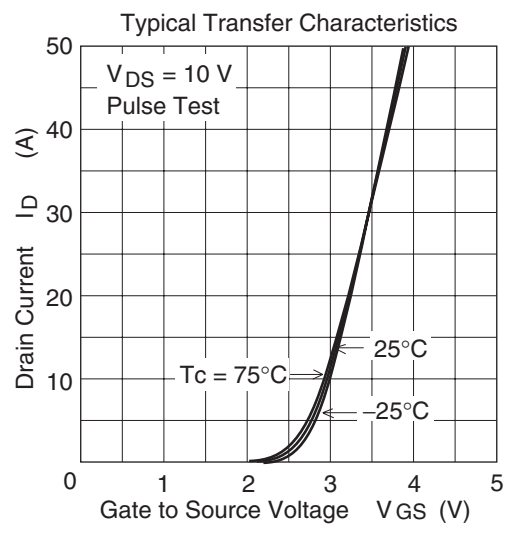
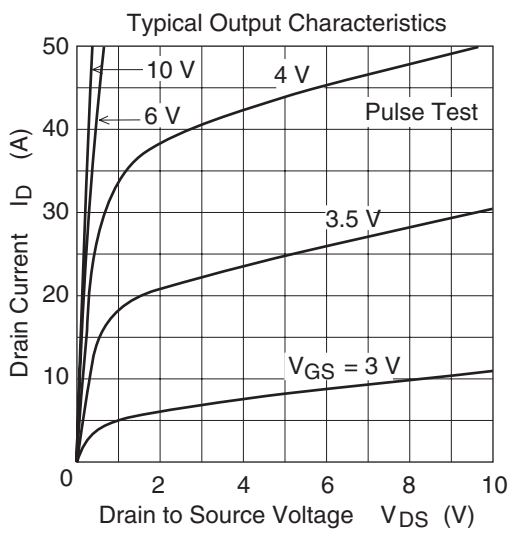
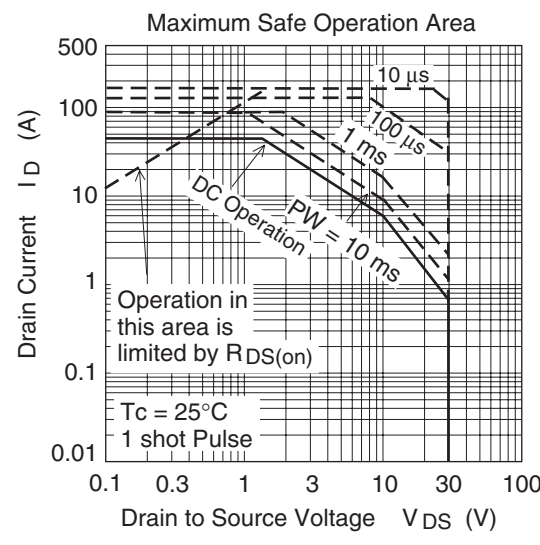
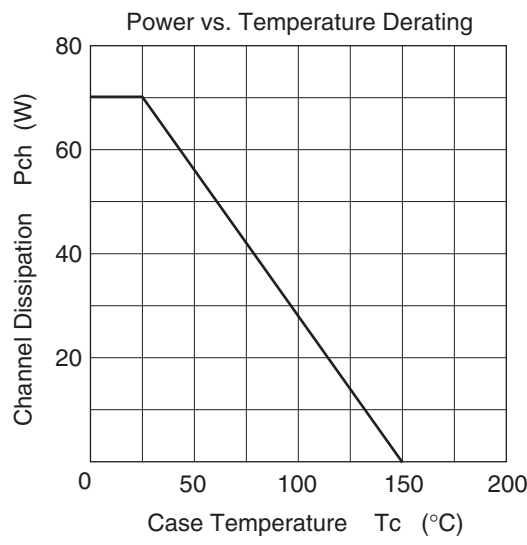
Electrical Characteristics

(Ta = 25°C)

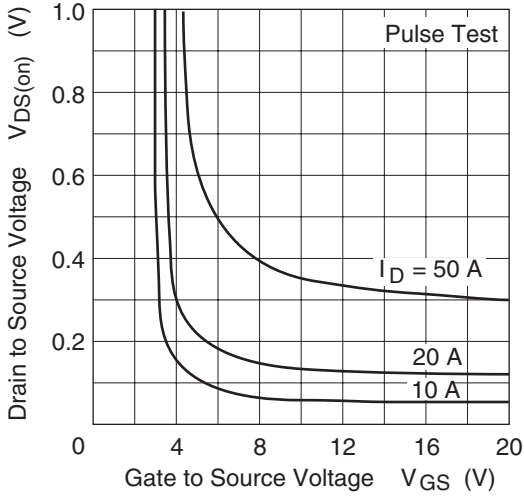
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$ ^{Note1}
Static drain to source on state resistance	$R_{DS(on)}$	—	7.0	8.8	m Ω	$I_D = 22.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note1}
		—	11	16	m Ω	$I_D = 22.5 \text{ A}$, $V_{GS} = 5 \text{ V}$ ^{Note1}
Forward transfer admittance	$ y_{fs} $	27	45	—	S	$I_D = 22.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note1}
Input capacitance	Ciss	—	1650	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	440	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	250	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	28	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Qgs	—	6.0	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	5.4	—	nc	$I_D = 45 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	22	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 22.5 \text{ A}$
Rise time	t_r	—	310	—	ns	$R_L = 0.44 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	t_f	—	16	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.93	—	V	$I_F = 45 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 45 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Notes: 1. Pulse test

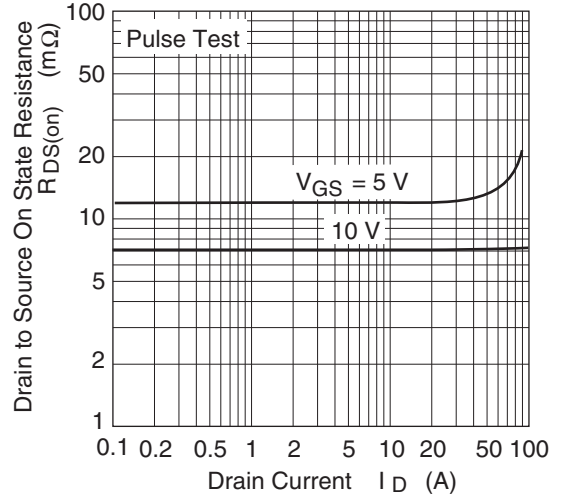
Main Characteristics



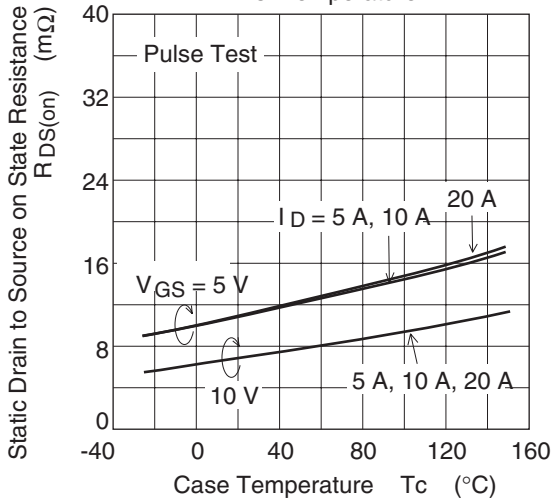
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



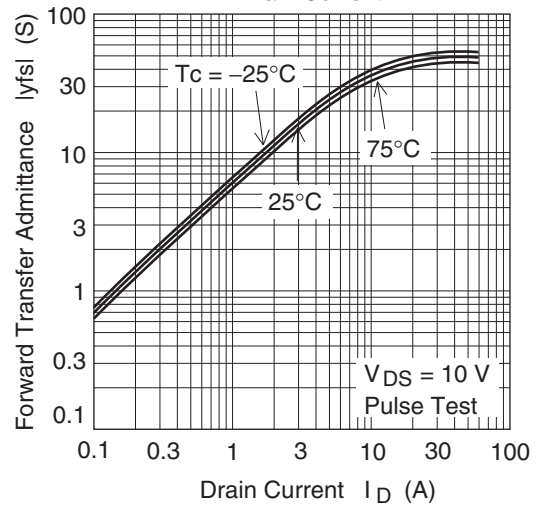
Static Drain to Source on State Resistance
vs. Drain Current



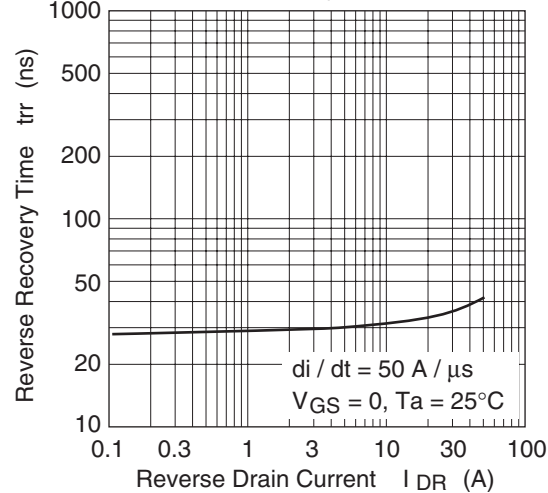
Static Drain to Source on State Resistance
vs. Temperature



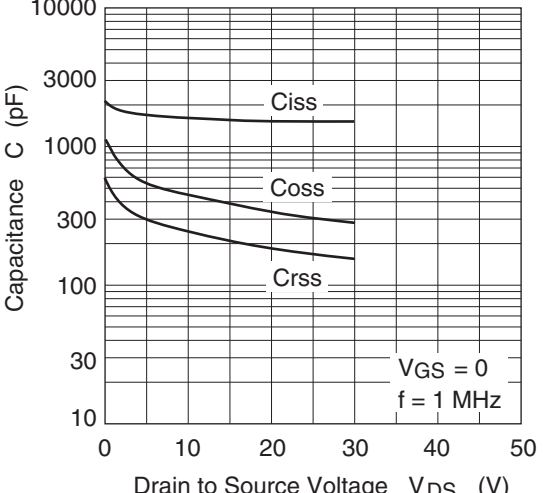
Forward Transfer Admittance vs.
Drain Current



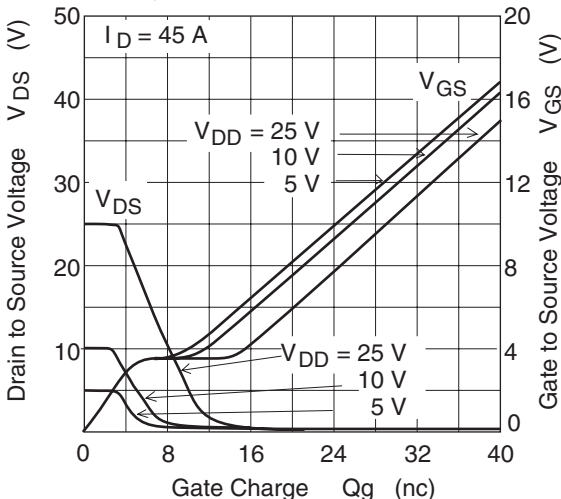
Body-Drain Diode Reverse Recovery Time



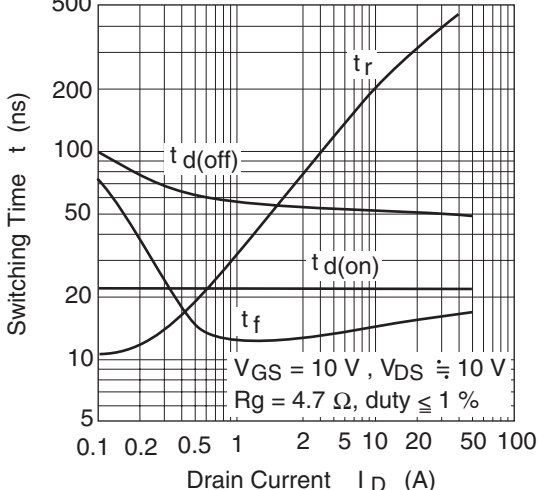
Typical Capacitance vs. Drain to Source Voltage

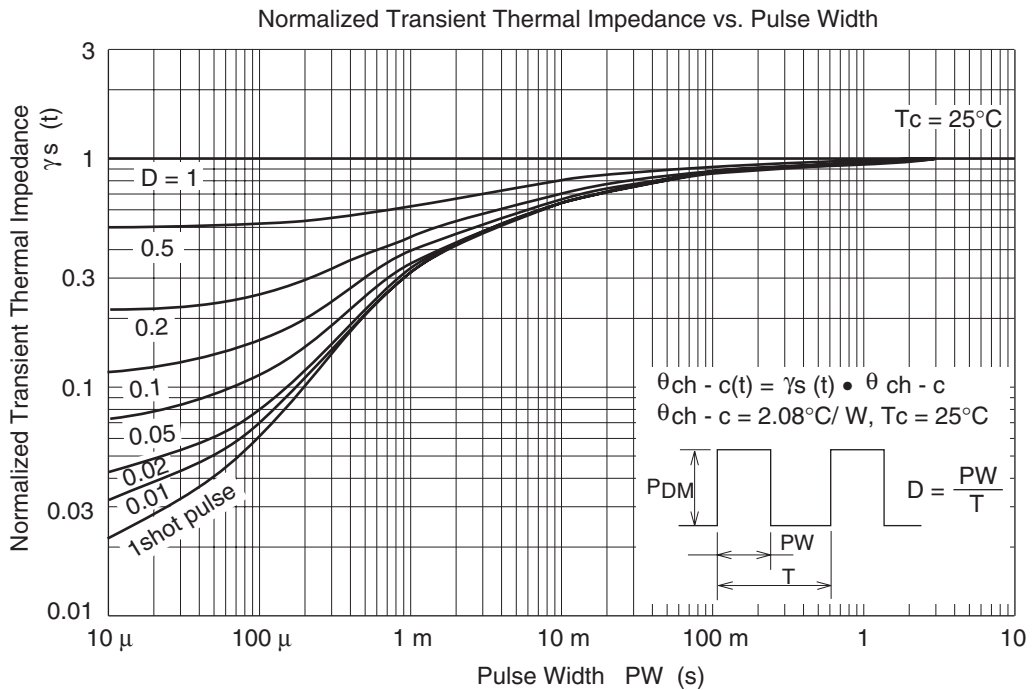
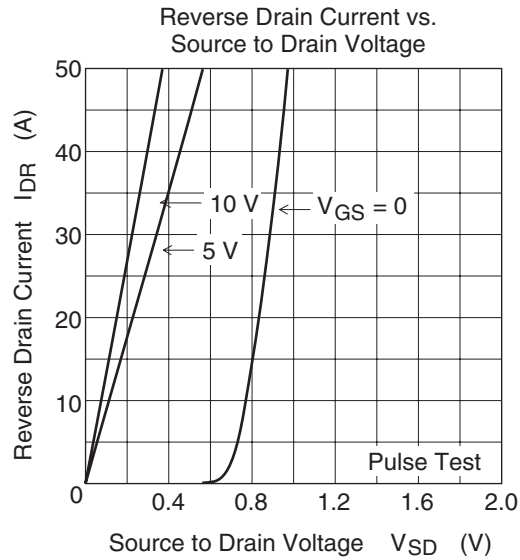


Dynamic Input Characteristics

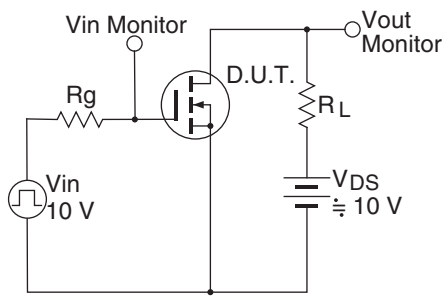


Switching Characteristics

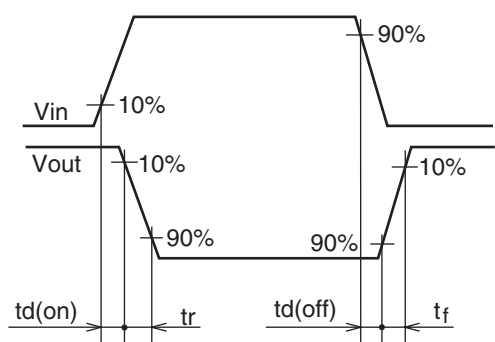




Switching Time Test Circuit



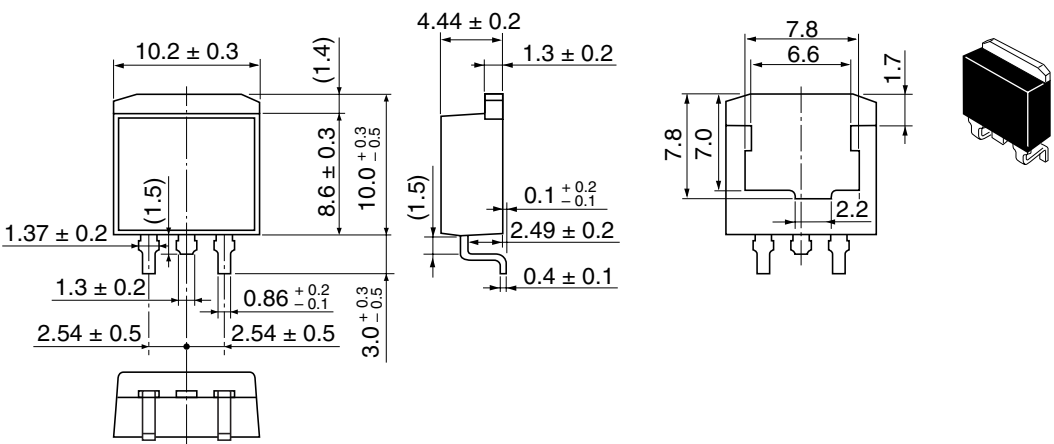
Switching Time Waveform



H7N0311LD, H7N0311LS, H7N0311LM

• H7N0311LS

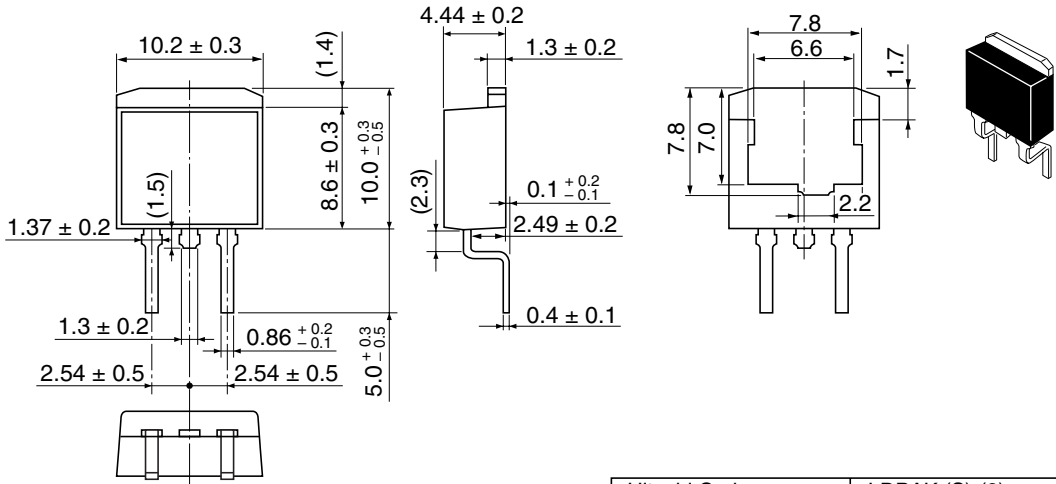
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

• H7N0311LM

Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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