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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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H7N0602LD, H7N0602LS, H7N0602LM

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

ADE-208-1526C (Z)

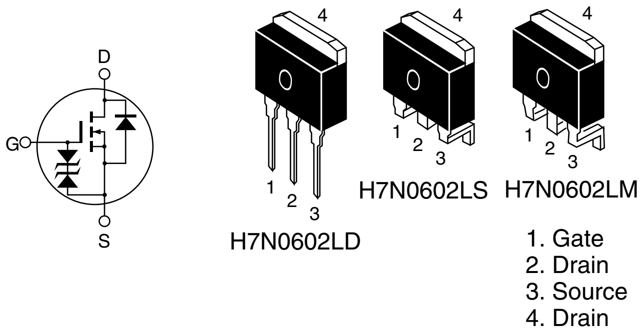
4th. Edition
May 2002

Features

- Low on-resistance
  $R_{DS(on)} = 4.1\ m\Omega$ typ.
- 4.5 V gate drive devices
- High Speed Switching

Outline

LDPAK



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	85	A
Drain peak current	I_D (pulse) Note1	340	A
Body-drain diode reverse drain current	I_{DR}	85	A
Avalanche current	I_{AP} Note3	65	A
Avalanche energy	E_{AR} Note3	362	mJ
Channel dissipation	Pch Note2	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

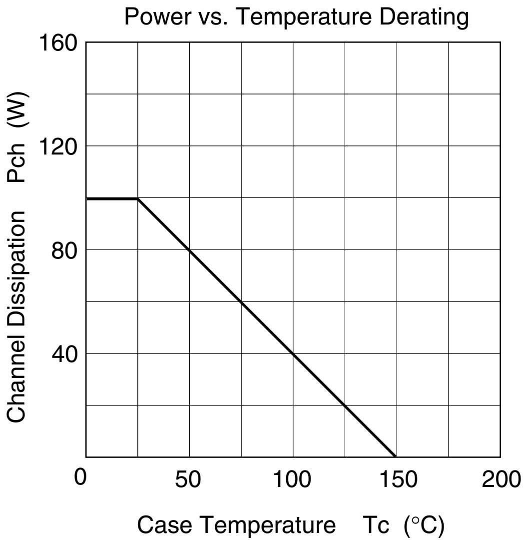
Electrical Characteristics

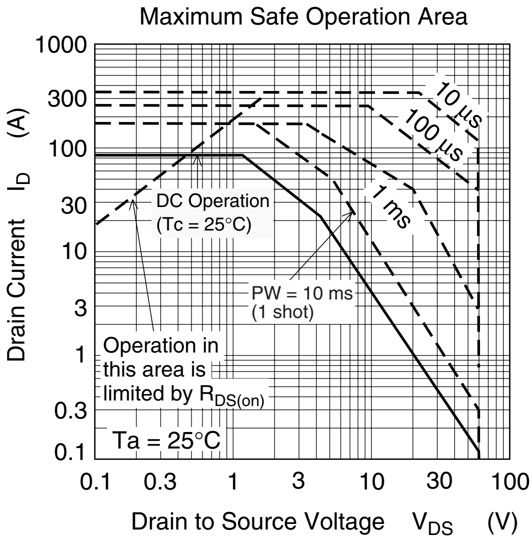
(Ta = 25°C)

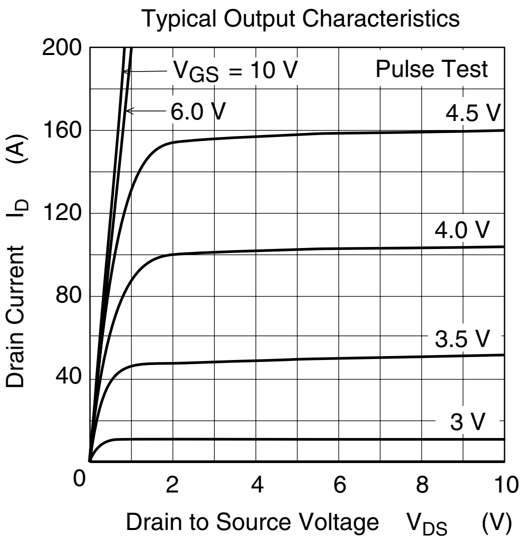
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA[Note1]
Forward transfer admittance	$\|y_{fs}\|$	70	120	—	S	I_D = 45 A, V_{DS} = 10 V[Note1]
Static drain to source on state resistance	$R_{DS(on)}$	—	4.1	5.2	mΩ	I_D = 45 A, V_{GS}= 10 V[note1]
Static drain to source on state resistance	$R_{DS(on)}$	—	6.2	9.0	mΩ	I_D = 45 A, V_{GS}=4.5 V[Note1]
Input capacitance	Ciss	—	9000	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	470	—	pF	f = 1 MHz
Total gate charge	Qg	—	140	—	nc	V_{DD} = 25 V
Gate to source charge	Qgs	—	30	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	30	—	nc	I_D = 85 A
Turn-on delay time	td(on)	—	55	—	ns	V_{GS} = 10 V
Rise time	tr	—	290	—	ns	I_D= 45 A
Turn-off delay time	td(off)	—	140	—	ns	R_L = 0.67 Ω
Fall time	tf	—	50	—	ns	R_g = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 85 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	45	—	ns	I_F = 85 A, V_{GS} = 0 diF/dt = 100 A/µs

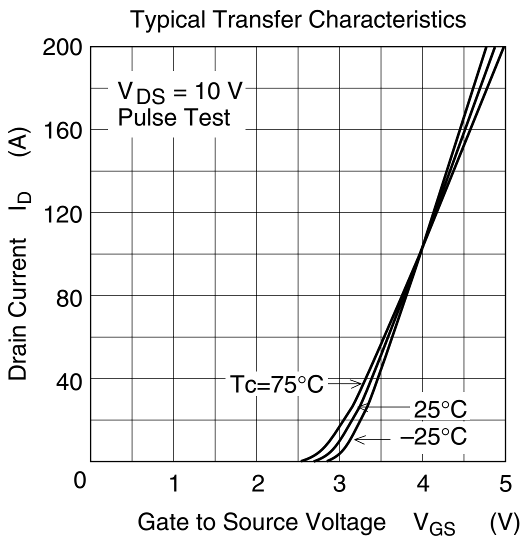
Notes: 1. Pulse test

Main Characteristics

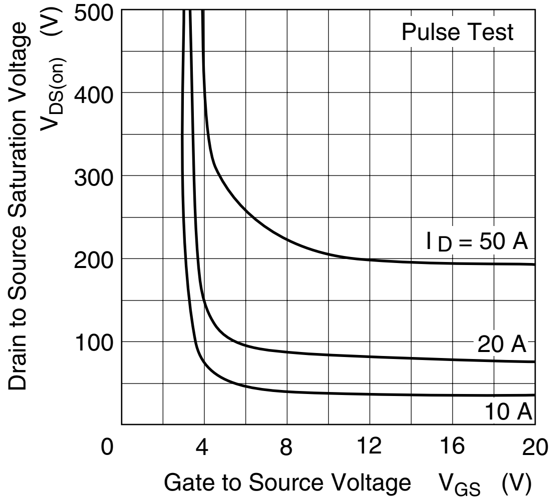




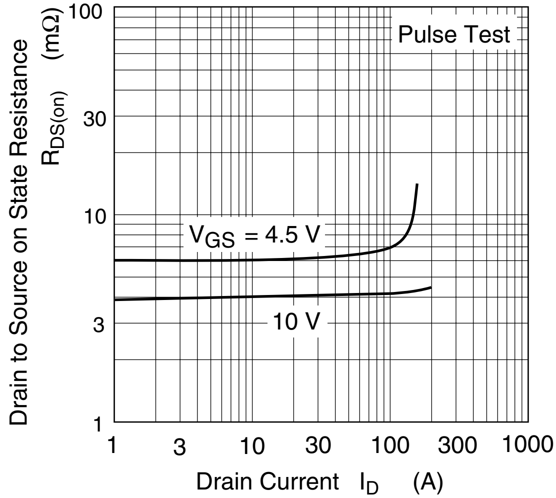




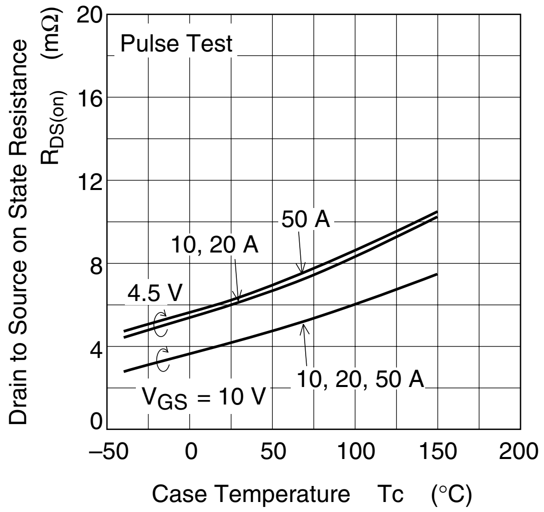
Drain to Source Saturation Voltage vs. Gate to Source Voltage



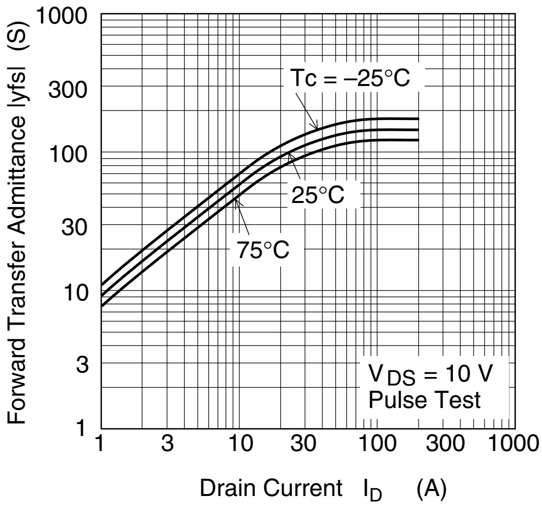
Static Drain to Source on State Resistance vs. Drain Current

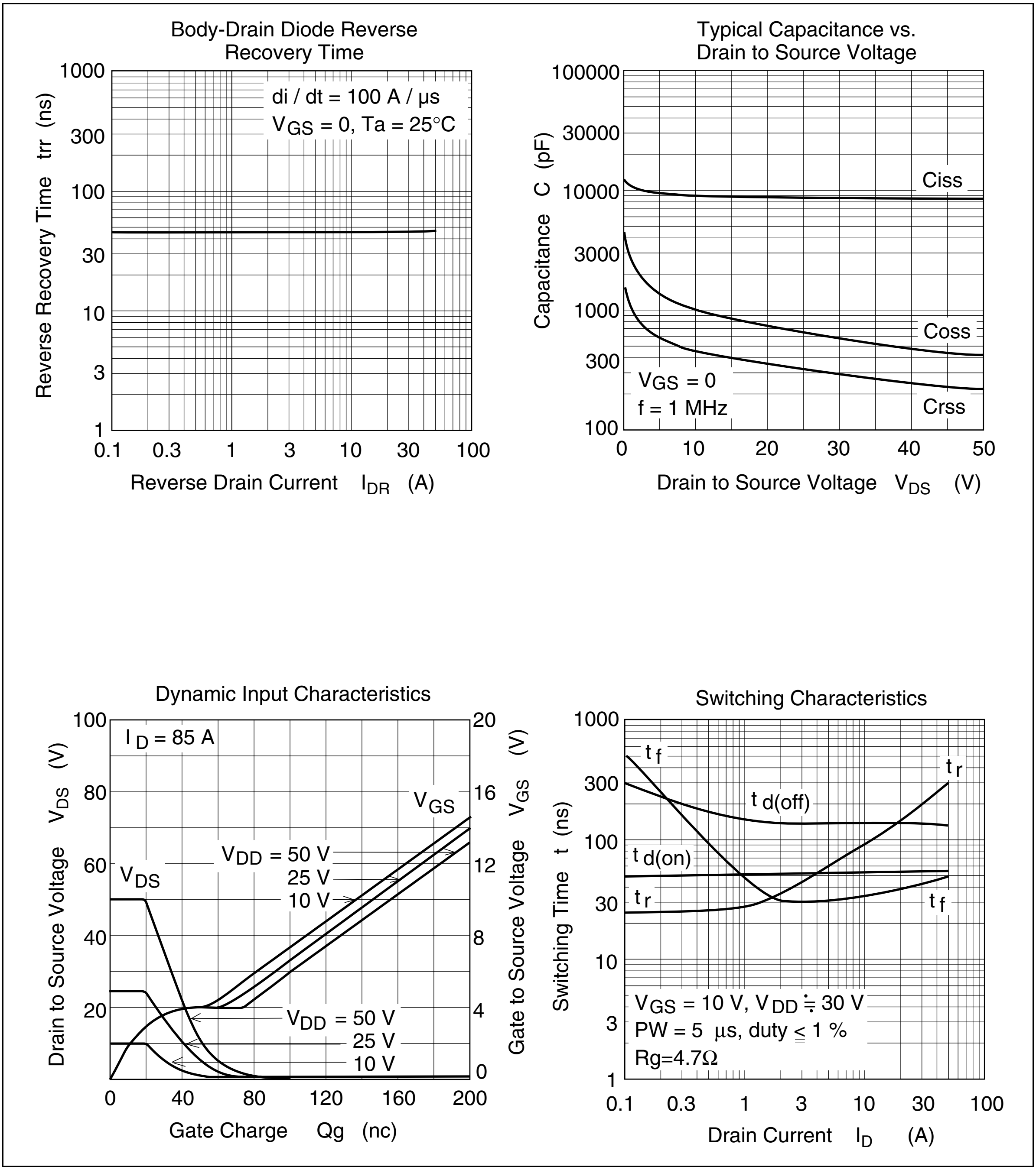


Static Drain to Source on State Resistance vs. Temperature



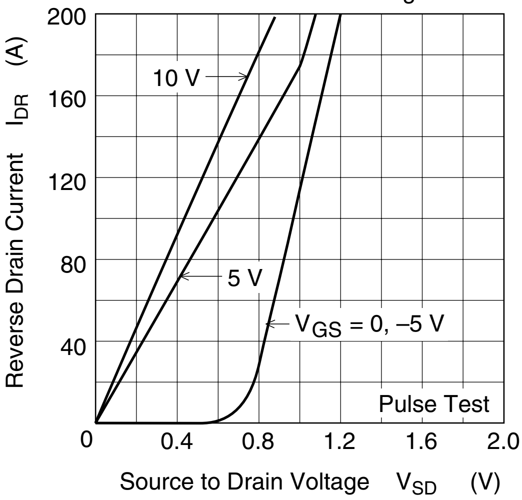
Forward Transfer Admittance vs. Drain Current



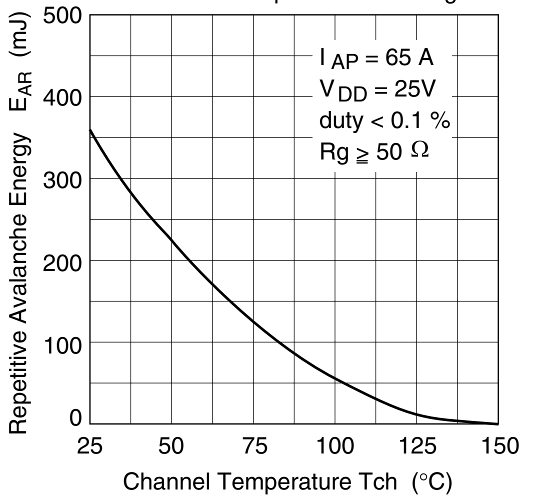


Body-Drain Diode Reverse Recovery Time
di / dt = 100 A / μs
VGS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
Reverse Drain Current IDR (A)
Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
Drain to Source Voltage VDS (V)
Dynamic Input Characteristics
I D = 85 A
VGS
VDD = 50 V
25 V
10 V
VDS
VDD = 50 V
25 V
10 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
Switching Characteristics
tf
tr
t d(off)
t d(on)
tr
tf
VGS = 10 V, VDD ≒ 30 V
PW = 5 μs, duty ≤ 1 %
Rg=4.7Ω
Switching Time t (ns)
Drain Current ID (A)

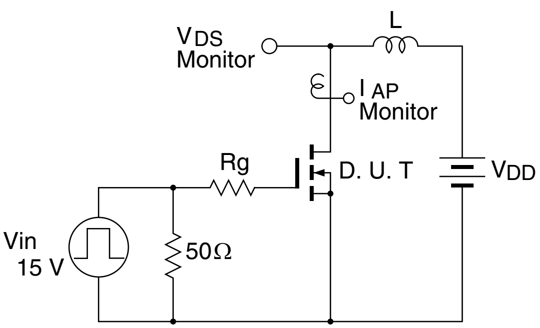
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

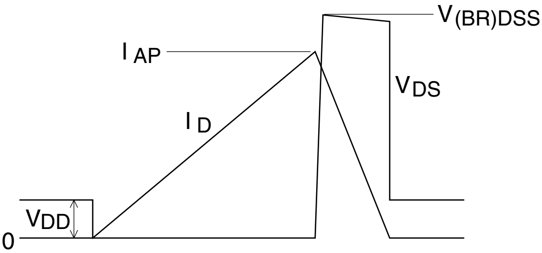


Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



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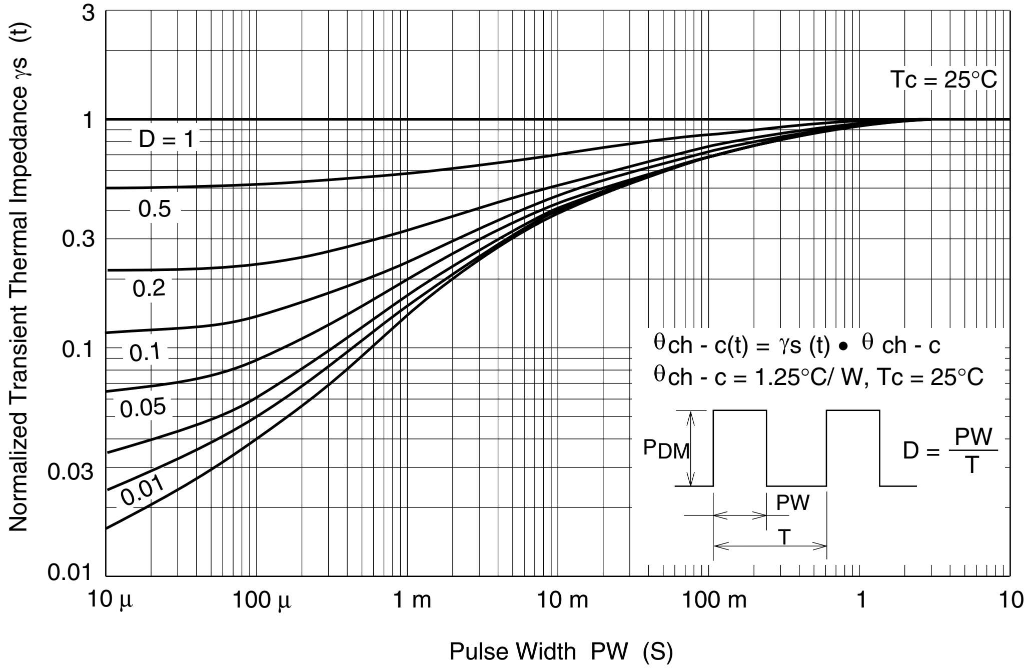
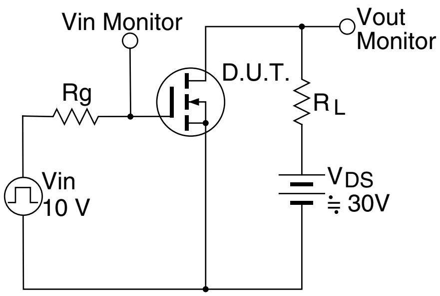
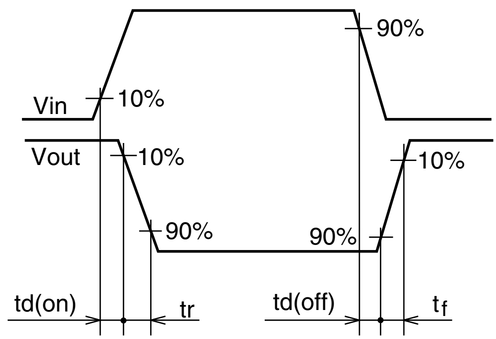
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

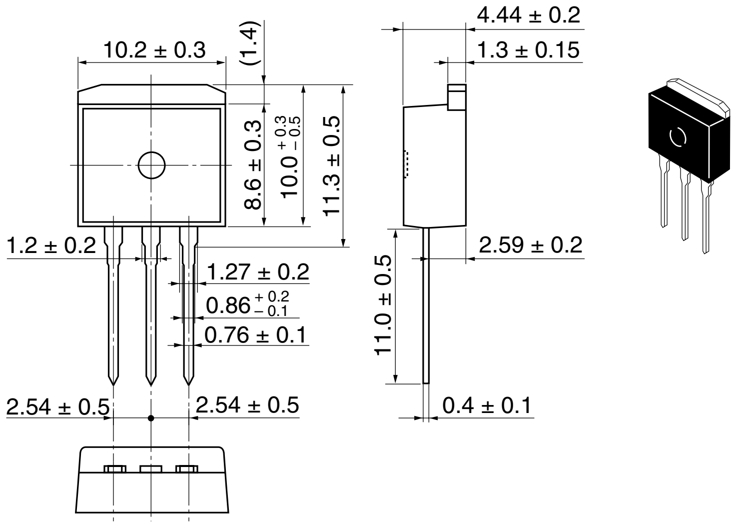


Waveform



Package Dimensions

As of January, 2002
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

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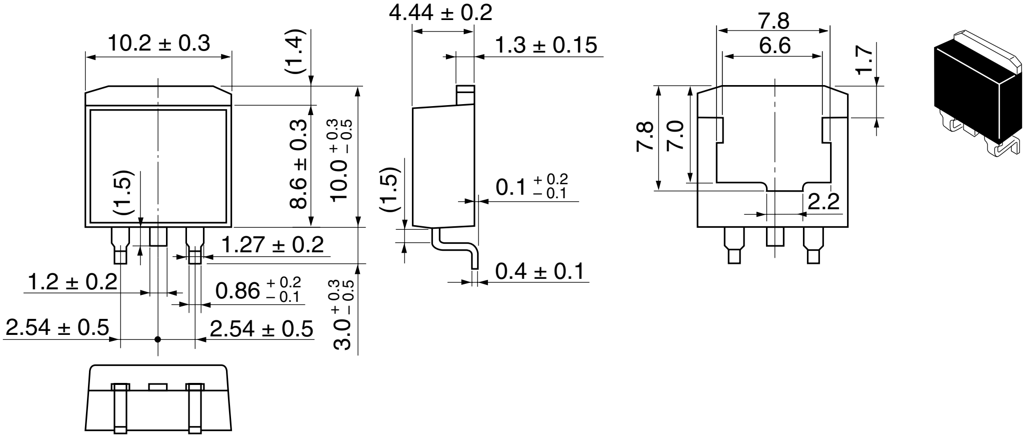
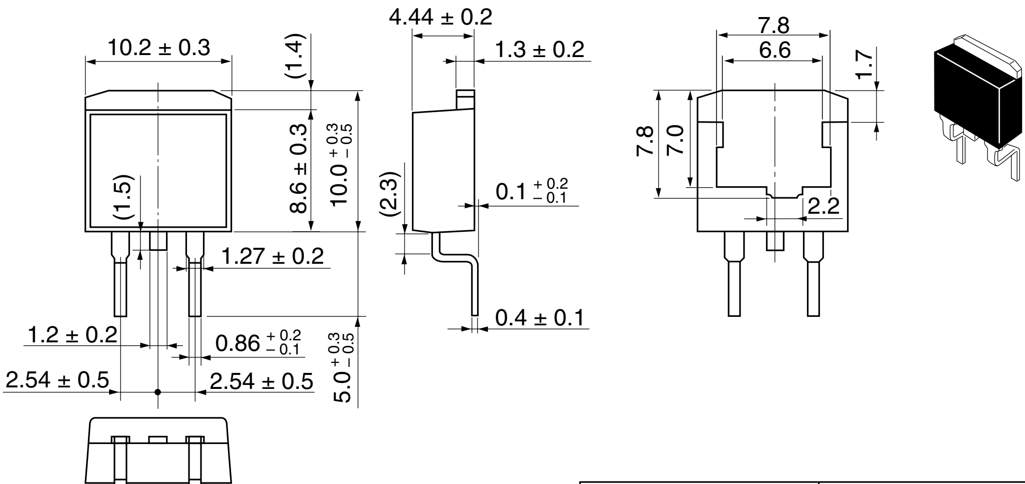
As of January, 2002
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

As of January, 2002
Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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Sales Offices

HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL http://www.hitachisemiconductor.com/

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel : <65>-6538-6533/6538-8577
Fax : <65>-6538-6933/6538-3877
URL : http://semiconductor.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel : <852>-2735-9218
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