

H7N1004LD, H7N1004LS, H7N1004LM

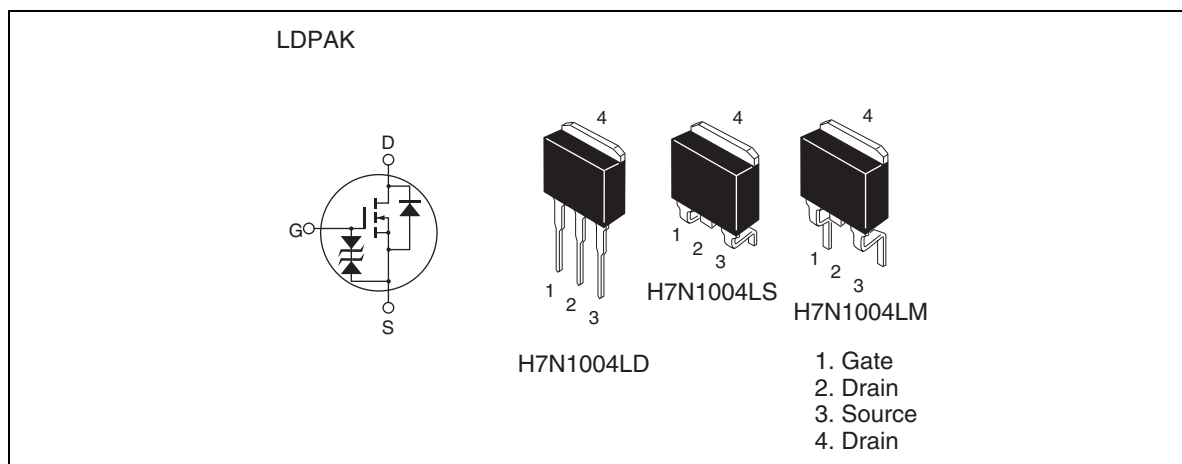
Silicon N-Channel MOSFET
High-Speed Power Switching

REJ03G0072-0600Z
(Previous ADE-208-1552E(Z))
Rev.6.00
Aug.27.2003

Features

- Low on-resistance
- $R_{DS(on)} = 25 \text{ m}\Omega$ typ.
- Low drive current
- Available for 4.5 V gate drive

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	100	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	30	A
Drain peak current	I _D (pulse) ^{Note1}	100	A
Body-drain diode reverse drain current	I _{DR}	30	A
Avalanche current	I _{AP} ^{Note 3}	15	A
Avalanche energy	E _{AR} ^{Note 3}	22.5	mJ
Channel dissipation	P _{ch} * ^{Note 2}	50	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	–55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at T_c = 25°C
3. Value at T_{ch} = 25°C, R_g $\geq 50 \Omega$

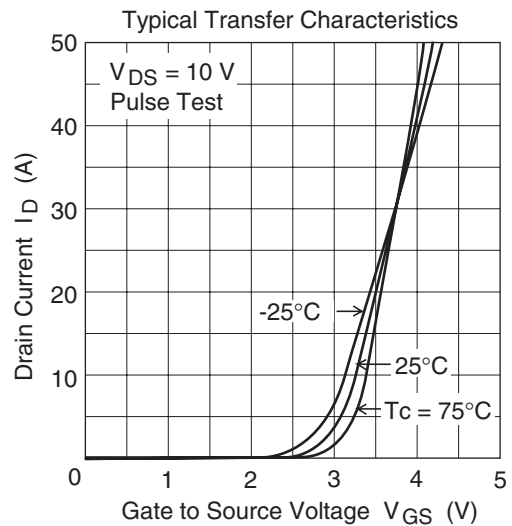
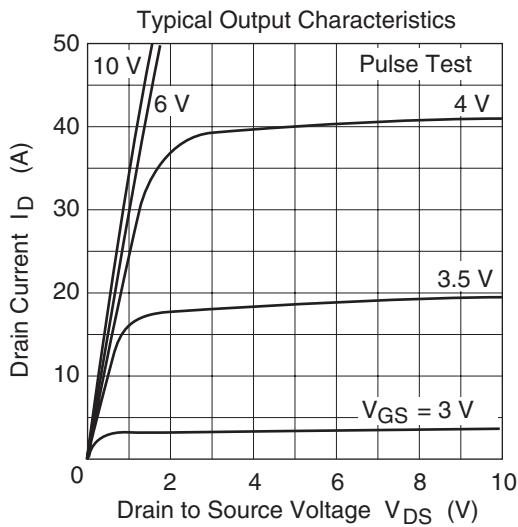
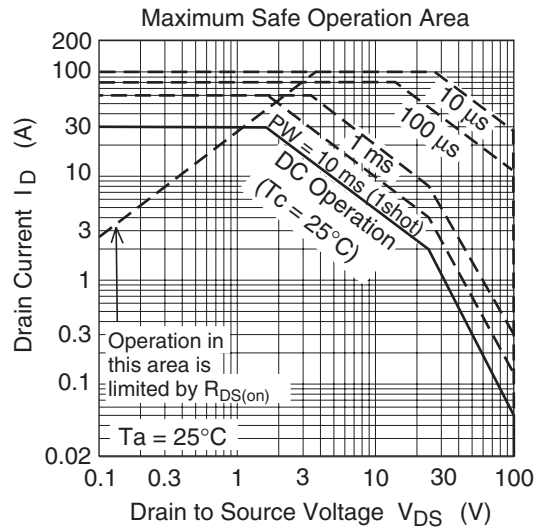
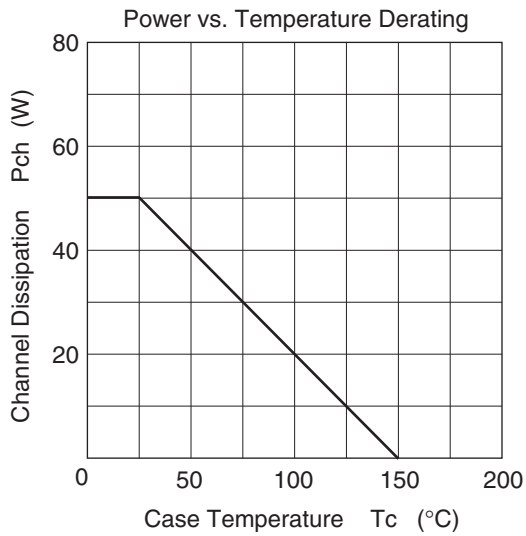
Electrical Characteristics

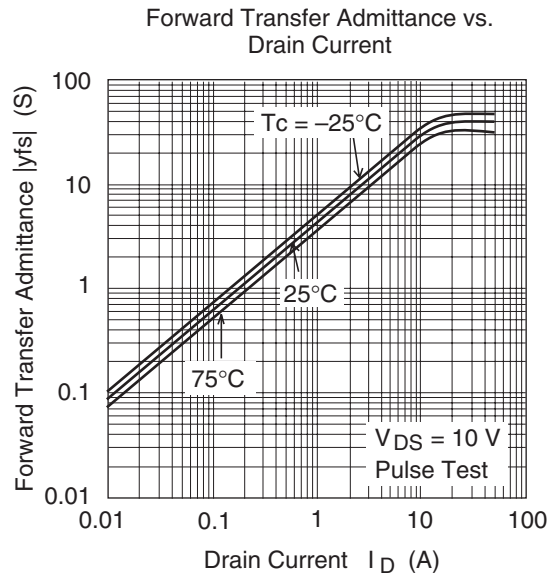
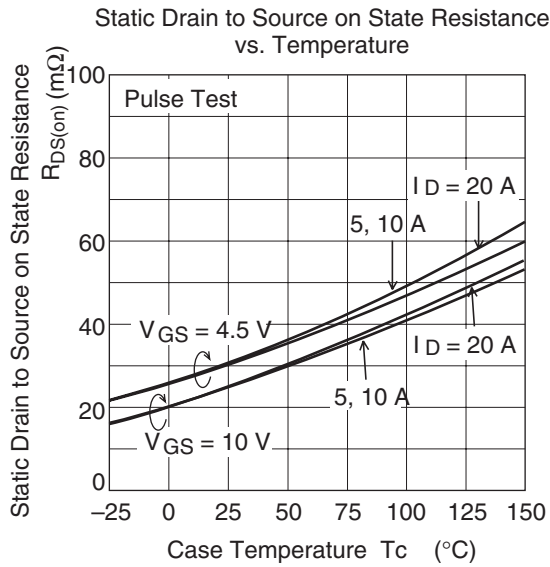
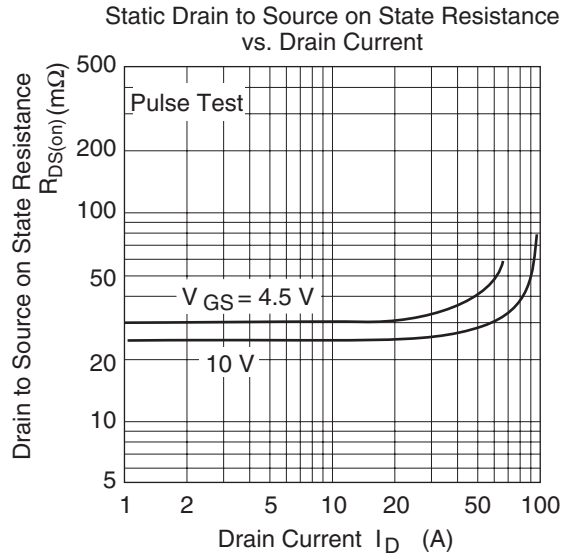
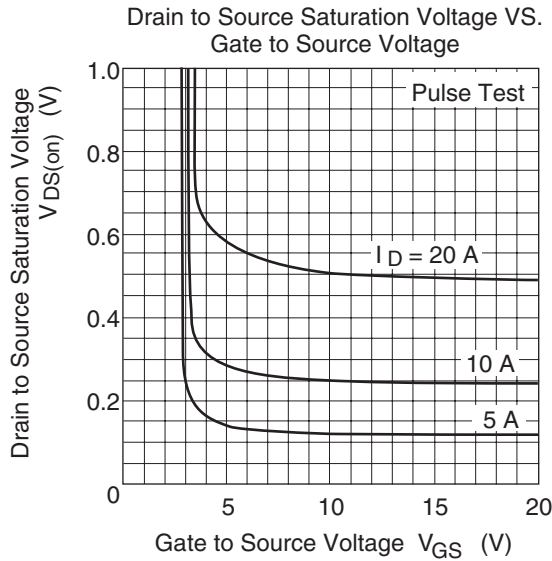
(Ta = 25°C)

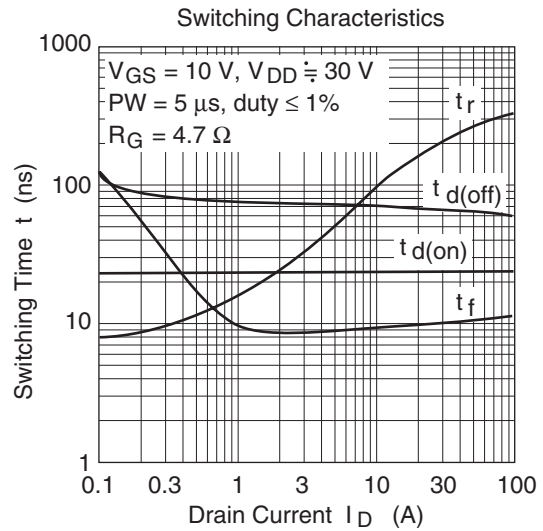
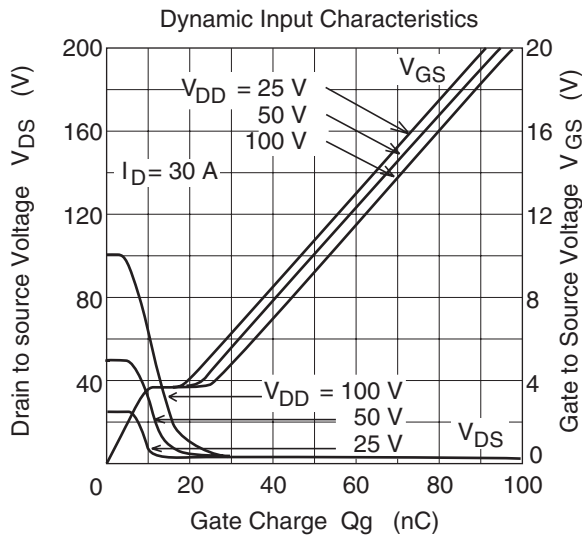
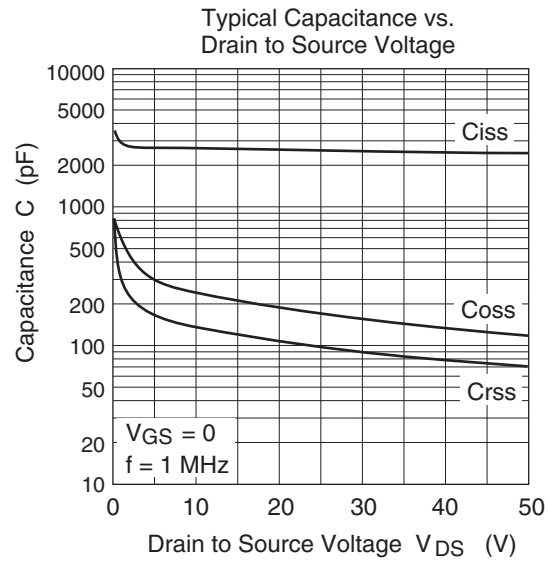
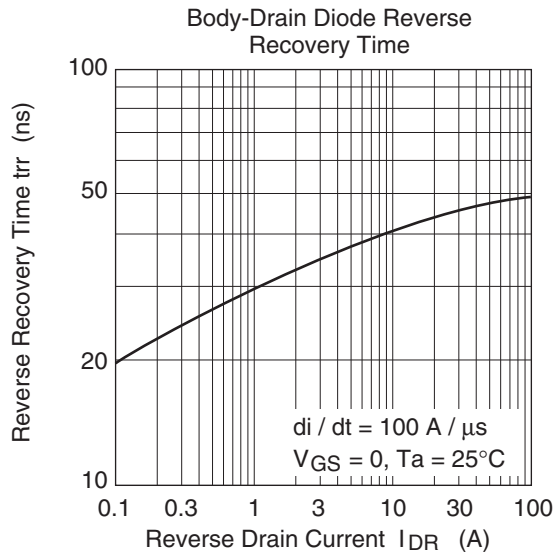
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$ ^{Note 1}
Static drain to source on state resistance	$R_{DS(on)}$	—	25	35	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 1}
		—	30	45	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note 1}
Forward transfer admittance	$ y_{fs} $	22	37	—	S	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 1}
Input capacitance	C_{iss}	—	2800	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	240	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	140	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	50	—	nC	$V_{DD} = 50 \text{ V}$
Gate to source charge	Q_{gs}	—	9	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	11	—	nC	$I_D = 30 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$
Rise time	t_r	—	120	—	ns	$R_L = 2 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	t_f	—	9.5	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 30 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	47	—	ns	$I_F = 30 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

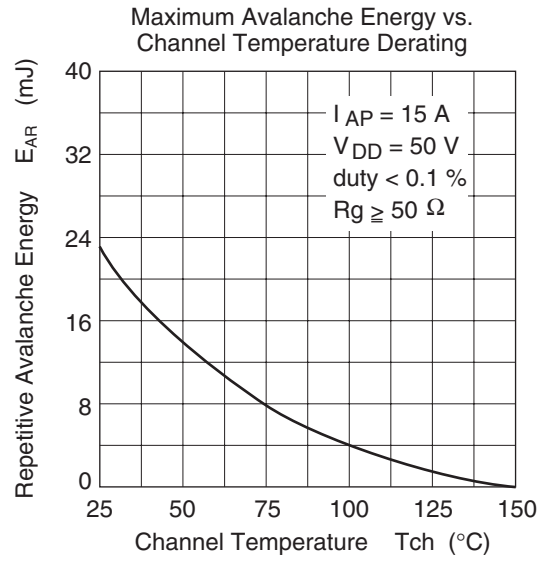
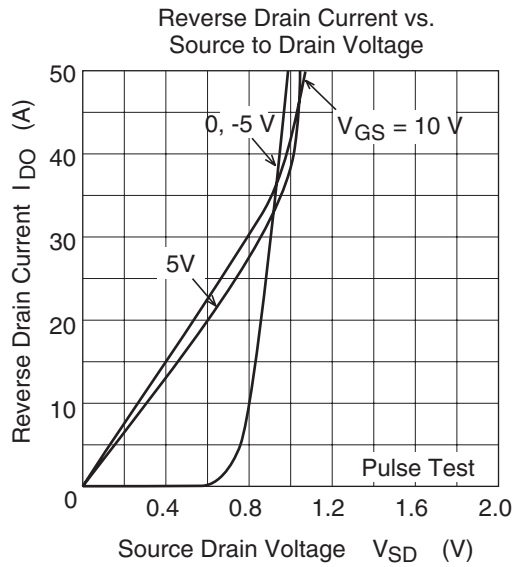
Notes: 1. Pulse test

Main Characteristics

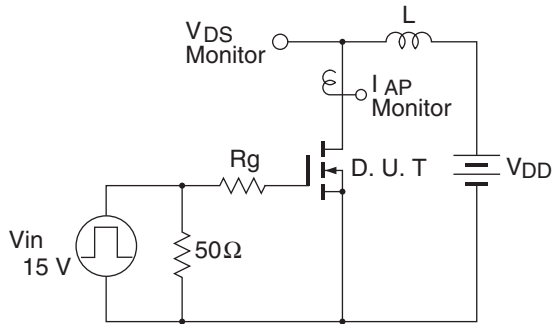




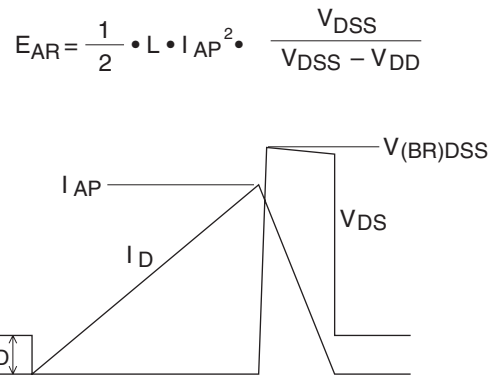


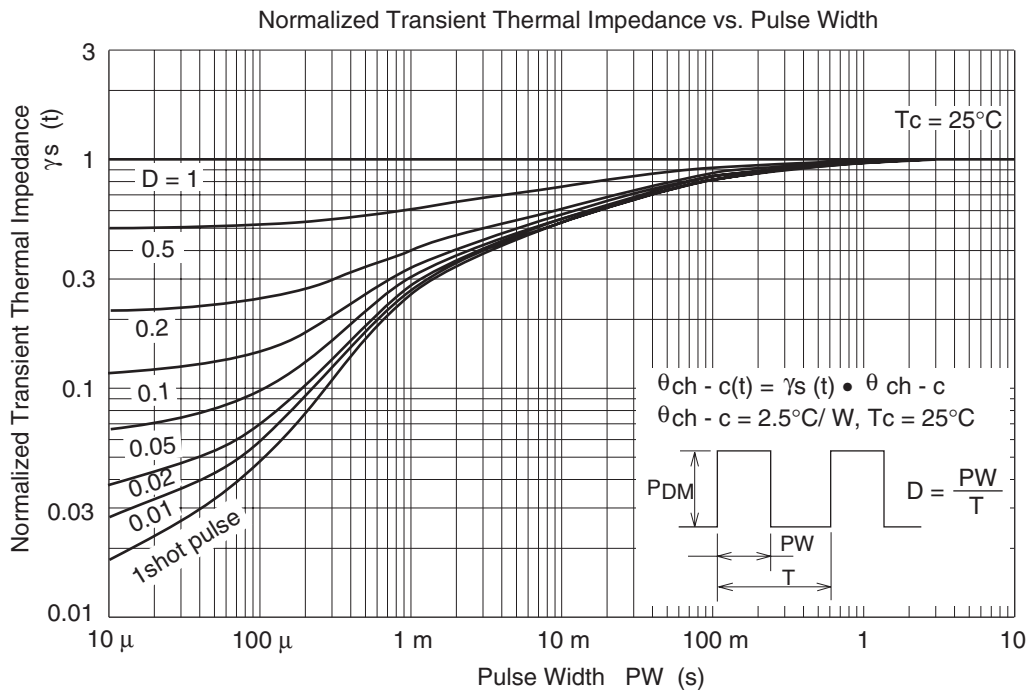


Avalanche Test Circuit

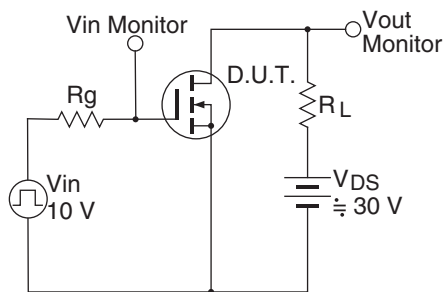


Avalanche Waveform

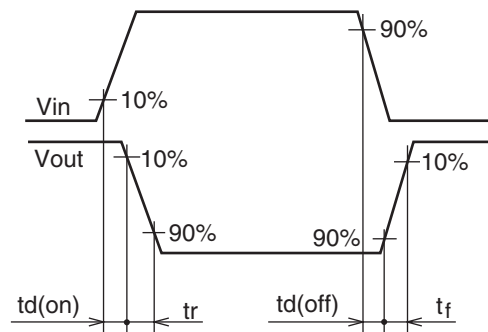




Switching Time Test Circuit



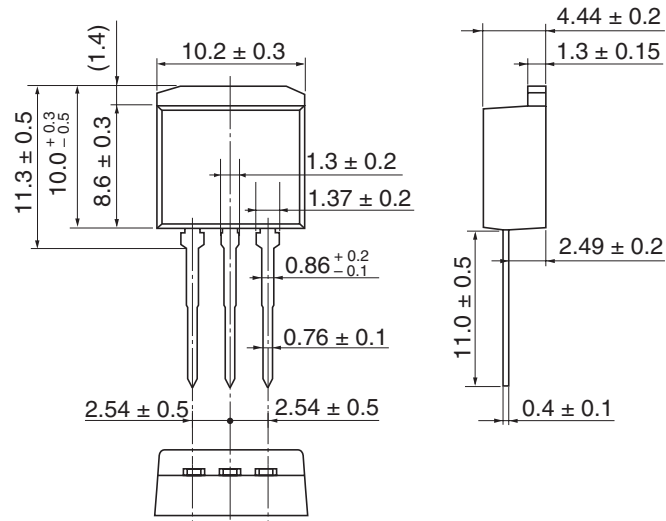
Switching Time Waveform



Package Dimensions

• H7N1004LD

As of January, 2003
Unit: mm

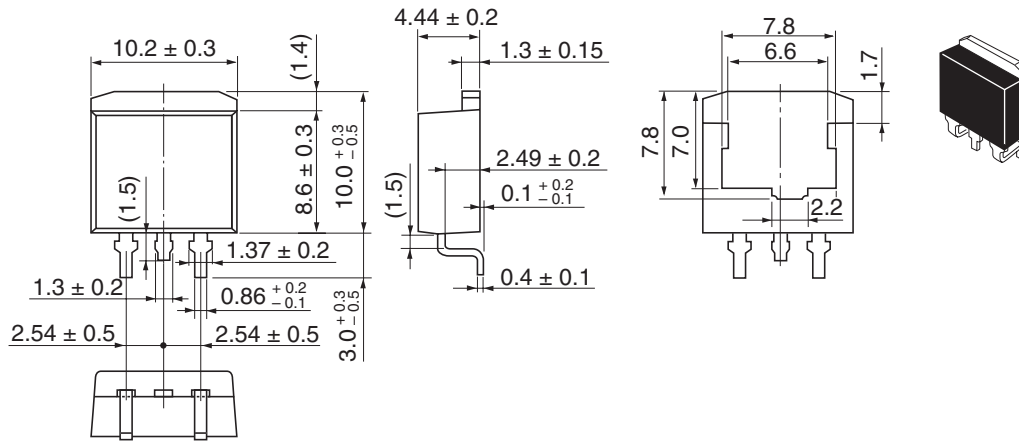


Package Code	LDBAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.40 g

H7N1004LD, H7N1004LS, H7N1004LM

• H7N1004LS

As of January, 2003
Unit: mm



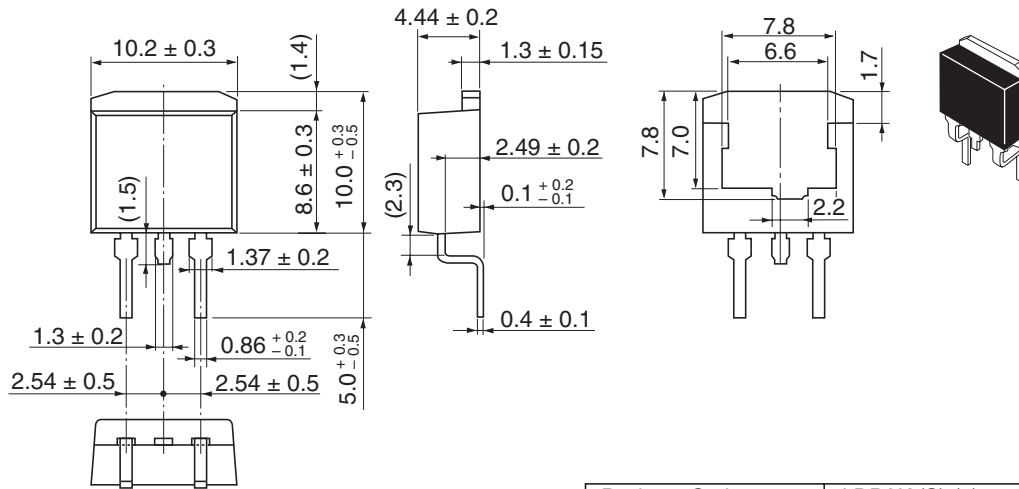
Package Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.30 g

H7N1004LD, H7N1004LS, H7N1004LM

• H7N1004LM

As of January, 2003

Unit: mm



Package Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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