MICROCHIP

HCS410/WM

KEELOQ® Crypto Read/Write Transponder Module

FEATURES

Security

- Two programmable 64-bit encryption keys
- 16/32-bit bi-directional challenge and response using one of two keys
- Programmable 32-bit serial number
- Three IFF encryption algorithms

Operating

- Selectable baud rate
- Anti-collision of multiple transponders
- Intelligent damping for high Q LC-circuits
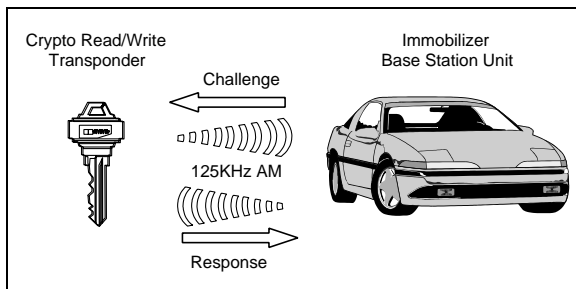- Asynchronous transponder communication
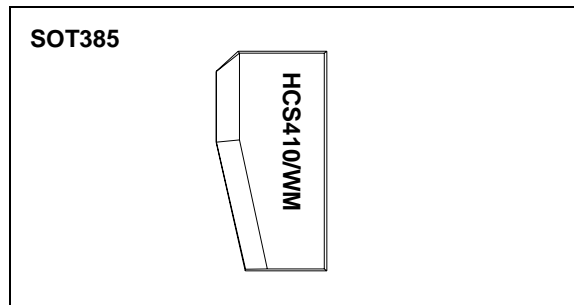
Other

- 64-bit user EEPROM

Typical Applications

- Access control systems
- Automotive immobilizers
- Electronic door locks (Home/Office/Hotel)
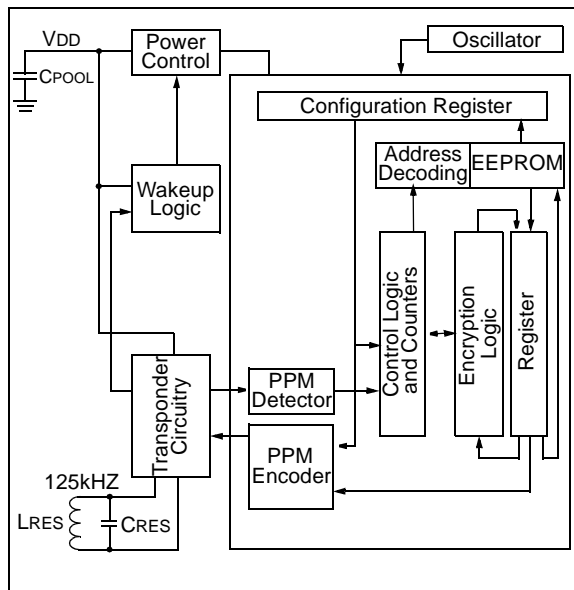- Burglar alarm systems
- Proximity access control

HCS410 IMMOBILIZER TRANSPONDER

PACKAGE TYPES

SOT385

BLOCK DIAGRAM

GENERAL DESCRIPTION

The HCS410/WM is a transponder device designed for secure entry systems. The HCS410/WM utilizes bi-directional challenge-and-response for logical and physical access control.

The HCS410/WM integrates an LC-resonant circuit with the HCS410 silicon into a leadless SOT-385 package.

HCS410/WM

1.0   SYSTEM OVERVIEW

1.1   Key Terms

- Anticollision – Allows multiple transponders to be in the magnetic field simultaneously and be verified individually.
- Encoder Key – A unique 64-bit key generated and programmed into the encoder during the manufacturing process. The encoder key controls the encryption algorithm and is stored in EEPROM on the transponder device.
- IFF – Identify friend or foe is a means of validating a token. A decoder sends a random challenge to the token and checks that the response of the token is a valid response.
- KEELOQ Encryption Algorithm – The high security level of the HCS410/WM is based on the patented KEELOQ technology. A block cipher encryption algorithm based on a block length of 32 bits and a key length of 64 bits is used. The algorithm obscures the information in such a way that even if the unencrypted/challenge information differs by only one bit from the information in the previous challenge, the next coded response will be totally different. Statistically, if only one bit in the 32-bit string of information changes, approximately 50 percent of the coded transmission will change.
- Learn – The HCS product family facilitates several learning strategies to be implemented on the decoder.
- Manufacturer's Code – A 64-bit word, unique to each manufacturer, used to produce a unique encoder key in each transmitter (encoder).
- Transport Code – A 32-bit transport code needs to be given before the HCS410/WM can be inductively programmed. This prevents accidental programming of the HCS410.

1.2   KEELOQ IFF

The HCS410/WM is an IFF transponder for verification of a token. In IFF mode the HCS410/WM is ideally suited for authentication of a key before disarming a vehicle immobilizer. Once the key has been inserted in the car's ignition the decoder would inductively poll the key, validating it before disarming the immobilizer.

IFF validation of the token involves a random challenge being sent by a decoder to a token. The token then generates a response to the challenge and sends this response to the decoder (Figure 1-1). The decoder calculates an expected response using the same challenge. The expected response is compared to the response received from the token. If the responses match, the token is identified as a valid token and the decoder can take appropriate action.

The HCS410/WM can do either 16 or 32-bit IFF. The HCS410/WM has two encryption algorithms that can be used to generate a response to a challenge. In addition there are up to two encoder keys that can be used by the HCS410/WM. Typically each HCS410/WM will be programmed with a unique encoder key(s).

In IFF mode, the HCS410/WM will wait for a command from the base station and respond to the command. The command can either request a read/write from user EEPROM or an IFF challenge response. A given 16 or 32-bit challenge will produce a unique 16/32-bit response, based on the IFF key and IFF algorithm used.

**FIGURE 1-1:   BASIC OPERATION OF AN IFF TOKEN**
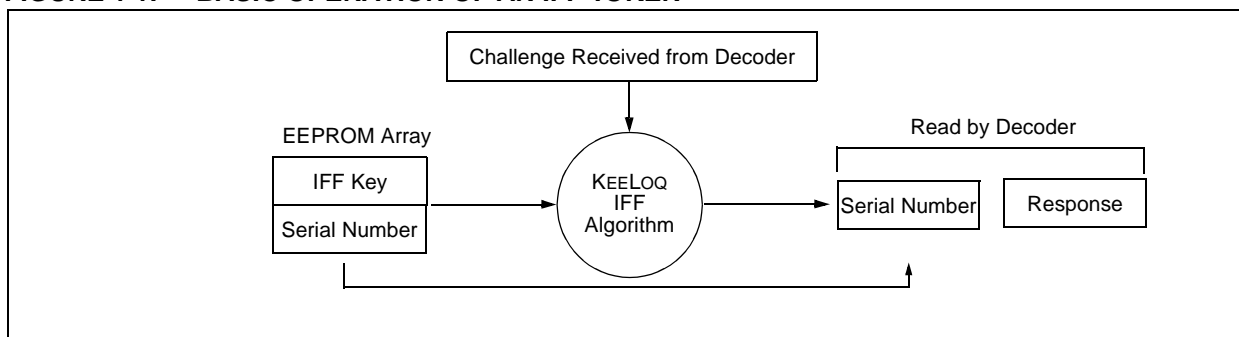
2.0 DEVICE DESCRIPTION

Figure 2-1 shows the internal components of the HCS410/WM. The resonant LC circuit has 2 functions:

- Inductive antenna for communications between the HCS410 and the base station
- Power source to charge the pool capacitor. The pool capacitor functions as a battery when the HCS410/WM is used.

FIGURE 2-1: TRANSPONDER CIRCUIT
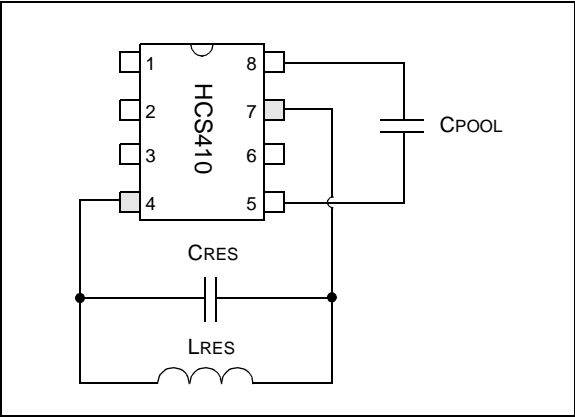
3.0 DEVICE OPERATION

The user can perform an IFF validation, write to the user EEPROM and read from the user EEPROM. Each operation consists of the decoder sending an opcode and data while the HCS410/WM gives a response.

There are two IFF modes: IFF1 and IFF2. IFF1 allows only one key IFF, while IFF2 allows two keys to be used.

3.1 IFF Mode Activation

The HCS410/WM will enter IFF mode if the capacitor/inductor resonant circuit generates a voltage large enough so that the pool capacitor can power the device. After the verified application of power and elapse of the reset period, the device will start responding by pulsing the field with ACK pulses as shown in Figure 3-3. This action will continue until the pulse train is terminated by receiving a start signal of duration $2T_E$, on the LC inputs before the next expected ACK pulse. The device now enters the IFF mode and expects to receive an 'Opcode' and a 0/16/32-bit Data-stream to react on. The data rate (T_E) is determined by the Transponder Baud Select (IFFB) configuration option.

3.2 IFF Decoder Commands

As shown in Figure 3-1, a logic 1 and 0 are differentiated by the time between two rising edges. A long pulse indicates a 1; a short pulse, a 0.

FIGURE 3-1: MODULATION FOR IFF COMMUNICATION
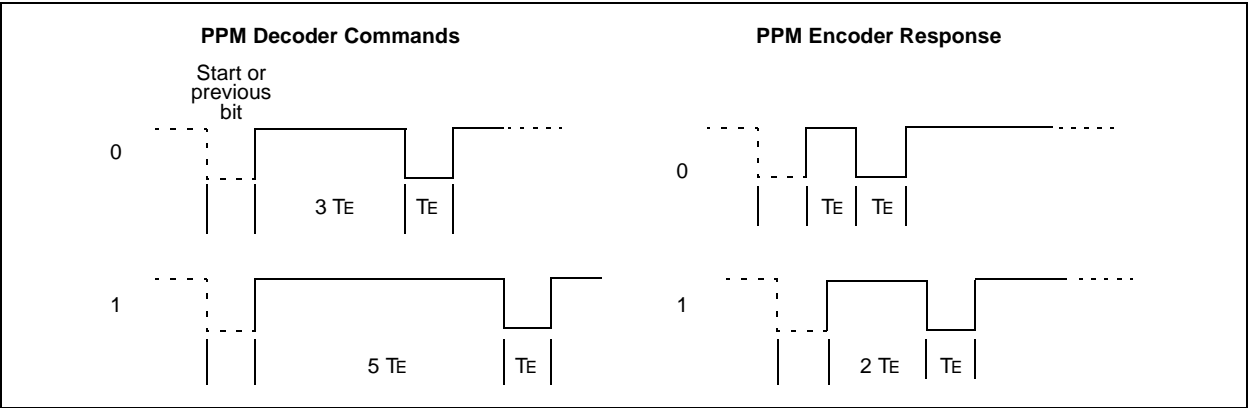
FIGURE 3-2: OVERVIEW OF IFF OPERATION
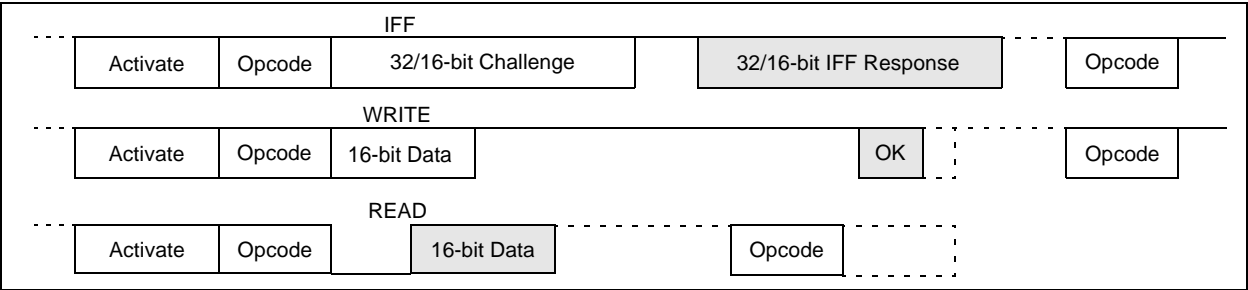
FIGURE 3-3: **DECODER IFF COMMANDS AND WAVEFORMS**
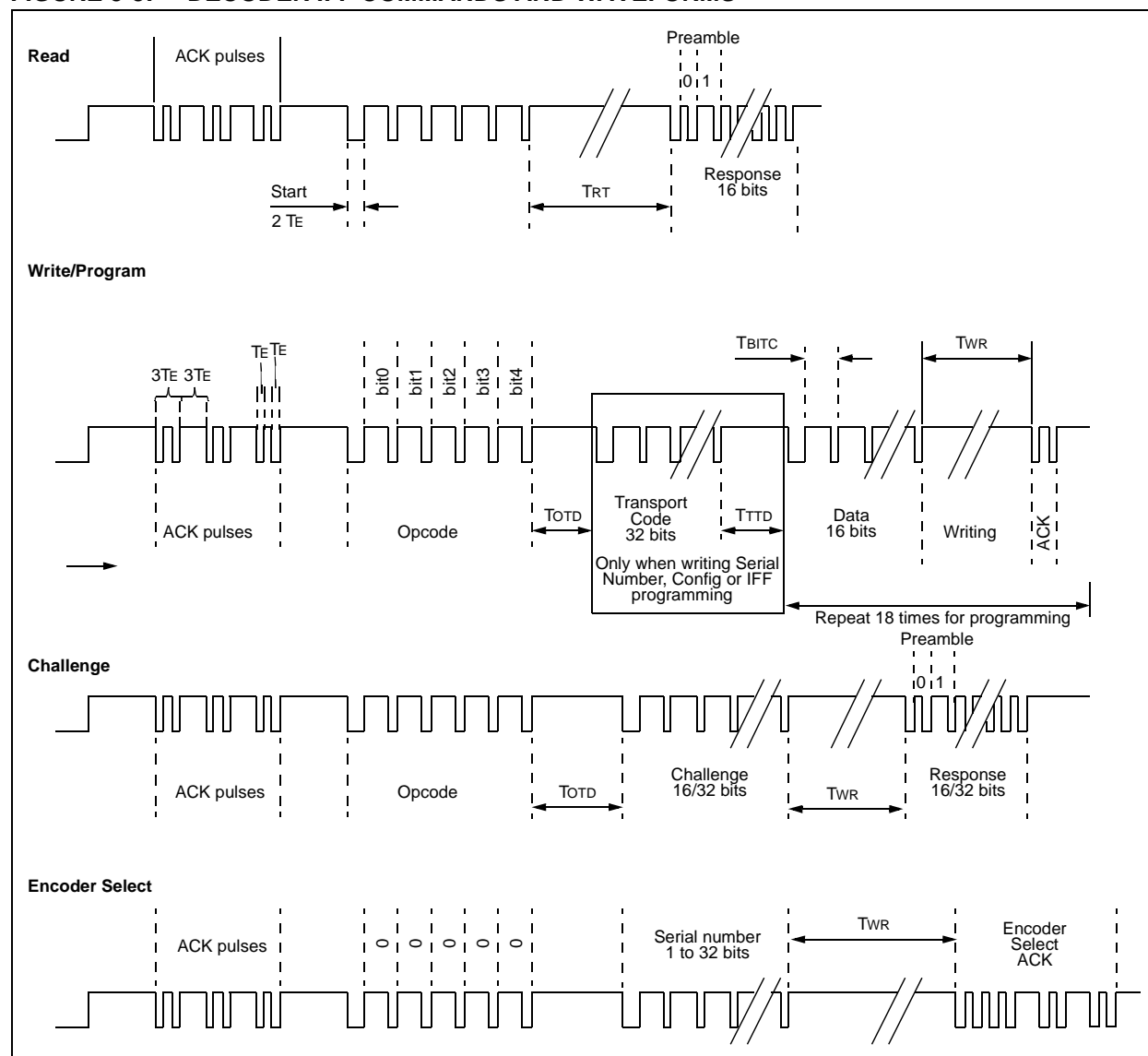
TABLE 3-1: **IFF TIMING PARAMETERS**

Parameter	Sym.	Min.	Typical	Max.	Units
Time Element IFFB = 0	T_E	—	200	—	μs

PPM Command Bit Time
    Data = 1
    Data = 0
	T_{BITC}	3.5
		5.5
			6
			4
				—
				—
					T_E

PPM Response Bit Time
    Data = 1
    Data = 0
	T_{BITR}	—
		—
			3
			2
				—
				—
					T_E

PPM Command Minimum High Time	T_{PMH}	1.5	—	—	T_E
Response Time (Minimum for Read)	T_{RT}	6.5	—	—	ms
Opcode to Data Input Time	T_{OTD}	1.8	—	—	ms
Transport Code to Data Input Time	T_{TTD}	6.8	—	—	ms
IFF EEPROM Write Time (16 bits)	T_{WR}	—	16	30	ms

3.3 HCS410/WM Responses

The responses from the HCS410/WM are in PPM format. See Figure 3-3 for additional information. Every response from the HCS410 is preceded by a "2 bit preamble" of 01_2, and then 16/32 bits of data.

3.4 IFF Response

The 16/32-bit response to a 16/32-bit challenge, is transmitted once, after which the device is ready to accept another command. The same applies to the result of a Read command. The opcode written to the device specifies the challenge length and algorithm used. The response always starts with a leading preamble of 01_2 followed by the 16/32 bits of data.

3.5 IFF Write

The decoder can write to USER[0:3], SER[0:1], and the configuration word in the EEPROM.

After the HCS410/WM has written the word into the EEPROM, it will give two acknowledge pulses (T_E wide and T_E apart) on the LC pins.

When writing to the serial number or configuration word, the user must send the transport code before the write will begin.

> **Note:** If the configuration word is written, the device must be reset to allow the new configuration settings to come into effect.

3.6 IFF Read

The decoder can read USER[0:3], SER[0:1], and the configuration word in the EEPROM. After the data has been read, the device is ready to receive a command again.

Each read command is followed by a 16-bit data response. The response always starts with a leading preamble of 01_2 and then the 16-bits of data.

TABLE 3-1: LIST OF IFF COMMANDS

Command	Description	Expected data In	Response
00000	Select HCS410/WM, used if Anti-collision enabled	1 to 32 bits of the serial number (SER)	Encoder select acknowledge if SER match
00001	Read configuration word	None	16-bit configuration word
00010	Read low serial number	None	16 bits of serial number (SER0)
00011	Read high serial number	None	16 bits of serial number (SER1)
00100	Read user area 0	None	16 Bits of User EEPROM USR0
00101	Read user area 1	None	16 Bits of User EEPROM USR1
00110	Read user area 2	None	16 Bits of User EEPROM USR2
00111	Read user area 3	None	16 Bits of User EEPROM USR3
01000	Program HCS410 EEPROM	Transport code (32 bits); Complete memory map: 18 x 16 bit words (288 bits)	Write acknowledge pulse after each 16-bit word, 288 bits transmitted in 18 bursts of 16-bits
01001	Write configuration word	Transport code (32 bits); 16 Bit configuration word	Write acknowledge pulse
01010	Write low serial number	Transport code (32 bits); Lower 16 bits of serial number (SER0)	Write acknowledge pulse
01011	Write high serial number	Transport code (32 bits); Higher 16 bits of serial number (SER1)	Write acknowledge pulse
01100	Write user area 0	16 Bits of User EEPROM USR0	Write acknowledge pulse
01101	Write user area 1	16 Bits of User EEPROM USR1	Write acknowledge pulse
01110	Write user area 2	16 Bits of User EEPROM USR2	Write acknowledge pulse
01111	Write user area 3	16 Bits of User EEPROM USR3	Write acknowledge pulse
1X000	IFF1 using key-1 and IFF algorithm	32-Bit Challenge	32-Bit Response
1X001	IFF1 using key-1 and HOP algorithm	32-Bit Challenge	32-Bit Response
1X100	IFF2 32-bit using key-2 and IFF algorithm	32-Bit Challenge	32-Bit Response
1X101	IFF2 32-bit using key-2 and HOP algorithm	32-Bit Challenge	32-Bit Response

3.7   IFF Special Features

3.7.1   ANTI-COLLISION (ACOLI)

When the ACOLI bit is set in the configuration word, anti-collision mode is entered. The HCS410/WM will start sending ACK pulses when it enters a magnetic field. The ACK pulses stop as soon as the HCS410/WM detects a start bit from the decoder. A 'select encoder' opcode (00000) is then sent out by the decoder, followed by a 32-bit serial number. If the serial number matches the HCS410/WM's serial number, the HCS410/WM will acknowledge with the acknowledge sequence as shown in Figure 3-4. The HCS410/WM can then be addressed as normal. If the serial number does not match, the IFF encoder will stop transmitting ACK pulses until it is either removed from the field or the correct serial number is given.

FIGURE 3-4:   SERIAL NUMBER CORRECT ACKNOWLEDGE SEQUENCE
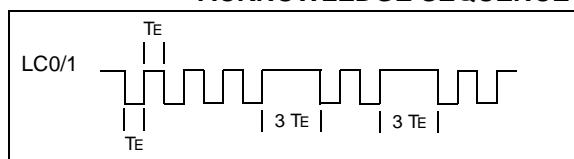
3.7.2   INTELLIGENT DAMPING

If the IDAMP bit is set to 0, the HCS410/WM will clamp the LC pins for 5 µs every 1/4 T_E, whenever the HCS410/WM is expecting data from the decoder. The intelligent damping pulses start 64 T_E after the acknowledge pulses have been sent and continue for 64 T_E. If the HSC410 detects data from the base station while sending out damp pulses, the damp pulses will continue to be sent. The damping will help the LC circuit resonance decay faster when the field is removed. This can make high to low data field decay sharper.

Preliminary

4.0 EEPROM ORGANIZATION AND CONFIGURATION

The HCS410/WM has nonvolatile EEPROM memory which is used to store user programmable options. This information includes encoder keys, serial number, and up to 64-bits of user information.

4.1 IFF Programming

Upon receiving a programming opcode and the transport code, the EEPROM is erased. Thereafter, the first 16 bits of data can be written. After indicating that a write command has been successfully completed the device is ready to receive the next 16 bits. After a complete memory map was received, it will be transmitted in PPM format on the LC pins as 16-bit words.

After the EEPROM is erased, the configuration word is reloaded. This results in oscillator tuning bits of 0000 being used during programming. When using IFF programming, the user should read the configuration word and store the oscillator bits in the memory map to be programmed. A program command should be sent and the next set of ACK pulses transmitted by the HCS410/WM should be used to determine the T_E. A second program command can then be sent, and the device programmed using the T_E just calibrated.

4.2 Encoder Key 1 and 2

In IFF operation, the HCS410/WM uses encoder key1 or key2 to generate the response to a challenge received. The key or keys are created and programmed at the time of production using a key generation algorithm. Inputs to the key generation algorithm are the serial number and a secret manufacturer's code. While a number of key generation algorithms are supplied by Microchip, a user may elect to create their own method of key generation. This may be done providing that the decoder is programmed with the same means of creating the key for decryption purposes.

4.3 Transport Code

The least significant 32-bits of key2 are used as the transport code. The transport code is used to write-protect the serial number, configuration word and prevent accidental programming of the HCS410/WM.

4.4 Serial Number

There are 32 bits allocated for the serial number. The serial number is meant to be unique for every transmitter. The serial number can be programmed with a write command.

4.5 User Data

The 64-bit user EEPROM can be reprogrammed and read at any time using the IFF interface.

4.6 Configuration Data

The configuration data is used to select various encoder options. Further explanations of each of the bits are described in the following sections.

TABLE 4-1: CONFIGURATION OPTIONS

Symbol	Description
IDAMP	Intelligent Damping for High Q LC Tank.
IFF2	Enable IFF2 key
OSC0:3	Onboard Oscillator Tuning Bits
IFFB	Transponder Baud Rate
ACOLI	Anti Collision Communication Enable

4.6.1 IDAMP: INTELLIGENT DAMPING

If IDAMP is set to '1' intelligent damping is disabled.

4.6.2 IFF2: ENABLE IFF2 KEY

4.6.3 OSC: OSCILLATOR TUNING BITS

These bits allow the onboard oscillator to be tuned to within 10% of the nominal oscillator speed over both temperature and voltage.

TABLE 4-2: OSCILLATOR TUNING

OSC	Description
1000	Fastest
1001 1010 • • • 1111	Faster
0000	Nominal
0001 0010 • • • 0110	Slower
0111	Slowest

4.6.4 IFFB: TRANSPONDER BAUD RATE

This selects the baud rate for IFF communications for a T_E of 200 µs.

4.6.5 ACOLI: ANTI-COLLISION

If ACOLI is set, the anti-collision operation during bidirectional transponder mode (IFF) is enabled. This feature is useful in situations where multiple transponders enter the magnetic field simultaneously.
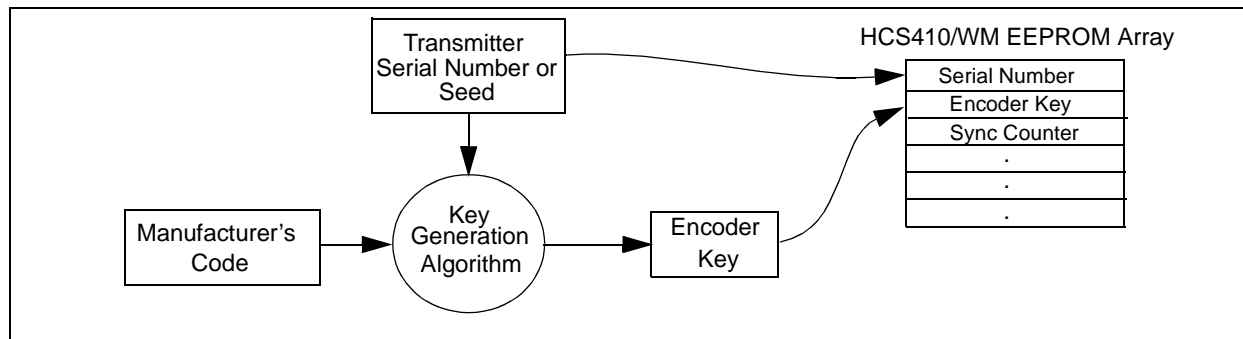
HCS410/WM

5.0 INTEGRATING THE HCS410/WM INTO A SYSTEM

Use of the HCS410/WM in a system requires a compatible decoder. This decoder is typically a microcontroller with compatible firmware. Firmware routines that accept transmissions from the HCS410/WM, decrypt the code hopping portion of the data stream and perform IFF functions are available. These routines provide system designers the means to develop their own decoding system.

5.1 Key Generation

The serial number for each transmitter is programmed by the manufacturer at the time of production. The generation of the encoder key is done using a key generation algorithm (Figure 5-1). Typically, inputs to the key generation algorithm are the serial number of the transmitter or seed value, and a 64-bit manufacturer's code. The manufacturer's code is chosen by the system manufacturer and must be carefully controlled. The manufacturer's code is a pivotal part of the overall system security.
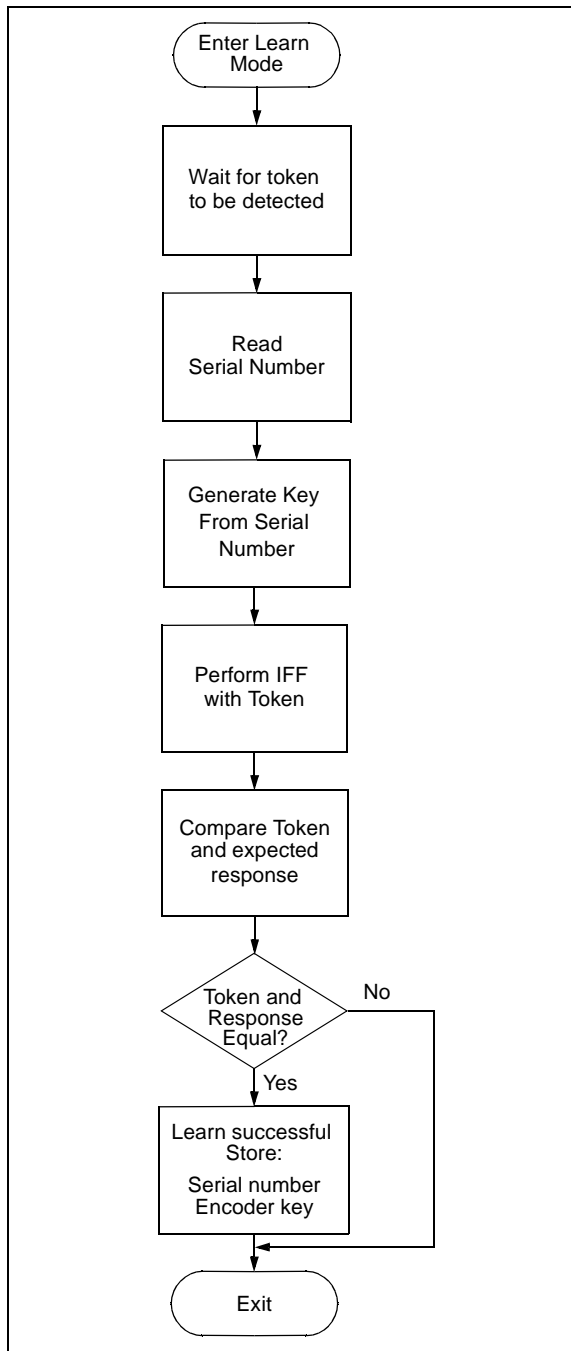
FIGURE 5-1: CREATION AND STORAGE OF ENCODER KEY DURING PRODUCTION

5.2 Receiver Learning an HCS410/WM

In order for a transmitter to be used with a decoder, the transmitter must first be 'learned'. Several learning strategies can be followed in the decoder implementation. When a transmitter is learned by a decoder, it is suggested that the decoder stores the serial number in EEPROM. The decoder must keep track of these values for every transmitter that is learned.

The maximum number of transmitters that can be learned is a function of how much EEPROM memory storage is available. The decoder must also store the manufacturer's code in order to learn an HCS410/WM, since this value will not change in a typical system, it is usually stored as part of the microcontroller ROM code. Storing the manufacturer's code as part of the ROM code is also better for security reasons.

Preliminary   © 2001 Microchip Technology Inc.

FIGURE 5-2: TYPICAL IFF LEARN SEQUENCE

```
        ╭──────────────╮
        │  Enter Learn │
        │     Mode     │
        ╰──────┬───────╯
               │
        ┌──────▼───────┐
        │ Wait for token│
        │ to be detected│
        └──────┬────────┘
               │
        ┌──────▼───────┐
        │    Read      │
        │ Serial Number│
        └──────┬───────┘
               │
        ┌──────▼───────┐
        │ Generate Key │
        │ From Serial  │
        │   Number     │
        └──────┬───────┘
               │
        ┌──────▼───────┐
        │ Perform IFF  │
        │  with Token  │
        └──────┬───────┘
               │
        ┌──────▼───────┐
        │ Compare Token│
        │ and expected │
        │  response    │
        └──────┬───────┘
               │
          ◇────▼────◇        No
          │Token and │──────────┐
          │ Response │          │
          │  Equal?  │          │
          ◇────┬────◇          │
            Yes │               │
        ┌───────▼──────┐        │
        │Learn successful│      │
        │   Store:      │       │
        │ Serial number │       │
        │ Encoder key   │       │
        └───────┬───────┘       │
                │◄──────────────┘
         ╭──────▼───────╮
         │     Exit     │
         ╰──────────────╯
```

5.3 IFF Decoder Operation

In a typical IFF decoder, the key generation on the decoder side is done by reading the serial number from a token and combining that with the manufacturer's code to recreate the encoder key that is stored on the token. The decoder polls for the presence of a token. Once detected the decoder reads the serial number. If the token has been learned, the decoder sends a challenge and reads the token's response. The decoder uses the encoder key stored in EEPROM to decrypt the response. The decrypted response is compared to the challenge. If they match, then identification was successful and the appropriate response is generated.
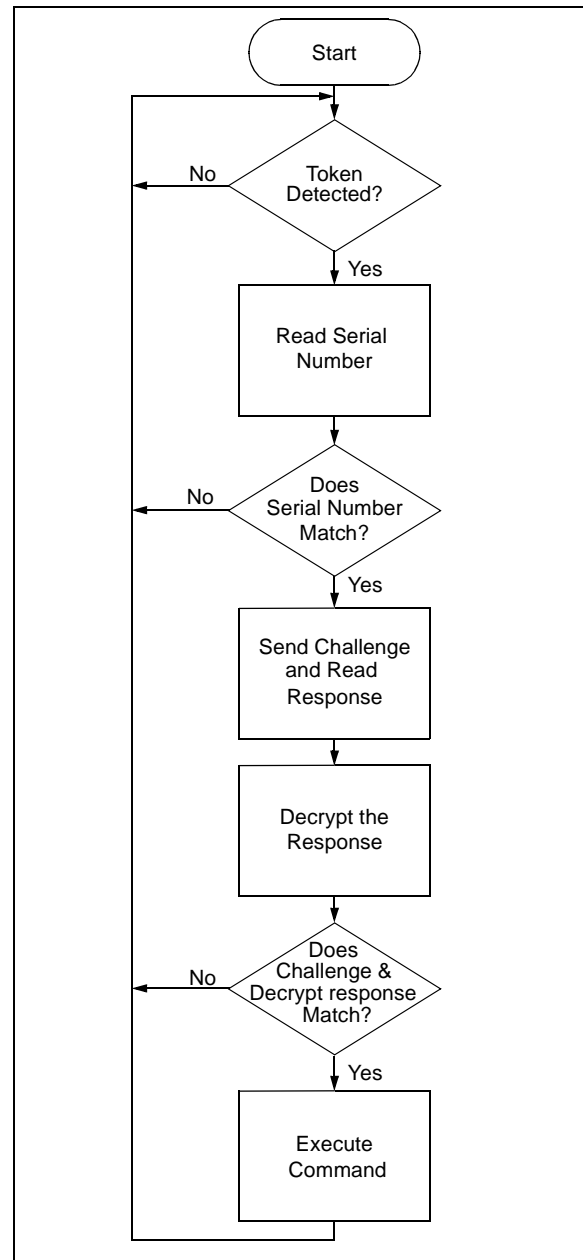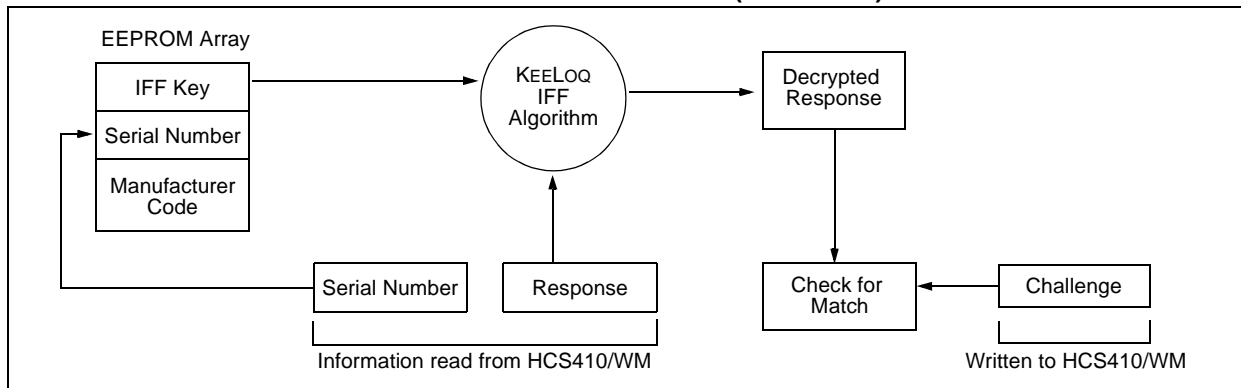
FIGURE 5-3: TYPICAL IFF DECODER OPERATION

```
          ╭──────────────╮
          │    Start     │
          ╰──────┬───────╯
                 │
          ◇──────▼──────◇
   No     │    Token     │
 ◄────────│  Detected?   │
 │        ◇──────┬──────◇
 │            Yes │
 │        ┌───────▼──────┐
 │        │ Read Serial  │
 │        │   Number     │
 │        └───────┬──────┘
 │                │
 │        ◇───────▼──────◇
 │  No    │    Does      │
 ◄────────│ Serial Number│
 │        │   Match?     │
 │        ◇───────┬──────◇
 │            Yes │
 │        ┌───────▼──────┐
 │        │Send Challenge│
 │        │  and Read    │
 │        │  Response    │
 │        └───────┬──────┘
 │                │
 │        ┌───────▼──────┐
 │        │ Decrypt the  │
 │        │  Response    │
 │        └───────┬──────┘
 │                │
 │        ◇───────▼──────◇
 │  No    │    Does      │
 ◄────────│  Challenge & │
 │        │Decrypt response│
 │        │   Match?     │
 │        ◇───────┬──────◇
 │            Yes │
 │        ┌───────▼──────┐
 │        │   Execute    │
 │        │   Command    │
 │        └───────┬──────┘
 └────────────────┘
```

FIGURE 5-4: **BASIC OPERATION OF AN IFF RECEIVER (DECODER)**

6.0   ELECTRICAL CHARACTERISTICS

Note: This package is IP67 qualified. This qualification rating is based on the ingress protection tests performed in IEC529 (which equates to European Standard EN 60529). This standard indicates the degree of protection provided by the device against access to hazardous parts, solid foreign objects, and ingress of water.

TABLE 6-1:   ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Value	Units
Operating Temperature Range	T_{AMB}	-40 to +85°	°C
Storage Temperature Range	T_{STG}	-40 to +100°	°C
Magnetic Field Strength	H	1000	A/m

TABLE 6-2:   OPERATING CHARACTERISTICS TRANSPONDER

T_{AMB} = 25°C, f = 125 kHz unless otherwise noted.						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions/Pins
Inductor						
Inductance	L_{RES}	—	895	—	µH	
Resonating Capacitor						
Capacitance	C_{RES}	—	1800	—	pF	
Pool Capacitor						
Capacitance	C_{POOL}	—	100	—	nF	
LC Circuit, H = 20 A/m						
Resonance Frequency	f_R	123.1	125	128.4	kHz	
Quality Factor	Q	—	40	—		Read Mode

TABLE 6-3:   MAGNETIC FIELD STRENGTH (H)

T_{AMB} = 25°C, f_R = 125 kHz unless otherwise noted.						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions/Pins
Minimum Field Strength						

Read Mode **(Note)**
    T_{AMB} = -40°C
    T_{AMB} = 25°C
    T_{AMB} = 85°C
	H_{READ}	
		—
		—
		—
			
			11.0
			7.5
			10.5
				
				—
				—
				—
					A/m	

Write Mode **(Note)**
    T_{AMB} = -40°C
    T_{AMB} = 25°C
    T_{AMB} = 85°C
	H_{PROG}	
		—
		—
		—
			
			35
			20
			30
				
				—
				—
				—
					A/m	

Data Retention EEPROM	$t_{RETENTION}$	10	—	—	Years	
Programming Cycles EEPROM	—	100,000	—	—		
Programming/Time/Word	t_P	—	16	30	ms	

Note: Optimal coupling factor between base station and HCS410/WM.

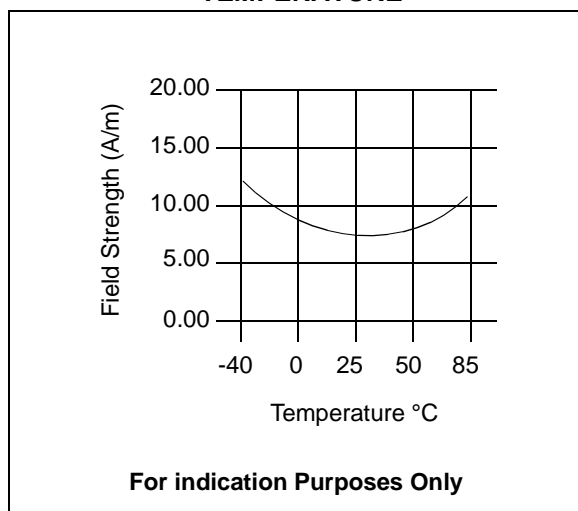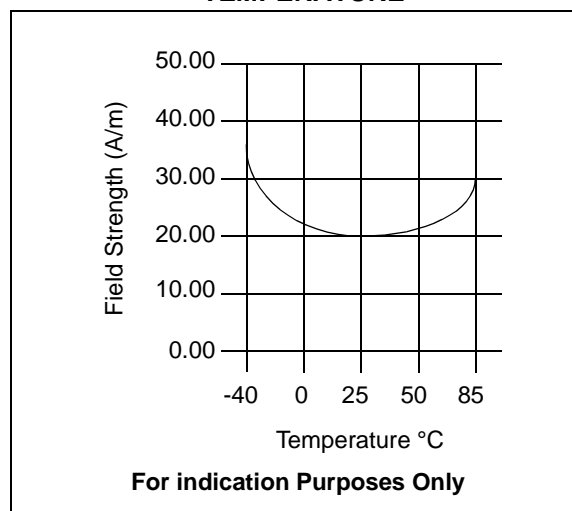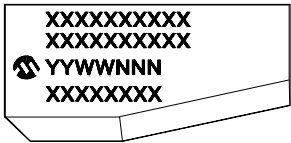**FIGURE 6-1:** **TYPICAL READ FIELD STRENGTH OVER TEMPERATURE**

For indication Purposes Only

FIGURE 6-2: **TYPICAL PROGRAM FIELD STRENGTH OVER TEMPERATURE**

For indication Purposes Only

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

SOT385

```
XXXXXXXXXX
XXXXXXXXXX
Ⓜ YYWWNNN
XXXXXXXX
```

Example

```
HCS410/WM
XXXXXXXXXX
0025NNN
Ⓜ XXXXXXXX
```
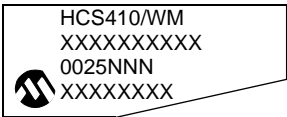
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

HCS410/WM

7.2   Package Details

Leadless Wedge Module Plastic Small Outline Transistor (WM) (SOT385)
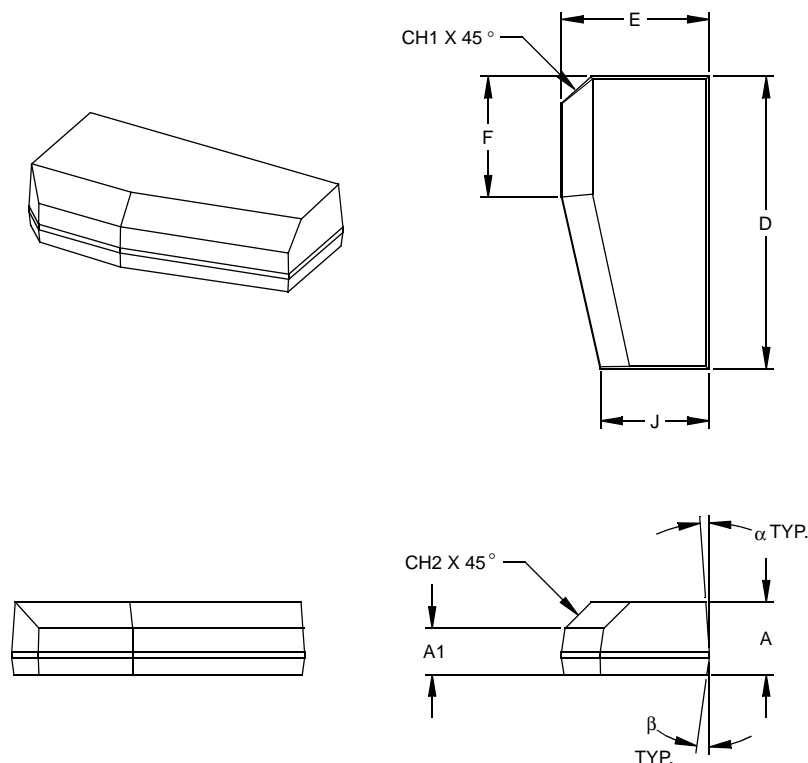
	Units	INCHES			MILLIMETERS*		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Overall Height	A	.114	.118	.120	2.90	3.00	3.05
Bottom of Package to Chamfer	A1	.075	.079	.083	1.90	2.00	2.10
Overall Width	E	.236	.240	2.44	6.00	6.10	6.20
Overall Length	D	.472	.476	.480	12.00	12.10	12.20
Width at Tapered End	J	.173	.177	.181	4.40	4.50	4.60
Length of Flat	F	.193	.197	.200	4.90	5.00	5.10
Chamfer Distance, Horizontal	CH1	.039	.043	.047	1.00	1.10	1.20
Chamfer Distance, Vertical	CH2	.039	.043	.047	1.00	1.10	1.20
Mold Draft Angle Top	α	4	6	8	4	6	8
Mold Draft Angle Bottom	β	4	6	8	4	6	8

*Controlling Parameter

Notes:

Dimensions D, E, F and J do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.

Drawing No. C04-109

Preliminary

ON-LINE SUPPORT

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HCS410/WM

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Device: **HCS410/WM**   Literature Number: **DS41116B**

Questions:

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    _____

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6.   Is there any incorrect or misleading information (what and where)?

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7.   How would you improve this document?

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8.   How would you improve our software, systems, and silicon products?

    _____

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NOTES:

HCS410/WM PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

HCS410/WM /X /XX

Package: SOT385 = Leadless Wedge Module (WM)

Temperature Range: I = −40°C to +85°C

Device: HCS410 = Crypto Read/Write Transponder Module

Sales and Support

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Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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