



## 3.3V CMOS OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

**IDT74LVC573A**

### FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,  
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of - 40°C to +85°C
- V<sub>CC</sub> = 3.3V ± 0.3V, Normal Range
- V<sub>CC</sub> = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

### Drive Features for LVC573A:

- High Output Drivers: ±24mA
- Reduced system switching noise

### APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

### DESCRIPTION:

The LVC573A octal transparent D-type latch is built using advanced dual metal CMOS technology. The device features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads, and is particularly suitable for implementing buffer registers, input-output (I/O) ports, bidirectional bus drivers, and working registers.

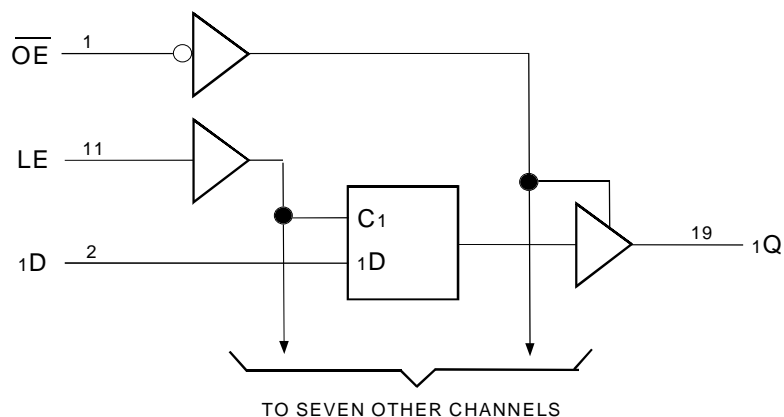
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.  $\overline{OE}$  does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

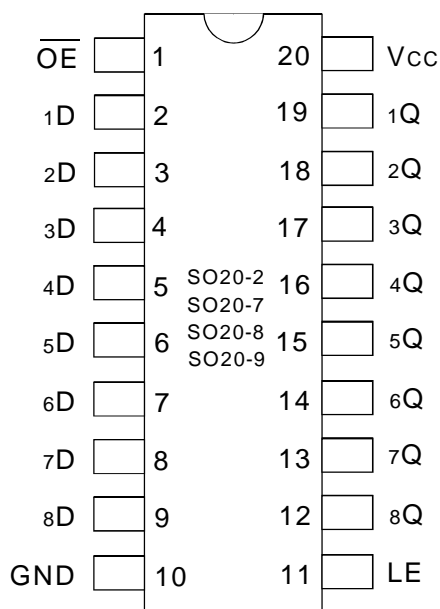
The LVC573A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP  
TOP VIEW

## PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output-enable Input (Active LOW)
LE	Latch-enable Input
xD	Data Inputs
xQ	3-State Outputs

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
I <sub>OUT</sub>	DC Output Current	- 50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	- 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

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### NOTE:

- As applicable to the device type.

## FUNCTION TABLE (each latch)<sup>(1)</sup>

Inputs			Outputs
$\overline{OE}$	LE	xD	xQ
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
Q<sub>0</sub> = Level of Q before the indicated steady-state input conditions were established

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  To  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V to } 2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V to } 2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0 \text{ to } 5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0 \text{ to } 5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND or } V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

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### NOTES:

- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.3\text{V to } 3.6\text{V}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3.0\text{V}$		2.4	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.3\text{V to } 3.6\text{V}$	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3.0\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

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### NOTE:

- $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

**OPERATING CHARACTERISTICS,  $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 25^\circ C$**

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power dissipation capacitance per latch outputs enabled	$C_L = 0pF$ , $f = 10MHz$	37	pF
CPD	Power dissipation capacitance per latch outputs disabled		4	pF

**SWITCHING CHARACTERISTICS <sup>(1)</sup>**

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay xD to xQ	—	—	—	7.7	1.5	6.9	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to xQ	—	—	—	8.4	2	7.7	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time OE to xQ	—	—	—	8.5	1.5	7.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time OE to xQ	—	—	—	7	1.6	6.5	ns
$t_W$	Pulse Duration, LE HIGH	—	—	3.3	—	3.3	—	ns
$t_{SU}$	Setup Time, data before LE↓	—	—	2	—	2	—	ns
$t_H$	Hold Time, data after LE↓	—	—	1.5	—	1.5	—	ns
$t_{SK(0)}$	Output Skew <sup>(2)</sup>	—	—	—	—	—	1	ns

**NOTES:**

1. See test circuits and waveforms.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
2. Skew between any two outputs of the same package and switching in the same direction.

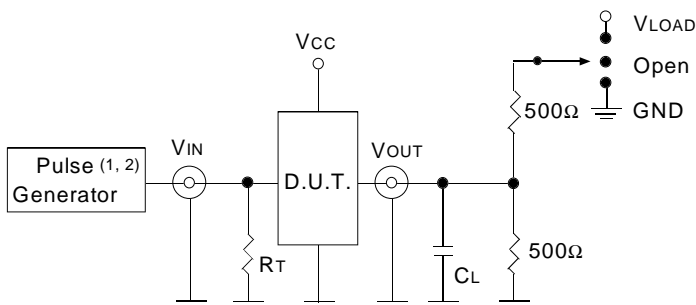
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> (1) = 3.3V ± 0.3V	V <sub>CC</sub> (1) = 2.7V	V <sub>CC</sub> (2) = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.

R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

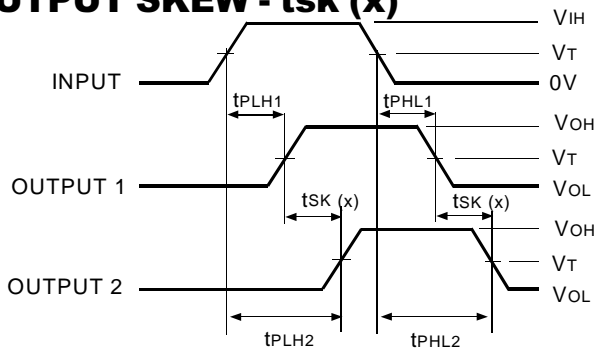
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain	V <sub>LOAD</sub>
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

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### OUTPUT SKEW - t<sub>SK</sub>(x)



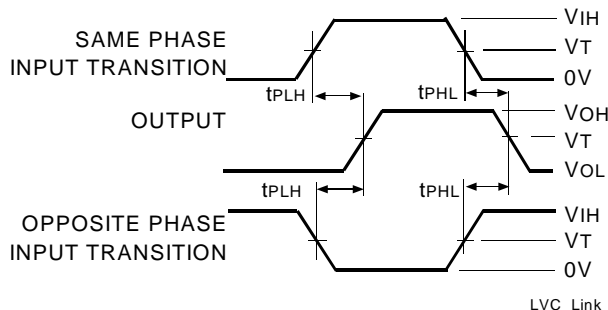
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

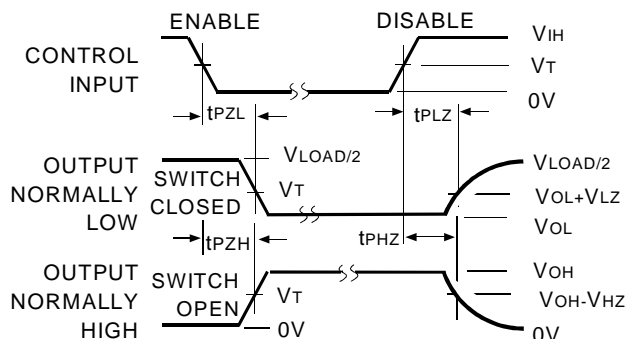
1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

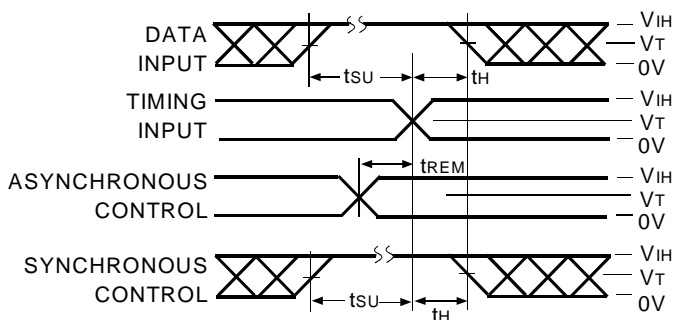


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#### NOTE:

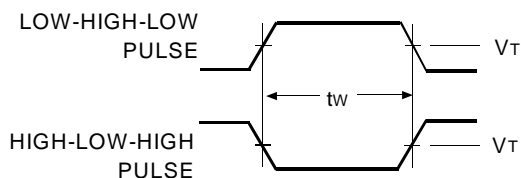
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



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### PULSE WIDTH



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## ORDERING INFORMATION

IDT    XX    LVC    X    XXXX    XX  
          Temp. Range    Bus-Hold    Device Type    Package

SO    Small Outline IC (gull wing) (SO20-2)  
 PY    Shrink Small Outline Package (SO20-7)  
 Q    Quarter Size Small Outline Package (SO20-8)  
 PG    Thin Shrink Small Outline Package (SO20-9)

573A    Octal Transparent D-Type Latch with 3-State Outputs,  $\pm 24\text{mA}$

Blank    No Bus-hold

74     $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$



### CORPORATE HEADQUARTERS

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