



3.3V CMOS 16-BIT BUS TRANSCIEVER AND REGISTER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCH16652A

FEATURES:

- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH16652A:

- High Output Drivers: ±24mA
- Reduced System Switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

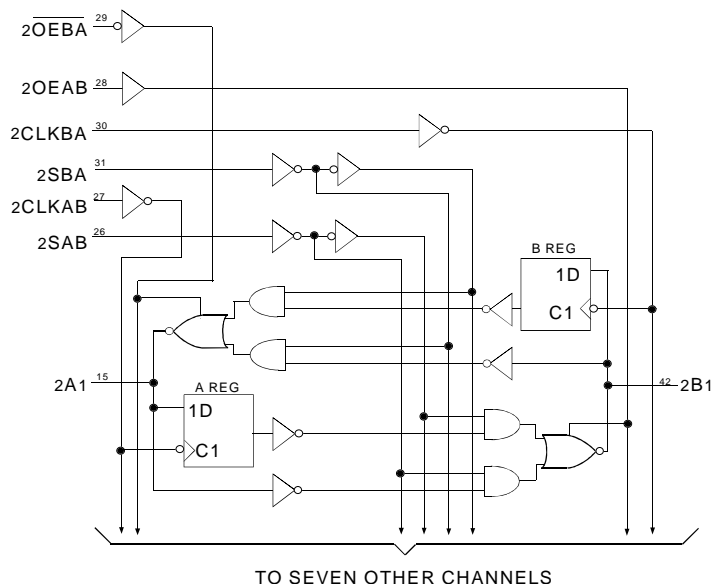
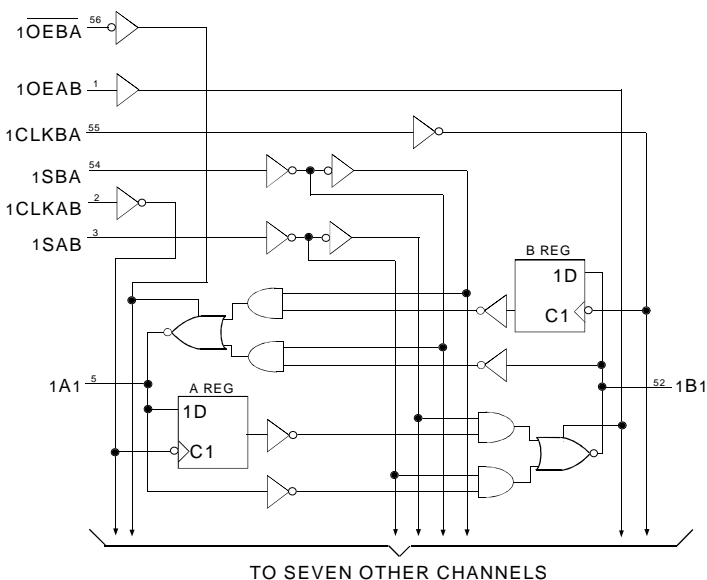
DESCRIPTION:

This 16-bit transceiver and register is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features complementary Output Enable (OEAB and \overline{OEBA}) inputs to control the transceiver functions and Select lines (SAB and SBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

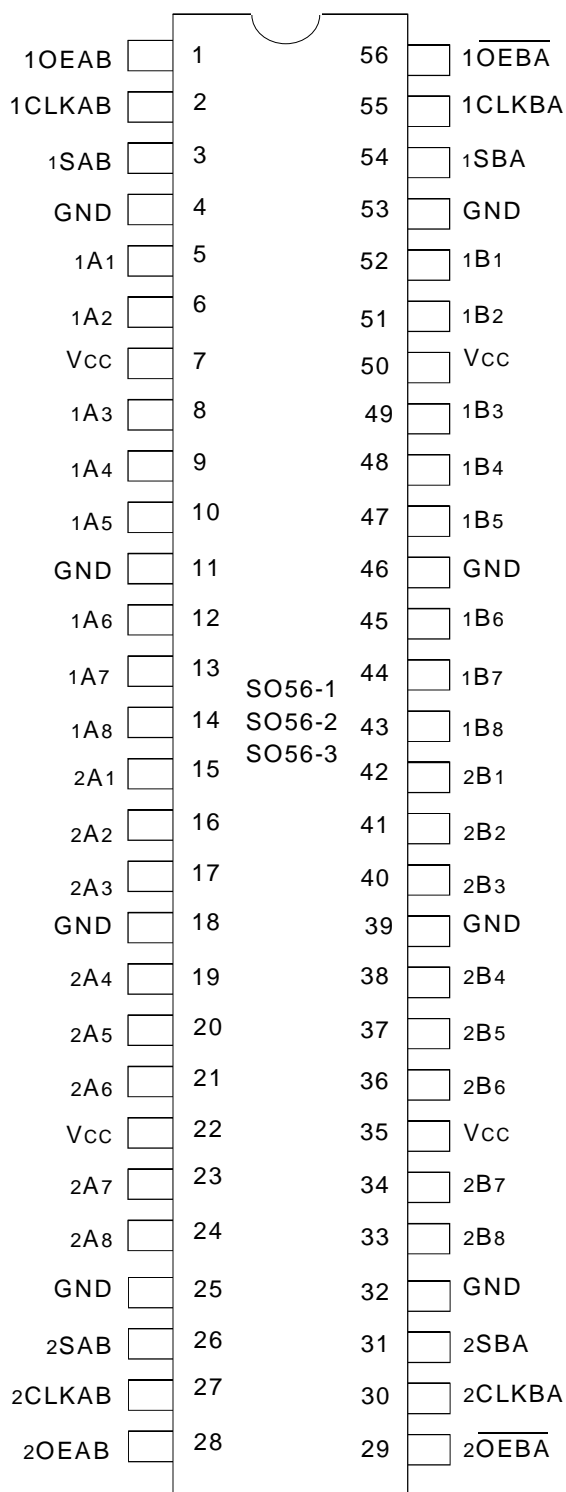
The LVCH16652A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16652A has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|------------------------------------|---|---------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | - 0.5 to +6.5 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | - 0.5 to +6.5 | V |
| TSTG | Storage Temperature | - 65 to +150 | °C |
| IOUT | DC Output Current | - 50 to +50 | mA |
| I _{IK} I _{OK} | Continuous Clamp Current, V _I < 0 or V _O < 0 | - 50 | mA |
| I _{CC} I _{SS} | Continuous Current through each V _{CC} or GND | ±100 | mA |

LVC Link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 4.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 6.5 | 8 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 6.5 | 8 | pF |

LVC Link

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

| Pin Names | Description |
|----------------|--|
| xAx | Data Register A Inputs ⁽¹⁾ Data Register B Outputs |
| xBx | Data Register B Inputs ⁽¹⁾ Data Register A Outputs |
| xCLKAB, xCLKBA | Clock Pulse Inputs |
| xSAB, xSBA | Output Data Source Select Inputs |
| xOEAB, xOEBA | Output Enable Inputs |

NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (1)

| Inputs | | | | | | Data I/O (2) | | Operation or Function |
|--------|-------|--------|--------|------------------|------------------|----------------------------|----------------------------|--|
| xOEAB | xOEBA | xCLKAB | xCLKBA | xSAB | xSBA | xAx | xBx | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B Data |
| X | H | ↑ | H or L | X | X | Input | Unspecified ⁽³⁾ | Store A, Hold B |
| H | H | ↑ | ↑ | X ⁽³⁾ | X | Input | Output | Store A in Both Registers |
| L | X | H or L | ↑ | X | X | Unspecified ⁽³⁾ | Input | Hold A, Store B |
| L | L | ↑ | ↑ | X | X ⁽³⁾ | Output | Input | Store B in Both Registers |
| L | L | X | X | X | L | Output | Input | Real Time B Data to A Bus |
| L | L | X | H or L | X | H | Output | Input | Stored B Data to A Bus |
| H | H | X | X | L | X | Input | Output | Real Time A Data to B Bus |
| H | H | H or L | X | H | X | Input | Output | Stored A Data to B Bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A Data to B Bus and Stored B Data to A Bus |

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
- The data-output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data-input functions are always enabled, i.e. data at the bus pins will be stored on every low-to-high transition of the clock inputs.
- Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

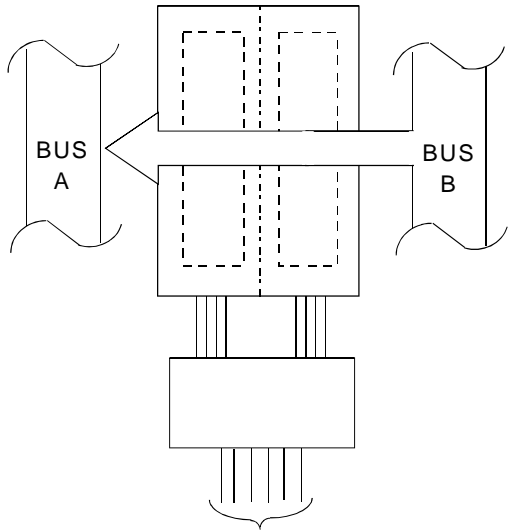
Operating Condition: TA = -40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|-----------------------|--|---|------------------|------|---------------------|------|------|
| VIH | Input HIGH Voltage Level | VCC = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | VCC = 2.7V to 3.6V | | 2 | — | — | |
| VIL | Input LOW Voltage Level | VCC = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | VCC = 2.7V to 3.6V | | — | — | 0.8 | |
| IIH IIL | Input Leakage Current | VCC = 3.6V | VI = 0 to 5.5V | — | — | ±5 | μA |
| IOZH IOZL | High Impedance Output Current (3-State Output pins) | VCC = 3.6V | VO = 0 to 5.5V | — | — | ±10 | μA |
| IOFF | Input/Output Power Off Leakage | VCC = 0V, VIN or VO ≤ 5.5V | | — | — | ±50 | μA |
| VIK | Clamp Diode Voltage | VCC = 2.3V, IIN = -18mA | | — | -0.7 | -1.2 | V |
| VH | Input Hysteresis | VCC = 3.3V | | — | 100 | — | mV |
| ICCL ICCH IC CZ | Quiescent Power Supply Current | VCC = 3.6V | VIN = GND or VCC | — | — | 10 | μA |
| | | 3.6 ≤ VIN ≤ 5.5V ⁽²⁾ | | — | — | 10 | |
| ΔICC | Quiescent Power Supply Current Variation | One input at VCC - 0.6V other inputs at VCC or GND | | — | — | 500 | μA |

LVC Link

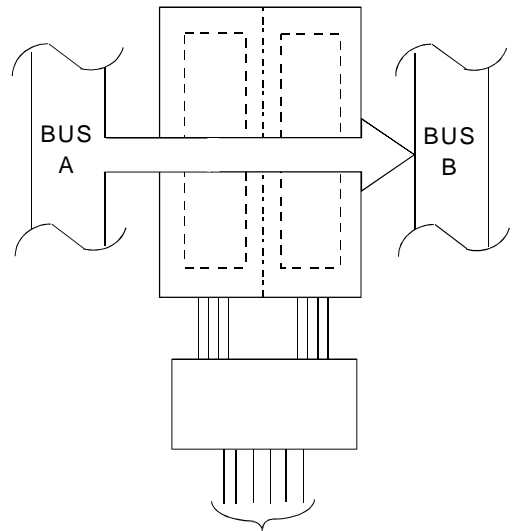
NOTES:

- Typical values are at VCC = 3.3V, +25°C ambient.
- This applies in the disabled state only.



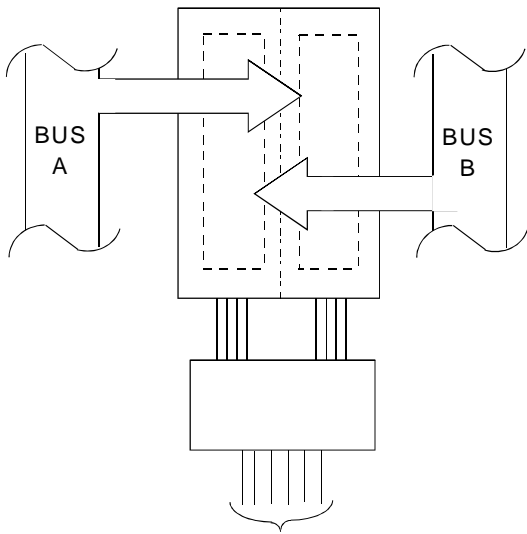
xOEAB L xOEBA L xCLKAB X xCLKBA X xSAB X xSBA L

**REAL-TIME TRANSFER
 BUS B TO A**



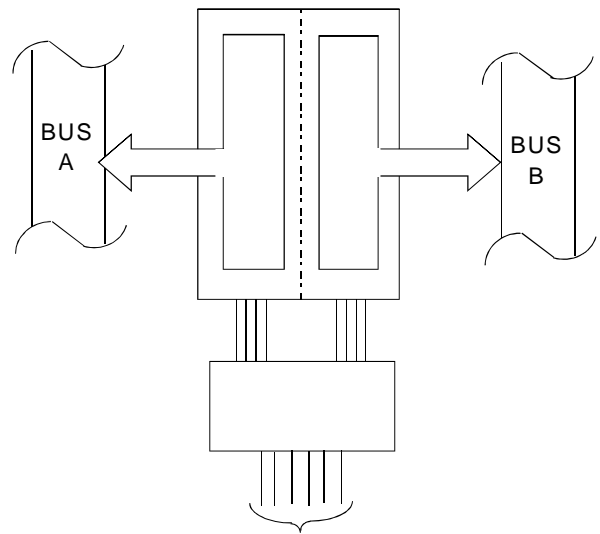
xOEAB H xOEBA H xCLKAB X xCLKBA X xSAB L xSBA X

**REAL-TIME TRANSFER
 BUS A TO B**



| | | | | | |
|-------|-------|--------|--------|------|------|
| xOEAB | xOEBA | xCLKAB | xCLKBA | xSAB | xSBA |
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE
 FROM A AND/OR B**



| | | | | | |
|-------|-------|--------|--------|------|------|
| xOEAB | xOEBA | xCLKAB | xCLKBA | xSAB | xSBA |
| H | L | H or L | H or L | H | H |

**TRANSFER
 STORED DATA TO A AND/OR B**

BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|----------------|----------------------------------|------------------------|----------------------------|------|---------------------|-------|------|
| IBHH IBHL | Bus-Hold Input Sustain Current | V _{CC} = 3.0V | V _I = 2.0V | - 75 | — | — | μA |
| | | | V _I = 0.8V | 75 | — | — | |
| IBHH IBHL | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | V _I = 1.7V | — | — | — | μA |
| | | | V _I = 0.7V | — | — | — | |
| IBHHO IBHLO | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | V _I = 0 to 3.6V | — | — | ± 500 | μA |

LVC Link

NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|--------|---------------------|--------------------------------|---------------------------|--------------------------|------|------|
| VOH | Output HIGH Voltage | V _{CC} = 2.3V to 3.6V | I _{OH} = - 0.1mA | V _{CC} - 0.2 | — | V |
| | | V _{CC} = 2.3V | I _{OH} = - 6mA | 2 | — | |
| | | V _{CC} = 2.3V | I _{OH} = - 12mA | 1.7 | — | |
| | | V _{CC} = 2.7V | | 2.2 | — | |
| | | V _{CC} = 3.0V | | 2.4 | — | |
| | | | V _{CC} = 3.0V | I _{OH} = - 24mA | 2.2 | |
| VOL | Output LOW Voltage | V _{CC} = 2.3V to 3.6V | I _{OL} = 0.1mA | — | 0.2 | V |
| | | V _{CC} = 2.3V | I _{OL} = 6mA | — | 0.4 | |
| | | | I _{OL} = 12mA | — | 0.7 | |
| | | V _{CC} = 2.7V | I _{OL} = 12mA | — | 0.4 | |
| | | V _{CC} = 3.0V | I _{OL} = 24mA | — | 0.55 | |

LVC Link

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|--------|--|---------------------------------|---------|------|
| CPD | Power Dissipation Capacitance per transceiver Outputs enabled | C _L = 0pF, f = 10MHz | 55 | pF |
| CPD | Power Dissipation Capacitance per transceiver Outputs disabled | | 12 | pF |

SWITCHING CHARACTERISTICS (1)

| Symbol | Parameter | V _{CC} = 2.7V | | V _{CC} = 3.3V±0.3V | | Unit |
|--------------------------------------|--|------------------------|------|-----------------------------|------|------|
| | | Min. | Max. | Min. | Max. | |
| f _{MAX} | | 150 | — | 150 | — | MHz |
| t _{PLH} t _{PHL} | Propagation Delay xAx to xBx or xBx to xAx | — | 6.4 | 1.4 | 6.3 | ns |
| t _{PLH} t _{PHL} | Propagation Delay xCLKAB or xCLKBA to xAx or xBx | — | 7.3 | 2.4 | 6.4 | ns |
| t _{PLH} t _{PHL} | Propagation Delay xSBA or xSAB to xAx or xBx | — | 8.8 | 1.9 | 7.4 | ns |
| t _{PZH} t _{PZL} | Output Enable Time xOEBA to xAx | — | 6.6 | 1.6 | 6.3 | ns |
| t _{PZH} t _{PZL} | Output Enable Time xOEAB to xBx | — | 6.6 | 1.6 | 6.3 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time xOEBA to xAx | — | 6.6 | 1.2 | 6.2 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time xOEAB to xBx | — | 6.6 | 1.2 | 6.2 | ns |
| t _{SU} | Set-up Time, xAx or xBx before xCLKAB↑ or xCLKBA↑ | 3.4 | — | 3 | — | ns |
| t _H | Hold Time, xAx or xBx after xCLKAB↑ or xCLKBA↑ | 0 | — | 0.2 | — | ns |
| t _w | Pulse duration, CLKAB or CLKBA HIGH or LOW | 3.3 | — | 3.3 | — | ns |
| t _{sk(o)} | Output Skew ⁽²⁾ | — | — | — | 500 | ps |

NOTES:

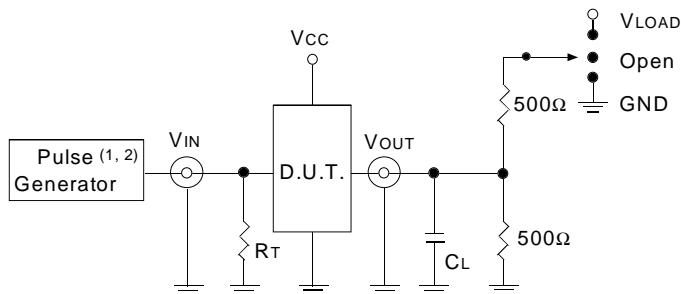
1. See test circuits and waveforms. T_A = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{CC} (1) = 3.3V ± 0.3V | V _{CC} (1) = 2.7V | V _{CC} (2) = 2.5V ± 0.2V | Unit |
|-------------------|-----------------------------------|----------------------------|-----------------------------------|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |

TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

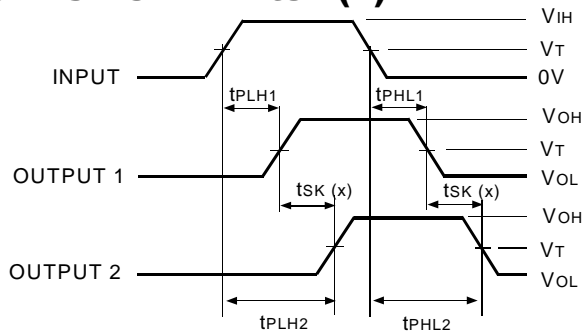
NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

| Test | Switch |
|-----------------------------------|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other tests | Open |

OUTPUT SKEW - t_{SK}(x)

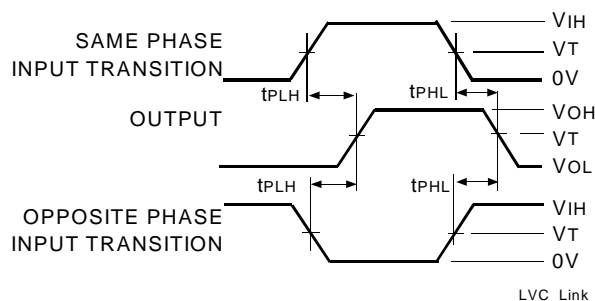


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

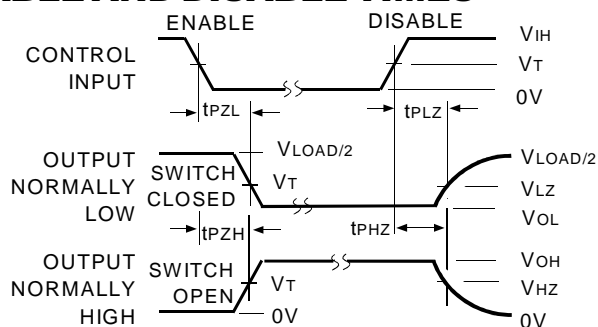
NOTES:

1. For t_{SK}(a) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



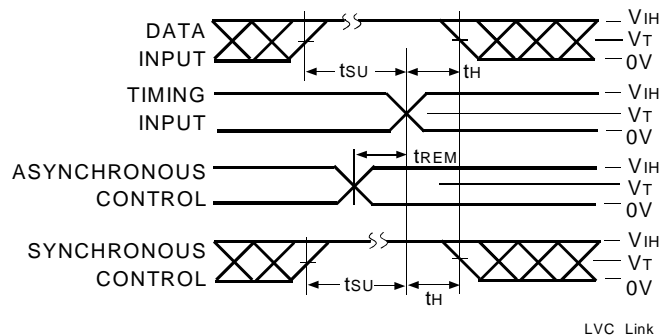
ENABLE AND DISABLE TIMES



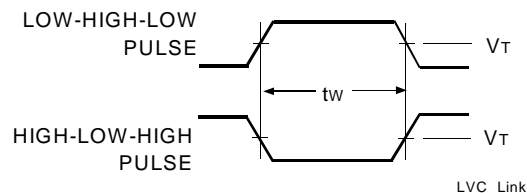
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

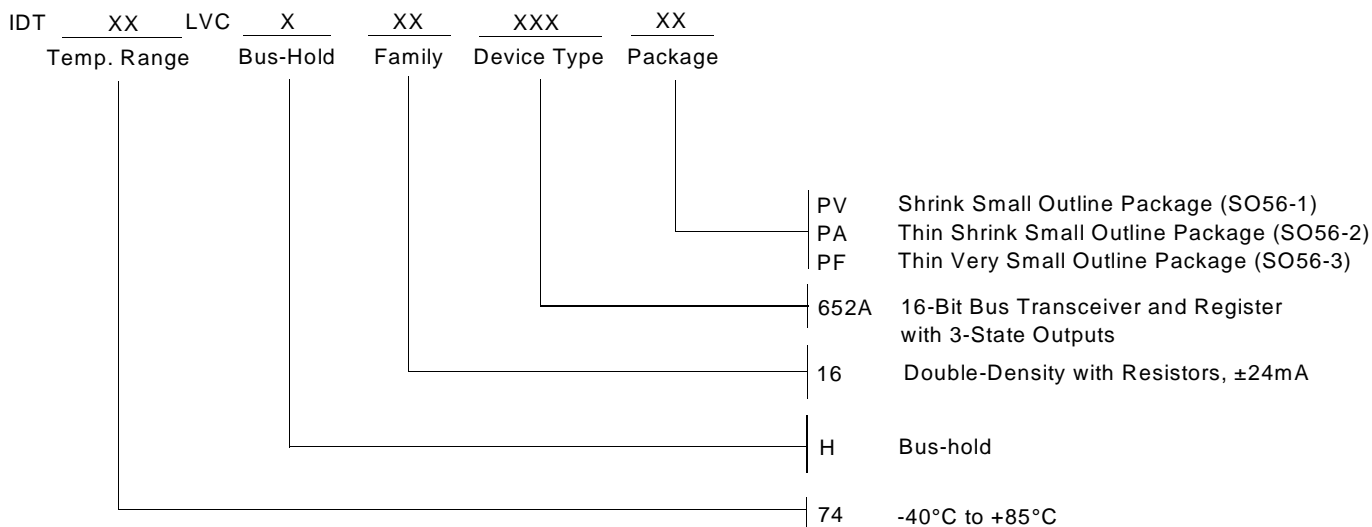
SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



ORDERING INFORMATION



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