Integrated Device Technology, Inc.

COMPACT PCI SMART I/O CARD

PRELIMINARY
IDT7M9532
IDT7M9533
IDT7M9534

FEATURES:

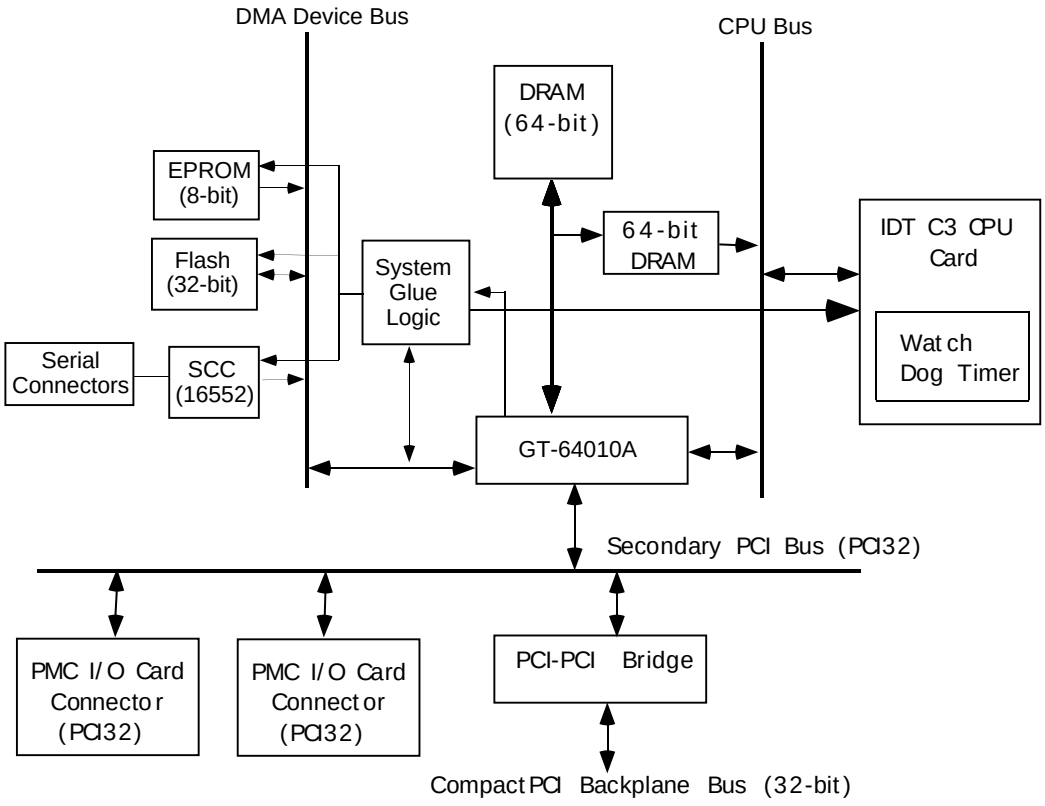
- High performance IDT Common-bus CPU Card (C3),
  - IDT MIPS processors RV4650, RV4700 or RV5000
  - Configurable with up to 1MB of L2 cache
- 6U size CompactPCI peripheral board
- Two PCI Mezzanine Card (PMC) slots on board to support a wide range of PCI based I/O devices
- Digital 21152 PCI to PCI Bridge
  - Separates Secondary (on board) PCI bus traffic from backplane PCI bus traffic
  - 32-bit backplane and secondary PCI buses
- Galileo GT64010A single chip PCI system controller
  - Up to 50MHz CPU bus frequency
- 8Mbyte on board DRAM
  - Fast Page/EDO DRAM
  - 64 bit DRAM data path (1M x 64)
- Two 72 Pin DRAM SODIMM sockets for DRAM expansion
  - Fast Page/EDO DRAM
  - 32 or 64 bit DRAM data path
  - 4Mbyte to 64Mbyte of additional DRAM
- Flash
  - 32 bit Width
  - 4Mbyte standard configurations
  - 8MByte available-consult factory
- Boot Prom
  - 8-bit Width
  - Up to 512KB
- Dual serial interface ports
  - 16550A compatible
  - 10 pin (2x5) headers
- Two General Purpose Registers
- On Board Reset Generation

DESCRIPTION:

The IDT7M9532/33/34 is a standard 6U CompactPCI Card which consists of an IDTC3 CPU Card based subsystem that can be used as an I/O processor in a CompactPCI based system.

It is designed to be plugged into any CPCI backplane peripheral slot that can accept a standard 6U size card. The card contains all of the features required of a typical CPU subsystem for embedded I/O processing applications.

FUNCTIONAL BLOCK DIAGRAM



4265 dwg 01

BOARD OVERVIEW

The IDT7M9532/33/34 consists of the following functional blocks: 21152 PCI to PCI Bridge, C3 processor, GT64010A PCI System Controller Chip, DRAM memory, system glue logic, Flash/EPROM and serial port controller. The IDT7M9532/33/34 CPU subsystem is designed to interface with its targeted system through a standard CompactPCI bus interface.

PCI TO PCI BRIDGE

The 21152 PCI to PCI Bridge is a high performance 32-bit to 32-bit PCI bridge that is compliant to PCI Revision 2.1. This chip isolates the primary (backplane) and on board secondary PCI busses. This isolation allows concurrent PCI traffic on the backplane and secondary PCI busses.

IDT C3 PROCESSOR CARD

The IDT C3 (Common-bus CPU Card) is a mezzanine based card that provides a common hardware interface for IDT's family of 64-bit MIPS processors (RV4650, RV4700 and RV5000). This card also has the following features:

- up to 1MB of optional L2 cache.
- 5V tolerant Inputs and I/Os.
- Watchdog Timer.

PCI SYSTEM CONTROLLER

The GT64010A from Galileo Technology, Inc. is designed to connect a high speed processor to peripheral devices. It is specifically designed to interface with the MIPS family of 64-bit processors. It connects the CPU to an asynchronous local device bus which is used to interface with the boot EPROM, Serial I/O, and Flash memory. It also has a built-in DRAM controller for interfacing the processor to the DRAM main memory. In addition, the chip provides a CPU bus to PCI bus bridge. The GT64010A can be configured as either a PCI bus master or a PCI bus slave device.

DRAM

The main memory consists of two elements: on board DRAM which is soldered down, and sockets for DRAM SODIMMs (expansion memory) which can be used to increase the total amount of memory available. The default memory configuration with the on board DRAM is 8MB which is organized as a single bank of 1Meg x 64. Parity is not supported by the on board DRAM.

The expansion memory consists of two standard 72 pin DRAM SODIMMs. The expansion memory can be configured to operate in either 32-bit mode or in 64-bit mode; however, if the expansion memory is configured in 32-bit mode, only one SODIMM socket is allowed to be populated. When the expansion memory is configured in to 64-bit mode, both SIMMs must be of the same type (e.g., 1Meg x 32).

The expansion memory is designed to support one or two additional banks of DRAM dependent on the type of SODIMM being used. One bank is supported when single bank DRAM SODIMMs are used (e.g., 1Meg x 32), and two banks are supported when double bank DRAM SODIMMs are used (e.g., 2Meg x 32). The design can use any standard DRAM SODIMM containing from 4MB (1Meg x 32) to 32MB (8Meg x 32), allowing a maximum DRAM capacity on the IDT7M9532/33/34 of 72 Mbytes.

BOOT EPROM

The Boot EPROM is a JEDEC standard 32 pin PLCC EPROM socket which can support up to 512KB (512k x 8).

SERIAL I/O

The IDT7M9532/33/34 has two 16550A compatible RS232 serial ports. The serial ports come out to two 10 pin headers (2x5).

The 10 pin headers have the following pinout/definition:

Header Pinout/Definition (Top View)			
DCD	1	2	DSR
RD	3	4	RTS
TD	5	6	CTS
DTR	7	8	RI
GND	9	10	NC

WATCHDOG RESET

The watchdog reset is generated from the watchdog timer included on the C3. It is used to generate a warm reset to the processor if it has not been strobed within 1 second.

SYSTEM GLUE LOGIC

The system glue logic supports the following functions:

- Processor General Purpose Registers (GPR0, GPR1)
- Device Decoding
- Interrupt Masking/Mapping
- Primary PCI bus Interrupt Generation

INTERRUPTS

The processor on the IDT7M9532/33/34 supports the following onboard interrupt sources:

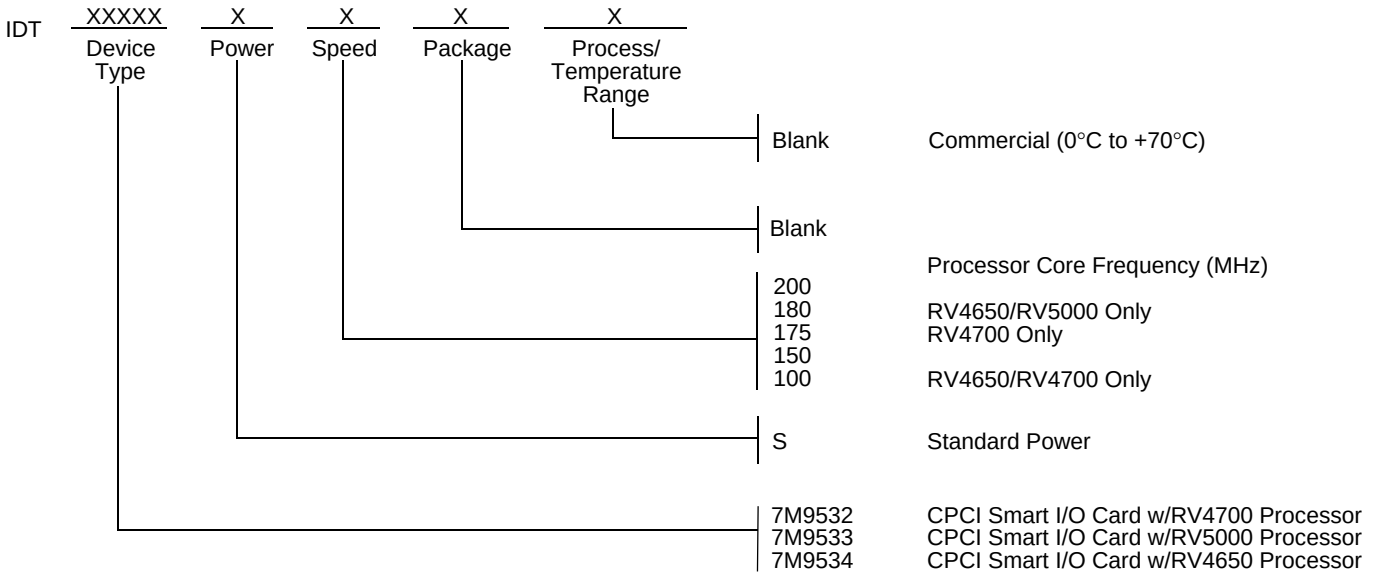
- GT64010A interrupt
- Serial I/O interrupts
- PMC Slot 1 interrupt
- PMC Slot 2 interrupt
- Processor internal timer interrupt

RESET

The IDT7M9532/33/34 supports several reset sources which include:

- Power on reset
- Manual Cold Reset (Front panel accessible)
- SW Warm Reset.
- Backplane CPCI Reset bus (Generates a Cold Reset to the card).
- Watchdog warm reset.

ORDERING INFORMATION



4265 dwg 02