



## HIGH-SPEED 2K x 8 FourPort™ STATIC RAM

IDT7052S/L

### Features

- ♦ High-speed access
  - Military: 25/35ns (max.)
  - Commercial: 20/25/35ns (max.)
- ♦ Low-power operation
  - IDT7052S  
Active: 750mW (typ.)  
Standby: 7.5mW (typ.)
  - IDT7052L  
Active: 750mW (typ.)  
Standby: 1.5mW (typ.)
- ♦ True FourPort memory cells which allow simultaneous access of the same memory locations
- ♦ Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- ♦ Versatile control for write-inhibit: separate  $\overline{\text{BUSY}}$  input to control write-inhibit for each of the four ports
- ♦ Battery backup operation—2V data retention

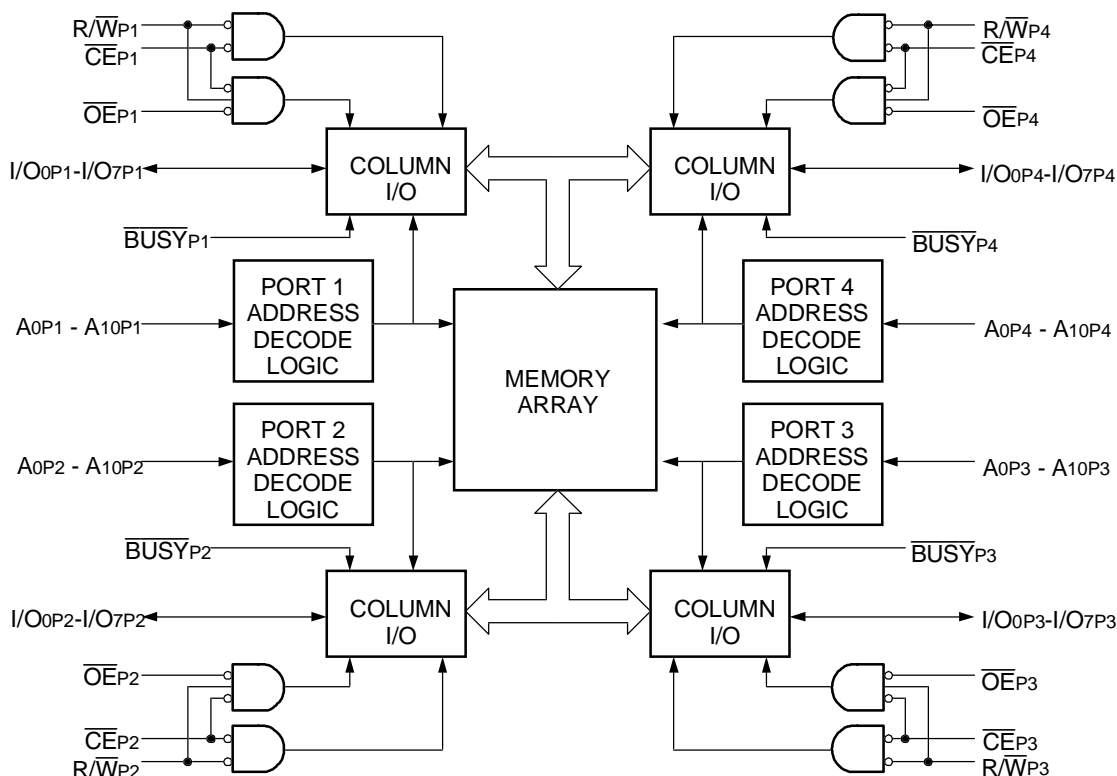
- ♦ TTL-compatible; single 5V ( $\pm 10\%$ ) power supply
- ♦ Available in 120 pin and 132 pin Thin Quad Flatpacks and 108 pin PGA
- ♦ Military product compliant to MIL-PRF-38535 QML
- ♦ Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available for selected speeds

### Description

The IDT7052 is a high-speed 2K x 8 FourPort™ Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7052 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those

### Functional Block Diagram



2674 drw 01

JUNE 1999

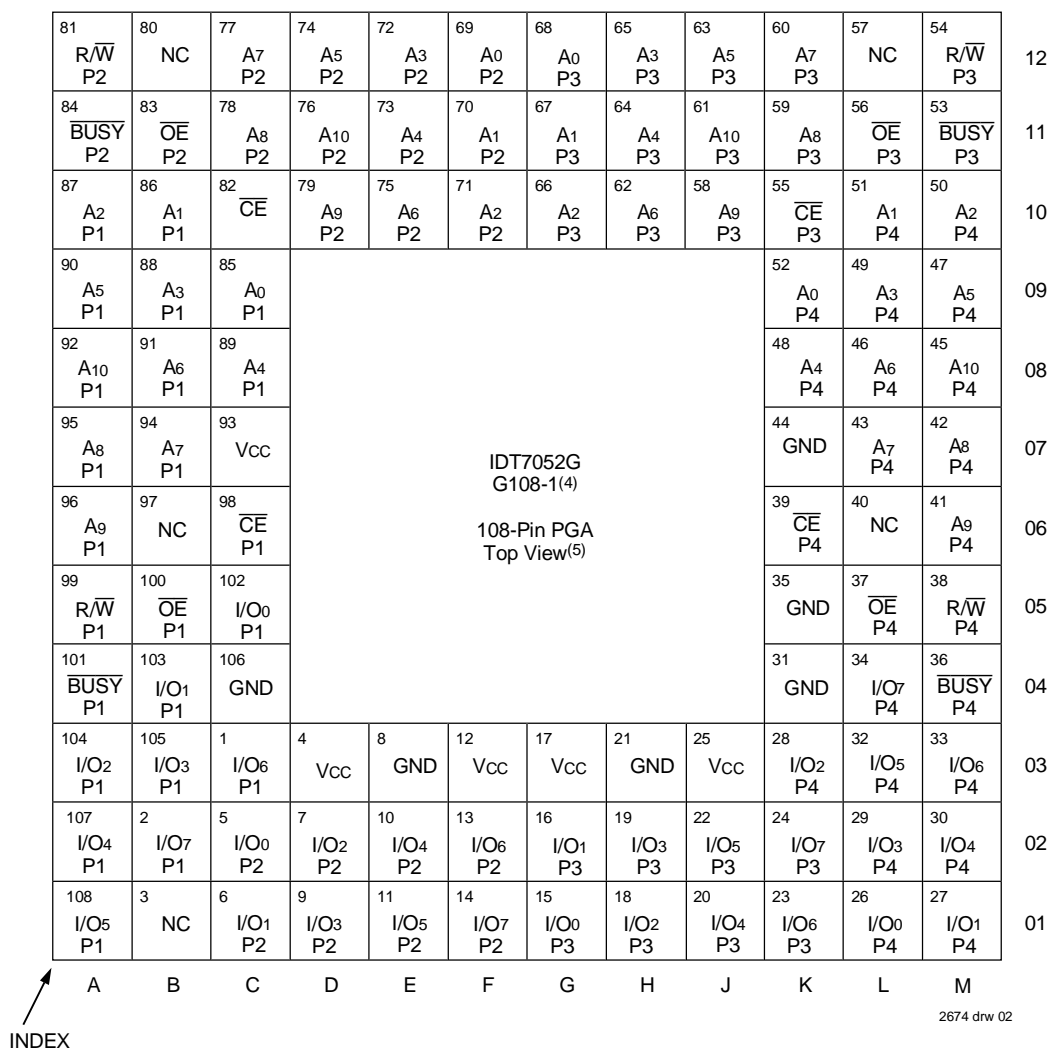
systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7052 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by  $\overline{CE}$ , permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CMOS high-performance technology, this FourPort SRAM typically operates on only 750mW of power. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50 $\mu$ W from a 2V battery.

The IDT7052 is packaged in a ceramic 108-pin Pin Grid Array (PGA), 120-pin Thin Quad Flatpack (TQFP) and 132-pin Plastic Quad Flatpack (PQF). Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

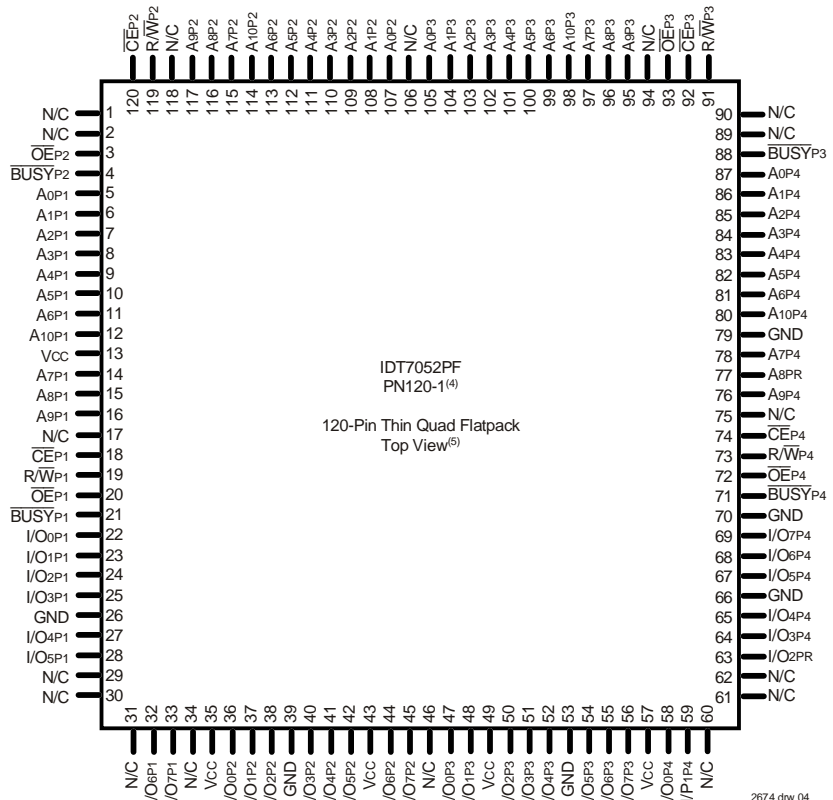
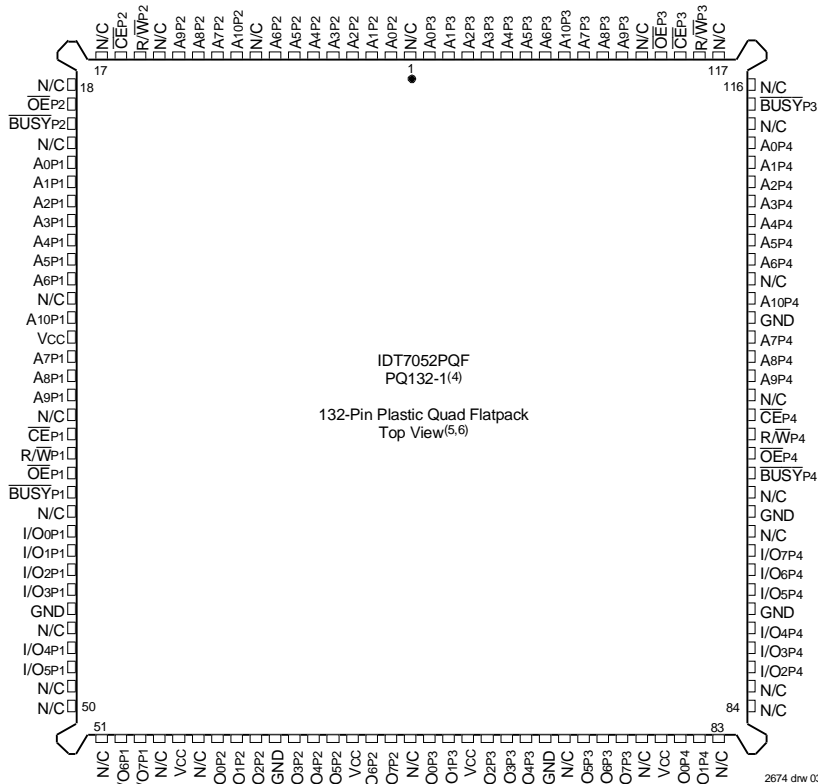
## Pin Configurations<sup>(1,2,3)</sup>



### NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 1.21 in x 1.21 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

## Pin Configurations<sup>(1,2,3)</sup> (con't.)



### NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. PQ132-1 package body is approximately .95 in x .95 in x .14 in.  
PN120-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking
6. The side of the package containing pin1 may have a bevelled edge in place of the indicator dot..

## Pin Configurations<sup>(1,2)</sup>

Symbol	Pin Name
A0 P1 - A10 P1	Address Line s - Port 1
A0 P2 - A10 P2	Address Line s - Port 2
A0 P3 - A10 P3	Address Line s - Port 3
A0 P4 - A10 P4	Address Line s - Port 4
I/O0 P1 - I/O7 P1	Data I/O - Port 1
I/O0 P2 - I/O7 P2	Data I/O - Port 2
I/O0 P3 - I/O7 P3	Data I/O - Port 3
I/O0 P4 - I/O7 P4	Data I/O - Port 4
R/W P1	Read/Write - Port 1
R/W P2	Read/Write - Port 2
R/W P3	Read/Write - Port 3
R/W P4	Read/Write - Port 4
GND	Ground
CE P1	Chip Enable - Port 1
CE P2	Chip Enable - Port 2
CE P3	Chip Enable - Port 3
CE P4	Chip Enable - Port 4
OE P1	Output Enable - Port 1
OE P2	Output Enable - Port 2
OE P3	Output Enable - Port 3
OE P4	Output Enable - Port 4
BUSY P1	Write Disable - Port 1
BUSY P2	Write Disable - Port 2
BUSY P3	Write Disable - Port 3
BUSY P4	Write Disable - Port 4
Vcc	Power

### NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply

2674 tbl 01

## Capacitance<sup>(1)</sup>

(TA = +25°C, f = 1.0MHz) TQFP only

Symbol	Parameter	Conditions <sup>(2)</sup>	Max	Unit
CIN	Input Capacitance	VIN = 0V	9	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

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### NOTES:

1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2674 tbl 02

### NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

## Maximum Operating Temperature and Supply Voltage<sup>(1,2)</sup>

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2674 tbl 04

### NOTES:

1. This is the parameter TA.
2. Industrial temperature: for specific speeds, packages and powers, contact your sales office

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 <sup>(2)</sup>	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

2674 tbl 05

### NOTES:

1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 10%.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1,5,6)</sup> (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Condition	Version	7052X20 Com'l Only		7052X25 Com'l & Military		7052X35 Com'l & Military		Unit
				Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	
I <sub>CC1</sub>	Operating Power Supply Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open $f = 0^{(3)}$	COM'L. S	150	300	150	300	150	300	mA
			L	150	250	150	250	150	250	
			MIL. & IND. S	—	—	150	360	150	360	
			L	—	—	150	300	150	300	
I <sub>CC2</sub>	Dynamic Operating Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open $f = f_{MAX}^{(4)}$	COM'L. S	240	370	225	350	210	335	mA
			L	210	325	195	305	180	290	
			MIL. & IND. S	—	—	225	400	210	395	
			L	—	—	195	340	180	330	
I <sub>SB</sub>	Standby Current (All Ports - TTL Level Inputs)	$\overline{CE} = V_{IH}$ $f = f_{MAX}^{(4)}$	COM'L. S	70	95	45	85	40	75	mA
			L	60	80	40	70	35	60	
			MIL. & IND. S	—	—	45	115	40	110	
			L	—	—	40	85	35	80	
I <sub>SB1</sub>	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(5)}$	COM'L. S	1.5	15	1.5	15	1.5	15	mA
			L	0.3	1.5	0.3	1.5	0.3	1.5	
			MIL. & IND. S	—	—	1.5	30	1.5	30	
			L	—	—	0.3	4.5	0.3	4.5	

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### NOTES:

- 'X' in part number indicates power rating (S or L).
- V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C and are not production tested.
- f = 0 means no address or control lines change.
- At f = f<sub>MAX</sub>, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- For the case of one port, divide the appropriate current above by four.
- Industrial temperature: for specific speeds, packages and powers contact your sales office.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7052S		7052L		Unit
			Min.	Max.	Min.	Max.	
I <sub>L</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 4mA	—	0.4	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA	2.4	—	2.4	—	V

### NOTE:

- At V<sub>CC</sub> ≤ 2.0V input leakages are undefined.

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## Data Retention Characteristics Over All Temperature Ranges<sup>(4)</sup>

(L Version Only)  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$

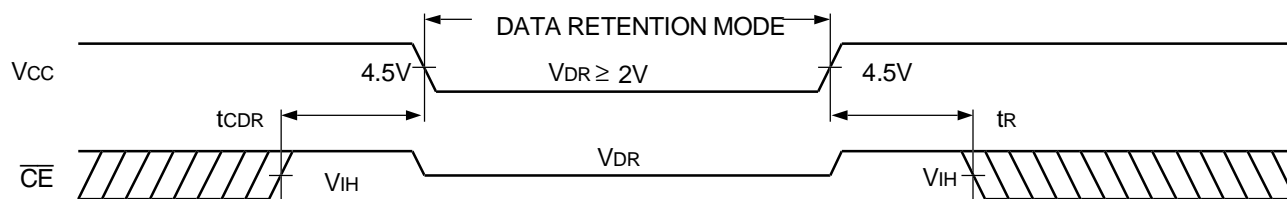
Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	$V_{CC} = 2V$	2.0	—	—	V
$I_{CCDR}$	Data Retention Current	$\overline{CE} \geq V_{HC}$	—	25	600	$\mu A$
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	—	25	1800	
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R^{(3)}$	Operation Recovery Time		$t_{RC}^{(2)}$	—	—	ns

2674 tbl 08a

### NOTES:

- $V_{CC} = 2V$ ,  $T_A = +25^\circ C$
- $t_{RC}$  = Read Cycle Time
- This parameter is guaranteed but not production tested.
- Industrial temperature: For other speeds, packages and powers contact your sales office.

## Low $V_{CC}$ Data Retention Waveform



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## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2674 tbl 08b

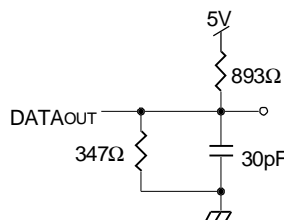


Figure 1. AC Output Test Load

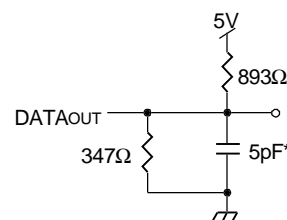


Figure 2. Output Test Load  
(for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{WZ}$ ,  $t_{OW}$ )  
\*Including scope and jig

2674 drw 06

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(3,4)</sup>

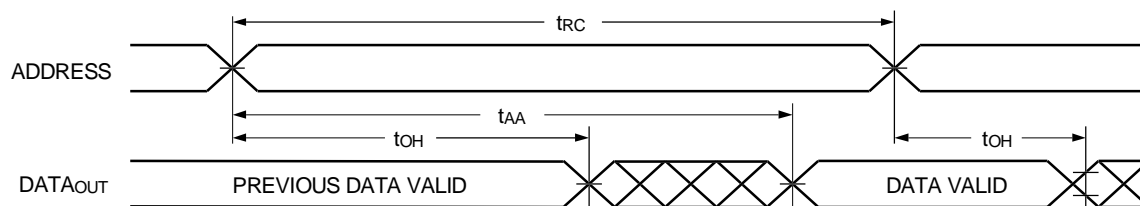
Symbol	Parameter	7052X20 Com'l Only		7052X25 Com'l & Military		7052X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	20	—	25	—	35	—	ns
tAA	Address Access Time	—	20	—	25	—	35	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	ns
tAOE	Output Enable Access Time	—	10	—	15	—	25	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	ns
tLZ	Output Low-Z Time <sup>(1,2)</sup>	5	—	5	—	5	—	ns
tHZ	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	—	15	ns
tPU	Chip Enable to Power Up Time <sup>(2)</sup>	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time <sup>(2)</sup>	—	20	—	25	—	35	ns

### NOTES:

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1. Transition is measured  $\pm 200\text{mV}$  from Low or High-Impedance voltage with the Output Test Load (Figure 2)
2. This parameter is guaranteed by device characterization but is not production tested.
3. 'X' in part number indicates power rating (S or L)
4. Industrial temperature: for specific speeds, packages and powers contact your sales office.

## Timing Waveform of Read Cycle No. 1, Any Port<sup>(1)</sup>

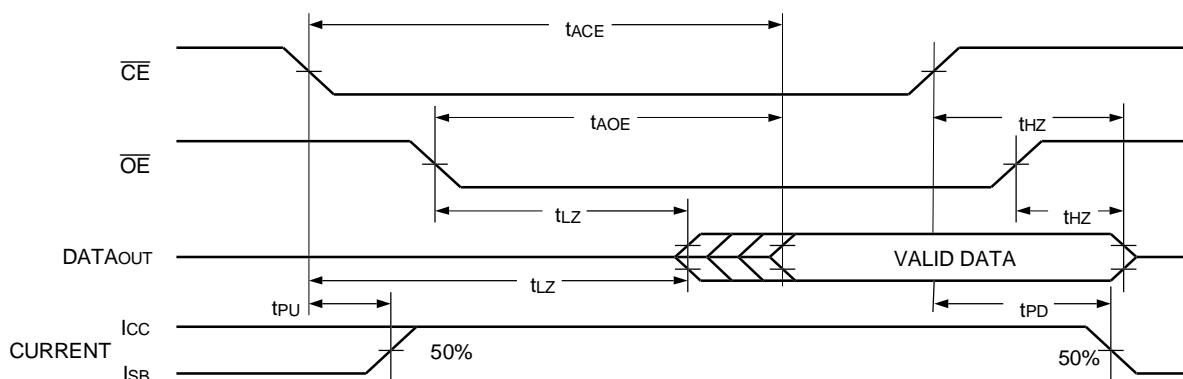


2674 drw 07

### NOTES:

1.  $R/\bar{W} = V_{IH}$ ,  $\bar{OE} = V_{IL}$  and  $\bar{CE} = V_{IL}$ .

## Timing Waveform of Read Cycle No. 2, Any Port<sup>(1,2)</sup>



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### NOTES:

1.  $R/\bar{W} = V_{IH}$  for Read Cycles.
2. Addresses valid prior to or coincident with  $\bar{CE}$  transition LOW.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(7,8)</sup>

Symbol	Parameter	7052X20 Com'l Only		7052X25 Com'l & Military		7052X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	20	—	25	—	35	—	ns
tEW	Chip Enable to End-of-Write <sup>(3)</sup>	15	—	20	—	30	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width <sup>(3)</sup>	15	—	20	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	20	—	ns
tHZ	Output High-Z Time <sup>(1,2)</sup>	—	15	—	15	—	15	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z <sup>(1,2)</sup>	—	12	—	15	—	15	ns
tOW	Output Active from End-of-Write <sup>(1,2)</sup>	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay <sup>(4)</sup>	—	35	—	45	—	55	ns
tWDD	Write Data Valid to Read Data Delay <sup>(4)</sup>	—	30	—	35	—	45	ns
BUSY INPUT TIMING								
tWB	Write to $\overline{\text{BUSY}}^{(6)}$	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{\text{BUSY}}^{(6)}$	15	—	15	—	20	—	ns

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### NOTES:

1. Transition is measured  $\pm 200\text{mV}$  from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. If  $\overline{\text{OE}} = \text{V}_{\text{IL}}$  during a R/W controlled write cycle, the write pulse width must be the larger of t<sub>WP</sub> or (t<sub>WZ</sub> + t<sub>DW</sub>) to allow the I/O drivers to turn off data to be placed on the bus for the required t<sub>DW</sub>. If  $\overline{\text{OE}} = \text{V}_{\text{IH}}$  during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t<sub>WP</sub>. Specified for  $\overline{\text{OE}} = \text{V}_{\text{IH}}$  (refer to "Timing Waveform of Write Cycle", Note 8).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. To ensure that the write cycle is inhibited on port "A" during contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
6. To ensure that a write cycle is completed on port "A" after contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
7. 'X' in part number indicates power rating.
8. Industrial temperature: for specific speeds, packages and powers contact your sales office.

The timing diagram illustrates the relationship between several control and data signals during memory access operations:

- ADDRESS**: The address bus signal.
- $\overline{OE}$** : Output Enable signal.
- $\overline{CE}^{(9)}$** : Chip Enable signal.
- R/ $\overline{W}$** : Read/Write control signal.
- DATA<sub>out</sub>**: Data output bus.
- DATA<sub>in</sub>**: Data input bus.

Key timing parameters shown include:

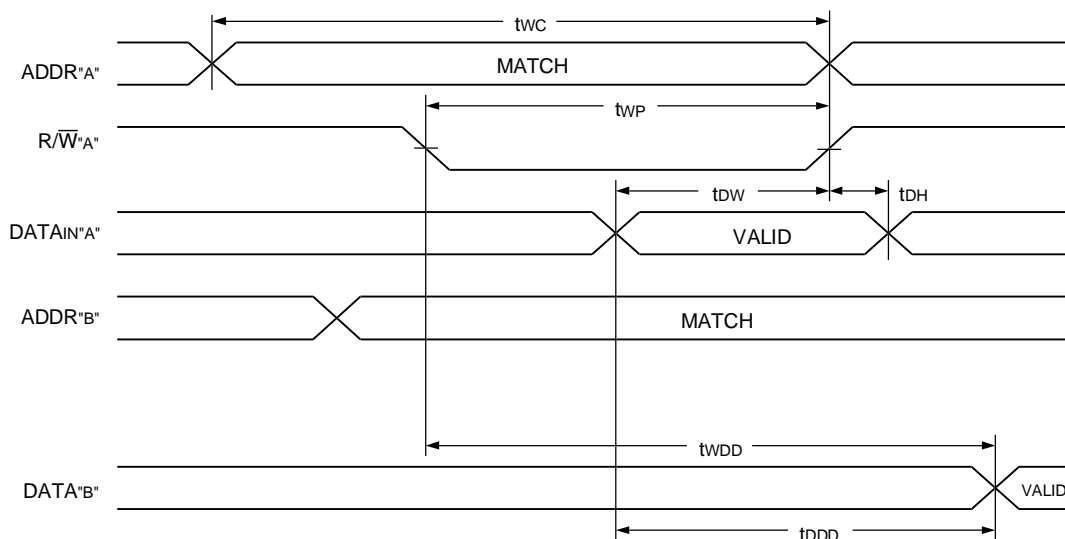
- $t_{WC}$ : Write Cycle time.
- $t_{AS}^{(6)}$ : Address Setup time before  $\overline{OE}$ .
- $t_{AW}$ : Address Valid time after  $\overline{OE}$ .
- $t_{WR}^{(3)}$ : Write Recovery time after  $\overline{OE}$ .
- $t_{WP}^{(2)}$ : Write Pulse width.
- $t_{WZ}^{(7)}$ : Write Zero time from R/ $\overline{W}$  transition.
- $t_{OW}$ : Output Valid time after  $\overline{OE}$ .
- $t_{LZ}$ : Output Latency time from  $\overline{OE}$  to DATA<sub>out</sub>.
- $t_{DZ}^{(7)}$ : Data Zero time from R/ $\overline{W}$  transition.
- $t_{DR}^{(8)}$ : Data Recovery time after R/ $\overline{W}$  transition.
- $t_{DW}$ : Data Write time.
- $t_{DH}$ : Data Hold time.
- $t_{HZ}^{(7)}$ : High-Z time from R/ $\overline{W}$  transition.
- $t_R$ : Read time from  $\overline{OE}$  to DATA<sub>out</sub>.

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2674 drw 10

1.  $R/\overline{W}$  or  $\overline{CE} = V_{IH}$  during all address transitions.
2. A write occurs during the overlap ( $t_{EW}$  or  $t_{WP}$ ) of a  $\overline{CE} = V_{IL}$  and a  $R/\overline{W} = V_{IL}$ .
3.  $t_{wR}$  is measured from the earlier of  $\overline{CE}$  or  $R/\overline{W} = V_{IH}$  to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE} = V_{IL}$  transition occurs simultaneously with or after the  $R/\overline{W} = V_{IL}$  transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last,  $\overline{CE}$  or  $R/\overline{W}$ .
7. Transition is measured  $\pm 20\text{mV}$  from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed but is not production tested.
8. If  $\overline{OE} = V_{IL}$  during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or ( $t_{wZ} + t_{wR}$ ) to allow the I/O drivers to turn off data to be placed on the bus for the required  $t_{wR}$ . If  $\overline{OE} = V_{IH}$  during an  $R/\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

## Timing Waveform of Write with Port-to-Port Read<sup>(1,2,3)</sup>

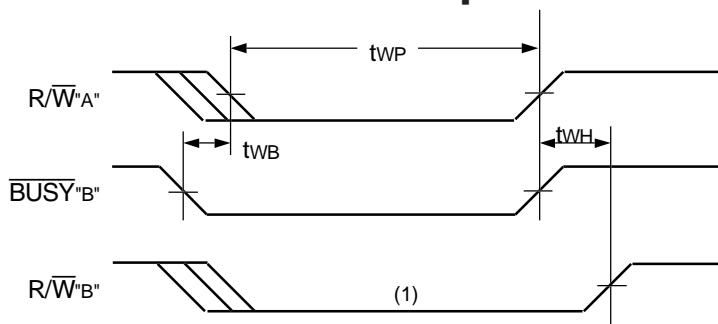


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### NOTES:

1. Assume  $\overline{\text{BUSY}}$  input =  $V_{IH}$  and  $\overline{\text{CE}} = V_{IL}$  for the writing port.
2.  $\overline{\text{OE}} = V_{IL}$  for the reading ports.
3. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

## Timing Waveform of Write with $\overline{\text{BUSY}}$ Input



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### NOTES:

1.  $\overline{\text{BUSY}}$  is asserted on Port "B" blocking  $\text{R}/\overline{\text{W}}^{\text{B}}$  until  $\overline{\text{BUSY}}^{\text{B}}$  goes HIGH.

## Functional Description

The IDT7052 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by  $\overline{\text{CE}}$ . The  $\overline{\text{CE}}$  controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ( $\overline{\text{CE}} = V_{IH}$ ). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ( $\overline{\text{OE}}$ ). In the read mode, the port's  $\overline{\text{OE}}$  turns on the output drivers when set LOW. READ/ WRITE conditions are illustrated in the table below.

## Truth Table I – Read/Write Control<sup>(3)</sup>

Any Port <sup>(1)</sup>				Function
R/W	$\overline{\text{CE}}$	$\overline{\text{OE}}$	D0-7	
X	H	X	Z	Port Deselected: Power-Down
X	H	X	Z	$\overline{\text{CE}}\text{P1}=\overline{\text{CE}}\text{P2}=\overline{\text{CE}}\text{P3}=\overline{\text{CE}}\text{P4}=V_{IH}$ Power Down Mode ISB or ISB1
L	L	X	DATAin	Data on port written into memory <sup>(2)</sup>
H	L	L	DATAout	Data in memory output on port
X	X	H	Z	Outputs Disabled

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### NOTES:

1. "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care, "Z" = High Impedance
2. If  $\overline{\text{BUSY}} = V_{IL}$ , write is blocked.
3. For valid write operation, no more than one port can write to the same address location at the same time.

## Ordering Information

IDT	XXXX	A	999	A	A	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank (1)	Commercial (0°C to +70°C)
					B	Industrial (-40°C to +85°C)
						Military (-55°C to +125°C)
						Compliant to MIL-PRF-38535 QML
					G	108-Pin Pin Grid Array (G108-1)
					PQF	132-Pin Plastic Quad Flatpack (PQ132-1)
					PF	120-Pin Thin Quad Plastic Flatpack (PN120-1)
					20	Commercial Only
					25	Commercial & Military
					35	Commercial & Military
						Speed in nanoseconds
					L	Low Power
					S	Standard Power
					7052	16K (2K x 8) FourPort RAM

2674 drw 13

### NOTE:

1. Industrial temperature range is available.  
For specific speeds, packages and powers contact your sales office.

## Datasheet Document History

1/18/99:	Initiated datasheet document history Converted to new format Cosmetic typographical corrections
6/4/99:	Added additional notes to pin configurations Changed drawing format Page1 Corrected DSC number



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