



# 32K x 32 3.3V Synchronous SRAM Flow-Through Outputs

**IDT71V433**

## Features

- ◆ 32K x 32 memory configuration
- ◆ Supports high performance system speed:  
*Commercial and Industrial:*
  - 11 11ns Clock-to-Data Access (50MHz)
  - 12 12ns Clock-to-Data Access (50MHz)
- ◆  $\overline{\text{LBO}}$  input selects interleaved or linear burst mode
- ◆ Self-timed write cycle with global write control ( $\overline{\text{GW}}$ ), byte write enable ( $\overline{\text{BWE}}$ ), and byte writes ( $\overline{\text{BWx}}$ )
- ◆ Power down controlled by ZZ input
- ◆ Single 3.3V power supply (+10/-5%)
- ◆ Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP).

## Description

The IDT71V433 is a 3.3V high-speed 1,048,576-bit SRAM organized as 32K x 32 with full support of various processor interfaces including the Pentium™ and PowerPC™. The flow-through burst architecture provides cost-effective 2-1-1-1 performance for processors up to 50 MHz.

The IDT71V433 SRAM contains write, data-input, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V433 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected ( $\overline{\text{ADV}}=\text{LOW}$ ), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the  $\overline{\text{LBO}}$  input pin.

The IDT71V433 SRAM utilizes IDT's high-performance 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP).

## Pin Description

A <sub>0</sub> -A <sub>14</sub>	Address Inputs	Input	Synchronous
$\overline{\text{CE}}$	Chip Enable	Input	Synchronous
CS <sub>0</sub> , CS <sub>1</sub>	Chips Selects	Input	Synchronous
$\overline{\text{OE}}$	Output Enable	Input	Asynchronous
$\overline{\text{GW}}$	Global Write Enable	Input	Synchronous
$\overline{\text{BWE}}$	Byte Write Enable	Input	Synchronous
$\overline{\text{BW}}_1\text{-}\overline{\text{BW}}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock Input	Input	N/A
$\overline{\text{ADV}}$	Burst Address Advance	Input	Synchronous
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{\text{ADSP}}$	Address Status (Processor)	Input	Synchronous
$\overline{\text{LBO}}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O <sub>0</sub> -I/O <sub>31</sub>	Data Input/Output	I/O	Synchronous
V <sub>DD</sub> , V <sub>DDQ</sub>	Core and I/O Power Supply (3.3V)	Power	N/A
V <sub>SS</sub> , V <sub>SSQ</sub>	Array Ground, I/O Ground	Power	N/A

3729 tbl 01

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PowerPC is a trademark of International Business Machines, Inc.

**AUGUST 2001**

## Pin Definitions<sup>(1)</sup>

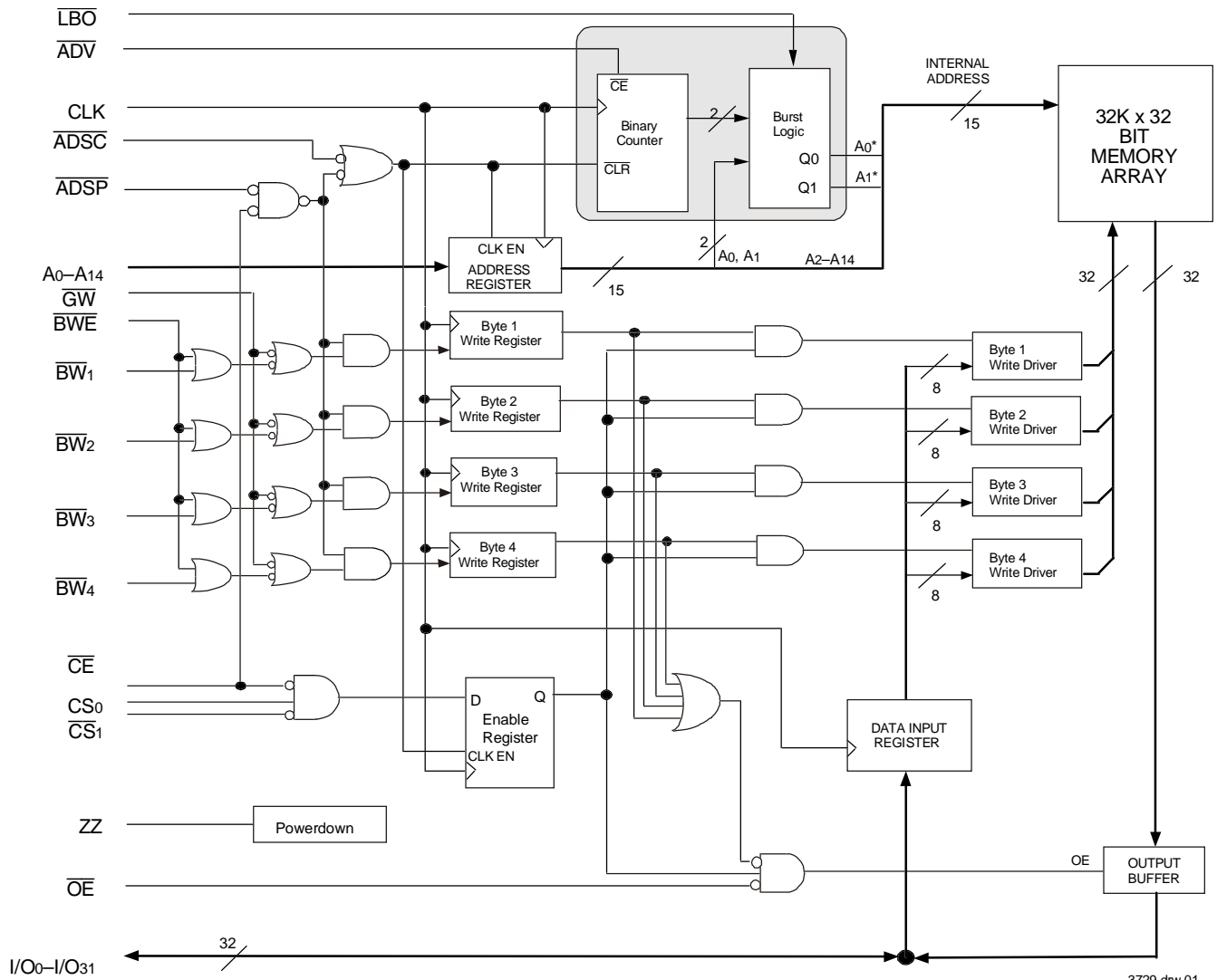
Symbol	Pin Function	I/O	Active	Description
A <sub>0</sub> –A <sub>14</sub>	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{\text{ADSC}}$ Low or $\overline{\text{ADSP}}$ Low and $\overline{\text{CE}}$ Low.
$\overline{\text{ADSC}}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{\text{ADSC}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSC}}$ is NOT gated by $\overline{\text{CE}}$ .
$\overline{\text{ADSP}}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{\text{ADSP}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSP}}$ is gated by $\overline{\text{CE}}$ .
$\overline{\text{ADV}}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{\text{ADV}}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When this input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{\text{BWE}}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{\text{BW}}_1$ – $\overline{\text{BW}}_4$ . If $\overline{\text{BWE}}$ is LOW at the rising edge of CLK then $\overline{\text{BW}}_x$ inputs are passed to the next stage in the circuit. A byte write can still be blocked if $\overline{\text{ADSP}}$ is LOW at the rising edge of CLK. If $\overline{\text{ADSP}}$ is HIGH and $\overline{\text{BW}}_x$ is LOW at the rising edge of CLK then data will be written to the SRAM. If $\overline{\text{BWE}}$ is HIGH then the byte write inputs are blocked and only $\overline{\text{GW}}$ can initiate a write cycle.
$\overline{\text{BW}}_1$ – $\overline{\text{BW}}_4$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{\text{BW}}_1$ controls I/O(7:0), $\overline{\text{BW}}_2$ controls I/O(15:8), etc. Any active byte write causes all outputs to be disabled. $\overline{\text{ADSP}}$ LOW disables all byte writes. $\overline{\text{BW}}_1$ – $\overline{\text{BW}}_4$ must meet specified setup and hold times with respect to CLK.
$\overline{\text{CE}}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{\text{CE}}$ is used with $\text{CS}_0$ and $\overline{\text{CS}}_1$ to enable the IDT71V433. $\overline{\text{CE}}$ also gates $\overline{\text{ADSP}}$ .
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
$\text{CS}_0$	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. $\text{CS}_0$ is used with $\overline{\text{CE}}$ and $\overline{\text{CS}}_1$ to enable the chip.
$\overline{\text{CS}}_1$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{\text{CS}}_1$ is used with $\overline{\text{CE}}$ and $\text{CS}_0$ to enable the chip.
$\overline{\text{GW}}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 8-bit data bytes when LOW on the rising edge of CLK. $\overline{\text{GW}}$ supercedes individual byte write enables.
I/O <sub>0</sub> –I/O <sub>31</sub>	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Only the data input path is registered and triggered by the rising edge of CLK. Outputs are Flow-Through.
$\overline{\text{LBO}}$	Linear Burst	I	LOW	When $\overline{\text{LBO}}$ is HIGH the Interleaved Order (Intel) burst sequence is selected. When $\overline{\text{LBO}}$ is LOW the Linear (PowerPC) burst sequence is selected. $\overline{\text{LBO}}$ has an internal pull-up resistor.
$\overline{\text{OE}}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{\text{OE}}$ is HIGH the I/O pins are in a high-impedance state. When $\overline{\text{OE}}$ is LOW the data output drivers are enabled if the chip is also selected.
V <sub>DD</sub>	Power Supply	N/A	N/A	3.3V core power supply inputs.
V <sub>DDQ</sub>	Power Supply	N/A	N/A	3.3V I/O power supply inputs.
V <sub>SS</sub>	Ground	N/A	N/A	Core ground pins.
V <sub>SSQ</sub>	Ground	N/A	N/A	I/O ground pins.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the chip.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V433 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. ZZ has an internal pull-down resistor.

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### NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

### Functional Block Diagram



3729 drw 01

**Absolute Maximum DC Ratings<sup>(1)</sup>**

Symbol	Rating	Value	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> +0.5	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
P <sub>T</sub>	Power Dissipation	1.2	W
I <sub>OUT</sub>	DC Output Current	50	mA

3729 tbl 05

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>DD</sub>, V<sub>DDQ</sub> and input terminals only.
- I/O terminals.

**Capacitance**(T<sub>A</sub> = +25°C, f = 1.0MHz, TQFP package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	4	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	8	pF

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**NOTE:**

- This parameter is guaranteed by device characterization, but not production tested.

**Recommended Operating Temperature and Supply Voltage**

Grade	Temperature	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	0V	3.3V+10/-5%	3.3V+10/-5%
Industrial	-40°C to +85°C	0V	3.3V+10/-5%	3.3V+10/-5%

3729 tbl 03

**Recommended DC Operating Conditions**

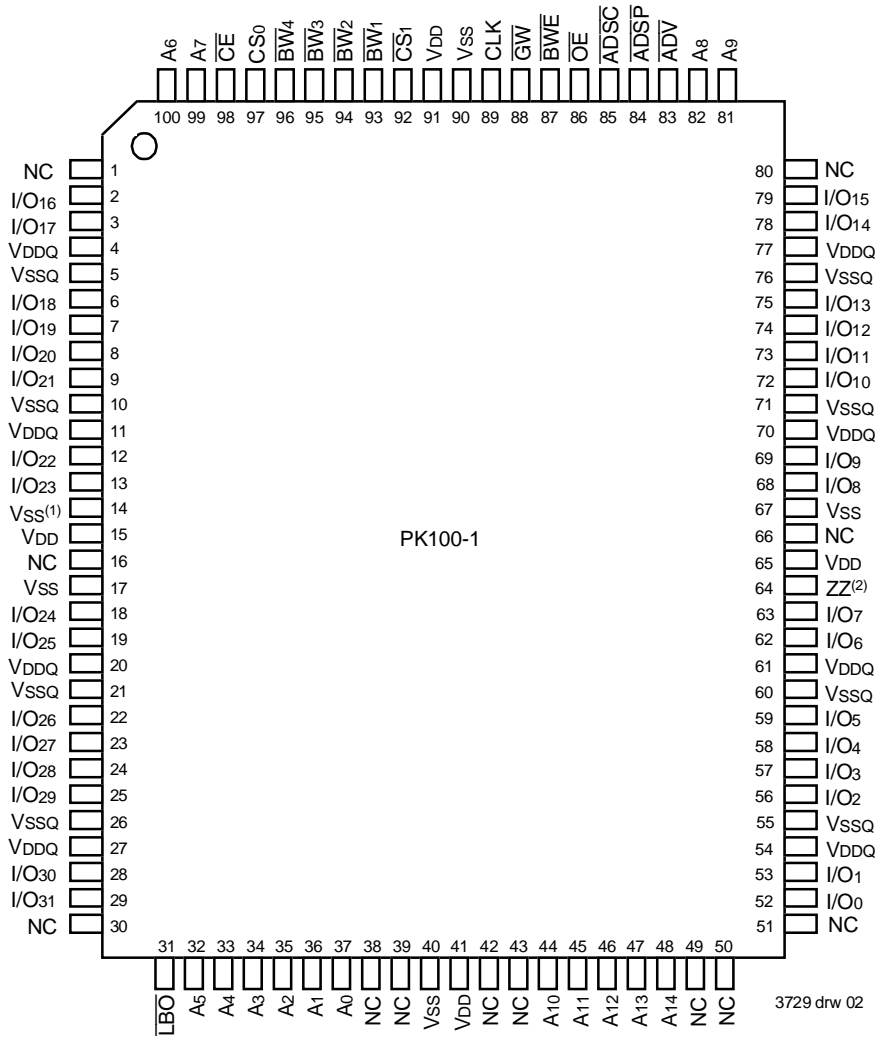
Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.135	3.3	3.63	V
V <sub>DDQ</sub>	I/O Supply Voltage	3.135	3.3	3.63	V
V <sub>SS</sub> , V <sub>SSQ</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.0 <sup>(1)</sup>	—	V <sub>DDQ</sub> +0.3 <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(3)</sup>	—	0.8	V

3729 tbl 04

**NOTES:**

- V<sub>IH</sub> and V<sub>IL</sub> as indicated is for both input and I/O pins.
- V<sub>IH</sub> (max) = 6.0V for pulse width less than tcyc/2, once per cycle.
- V<sub>IL</sub> (min) = -1.0V for pulse width less than tcyc/2, once per cycle.

## Pin Configuration



### Top View TQFP

**NOTES**

1. Pin 14 does not have to be directly connected to Vss as long as the input voltage is  $\leq V_{IL}$ .
2. Pin 64 can be left unconnected and the device will always remain in active mode.

**Synchronous Truth Table<sup>(1,2)</sup>**

Operation	Address Used	$\overline{CE}$	$CS_0$	$\overline{CS}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_x$	$\overline{OE}^{(3)}$	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	Hi-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	Hi-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	Hi-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	DIN
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	DIN
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	Hi-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	DIN
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	DIN
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	↑	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	↑	Hi-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	DIN
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	↑	DIN

3729 bl 07

**NOTES:**

1. L =  $V_{IL}$ , H =  $V_{IH}$ , X = Don't Care.
2. ZZ = LOW for this table.
3.  $\overline{OE}$  is an asynchronous input.

**Synchronous Write Function Truth Table<sup>(1)</sup>**

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	$\overline{BW}_4$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1 <sup>(2)</sup>	H	L	L	H	H	H
Write Byte 2 <sup>(2)</sup>	H	L	H	L	H	H
Write Byte 3 <sup>(2)</sup>	H	L	H	H	L	H
Write Byte 4 <sup>(2)</sup>	H	L	H	H	H	L

3729 tbl 08

**NOTES:**

1. L =  $V_{IL}$ , H =  $V_{IH}$ , X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

**Asynchronous Truth Table<sup>(1)</sup>**

Operation	$\overline{OE}$	$\overline{ZZ}$	I/O Status	Power
Read	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>31</sub> )	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z — Data In (I/O <sub>0</sub> –I/O <sub>31</sub> )	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

3729 tbl 09

**NOTES:**

1. L =  $V_{IL}$ , H =  $V_{IH}$ , X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

**Interleaved Burst Sequence Table ( $\overline{LBO}=V_{DD}$ )**

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	1	0	0	1	0	0

3729 tbl 10

**NOTE:**

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

**Linear Burst Sequence Table ( $\overline{LBO}=V_{SS}$ )**

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	0	0	0	1	1	0

3729 tbl 11

**NOTE:**

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V +10/-5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DD</sub>	---	5	μA
I <sub>LI</sub>	ZZ & $\overline{\text{LBO}}$ Input Leakage Current <sup>(1)</sup>	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DD</sub>	---	30	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{\text{CE}} \geq V_{IH}$ or $\overline{\text{OE}} \geq V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>DD</sub> , V <sub>DD</sub> = Max.	---	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 5mA, V <sub>DD</sub> = Min.	---	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -5mA, V <sub>DD</sub> = Min.	2.4	---	V

NOTE:

1. The  $\overline{\text{LBO}}$  pin will be internally pulled to V<sub>DD</sub> if it is not actively driven in the application and the ZZ pin will be internally pulled to V<sub>SS</sub> if not actively driven.

3729 tbl 12

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1)</sup> (V<sub>HD</sub> = V<sub>DDQ</sub>-0.2V, V<sub>LD</sub> = 0.2V)

Symbol	Parameter	Test Conditions	IDT71V433S11		IDT71V433S12		Unit
			Com'l.	Ind.	Com'l.	Ind.	
I <sub>DD</sub>	Operating Core Power Supply Current	Device Selected, Outputs Open, V <sub>DD</sub> = Max., V <sub>DDQ</sub> = Max., V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	220	220	210	210	mA
I <sub>SB</sub>	Standby Core Power Supply Current	Device Deselected, Outputs Open, V <sub>DD</sub> = Max., V <sub>DDQ</sub> = Max., V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	45	45	40	40	mA
I <sub>SB1</sub>	Full Standby Core Power Supply Current	Device Deselected, Outputs Open, V <sub>DD</sub> = Max., V <sub>DDQ</sub> = Max., V <sub>IN</sub> ≥ V <sub>HD</sub> or ≤ V <sub>LD</sub> , f = 0 <sup>(2)</sup>	15	15	15	15	mA
I <sub>ZZ</sub>	Full Sleep Mode Core Power Supply Current	ZZ ≥ V <sub>HD</sub> , V <sub>DD</sub> = Max.	15	15	15	15	mA

NOTES:

- All values are maximum guaranteed values.
- At f = f<sub>MAX</sub>, inputs are cycling at the maximum frequency of read cycles of 1/t<sub>cyC</sub> while  $\overline{\text{ADSC}} = \text{LOW}$ ; f=0 means no input lines are changing.

3729 tbl 13

### AC Test Loads

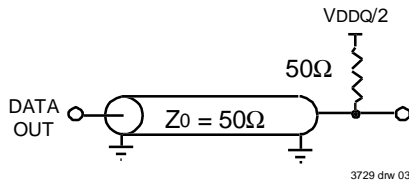
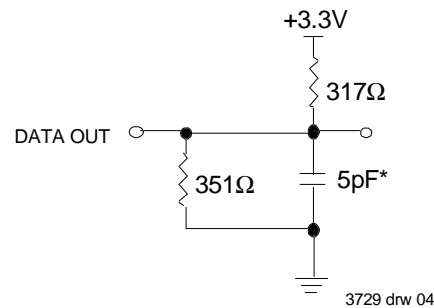


Figure 1. AC Test Load



\* Including scope and jig capacitance.

Figure 2. High-Impedance Test Load (for t<sub>OHZ</sub>, t<sub>CHZ</sub>, t<sub>OLZ</sub>, and t<sub>bc1</sub>)

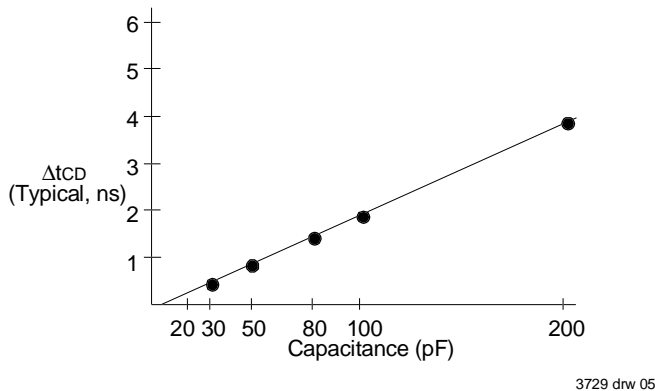


Figure 3. Lumped Capacitive Load, Typical Derating

### AC Test Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3729 tbl 14



**AC Electrical Characteristics****(VDD = 3.3V +10/-5%, Commercial and Industrial Temperature Ranges)**

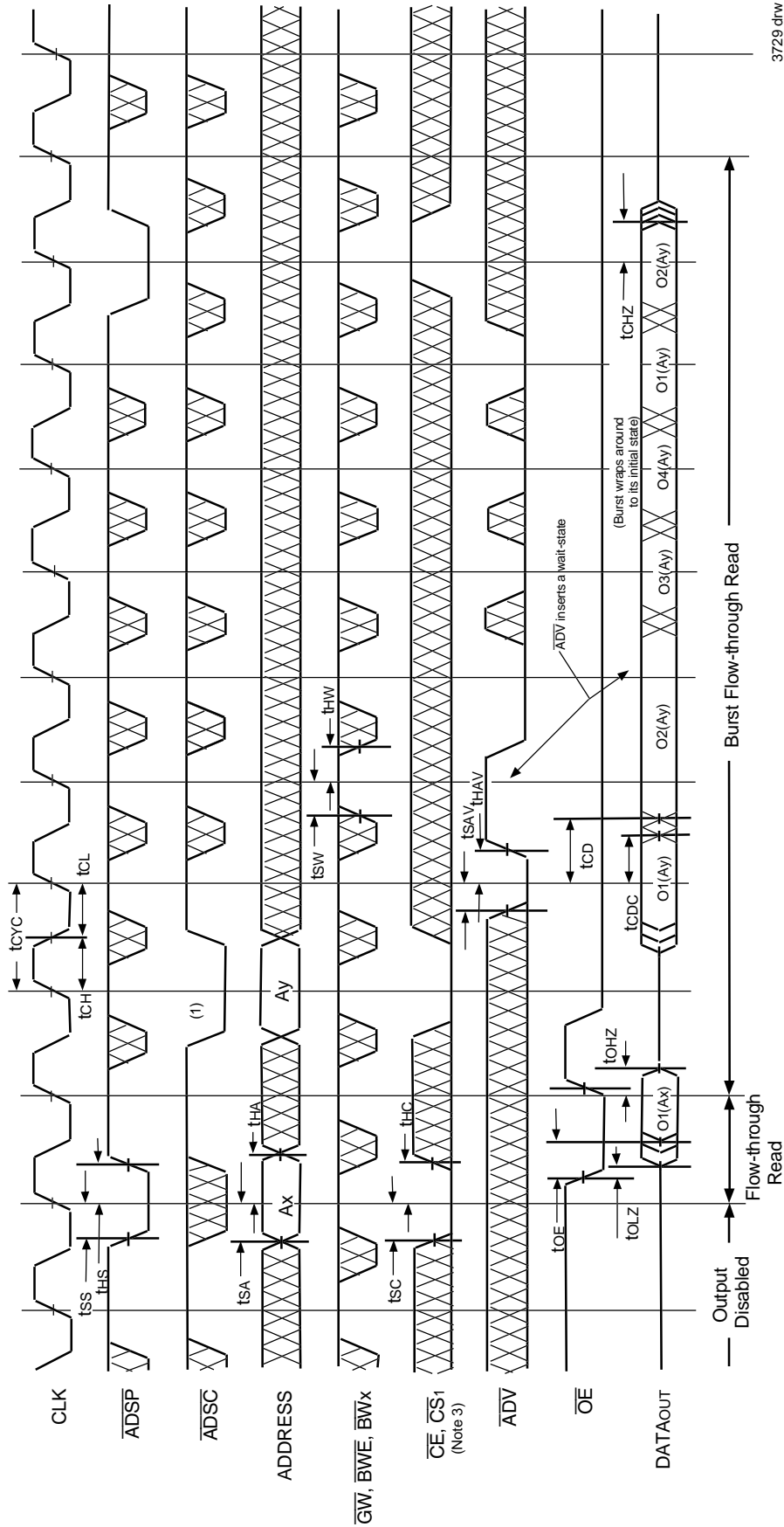
Symbol	Parameter	71V433S11		71V433S12		Unit
		Min.	Max.	Min.	Max.	
<b>Clock Parameters</b>						
t <sub>CYC</sub>	Clock Cycle Time	20	—	20	—	ns
t <sub>CH</sub> <sup>(1)</sup>	Clock High Pulse Width	6	—	6	—	ns
t <sub>CL</sub> <sup>(1)</sup>	Clock Low Pulse Width	6	—	6	—	ns
<b>Output Parameters</b>						
t <sub>CD</sub>	Clock High to Valid Data	—	11	—	12	ns
t <sub>CDC</sub>	Clock High to Data Change	3	—	3	—	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Clock High to Output Active	0	—	0	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Clock High to Data High-Z	3	6	3	6	ns
t <sub>OE</sub>	Output Enable Access Time	—	4	—	4	ns
t <sub>OLZ</sub> <sup>(2)</sup>	Output Enable Low to Data Active	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(2)</sup>	Output Enable High to Data High-Z	—	6	—	6	ns
<b>Setup Times</b>						
t <sub>SA</sub>	Address Setup Time	2.5	—	2.5	—	ns
t <sub>SS</sub>	Address Status Setup Time	2.5	—	2.5	—	ns
t <sub>SD</sub>	Data in Setup Time	2.5	—	2.5	—	ns
t <sub>SW</sub>	Write Setup Time	2.5	—	2.5	—	ns
t <sub>SAV</sub>	Address Advance Setup Time	2.5	—	2.5	—	ns
t <sub>SC</sub>	Chip Enable/Select Setup Time	2.5	—	2.5	—	ns
<b>Hold Times</b>						
t <sub>HA</sub>	Address Hold Time	0.5	—	0.5	—	ns
t <sub>HS</sub>	Address Status Hold Time	0.5	—	0.5	—	ns
t <sub>HD</sub>	Data In Hold Time	0.5	—	0.5	—	ns
t <sub>HW</sub>	Write Hold Time	0.5	—	0.5	—	ns
t <sub>HAV</sub>	Address Advance Hold Time	0.5	—	0.5	—	ns
t <sub>HC</sub>	Chip Enable/Select Hold Time	0.5	—	0.5	—	ns
<b>Sleep Mode and Configuration Parameters</b>						
t <sub>ZZPW</sub>	ZZ Pulse Width	100	—	100	—	ns
t <sub>ZZR</sub> <sup>(3)</sup>	ZZ Recovery Time	100	—	100	—	ns
t <sub>CFG</sub> <sup>(4)</sup>	Configuration Set-up Time	80	—	80	—	ns

3729 tbl 15

**NOTES:**

1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured  $\pm 200$ mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t<sub>CFG</sub> is the minimum time required to configure the device based on the  $\overline{\text{LBO}}$  input.  $\overline{\text{LBO}}$  is a static input and must not change during normal operation.

### Timing Waveform of Read Cycle<sup>(1,2)</sup>

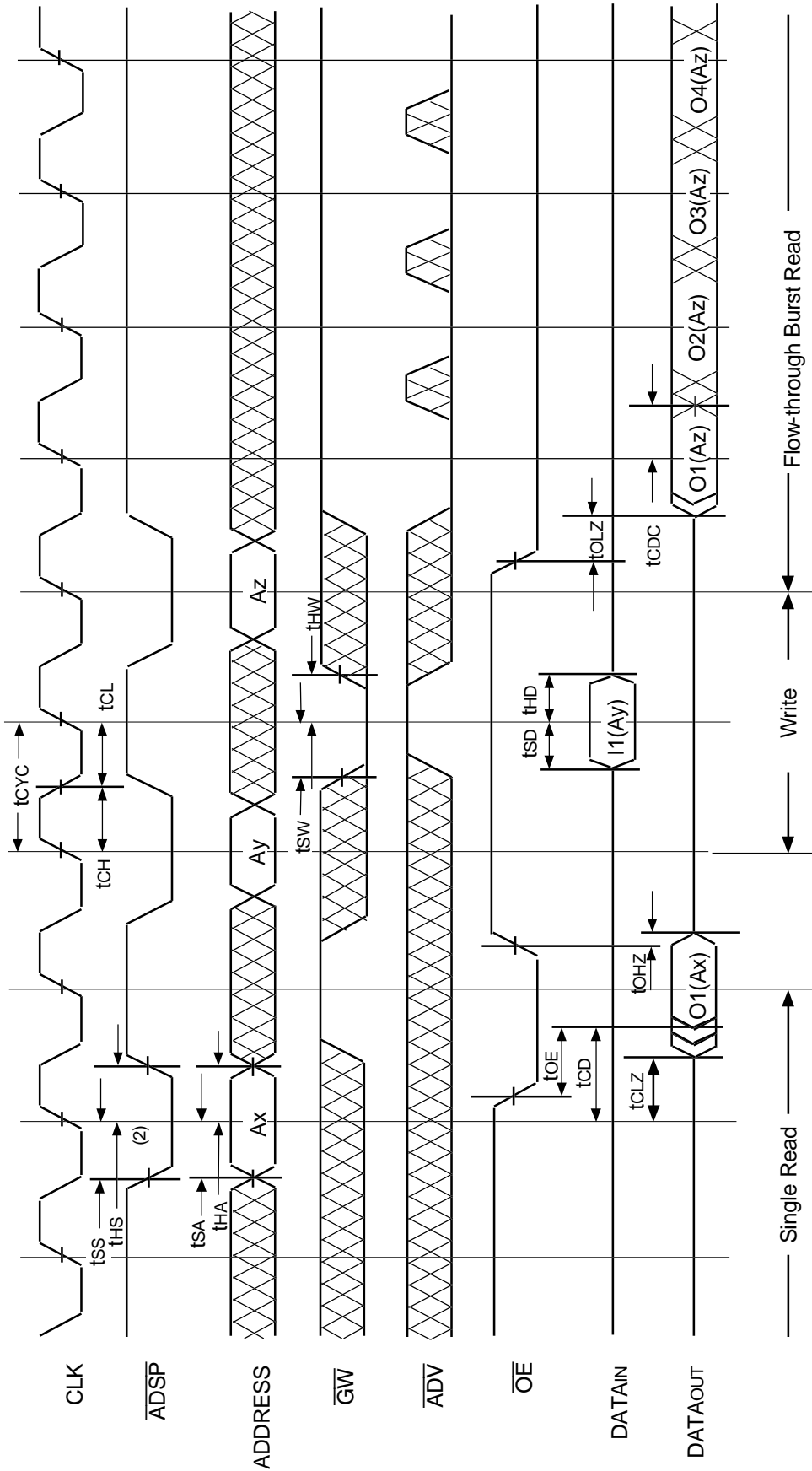


3729.drw.06

**NOTES:**

1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc., where Ao and Ai are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. ZZ input is LOW and LBO is Don't Care for this cycle.
3. CS0 timing transitions are identical but inverted to the  $\overline{CE}$  and  $\overline{CS1}$  signals. For example, when  $\overline{CE}$  and  $\overline{CS1}$  are LOW on this waveform, CS0 is HIGH.

### Timing Waveform of Combined Read and Write Cycles<sup>(1,2,3)</sup>

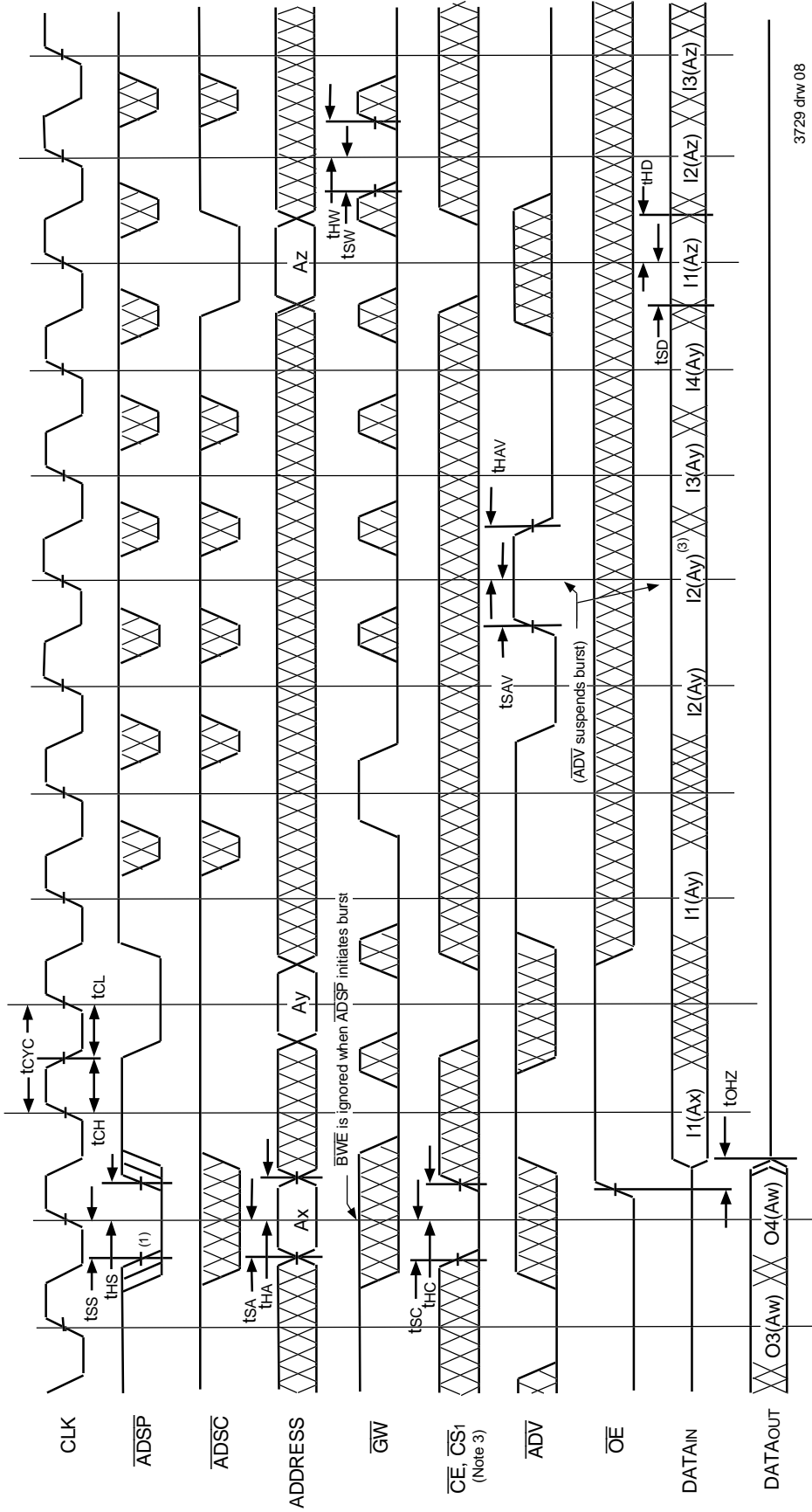


3729 drw 07

**NOTES:**

1. Device is selected through entire cycle;  $\overline{OE}$  and  $\overline{CS1}$  are LOW,  $\overline{CS0}$  is HIGH.
2. ZZ input is LOW and LBO is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay. O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc., where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.

**Timing Waveform of Write Cycle No. 1 —  $\overline{\text{GW}}$  Controlled<sup>(1,2,3)</sup>**

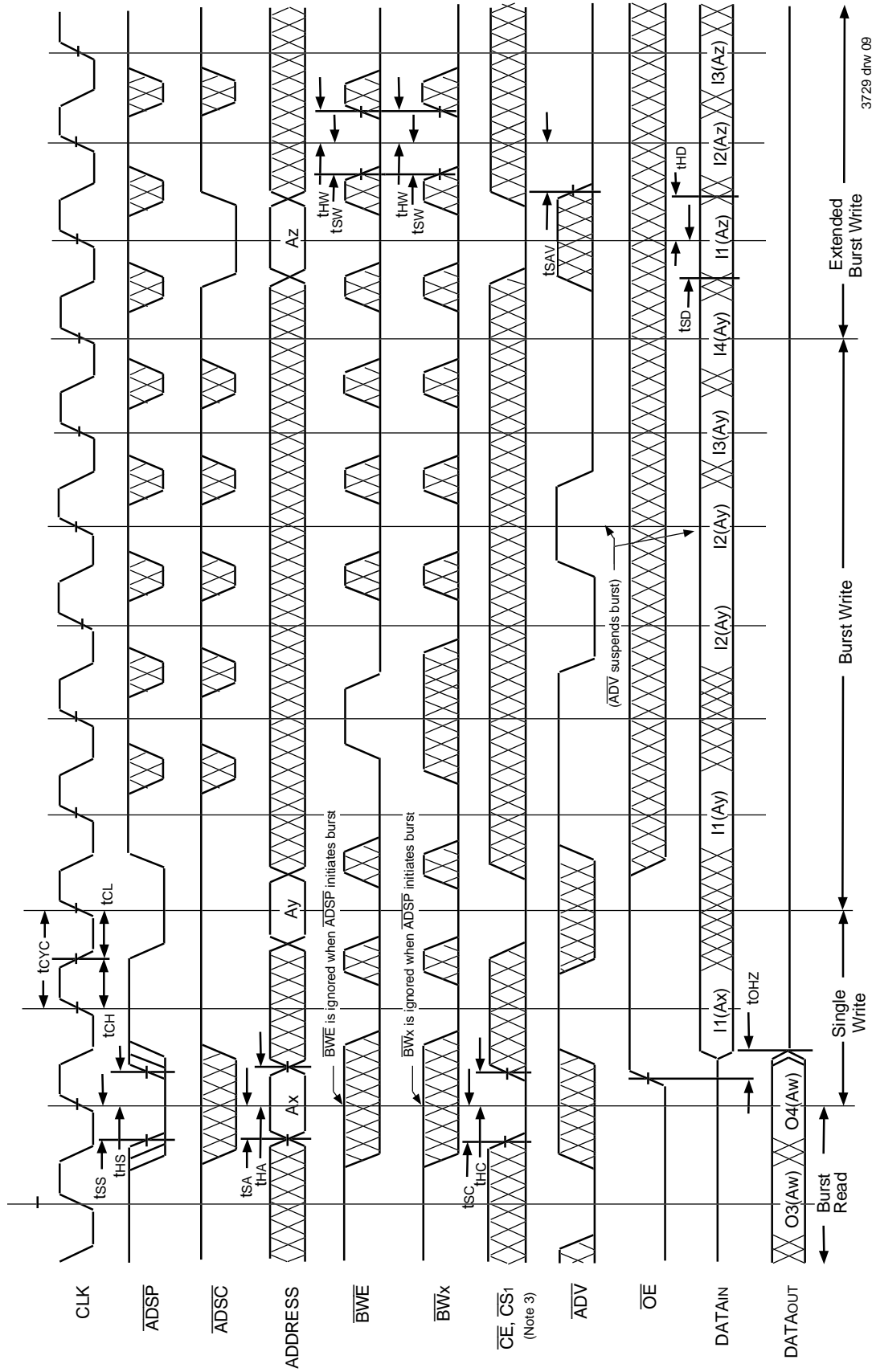


3729 drw 08

**NOTES:**

1. Z<sub>0</sub> input is LOW,  $\overline{\text{BWE}}$  is HIGH, and  $\overline{\text{LBO}}$  is Don't Care for this cycle.
2.  $O_4(A_w)$  represents the final output data in the burst sequence of the base address  $A_w$ .  $I_1(A_x)$  represents the first input from the external address  $A_x$ .  $I_1(A_y)$  represents the first input from the external address  $A_y$ , etc., where  $A_0$  and  $A_1$  are advancing for the four word burst in the sequence defined by the state of the LBO input. In the case of input  $I_2(A_y)$  this data is valid for two cycles because  $\overline{\text{ADV}}$  is high and has suspended the burst.
3.  $\text{CS}_0$  timing transitions are identical but inverted to the  $\overline{\text{CE}}$  and  $\overline{\text{CS}}_1$  signals. For example, when  $\overline{\text{CE}}$  and  $\overline{\text{CS}}_1$  are LOW on this waveform,  $\text{CS}_0$  is HIGH.

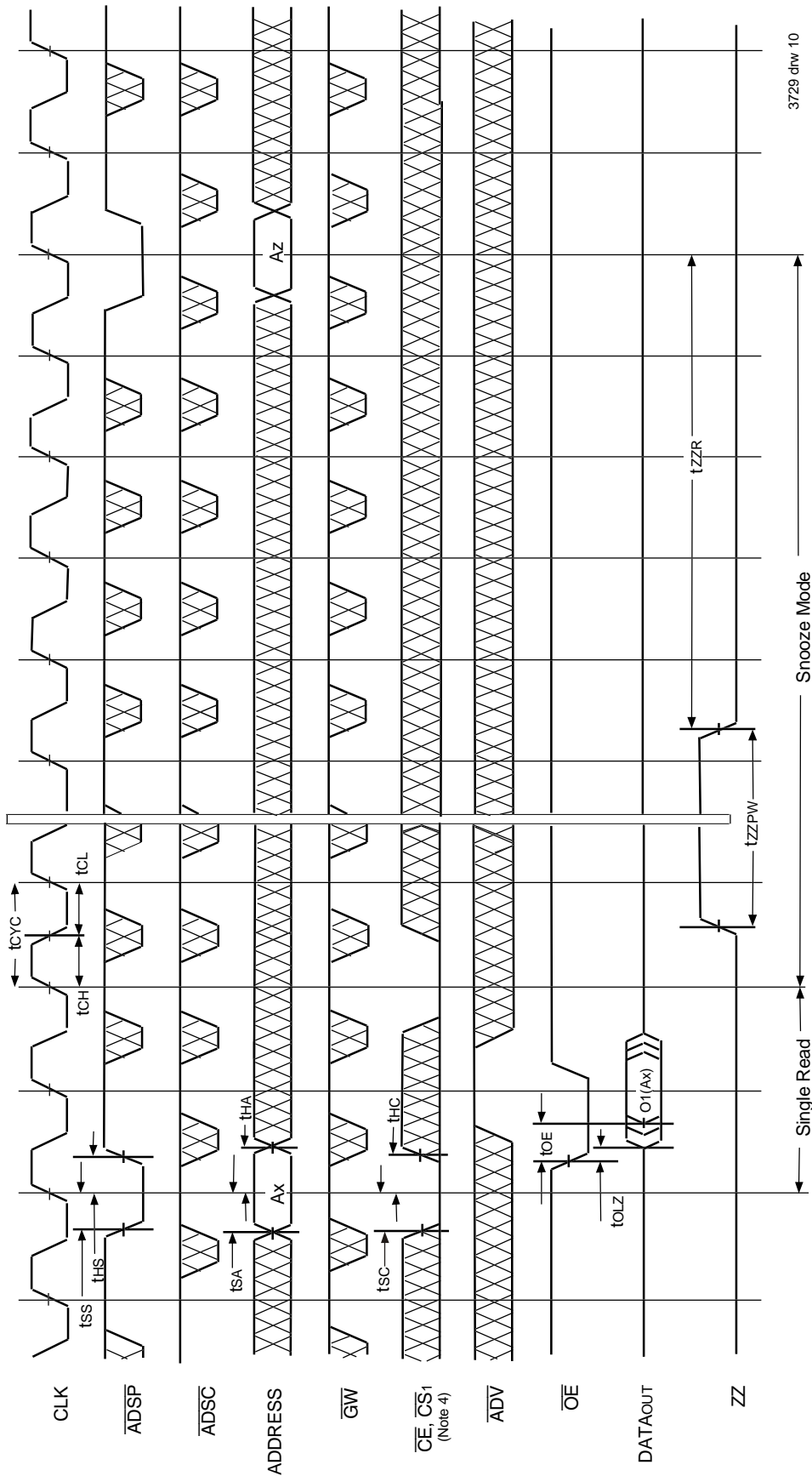
### Timing Waveform of Write Cycle No. 2 — Byte Controlled<sup>(1,2,3)</sup>



**NOTES:**

1. Z<sub>Z</sub> input is LOW,  $\overline{GW}$  is HIGH, and  $\overline{LBO}$  is Don't Care for this cycle.
2. O<sub>4</sub> (Aw) represents the final output data in the burst sequence of the base address Aw. I<sub>1</sub> (Ax) represents the first input from the external address Ax. I<sub>1</sub> (Ay) represents the first input from the external address Ay. I<sub>2</sub> (Ay) represents the next input data in the burst sequence of the base address Ay, etc., where A<sub>0</sub> and A<sub>1</sub> are advancing for the four word burst in the sequence defined by the state of the  $\overline{LBO}$  input. In the case of input I<sub>2</sub>(Ay) this data is valid for two cycles because  $\overline{ADV}$  is high and has suspended the burst.
3. CS<sub>0</sub> timing transitions are identical but inverted to the  $\overline{CE}$  and  $\overline{CS_1}$  signals. For example, when  $\overline{CE}$  and  $\overline{CS_1}$  are LOW on this waveform, CS<sub>0</sub> is HIGH.

## Timing Waveform of Sleep (ZZ) and Power-Down Modes<sup>(1,2,3)</sup>

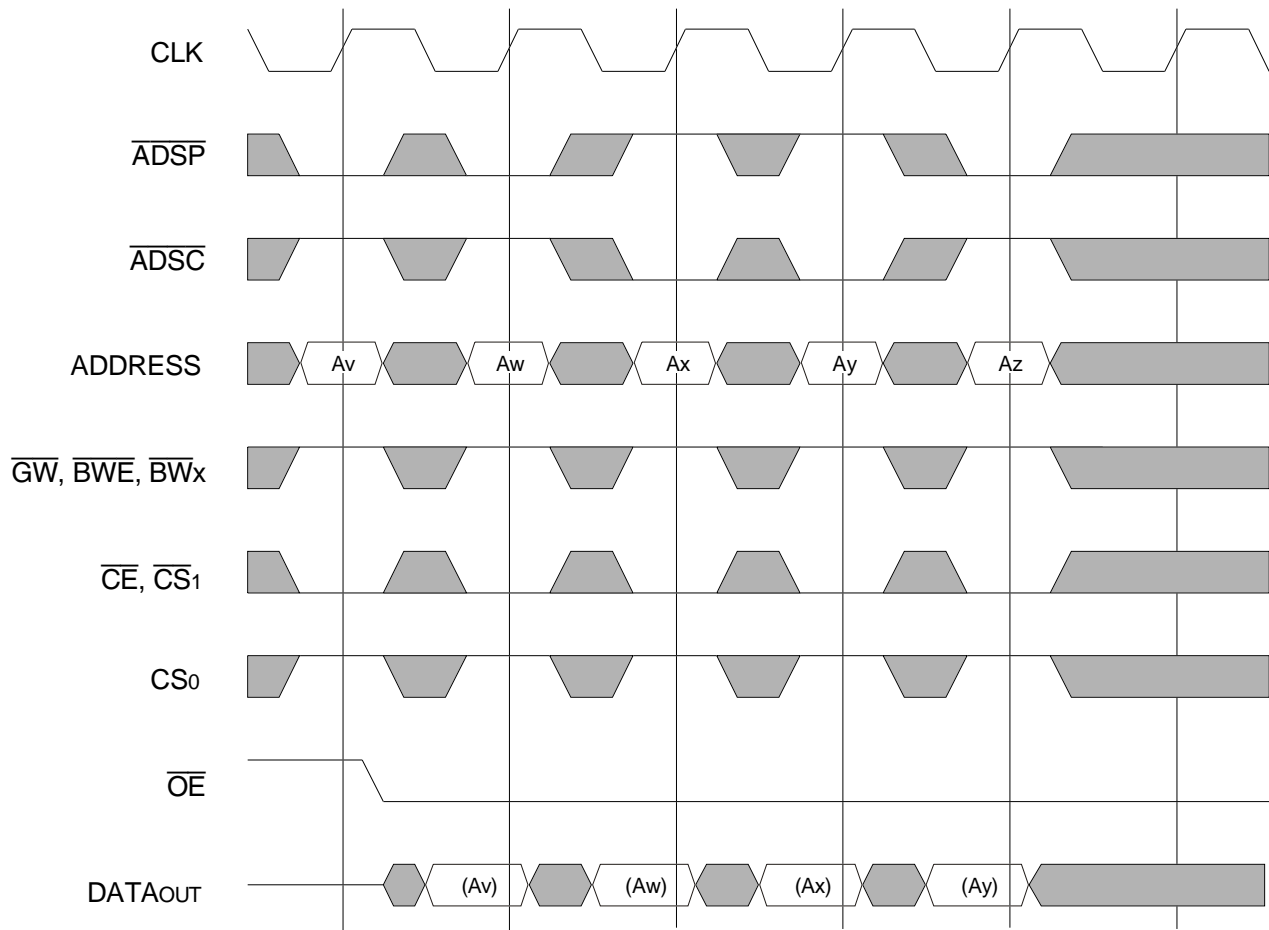


3729 dhw 10

**NOTES:**

1. Device must power up in deselected mode.
2. LBO input is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS<sub>0</sub> timing transitions are identical but inverted to the CE and CS<sub>1</sub> signals. For example, when  $\overline{CE}$  and  $\overline{CS}_1$  are LOW on this waveform, CS<sub>0</sub> is HIGH.

### Non-Burst Read Cycle Timing Waveform

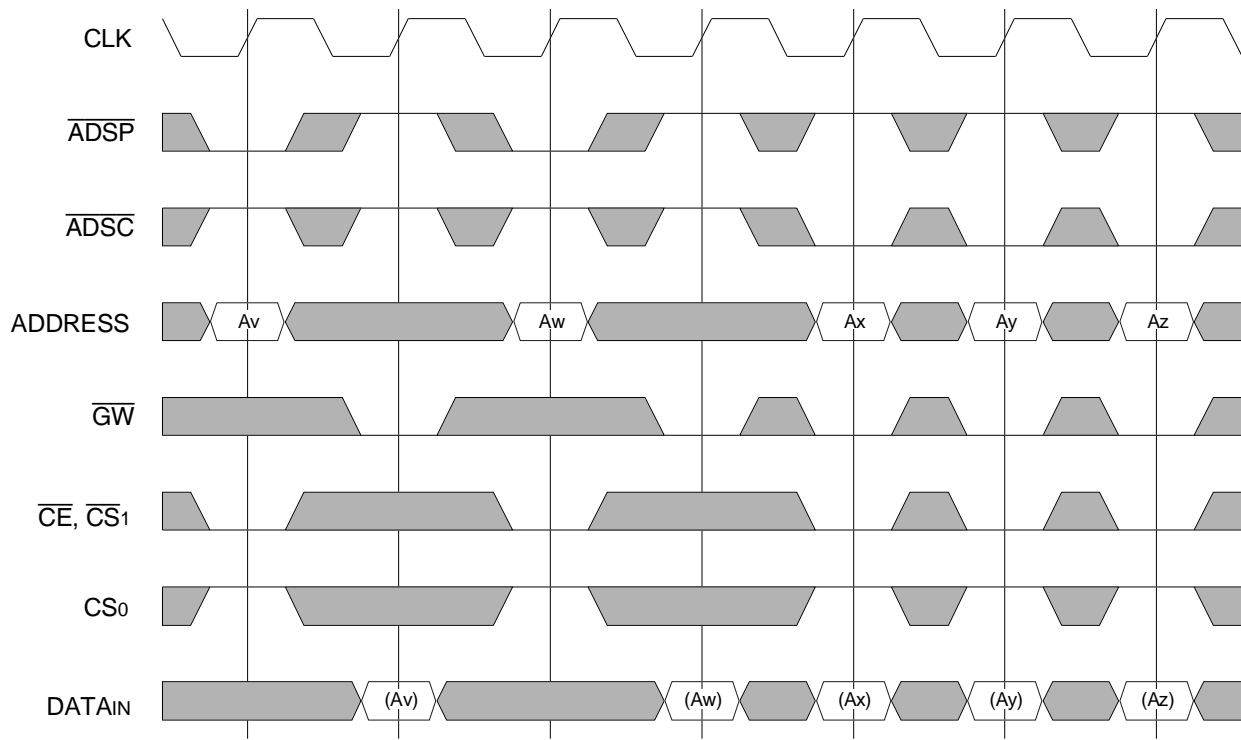


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**NOTES:**

1. ZZ input is LOW,  $\overline{ADV}$  is HIGH, and  $\overline{LBO}$  is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles,  $\overline{ADSP}$  and  $\overline{ADSC}$  function identically and are therefore interchangeable.

## Non-Burst Write Cycle Timing Waveform



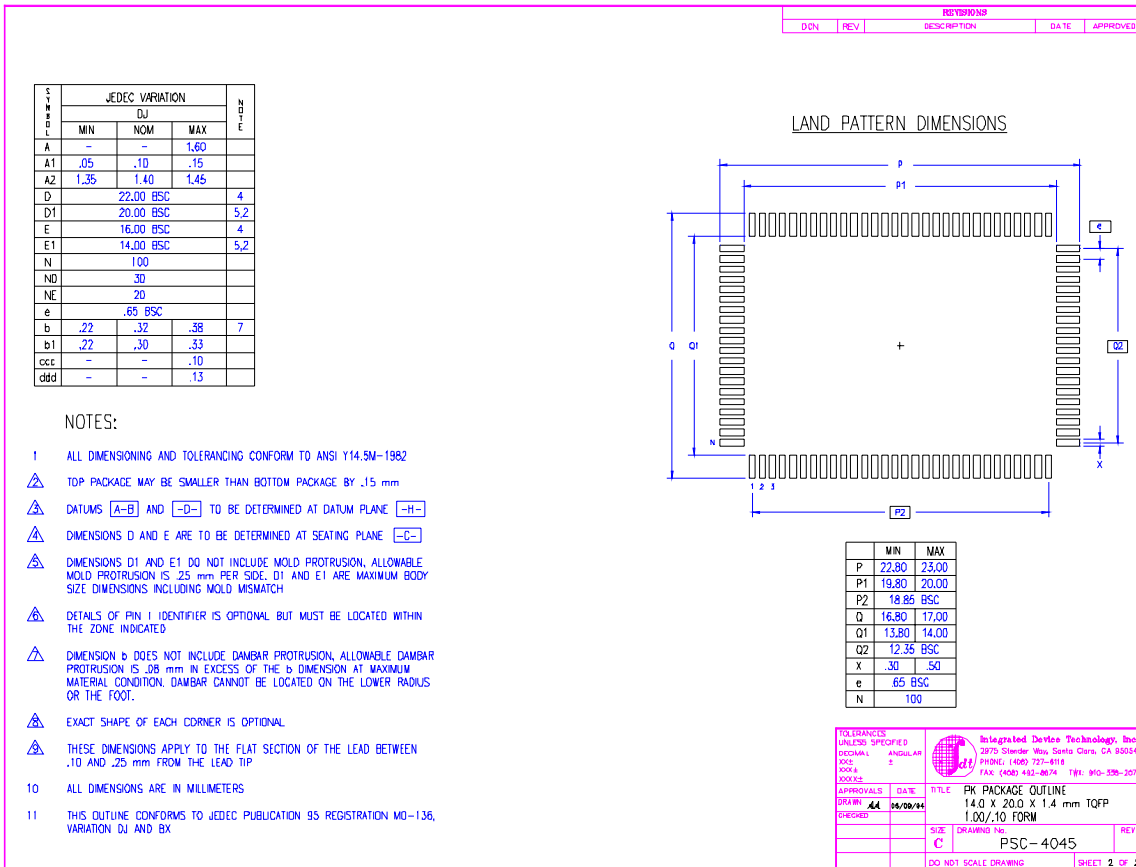
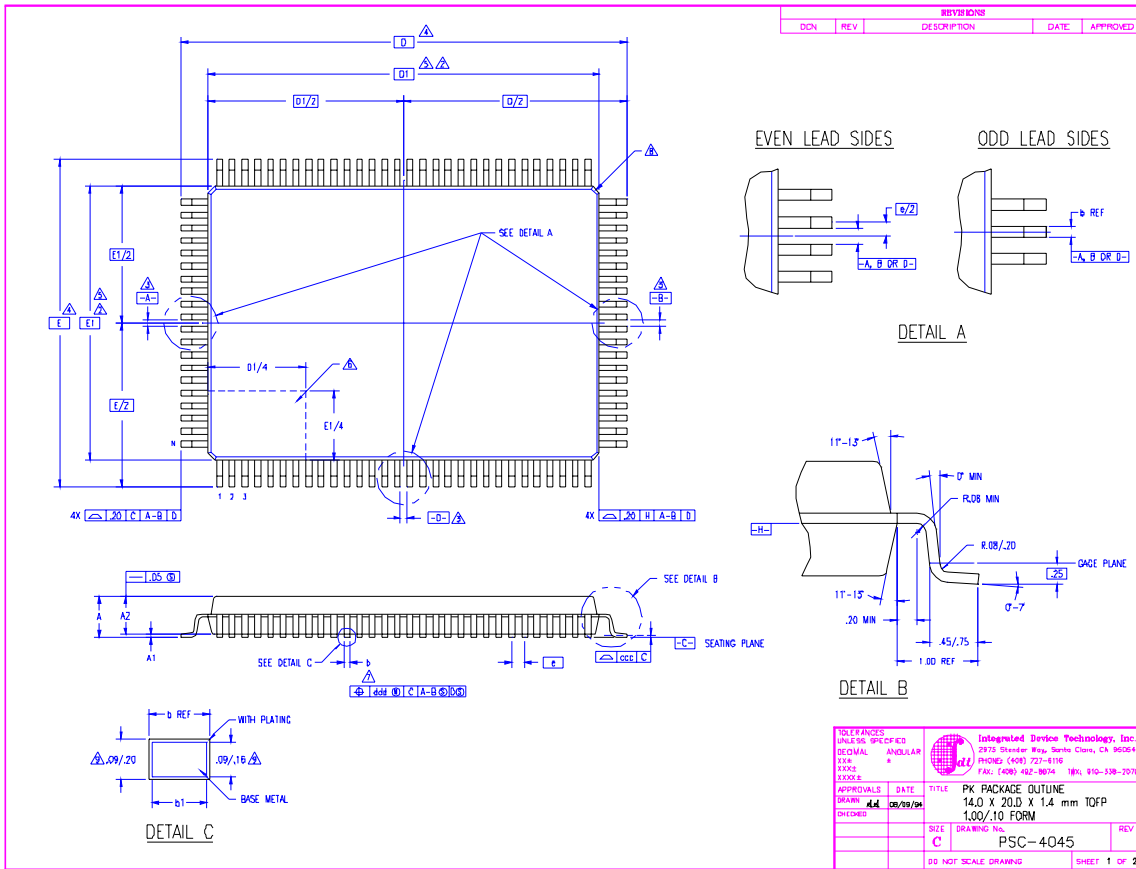
3729 drw 12

### NOTES:

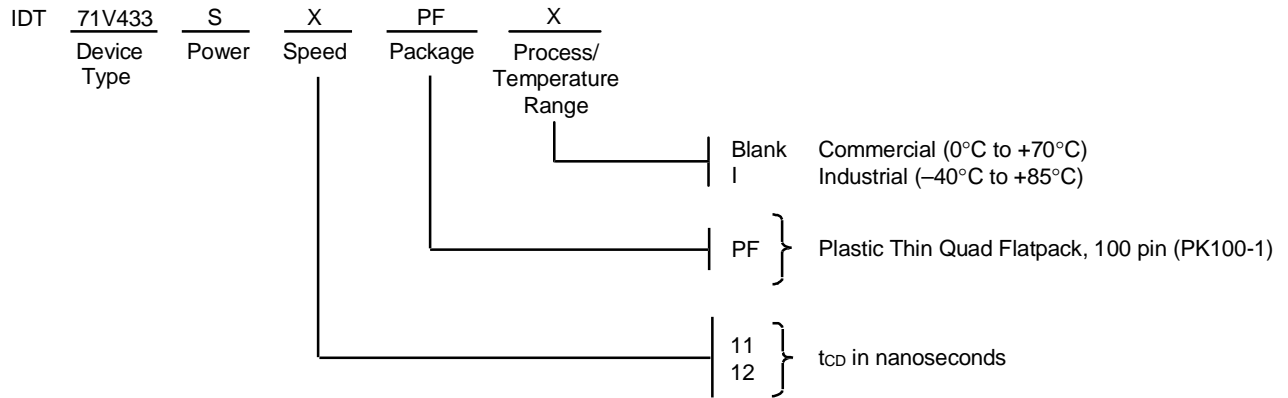
1.  $\overline{ZZ}$  input is LOW,  $\overline{ADV}$  and  $\overline{OE}$  are HIGH, and  $\overline{LBO}$  is Don't Care for this cycle.
2.  $(A_x)$  represents the data for address  $A_x$ , etc.
3. Although only  $\overline{GW}$  writes are shown, the functionality of  $\overline{BWE}$  and  $\overline{BWx}$  together is the same as  $\overline{GW}$ .
4. For write cycles,  $\overline{ADSP}$  and  $\overline{ADSC}$  have different limitations.



# 100-Pin Thin Quad Flatpack (TQFP) Package Diagram Outline



### Ordering Information



PART NUMBER	SPEED IN MEGAHERTZ	tCD PARAMETER	CLOCK CYCLE TIME
71V433S11PF	50 MHz	11 ns	20 ns
71V433S12PF	50 MHz	12 ns	20 ns

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## Datasheet Document History

09/10/99		Updated to new format
	Pg. 1, 8, 9, 17	Revised speed offerings to 11 and 12 ns at 50 MHz
	Pg. 3-5	Adjusted page layout, added extra page
	Pg. 5	Added notes to pin configuration
	Pg. 11-14	Updated notes
	Pg. 18	Added Datasheet Document History
10/08/99	Pg. 1, 4, 8, 9, 17	Added Industrial temperature range offerings
04/04/00	Pg. 17	Added 100pin TQFP Package Diagram Outline
08/09/00		Not recommended for new designs
08/17/01		Removed "Not recommended for new designs" from the background on the datasheet


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