TOSHIBA CMOS Integrated Circuits Silicon Monolithic

JBT6N81S

Single-Chip System LSI for RFID Card

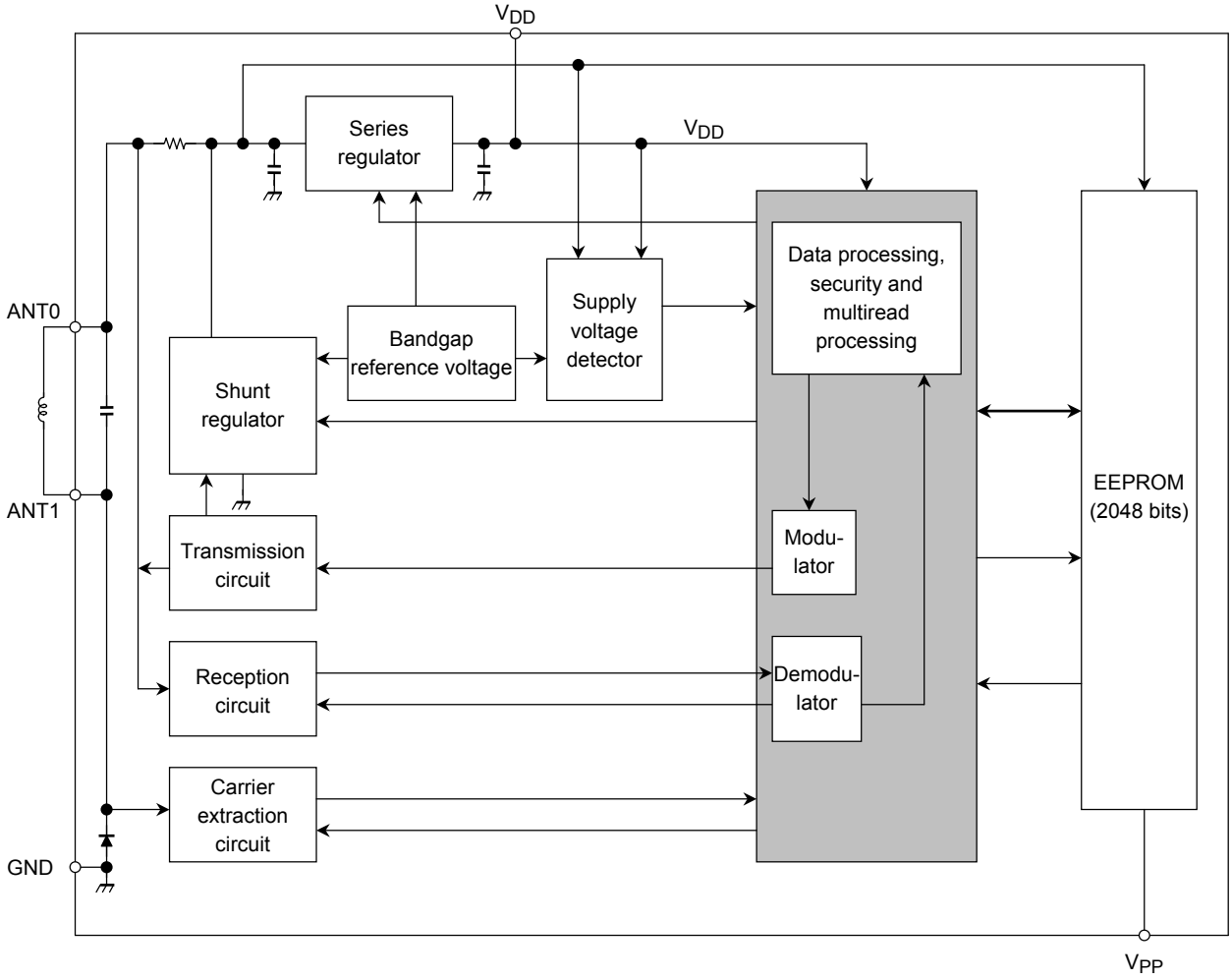
The JBT6N81S is a system LSI for radio frequency identification (RFID) wireless cards. The JBT6N81S incorporates an analog circuit, a data processing circuit and data memory in a single chip.

Features

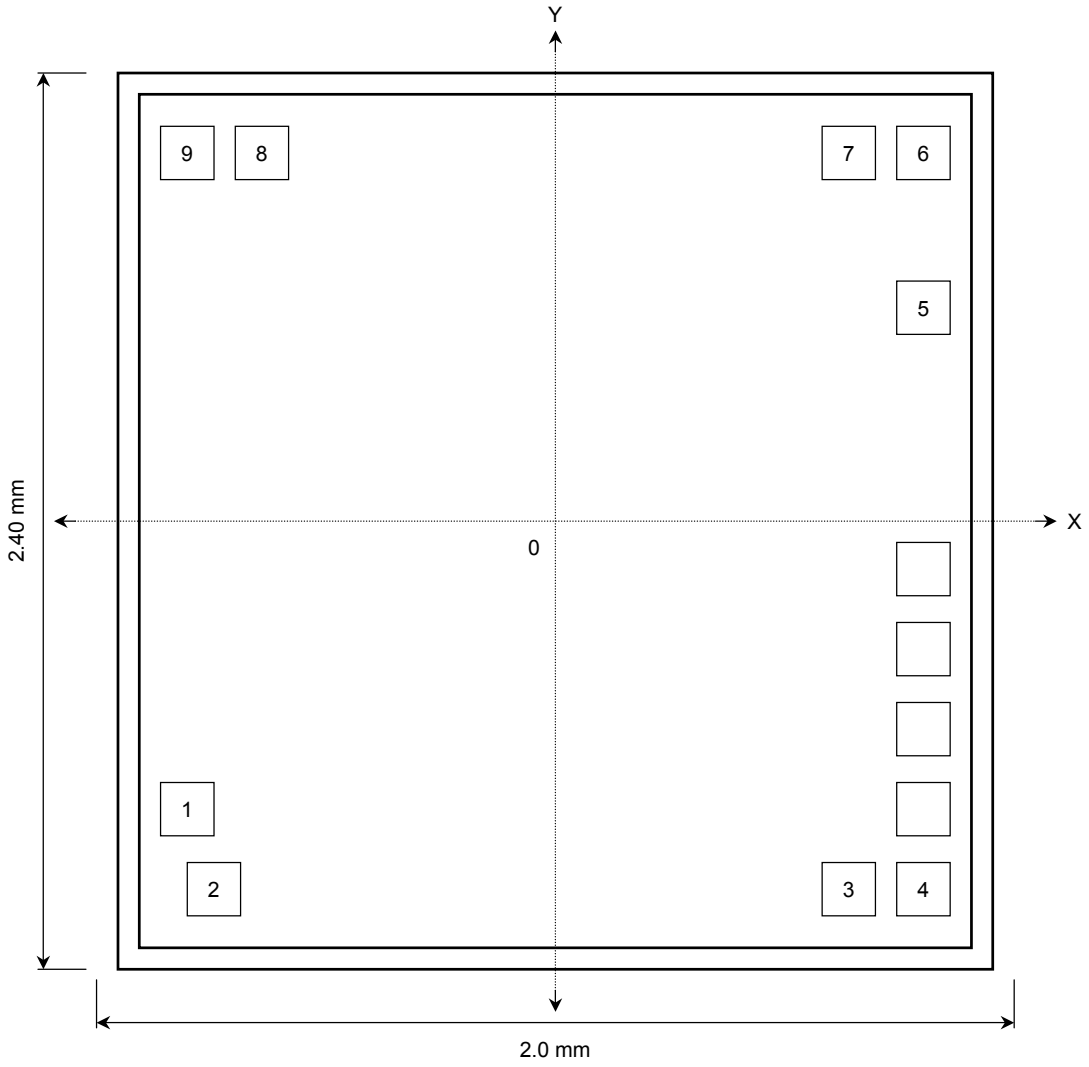
- Owing to dedicated analog and digital circuits, certain characteristics comply with ISO14443, type-B.
- Receive carrier frequency: 13.56 MHz
- Communication method: Low-amplitude modulation (at reception)/load modulation (BPSK) (at transmission)
- Incorporating a high-efficient power generator using electromagnetic induction (incorporating high-efficiency rectifier diode)
- Enables to operate in a high magnetic field: New shunt regulator, high-withstand voltage diode (reverse withstand voltage: 25 V or more)
- Employing high-speed multiread algorithm for communicating with approximately 75 tags/s (Note): New card ID assignment system which uses card ID to identify a tag

  Note: Calculated value. The number of tags that can be read simultaneously changes slightly according to a reader/writer and selected conditions such as time slot numbers.
- Programmable security: Data management using key verification method
- Auto-acknowledgement and auto-creation of CRC
- High-reliability EEPROM: 256-byte EEPROM (16 bytes/page)
  Maximum write time: 2.5 ms
  Overwrite: 100,000 times
  Data retention: 10 years
- Commands for varying operating mode (modulation subcarrier frequency, coding method)
- Supply format: Chip (chip size: 2.0 mm × 2.4 mm, thickness: 175 μm, bump height: 22 μm) which can be mounted using either a solder-bump technique or a bonding technique

System Block Diagram



Pad Allocation



Pad Coordinates

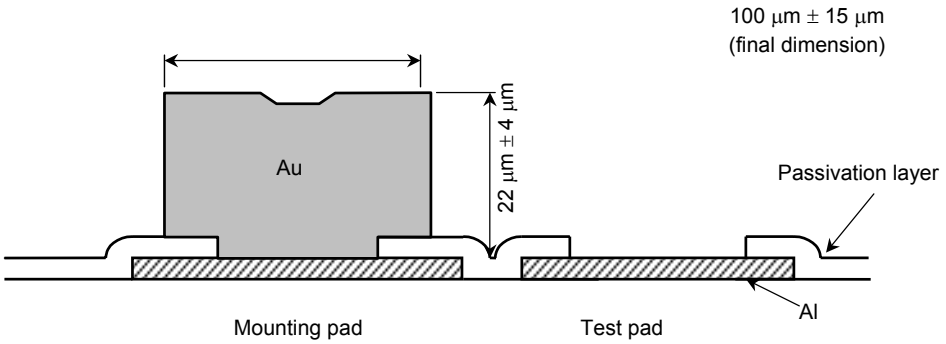
Pad No.	Pad Name	X-Coordinate (μm)	Y-Coordinate (μm)
1	Dummy (bump)	−794	−898
2	V_{PP}	−749	−1075
3	GND	643	−1011
4	GND (bump)	794	−996
5	V_{DD}	809	575
6	ANT1 (bump)	794	996
7	ANT1	643	1011
8	ANT0	−643	1011
9	ANT0 (bump)	−794	996

Note: Values for X-and Y-coordinates are pad center values.

Bump Dimensions

Gold bump width	100 μm ± 15 μm
Gold bump size	Refer to the figure below.
Gold bump height	22 μm ± 4 μm
Gold bump dent	2 μm (max)
Height variations in gold bumps of a chip	±3 μm

Gold Bump Size



Note: The passivation layer is coated with the polyimide layer.

Pin Functions

Pin No.	Symbol	Function
8	ANT0	Antenna pin 0, I/O pin for modulated signal
7	ANT1	Antenna pin 1, system clock input
5	V_{DD}	Rectified power supply output, voltage controlled by a regulator
3	GND	LSI voltage reference
2	V_{PP}	VPP monitor pin (do not connect to anything.)

LSI External Specifications

Parameter	Specifications
Power supply	Batteryless, external power supply system using electromagnetic induction
Coupling type	Electromagnetic induction
Power transmission frequency	13.56 MHz ± 6.78 kHz (Note 1: An antenna is connected externally.)
Communications method	Low-amplitude modulation (at reception)/load modulation (BPSK) (at transmission)
Transfer speed	105.9375 kb/s, 211.875 kb/s
Transfer method	Asynchronous (start bit: 1 bit, stop bit: 1 bit, data: 8 bits, LSB first)
Memory capacity	2 kbit EEPROM (256 bits for security area)
Overwrite	100,000 or more (data retention: 10 years)
Write time	Approximately 2 ms/16 bytes (page write: max)
Control circuit	• Key verification and access authorization control by hardware • Incorporating two access keys (1-byte security status + 7-byte key) × 2 • Access authorization for the access keys, selectable between read-only and read/write in units of 64 bytes (programmable security) • Block reading and writing in units of 16 bytes according to access key and physical address
Multiread	Approximately 75 tags/s (Note) <New card ID assignment system which uses card ID to identify a tag>
Operating temperature	−20°C to 85°C

Note: Calculated value. The number of tags that can be read simultaneously changes slightly according to a reader/writer and selected conditions such as time slot numbers.

Functions and Specifications of the Core Block

The JBT6N81S is comprised of the following three blocks: An RF analog block for power generation, carrier extraction and regulation; a digital block for data modulation, demodulation and data processing; and EEPROM block for data storage.

1. Analog Block

(1) Rectifier circuit
Receives radio wave via the (external) antenna circuit and generates DC power for operating internal circuits with half-wave rectification.

(2) Shunt regulator
Maintains the level of the voltage generated by the rectifier circuit at a fixed voltage level, 2.6 V (typ.). The digital circuits and EEPROM operate using the voltage supplied by the shunt regulator. The shunt regulator also protects internal circuits from the effect of a high magnetic field.

(3) Carrier extraction circuit
Transforms the received carrier, which was modulated using ASK, into a square wave. Then applies the wave to the logic circuits for demodulation.

(4) Transmission circuit
Modulates a signal, which was modulated by the logic circuits, onto data wave on which 13.56-MHz carrier is superimposed using PSK and transmits the data to a reader/writer (R/W) using load modulation.

(5) Supply voltage detector
Supports three types of voltage detectors for initializing the system and enabling/disabling EEPROM writing. As a result, operation is always stable.

2. Digital Block

(1) Demodulator
Converts the square wave transformed by the carrier extraction circuit of the analog block into binary data.

(2) Modulator
Modulates the binary data, which is a response to a command from the R/W, onto 847-kHz subcarrier using PSK.

(3) Data processing
Processes data according to the commands received. Processes include CRC check, EEPROM write and read, and reset of the entire LSI.

(4) Security logic
Two keys can be set simultaneously using the security area allocated to the EEPROM. Using the keys, write/read, read or no access can be set in units of 64-byte blocks (obtained by dividing EEPROM memory area by four). (For example, with key A, read/write for a particular block can be set and other blocks can be only read, while with key B, read/write for any blocks can be set.)

(5) Status response
Response to a command from the reader/writer consists of the status, the Cid (card ID), data and the CRC. The status indicates, the internal status of the LSI to the R/W. If the LSI status is normal, status data 00H is prefixed with the Cid (card ID), the data and the CRC. If the LSI status is abnormal, no data is added and only the status indicating the abnormality, the Cid (card ID) and the CRC are sent. The bit corresponding to each abnormality condition which has occurred is set to 1 in the status field.

(6) Multiread function
The multiread function is used for reading multiple RFIDs in the communications area using the same reader/writer (R/W). An RFID (LSI) generates a random number internally according to the Multiread command transmitted by the R/W. The RFID sends a response at a timing determined by the corresponding time slot. Thus, responses from the various RFIDs will not collide with each other, enabling data to be received properly by the R/W.
Note: Depending on the conditions (for example, a R/W to be used), the ability to read all the data may vary. In some cases, some data may be left unread (since it cannot be undetected). Toshiba recommends the use of a detection function other than the multi-read function.

Electrical Characteristics

1. Ratings

Parameter	Symbol	Operating Rating	Unit
Input current (among ANT1 → GND → ANT2)	I_{ANT}	DC20	mA
Operating temperature range	T_{opr}	−20 to 85	°C
Storage temperature range	T_{stg}	−50 to 150	°C

Note 1: Unless otherwise specified, the specifications are within the above operating temperature range.

Note 2: The storage temperature rating above does not guarantee the EEPROM data retention.

2. DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Minimum operating voltage 1	V_{DDmin}	Minimum operating voltage excluding memory write (Voltage monitor pin is V_{DD}.)	—	2.0	2.2	V
Minimum operating voltage 2	V_{DDeew}	Minimum operating voltage including memory write (Voltage monitor pin is V_{DD}.)	—	2.6	2.9	V
Operating current dissipation 1	I_{DDopr}	Current dissipation for operations excluding memory write (V_{DD} = 2.3 V)	—	100	200	μA
Operating current dissipation 2	I_{DDopr}	Current dissipation for all operations including memory write (V_{DD} = 2.8 V)	—	150	350	μA

3. Operating Characteristics

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Receive carrier frequency	fcrr	Carrier frequency at which the LSI can operate		13.56		MHz
Reply carrier frequency	fpsk	Subcarrier frequency: 847 kHz		13.56		MHz
Transfer rate	—	Transfer speed (either 105.9375 kb/s or 211.875 kb/s can be set using data rate setting command. Data is sent/received at the same transfer rate.)		105.9375		kb/s
				211.875		
Carrier period per bit (at transmission/reception)	—	Transfer speed: 105.9375 kb/s		128		period
		Transfer speed: 211.875 kb/s		64		
EEPROM write time	tpw	—	—	—	2.5	ms
EEPROM overwrite	Ted	—	10^5	—	—	times
EEPROM data retention period	Pre	Ambient temperature: −20°C to +85°C	10	—	—	y

Memory Map

Page No.	16 Bytes		16 Bytes	
	8 Bytes	8 Bytes	8 Bytes	8 Bytes
00H	ATQ data	(Last 8 bytes) Uid	01H SS2	Key2 SS3 Key3
02H	Any data		03H	Any data
04H	Any data		05H	Any data
06H	Any data		07H	Any data
08H	Any data		09H	Any data
0AH	Any data		0BH	Any data
0CH	Any data		0DH	Any data
0EH	Any data		0FH	Any data

Note 1: ATQ is an abbreviation for Answer To reQuest. The LSI sends back the ATQ data after receiving a reset command or self-reset.

Note 2: Uid is an abbreviation for Unique ID which indicates the last 8 bytes of ATQ data.

Note 3: SS2 for Key 2 and SS3 for Key 3 on page 01H are used for security status respectively. Based on the security status, read/write access permission in memory area can be set in units of 64 bytes (enclosed by heavy line).

Note 4: Data is read or written in units of 16 bytes.

The advantage of using this LSI is that it can be supplied as a single LSI for RFID allowing the user to configure peripherals (e.g. antennae, and reader/writers) so as to develop the desired system. However, because the peripheral environment may be highly user-specific, incompatibilities between the LSI and the user-configured environment (communications failures) may occur. Please carry out sufficient research before using this LSI.

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