

MC100EP140

3.3V ECL Phase-Frequency Detector

The MC100EP140 is a three state phase frequency–detector intended for phase–locked loop applications which require a minimum amount of phase and frequency difference at lock. Since the part is designed with fully differential internal gates, the noise is reduced throughout the circuit, especially at high speeds. The basic operation of a Phase/Frequency Detector (PFD) is to “compare” an incoming signal (feedback) to a set reference signal. When the Reference (R) and Feedback (FB) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which, when subtracted and integrated, provide an error voltage for control of a VCO. Detector states of operation are shown in the Figure 2 and the State Table.

The device is packaged in a small outline, surface mount 8–lead SOIC package. The typical output amplitude of the EP140 is 400 mV, allowing faster switching time and greater bandwidth. For proper operation, the input edge rate of the R and FB inputs should be less than 5 ns.

More information on Phase Lock Loop operation and application can be found in AND8040.

The pinout is shown in Figure 1, the logic diagram in Figure 3, and the typical termination in Figure 5.

- 500 ps Typical Propagation Delay
- Maximum Frequency > 2.1 GHz Typical
- Fully Differential Internally
- Advanced High Band Output Swing of 400 mV
- Transfer Gain: 1.0 mV/Degree at 1.4 GHz
1.2 mV/Degree at 1.0 GHz
- Rise and Fall Time: 100 ps Typical
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.6 V
with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$
with $V_{EE} = -3.0\text{ V}$ to -3.6 V
- Open Input Default State



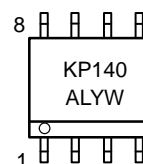
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MARKING DIAGRAM



SO–8
D SUFFIX
CASE 751



KP = MC100EP
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EP140D	SO–8	98 Units/Rail
MC100EP140DR2	SO–8	2500 Units/Reel

MC100EP140

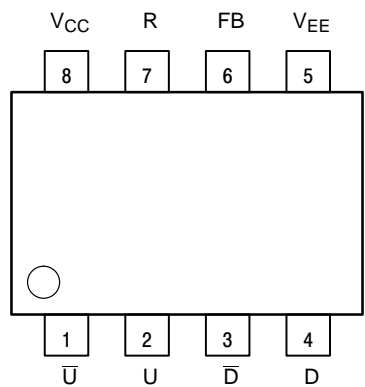


Figure 1. 8-Lead Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
D, \bar{D}	Differential Down Outputs
U, \bar{U}	Differential Up Outputs
R*	ECL Reference Input
FB*	ECL Feedback Input
V _{CC}	Positive Supply
V _{EE}	Negative Supply

* Pins will default LOW when left open.

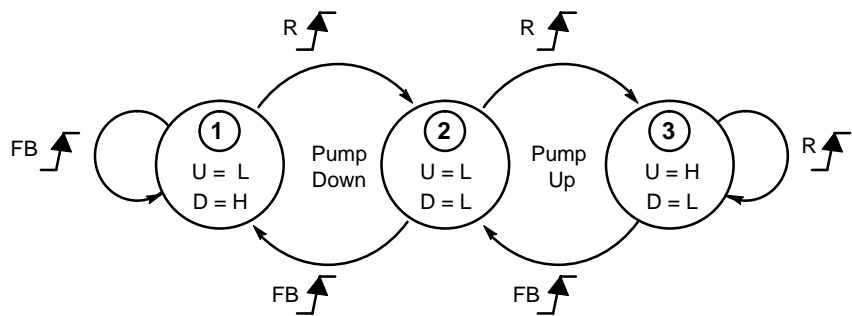


Figure 2. Phase Detector Logic Model

STATE TABLE

PHASE DETECTOR STATE	INPUT		OUTPUT	
	R	FB	U	D
PUMP DOWN 2-1-2				
2	L	L	L	L
2-1	L	H	L	H
1-2	H	L	L	L
2	L	L	L	L
PUMP UP 2-3-2				
2	L	L	L	L
2-3	H	L	H	L
3-2	H	H	L	L
2	L	L	L	L

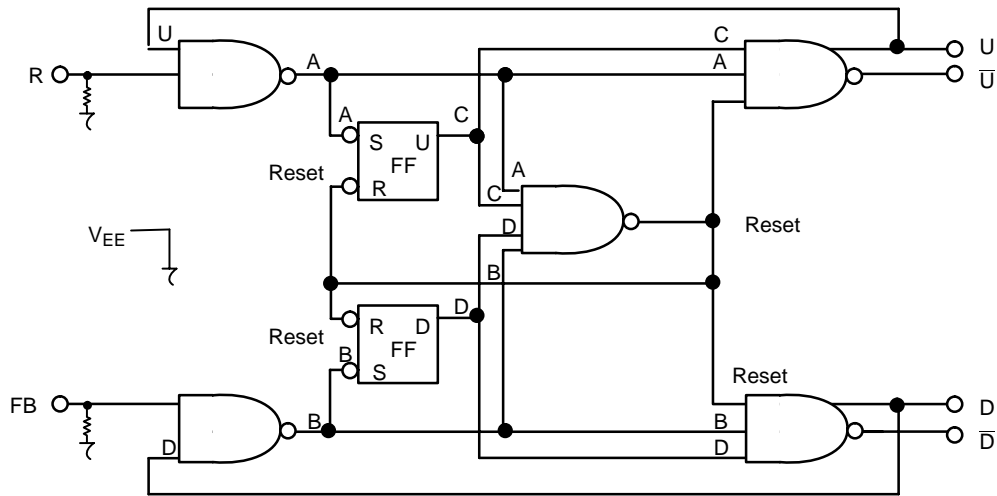


Figure 3. Logic Diagram

MC100EP140

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	37.5 k Ω
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 2 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL-94 V-0 @ 0.125 in
Transistor Count	457 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	55	70	85	60	74	90	63	78	93	mA
V _{OH}	Output HIGH Voltage (Note 4)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V _{OL}	Output LOW Voltage (Note 4)	1755	1880	2005	1755	1880	2005	1755	1880	2005	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V _{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -0.3 V.

4. All loading with 50 Ω to V_{CC}-2.0 volts.

MC100EP140

100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.6\text{ V}$ to -3.0 V (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	55	70	85	60	74	90	63	78	93	mA
V_{OH}	Output HIGH Voltage (Note 6)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 6)	-1545	-1420	-1295	-1545	-1420	-1295	-1545	-1420	-1295	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

5. Input and output parameters vary 1:1 with V_{CC} .

6. All loading with $50\ \Omega$ to $V_{CC}-2.0$ volts.

AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -3.6 V or $V_{CC} = 3.0\text{ V}$ to 3.6 V ; $V_{EE} = 0\text{ V}$ (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 4 $F_{\text{max}}/\text{JITTER}$)		> 2			> 2			> 2		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential R to U, FB to D FB to U, R to D	300 400	450 600	6002 800	325 450	475 650	625 850	350 500	500 700	650 900	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 4 $F_{\text{max}}/\text{JITTER}$)		.2	< 1		.2	< 1		.2	< 1	ps
V_{PP}	Input Voltage Swing	400	800	1200	400	800	1200	400	800	1200	mV
t_r , t_f	Output Rise/Fall Times (20% – 80%) Q, \bar{Q}	50	90	180	60	100	200	70	120	220	ps

7. Measured using a 750 mV V_{PP} pk-pk, 50% duty cycle, clock source. All loading with $50\ \Omega$ to $V_{CC}-2.0\text{ V}$.

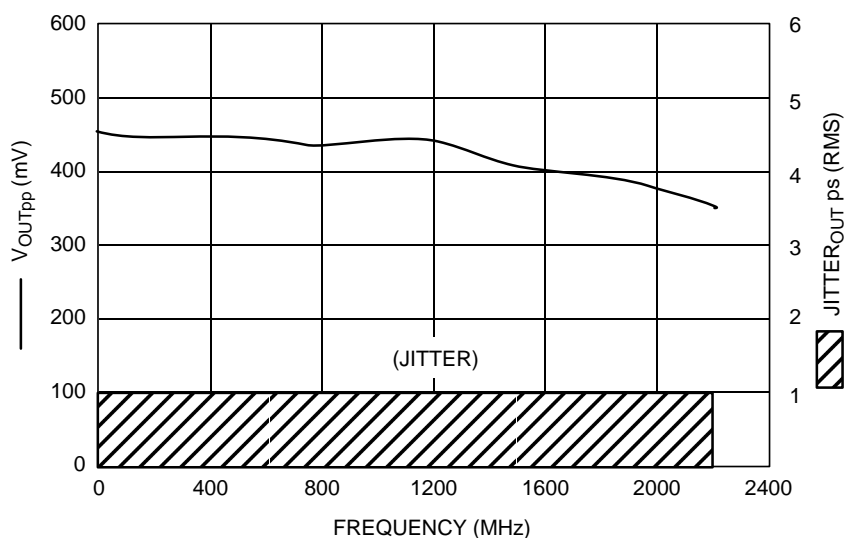


Figure 4. $F_{\text{max}}/\text{Jitter}$

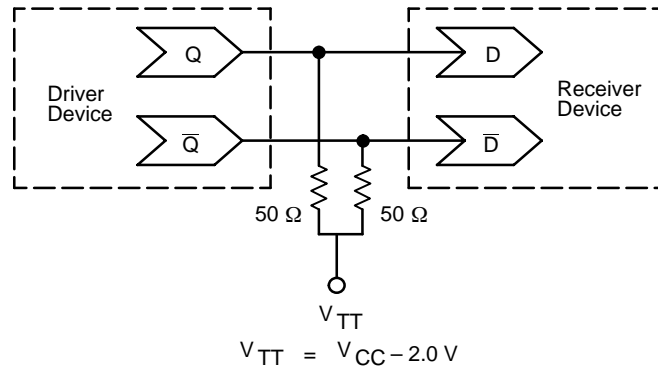


Figure 5. Typical Termination for Output Driver and Device Evaluation
 (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

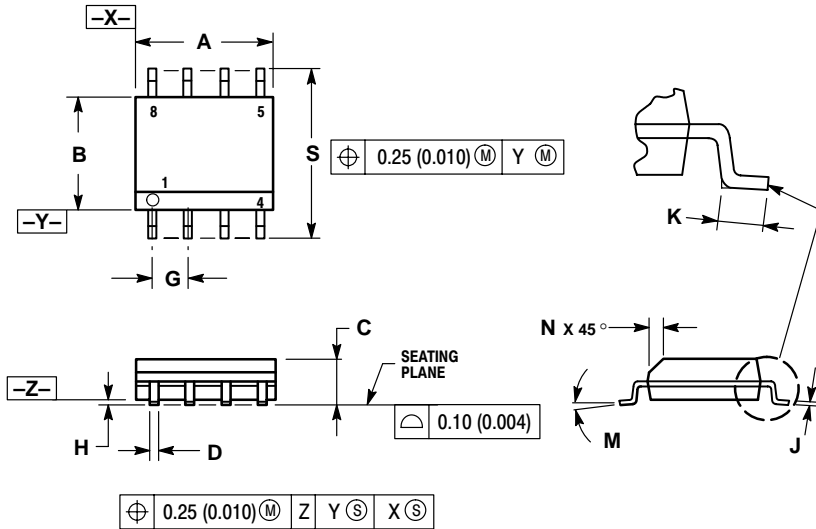
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices
- AND8040** – Phase Lock Loop Operation

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

MC100EP140

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

Notes

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