



# HIGH-SPEED CMOS DUAL 4-INPUT MULTIPLEXER

**IDTQS74FCT253AT**

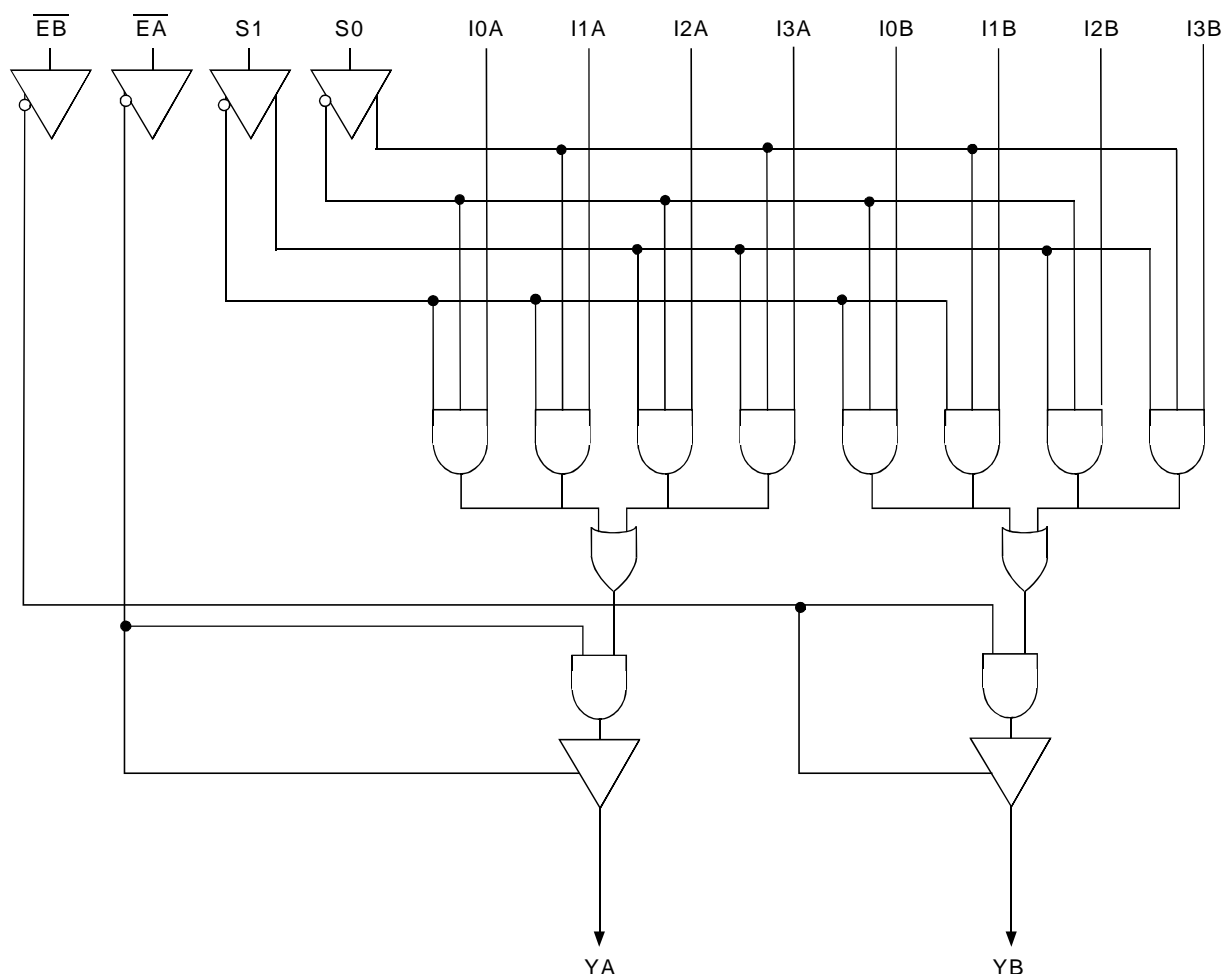
## FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- I<sub>OL</sub> = 48mA
- Available in SOIC and QSOP packages

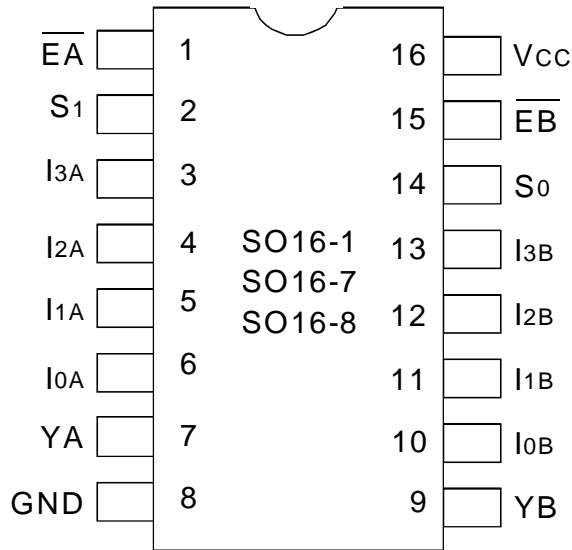
## DESCRIPTION:

The IDTQS74FCT253AT is a high-speed CMOS TTL-compatible dual 4-input multiplexer with 3-state outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V<sub>CC</sub> is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC/ QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	- 0.5 to +7	V
TSTG	Storage Temperature	- 65 to +150	°C
IOUT	DC Output Current Max Sink Current/Pin	120	mA
I <sub>IK</sub>	Input Diode Current, V <sub>IN</sub> < 0	- 20	mA
I <sub>OK</sub>	Output Diode Current, V <sub>OUT</sub> < 0	- 50	mA

**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4	—	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	—	pF

**NOTE:**

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
I <sub>0</sub> - I <sub>7</sub>	I	Data In
S <sub>0</sub> - S <sub>1</sub>	I	Select
$\overline{EA}$ , $\overline{EB}$	I	Enable
YA, YB	O	Data Out

## FUNCTION TABLE (1)

Enable		Select		Outputs		Function
$\overline{EA}$	$\overline{EB}$	S <sub>1</sub>	S <sub>0</sub>	YA	YB	
H	X	X	X	Z	Z	Disable A
X	H	X	X	X	Z	Disable B
L	L	L	L	I <sub>0A</sub>	I <sub>0B</sub>	S <sub>1</sub> -0 = 0
L	L	L	H	I <sub>1A</sub>	I <sub>1B</sub>	S <sub>1</sub> -0 = 1
L	L	H	L	I <sub>2A</sub>	I <sub>2B</sub>	S <sub>1</sub> -0 = 2
L	L	H	H	I <sub>3A</sub>	I <sub>3B</sub>	S <sub>1</sub> -0 = 3

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} < V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current						
$I_{OZ}$	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2)}$		-60	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(2)}$		—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 48\text{mA}$	—	—	0.5	V

### NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
2. This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ freq = 0	—	2	mA
$I_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

FCTL

### NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $I_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4\text{V}$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_i$  = Input Frequency  
 $N_i$  = Number of Inputs at  $f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE<sup>(1)</sup>**

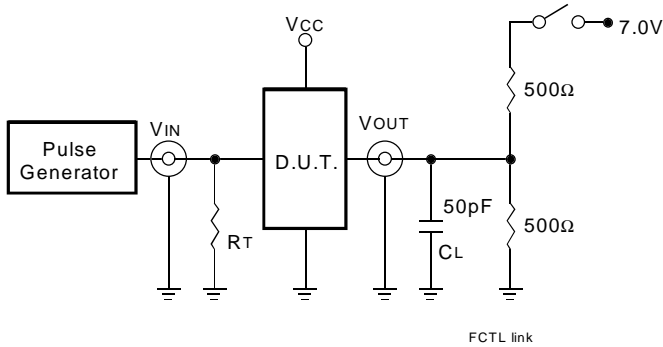
Symbol	Parameter <sup>(2)</sup>	Min.	Max.	Unit
t <sub>Y</sub>	Propagation Delay In to Y	1.5	5.2	ns
t <sub>SY</sub>	Propagation Delay S <sub>n</sub> to Y	1.5	6.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\bar{E}$ to Y	1.5	6	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Enable Time $\bar{E}$ to Y <sup>(3)</sup>	1.5	6	ns

**NOTES:**

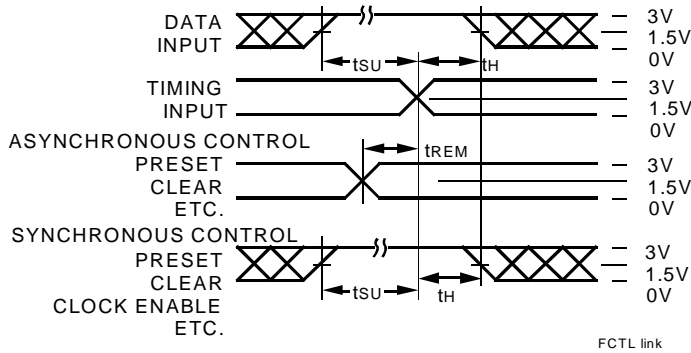
1. C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

## TEST CIRCUITS AND WAVEFORMS

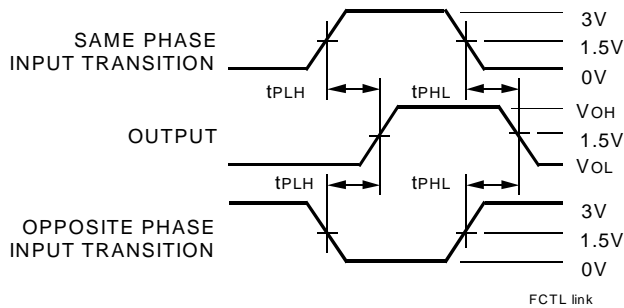
### TEST CIRCUITS FOR ALL OUTPUTS



### SET-UP, HOLD, AND RELEASE TIMES



### PROPAGATION DELAY



### SWITCH POSITION

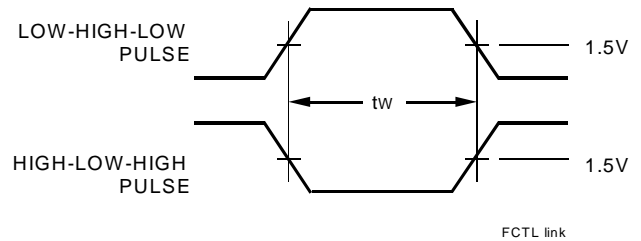
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

#### DEFINITIONS:

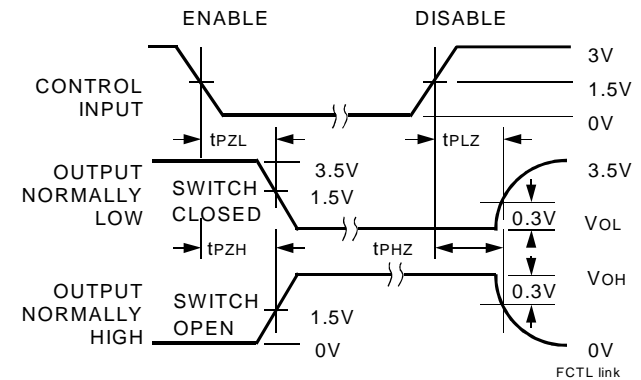
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

### PULSE WIDTH



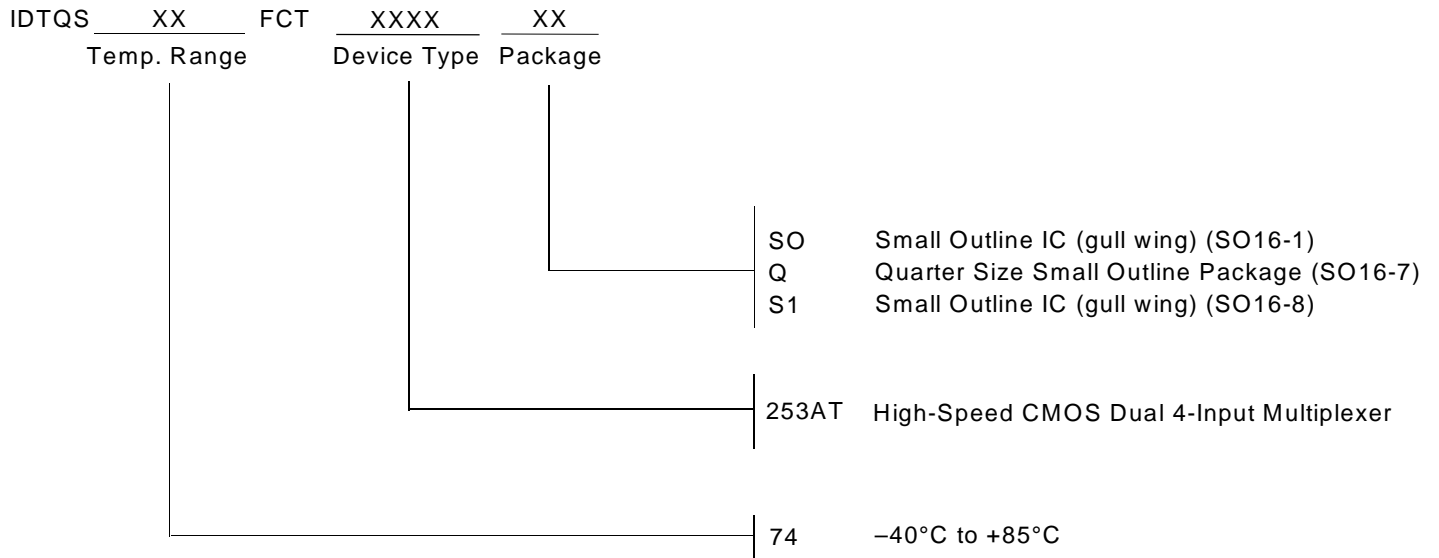
### ENABLE AND DISABLE TIMES



#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $Z_o \leq 50\Omega$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**  
800-345-7015 or 408-727-6116  
fax: 408-492-8674  
[www.idt.com](http://www.idt.com)\*

\*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.  
The IDT logo is a registered trademark of Integrated Device Technology, Inc.