# GUARANTEED LOW SKEW CMOS CLOCK DRIVER/BUFFER

***QS5805/A/B***

## FEATURES:

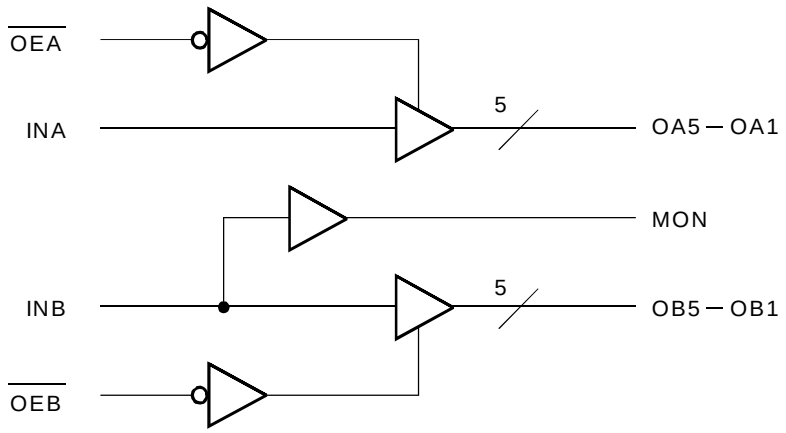
- 10 CMOS outputs
- Monitor output
- Rail-to-rail output voltage swing
- Input hysteresis for better noise margin
- Guaranteed low skew:
  - 0.7ns output skew (same bank)
  - 0.8ns output skew (different banks)
  - 1.2ns part-to-part skew
- Std., A, and B speed grades
- Available in QSOP and SOIC packages

## DESCRIPTION

The QS5805 clock buffer/driver circuits can be used for clock buffering schemes where low skew is a key parameter. This device offers two banks of five non-inverting outputs. The QS5805 device provides low propagation delay buffering with on-chip skew of 0.7ns for same-transition, same-bank signals.

The QS5805 is characterized for operation at -40°C to +85°C.

## FUNCTIONAL BLOCK DIAGRAM




**INDUSTRIAL TEMPERATURE RANGE** **JULY 2000**



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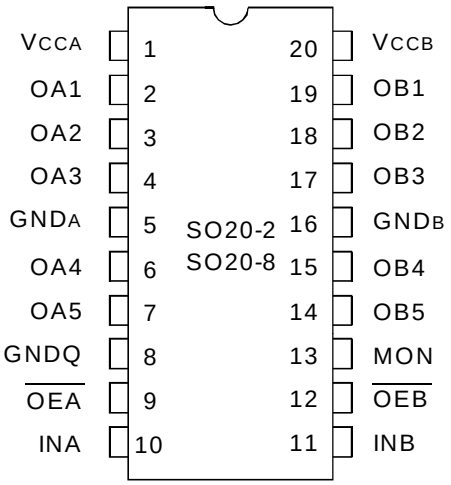
## PIN CONFIGURATION




**QSOP/ SOIC**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Supply Voltage to Ground | – 0.5 to +7 | V |
| | DC Output Voltage $V_{OUT}$ | – 0.5 to +7 | V |
| $V_{TERM}$(3) | DC Input Voltage $V_{IN}$ | – 0.5 to +7 | V |
| $V_{AC}$ | AC Input Voltage (pulse width ≤20ns) | -3 | V |
| $I_{OUT}$ | DC Output Current $V_{IN}$ < 0 | -20 | mA |
| | DC Output Current Max. Sink Current/Pin | 120 | mA |
| $T_{STG}$ | Storage Temperature | – 65 to +150 | °C |
| $T_J$ | Junction Temperature | 150 | °C |

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz, $V_{IN}$ = 0V)

| Pins | QSOP | | SOIC | | Unit |
|---|---|---|---|---|---|
| | Typ. | Max. (1) | Typ. | Max. (1) | |
| $C_{IN}$ | 4 | 6 | 5 | 7 | pF |
| $C_{OUT}$ | 7 | 9 | 7 | 9 | pF |

**NOTE:**
1. This parameter is guaranteed but not production tested.

## PIN DESCRIPTION

| Pin Names | I/O | Description |
|---|---|---|
| $\overline{OEA}$, $\overline{OEB}$ | I | Output Enable Inputs |
| INA, INB | I | Clock Inputs |
| OAn, OBn | O | Clock Outputs |
| MON | O | Monitor Outputs (non-disable) |

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Industrial: $T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%, $V_{HC}$ = $V_{CC}$ - 0.2V, $V_{LC}$ = 0.2V**

| Symbol | Parameter | Test Conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logic HIGH for All Inputs | 2 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logic LOW for All Inputs | — | — | 0.8 | V |
| $V_{IC}$ | Clamp Diode Voltage (3) | Vcc = Min., $I_{IN}$ = -18mA | — | –0.7 | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | Vcc = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = -300µA | $V_{HC}$ | Vcc | — | V |
| | | Vcc = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = -15mA | 3.6 | 4.3 | — | |
| | | Vcc = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = -24mA | 2.4 | 3.8 | — | |
| $V_{OL}$ | Output LOW Voltage | Vcc = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 300µA | — | GND | $V_{LC}$ | V |
| | | Vcc = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 64mA | — | 0.3 | 0.55 | |
| $I_{IN}$ | Input Leakage Current | Vcc = Max., $V_{IN}$ = Vcc or GND | — | — | ±1 | µA |
| $I_{OZ}$ | Output Leakage Current | Vcc = Max., $V_{OUT}$ = Vcc or GND | — | — | ±1 | µA |
| $I_{OFF}$ | Input Power Off Leakage | Vcc = 0V, $V_{IN}$ = Vcc or GND | — | — | ±1 | µA |
| $I_{OS}$ | Short Circuit Current (2,3) | Vcc = Max., $V_{OUT}$ = GND | –60 | — | — | mA |
| $\Delta V_T$ | Input Hysteresis | $V_{TLH}$ - $V_{THL}$ for All Inputs | — | 0.2 | — | V |

**NOTES:**
1. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = 25°C.
2. Not more than one output should be used to test this high power condition. Duration is less than one second.
3. Guaranteed by design but not tested.

# POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions (1) | | Typ. (3) | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or Vcc | | 0.005 | 0.5 | mA |
| $\Delta I_{CC}$ | Supply Current per Input HIGH | $V_{CC}$ = Max., $V_{IN}$ = 3.4V | | 0.5 | 2.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current per Output (2) | $V_{CC}$ = Max., $\overline{OEA}$ = $\overline{OEB}$ = GND<br>Outputs Enabled, 50% duty cycle | | 0.1 | 0.2 | mA/MHz |
| $I_C$ | Total Supply Current Examples (2,4) | $V_{CC}$ = Max.,<br>$\overline{OEA}$ = $\overline{OEB}$ = GND<br>50% duty cycle, $f_I$ = 10MHz<br>Five outputs toggling | $V_{IN}$ = GND or Vcc | 8.5 | 15.5 | mA |
| | | | $V_{IN}$ = GND or 3.4V | 9 | 16.8 | |
| | | $V_{CC}$ = Max.,<br>$\overline{OEA}$ = $\overline{OEB}$ = GND<br>50% duty cycle, $f_I$ = 2.5MHz<br>All outputs toggling | $V_{IN}$ = GND or Vcc | 5 | 8.8 | |
| | | | $V_{IN}$ = GND or 3.4V | 6 | 11.3 | |

**NOTES:**
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Guaranteed by design but not tested. $C_L$ = 0pF.
3. Typical values are for reference only. Conditions are $V_{CC}$ = 5.0V, $T_A$ = 25°C.
4. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
   where:
   $D_H$ = Input Duty Cycle
   $N_T$ = Number of TTL HIGH inputs at $D_H$
   $f_O$ = Output Frequency
   $N_O$ = Number of outputs at $f_O$

## SKEW CHARACTERISTICS OVER OPERATING RANGE

**$T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%**
**$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.**

| Symbol | Parameter (1) | QS5805 | | QS5805A | | QS5805B | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SK(01)}$ | Skew between all outputs, same transition, same bank | — | 0.7 | — | 0.7 | — | 0.7 | ns |
| $t_{SK(02)}$ | Skew between outputs of all banks, same transition | — | 0.8 | — | 0.8 | — | 0.8 | ns |
| $t_{SK(P)}$ | Pulse Skew; skew between opposite transitions of the same output ($t_{PHL}$ - $t_{PLH}$) | — | 1 | — | 1 | — | 1 | ns |
| $t_{SK(T)}$ | Part-to-part skew (2) | — | 1.5 | — | 1.5 | — | 1.2 | ns |

**NOTES:**
1. Skew parameters are guaranteed across temperature range, but not tested. Skew parameters are measured at 0.5Vcc.
2. $t_{SK(T)}$ only applies to devices of the same transition, part type, temperature, power supply voltage, loading, package, and speed grade.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

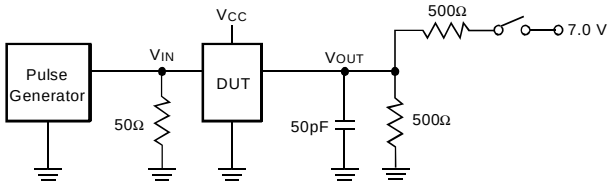
**$T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%**
**$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.**

| Symbol | Parameter (1) | | QS5805 | | QS5805A | | QS5805B | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay (2) INA to OAn, INB to OBn | | 1.5 | 5.6 | 1.5 | 5.3 | 1.5 | 5 | ns |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Time | | 1.5 | 8 | 1.5 | 8 | 1.5 | 7 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Time | | 1.5 | 7 | 1.5 | 7 | 1.5 | 6 | ns |
| $t_R$ | Output Rise Time | 0.8V to 2V (3) | — | 1.5 | — | 1.5 | — | 1.5 | ns |
| | | 0.2Vcc to 0.8Vcc | — | 3 | — | 3 | — | 3 | ns |
| $t_F$ | Output Fall Time | 0.8V to 2V (3) | — | 1.5 | — | 1.5 | — | 1.5 | ns |
| | | 0.2Vcc to 0.8Vcc | — | 3 | — | 3 | — | 3 | ns |

**NOTES:**
1. Minimums guaranteed but not production tested. Timing parameters are measured at 0.5Vcc.
2. The propagation delay other range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delays do not imply limit skew.
3. This parameter is guaranteed but not production tested.

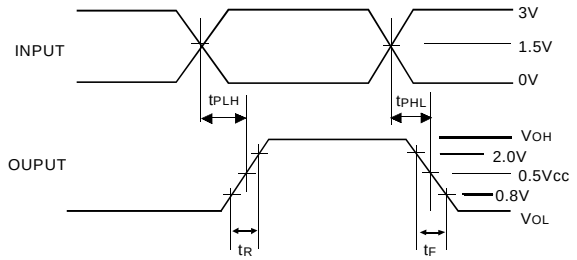
# TEST CIRCUITS AND WAVEFORMS

| Parameter Tested | Switch Position |
|---|---|
| $t_{PLZ}$, $t_{PZL}$ | Closed |
| All Others | Open |

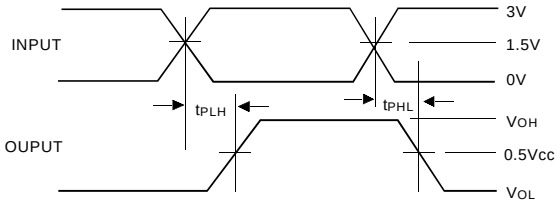



Pulse generator for all pulses: f ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

## PROPAGATION DELAY

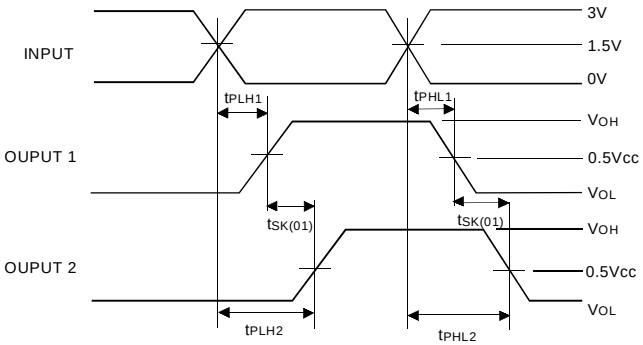



## PULSE SKEW — $t_{SK(P)}$



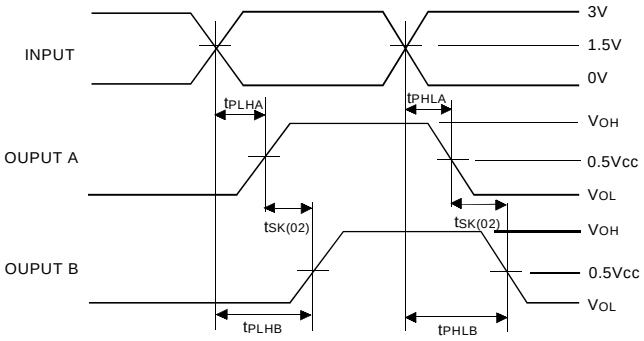

$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

## OUTPUT SKEW (SAME BANK) — $t_{SK(O1)}$



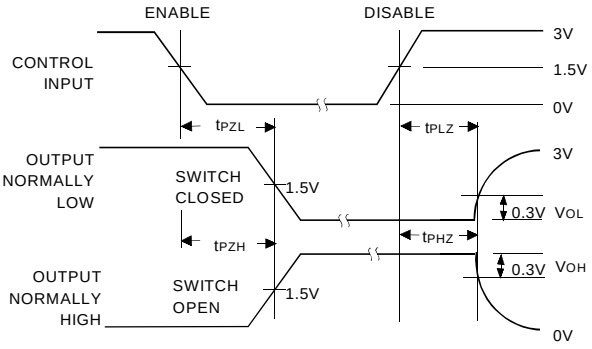

$t_{SK(01)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

## OUPUT SKEW (DIFFERENT BANKS) — $t_{SK(O2)}$

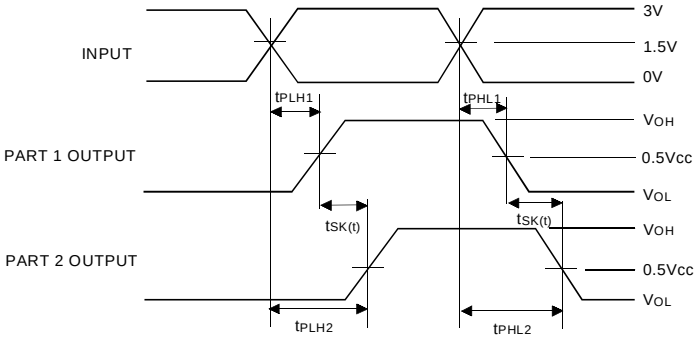



$t_{SK(02)} = |t_{PLHB} - t_{PLHA}|$ or $|t_{PHLB} - t_{PHLA}|$

## ENABLE AND DISABLE TIMES




## PART-TO-PART SKEW — $t_{SK(T)}$




$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

## ORDERING INFORMATION

QS XXXX XX

Device Type

Package

| | |
|---|---|
| Q | Quarter Size Small Outline Pacakge (SO20-8) |
| SO | Small Outline IC (SO20-2) |

| | |
|---|---|
| 5805 | Guaranteed Low Skew CMOS Clock Driver/Buffer |
| 5805A | |
| 5805B | |

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