GUARANTEED LOW SKEW CMOS CLOCK DRIVER/BUFFER

QS5807/A

FEATURES:

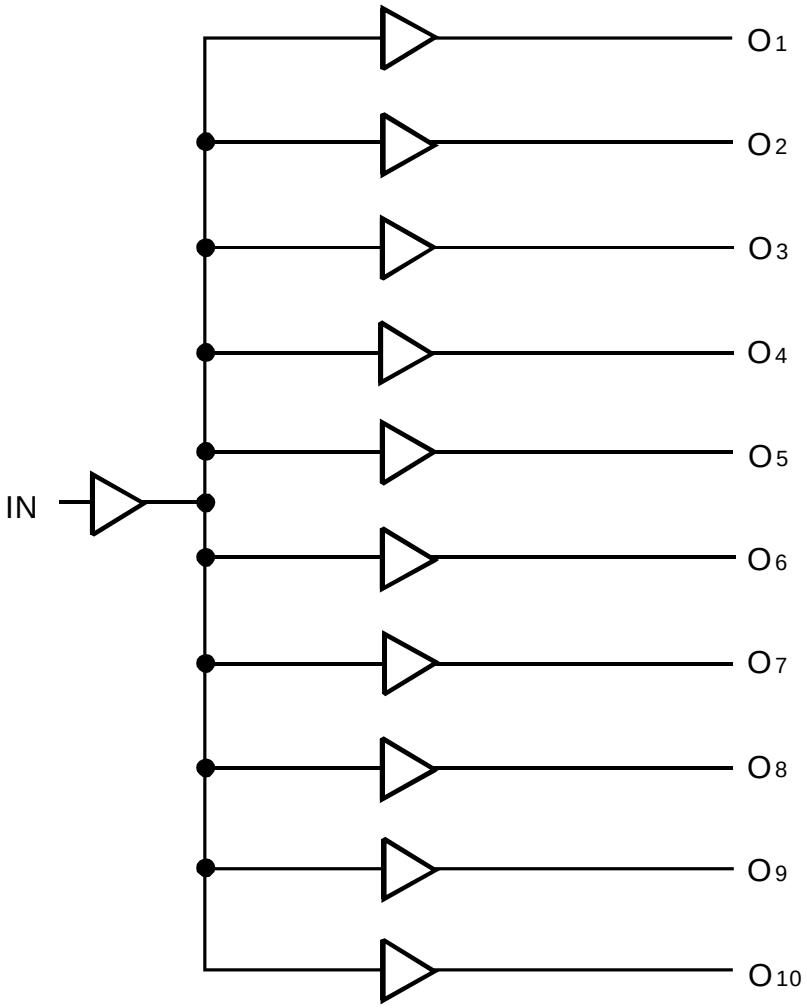
- 10 outputs
- Rail-to-rail output voltage swing
- Input hysteresis for better noise margin
- Guaranteed low skew:
  - 0.3ns output skew (same bank)
  - 0.6ns output skew (different bank)
  - 1ns part-to-part skew
- Std. and A speed grades
- Available in QSOP packages

DESCRIPTION:

The QS5807 clock driver/buffer circuits can be used for clock buffering schemes where low skew is a key parameter. The QS5807 offers ten non-inverting outputs. Designed in IDT's proprietary QCMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.3ns for same-transition signals.

The QS5807 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE **JANUARY 2001**

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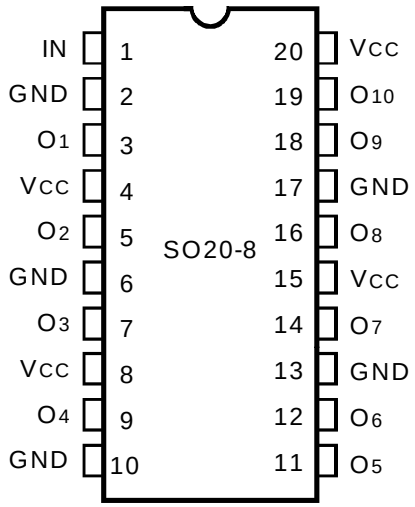
PIN CONFIGURATION



QSOP/ SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Supply Voltage to Ground	– 0.5 to +7	V
	DC Output Voltage V_{OUT}	– 0.5 to +7	V
V_{TERM}(3)	DC Input Voltage V_{IN}	– 0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I_{OUT}	DC Output Current V_{IN} < 0	-20	mA
	DC Output Current Max. Sink Current/Pin	120	mA
T_{STG}	Storage Temperature	– 65 to +150	°C
T_J	Junction Temperature	+150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{IN} = 0V)

Pins	Typ.	Max. (1)	Unit
C_{IN}	3	6	pF

NOTE:
1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
IN	I	Clock Input
Ox	O	Clock Outputs

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for All Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for All Inputs	—	—	0.8	V
V_{IC}	Clamp Diode Voltage (3)	Vcc = Min., I_{IN} = -18mA	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	Vcc = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = -300µA	V_{HC}	Vcc	—	V
		Vcc = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = -15mA	3.6	4.3	—	
		Vcc = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = -24mA	2.4	3.8	—	
V_{OL}	Output LOW Voltage	Vcc = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 300µA	—	GND	V_{LC}	V
		Vcc = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 64mA	—	0.3	0.55	
I_{IN}	Input Leakage Current	Vcc = Max., V_{IN} = V_{CC} or GND	—	—	±1	µA
I_{OFF}	Input Power Off Leakage	Vcc = 0V, V_{IN} = V_{CC} or GND	—	—	±1	µA
I_{OS}	Short Circuit Current (2,3)	Vcc = Max., V_{OUT} = GND	–60	—	—	mA
ΔV_T	Input Hysteresis	V_{TLH} - V_{THL} for All Inputs	—	0.2	—	V

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Not more than one output should be used to test this high power condition. Duration is less than one second.
3. Guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions		Typ.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or Vcc		0.005	0.5	mA
ΔI_{CC}	Supply Current per Input HIGH	V_{CC} = Max., V_{IN} = 3.4V Input toggling at 50% duty cycle		0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current per Output (1)	V_{CC} = Max., outputs Enabled		0.12	0.2	mA/MHz
I_C	Total Power Supply Current Examples (2)	V_{CC} = Max., Input at 50% duty cycle f_I = 10MHz	V_{IN} = GND or Vcc	12	21	mA
			V_{IN} = GND or 3V	12	2.2	
		V_{CC} = Max., Input at 50% duty cycle f_I = 2.5MHz	V_{IN} = GND or Vcc	3	6	
			V_{IN} = GND or 3V	3.5	7	

NOTES:
1. Guaranteed by design but not tested. C_L = 0pF.
2. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
   where:
   D_H = Input Duty Cycle
   N_T = Number of TTL HIGH inputs at D_H
   f_O = Output Frequency
   N_O = Number of outputs at f_O

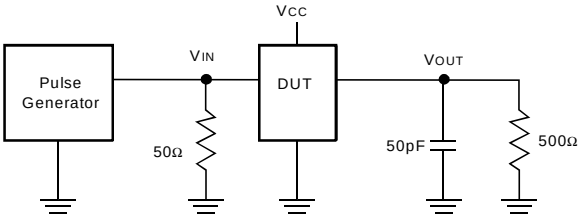
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Parameter [1]	QS5807		QS5807A		Unit
		Min.	Max.	Min.	Max.	
$t_{SK(01)}$	Skew between all outputs, same transition	—	0.5	—	0.35	ns
$t_{SK(P)}$	Pulse Skew; skew between opposite transitions of the same output (t_{PHL} - t_{PLH})	—	1	—	1	ns
$t_{SK(T)}$	Part-to-part skew [2]	—	1.5	—	1.5	ns
t_{PLH} t_{PHL}	Propagation Delay [2] IN to Ox	1.5	5.6	1.5	5.3	ns
t_R	Output Rise Time, 0.8V to 2V [3]	—	1.5	—	1.5	ns
t_F	Output Fall Time, 0.2Vcc to 0.8Vcc [3]	—	3	—	3	ns

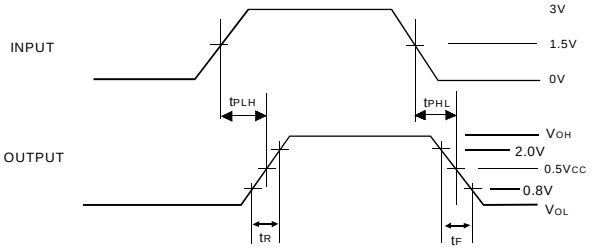
NOTES:
1. Skew parameters are guaranteed across temperature range, but not tested. Skew parameters are measured at 0.5Vcc.
2. $t_{SK(T)}$ only applies to devices of the same transition, part type, temperature, power supply voltage, loading, package, and speed grade.
3. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delays do not imply limit skew.

TEST CIRCUITS AND WAVEFORMS

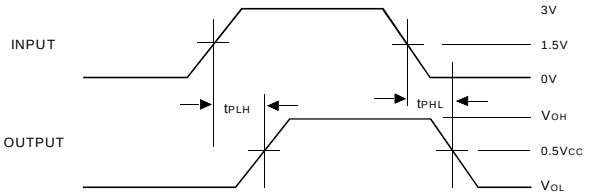


Pulse generator for all pulses: f ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

PROPAGATION DELAY

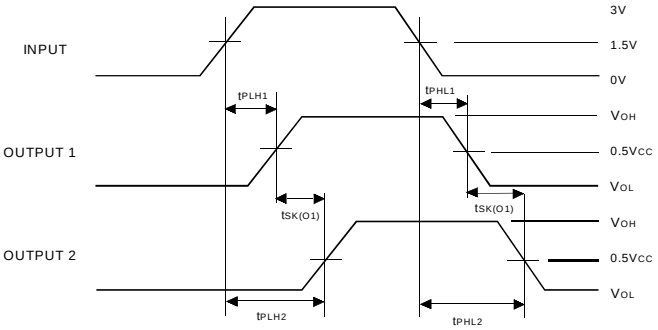


PULSE SKEW — $t_{SK(P)}$



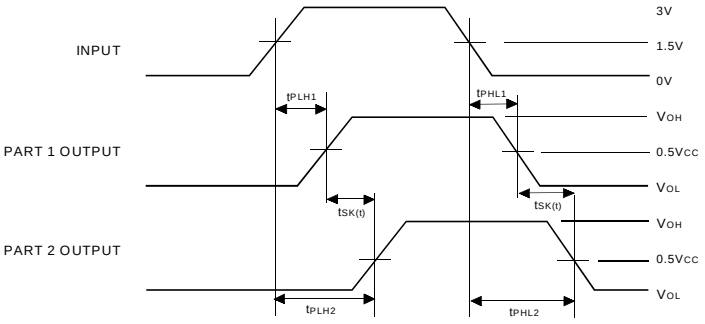
$t_{SK(p)} = |t_{PHL} - t_{PLHL}|$

OUTPUT SKEW — $t_{SK(O1)}$



$t_{SK(01)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

PART-TO-PART SKEW — $t_{SK(T)}$



$t_{SK(p)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

ORDERING INFORMATION

QS XXXX X

Device Type — Package

Q	Quarter-size Small Outline Package (SO20-8)
5807 5807A	Guaranteed Low Skew CMOS Clock Driver/Buffer

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